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(54) **FORMING CHARGE TRAP SEPARATION IN A FLASH MEMORY SEMICONDUCTOR DEVICE**

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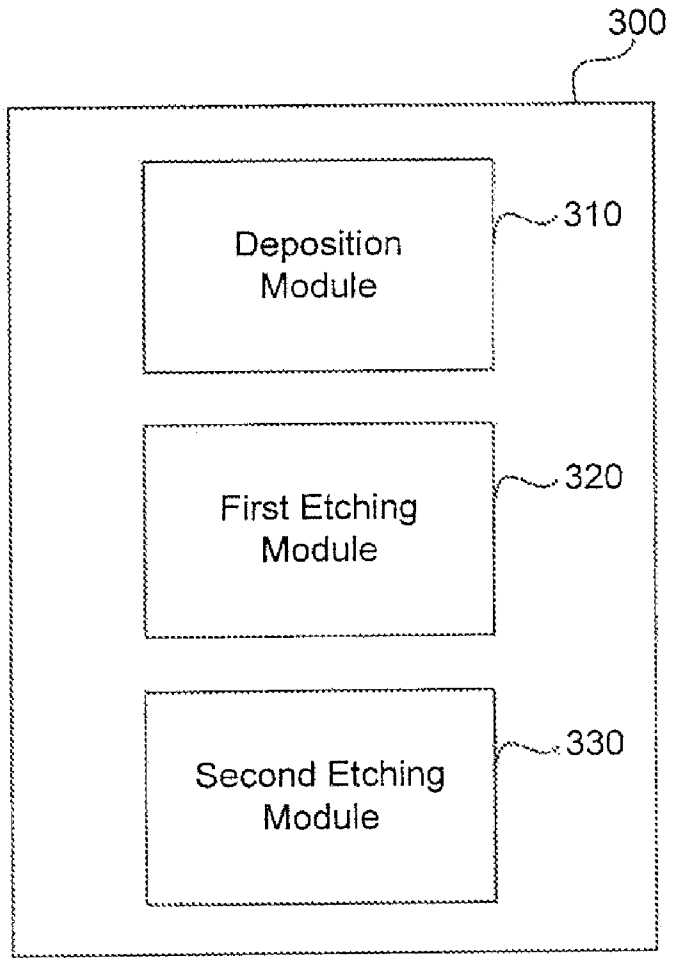
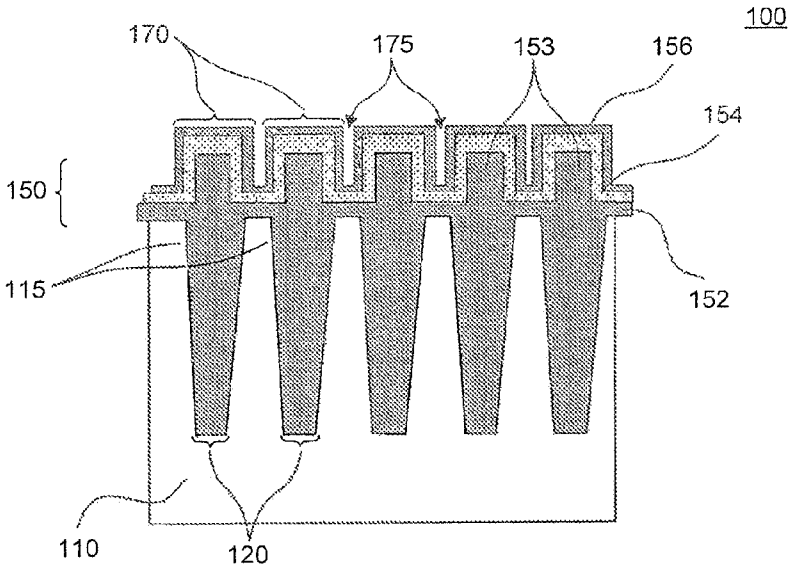
(57) **ABSTRACT**

During formation of a charge trap separation in a semiconductor device, a polymer deposition is formed in a reactor using a first chemistry. In a following step, a second chemistry can be used to etch the polymer deposition in the reactor. The same or similar second chemistry can be used in a second etching step to expose a first oxide layer in each of the cells of the semiconductor device and to form a flat upper surface. This additional etch step can also be performed by the reactor, thereby reducing the number of machines required in the formation process.




100
170
175
153
156
154
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110
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FIG. 1A

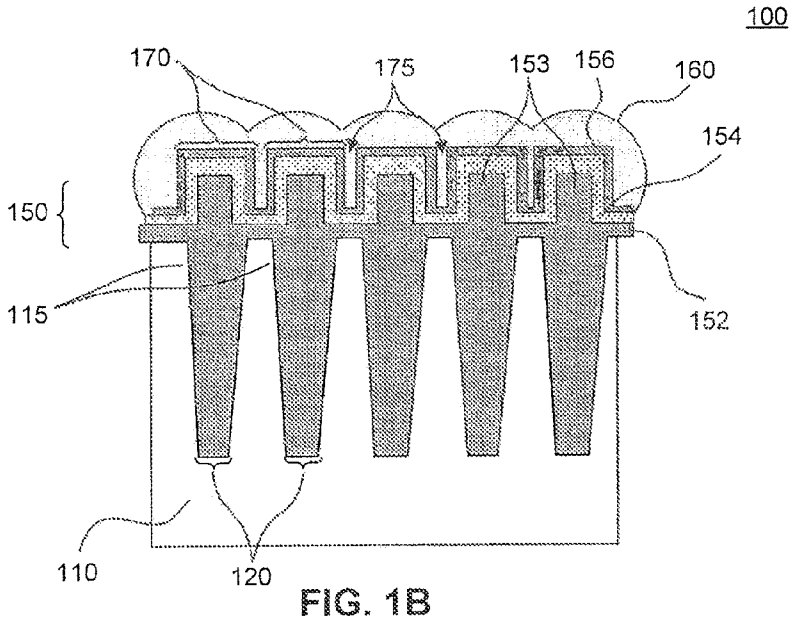
100
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FIG. 1B

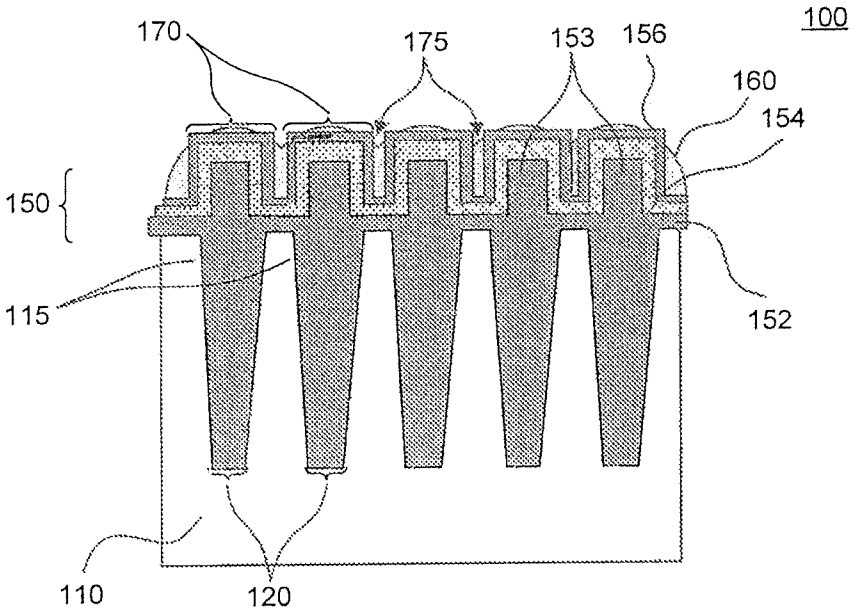
100
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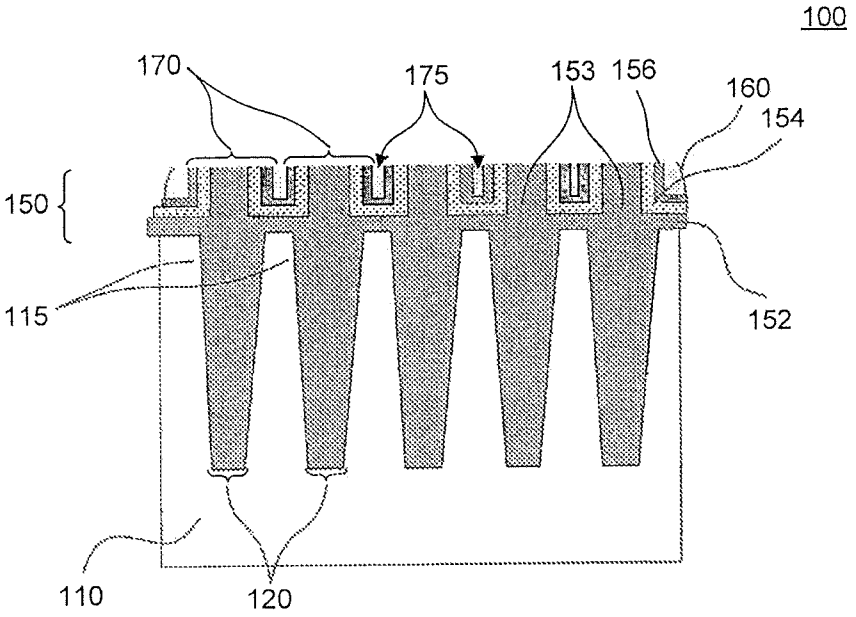
FIG. 1C


100
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152
110
120

FIG. 1D

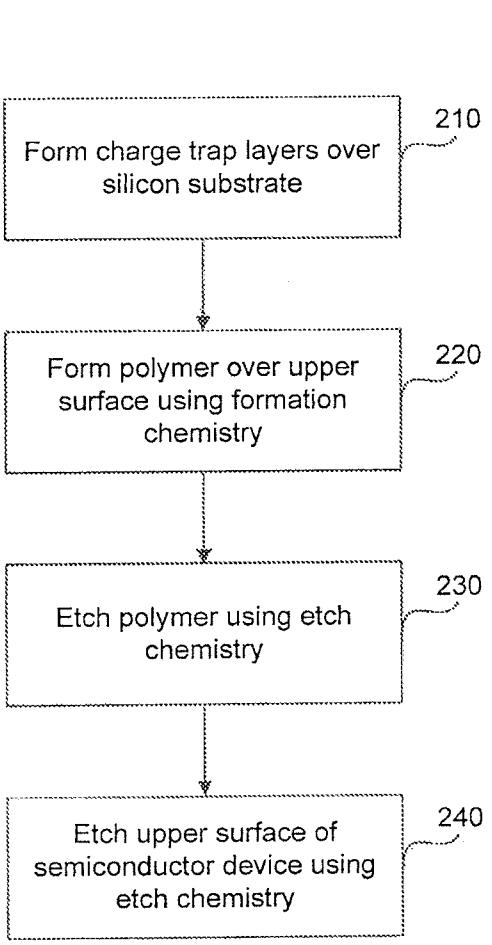
200
Form charge trap layers over silicon substrate
210
Form polymer over upper surface using formation chemistry
220
Etch polymer using etch chemistry
230
Etch upper surface of semiconductor device using etch chemistry
240

FIG. 2

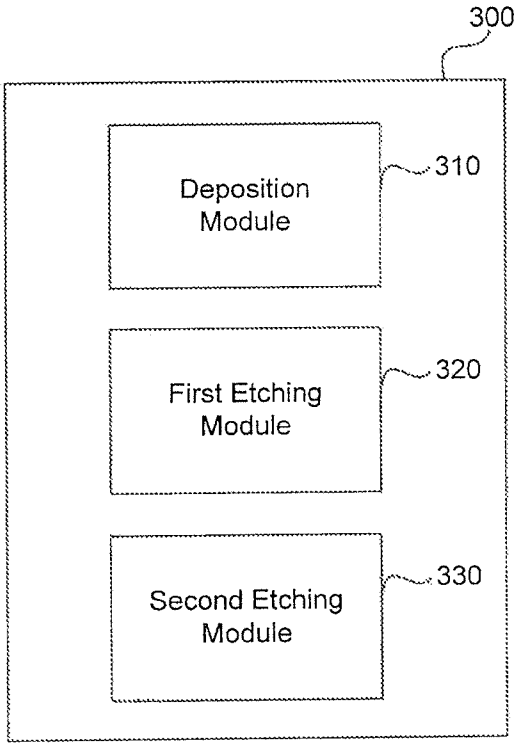
300
Deposition Module
310
First Etching Module
320
Second Etching Module
330

FIG. 3

FORMING CHARGE TRAP SEPARATION IN A FLASH MEMORY SEMICONDUCTOR DEVICE

BACKGROUND

[0001] 1. Technical Field

[0002] The disclosure generally relates to forming a charge trap separation in a semiconductor device, and specifically to reducing the number of different machines needed to perform the formation process.

[0003] 2. Related Art

[0004] Charge trap semiconductors have become commercially viable for use in flash memory devices. Charge trap semiconductor configurations provide significant advantages over other configurations by allowing multiple bits to be stored in each individual cell. However, the manufacturing of charge trap semiconductors can be somewhat time-consuming and complex.

[0005] Conventionally, several different machines are used to construct charge trap semiconductors for flash memories. For example, charge trap layers are grown on top of source/drain regions and field oxide regions of a base substrate using one or more first machines, such as a PECVD furnace. A second machine, such as track equipment, is then used to coat a thin organic material above the charge trap layers in order to fill gaps and planarize the surface of the semiconductor using a coating and/or spinning process. A third machine, such as an etcher, is then used to etch back the organic material and remove the exposed charge trap layers in order to create the separate cells of the final semiconductor device.

[0006] The need to move the semiconductor between different machines during the conventional manufacturing process greatly increases manufacturing time. In addition, the movements between different machines increase the likelihood of contaminating the semiconductor wafer, and therefore potentially decreases manufacturing yield.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0007] Embodiments are described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left most digit(s) of a reference number identifies the drawing in which the reference number first appears.

[0008] FIGS. **1**A-**1**D illustrate side views of a semiconductor device during manufacturing method steps for forming a charge trap separation according to an embodiment;

[0009] FIG. **2** illustrates a flowchart of a method for forming a charge trap separation in a flash memory semiconductor device according to an embodiment; and

[0010] FIG. **3** illustrates a block diagram of an apparatus configured to form a charge trap separation in a flash memory semiconductor device according to an embodiment.

DETAILED DESCRIPTION

[0011] The following Detailed Description refers to accompanying drawings to illustrate exemplary embodiments consistent with the disclosure. References in the Detailed Description to "one exemplary embodiment," "an exemplary embodiment," "an example exemplary embodiment," etc., indicate that the exemplary embodiment described may include a particular feature, structure, or characteristic, but every exemplary embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same exemplary embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an exemplary embodiment, it is within the knowledge of those skilled in the relevant art(s) to affect such feature, structure, or characteristic in connection with other exemplary embodiments whether or not explicitly described.

[0012] The exemplary embodiments described herein are provided for illustrative purposes, and are not limiting. Other exemplary embodiments are possible, and modifications may be made to the exemplary embodiments within the spirit and scope of the disclosure. Therefore, the Detailed Description is not meant to limit the invention. Rather, the scope of the invention is defined only in accordance with the following claims and their equivalents.

[0013] Method embodiments may be implemented in hardware (e.g., circuits), firmware, software, or any combination thereof. Method embodiments may also be implemented as instructions stored on a machine-readable medium, which may be read and executed by one or more processors. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computing device). For example, a machine-readable medium may include read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.), and others. Further, firmware, software, routines, instructions may be described herein as performing certain actions. However, it should be appreciated that such descriptions are merely for convenience and that such actions in fact results from computing devices, processors, controllers, or other devices executing the firmware, software, routines, instructions, etc. Further, any of the implementation variations may be carried out by a general purpose computer.

[0014] The following Detailed Description of the exemplary embodiments will so fully reveal the general nature of the invention that others can, by applying knowledge of those skilled in relevant art(s), readily modify and/or adapt for various applications such exemplary embodiments, without undue experimentation, without departing from the spirit and scope of the disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and plurality of equivalents of the exemplary embodiments based upon the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by those skilled in relevant art(s) in light of the teachings herein.

[0015] Those skilled in the relevant art(s) will recognize that this description may be applicable to many various semiconductor devices, and should not be limited to flash memory devices or any other particular type of semiconductor devices.

An Exemplary Semiconductor Device

[0016] FIG. **1**A illustrates a side view of an exemplary semiconductor device **100** prior to charge trap separation according to an embodiment.

[0017] The semiconductor device **100** includes a bulk semiconductor substrate **110** that includes a plurality of source/

drain regions **115** extending vertically from a base of the substrate **110**. Adjacent vertically-extending source/drain regions **115** define isolation trenches **120** therebetween.

[0018] Charge trap layers **150** are formed over a top surface of the substrate **110**. The charge trap layers **150** include a first oxide layer **152** that extends into the isolation trenches **120**, and which covers a top surface of the substrate **110**. The first oxide layer **152** includes substantially rectangular protrusions **153** that extend above the isolation trenches **120**. The charge trap layers **150** further include a silicon rich nitride layer **154** uniformly formed over the first oxide layer **152**, as well as a second oxide layer **156** uniformly formed over the silicon rich nitride layer **154**.

[0019] The combined first oxide layer **152**, silicon rich nitride layer **154** and second oxide layer **156** define cells **170** at each of the rectangular protrusions **153**. Adjacent cells **170** are separated from one another by, and together define, cell separation gaps **175**.

[0020] FIG. **1**B illustrates a side view of the semiconductor device **100** after a subsequent step in an exemplary charge trap separation formation method, according to an embodiment.

[0021] In an embodiment, in this step, the semiconductor device **100** is placed in a reactor. In an embodiment, the reactor is a plasma reactor. The reactor is used to grow a polymer deposition **160** over a top surface of the semiconductor device **100**, and specifically over the second oxide layer **156** of the charge trap layers **150**.

[0022] The polymer deposition **160** is formed so as to at least substantially fill the cell separation gaps **175**. Particularly, the polymer deposition **160** may be formed within the cell separation gaps **175** sufficiently high such that a future etching step (see FIG. **1**D) leaves cell separation gaps **175** completely filled with the polymer deposition **160**. Therefore, in an embodiment, in order to ensure sufficient polymer deposition **160**, the polymer deposition **160** is formed so as to at least completely fill the cell separation gaps **175**.

[0023] In an embodiment, in order to grow the polymer deposition **160** on the semiconductor device **100**, the reactor employs a chemistry (e.g., a "grow chemistry") selected from a plurality of hydrocarbon gases and/or fluorocarbon gases. Such chemistries may include, for example, HBr, CH_4, CH_3F and CH2F2. Other viable chemistries may include $C_xH_yF_z$, where x, y, and z are each positive integers.

[0024] FIG. **1**C illustrates a side view of the semiconductor device **100** after a subsequent step in the exemplary charge trap separation formation method, according to an embodiment.

[0025] According to an embodiment, in this step, using the same reactor, the semiconductor device **100** is etched using a different chemistry. For example, in this step the chemistry in the reactor is changed to an etch chemistry, such as a CF_4/O_2 mixture. With this new etch chemistry, the reactor etches away outer portions of the polymer deposition **160** in order to expose the upper edges of the charge trap layers **150**.

[0026] In an embodiment, this etching step etches the polymer deposition **160** below the top surface of the charge trap layers **150**, provided that the polymer deposition **160** still sufficiently fills the cell separation gaps **175** so as to completely fill those gaps **175** after a second subsequent etch (see FIG. **1**D).

[0027] FIG. **1**D illustrates a side view of the semiconductor device **100** after a subsequent step in the exemplary charge trap separation formation method, according to an embodiment.

[0028] In an embodiment, using the same reactor, the semiconductor device **100** is further etched in order to expose upper edges of the first oxide layer **152**. In order to expose the first oxide layer **152**, the reactor etches the polymer deposition **160** together with a portion of the second oxide layer **156** and silicon nitride layer **154** over each of the cells **170**. By performing the first etch (FIG. **1**C) to maintain the polymer deposition **160** in the cell separation gaps **175**, the polymer deposition **160** protects the active regions of the semiconductor device **100** during this second etch.

[0029] As a result of this second etch, the semiconductor device **100** includes a plurality of separate cells **170** separated from each other by the polymer deposition **160** filled into the cell separation gaps **175**. In addition, the semiconductor device **100** maintains a substantially flat upper surface as a result of the second etch.

[0030] By forming the charge trap separation in the manner described above, only a single machine is required for the growing and etching steps. This substantially reduces manufacturing costs, time and complexity. In addition, by maintaining the semiconductor device **100** in a single machine throughout the charge trap separation formation process, the likelihood of contracting contaminants is reduced. Consequently, manufacturing yield and efficiency can be improved over conventional methods.

Exemplary Method for Forming Charge Trap Separation in a Semiconductor Device

[0031] FIG. **2** illustrates a flowchart diagram **200** of a method for forming a charge trap separation in a flash memory semiconductor device according to an embodiment. For illustration purposes, flowchart **200** is described with continued reference to FIGS. **1**A-**1**D, although the method **200** is not limited to the example.

[0032] In step **210**, referring to FIG. **1**A, charge trap layers **150** are formed over a top surface of a substrate **110**. The charge trap layers **150** include a first oxide layer **152** that extends into isolation trenches **120** defined by vertically-extending source/drain regions **115** of the substrate **110**. The first oxide layer **152** includes substantially rectangular protrusions **153** that extend above the isolation trenches **120**. The charge trap layers **150** further include a silicon rich nitride layer **154** uniformly formed over the first oxide layer **152**, as well as a second oxide layer **156** uniformly formed over the silicon rich nitride layer **154**.

[0033] In step **220**, referring to FIG. **1**B, in a reactor, a polymer deposition **160** is formed on a top surface of the semiconductor device **100**. The polymer deposition **160** can be formed using a formation chemistry using hydrocarbon gases and/or fluorocarbon gases, such as those described above, although the method **200** is not limited to such examples. The polymer deposition **160** is formed so as to at least substantially fill cell separation gaps **175** defined by adjacent cells **170** of the semiconductor device **100**.

[0034] In step **230**, referring to FIG. **1**C, in the same reactor, the polymer deposition **160** is etched using an etch chemistry. The etch chemistry may include a mixture of CF_4 and O_2 (although the method **200** is not limited to these examples), and should etch the polymer deposition **160** to expose a top

surface of the charge trap layers **150** without significantly removing the polymer deposition **160** from the cell separation gaps **175**.

[0035] In step **240**, referring to FIG. **1**D, in the same reactor, the upper surface of the semiconductor **100** is etched using the etch chemistry. This second etch removes portions of the second oxide layer **156** and portions of the silicon rich nitride layer **154** so as to expose the first oxide layer **152** at each of the cells **170** of the semiconductor device **100**. In addition, the second etch removes portions of the polymer deposition **160** so as to maintain a substantially flat top surface in the resulting semiconductor device **100**. In an embodiment, the reactor is a plasma reactor. Also, in certain embodiments, more than one device (reactors) may be used to perform these steps of flowchart **200**.

[0036] Those skilled in the relevant art(s) will recognize that the above method can additionally or alternatively include any of the steps or substeps described above with respect to FIGS. **1**A-**1**D, as well as any of their modifications. Further, the above description of the exemplary method should not be construed to limit the description of the method depicted in FIGS. **1**A-**1**D.

Exemplary Apparatus for Forming Charge Trap Separation in a Semiconductor Device

[0037] FIG. **3** illustrates a block diagram of an exemplary apparatus **300** for forming charge trap separation in a semiconductor device. The apparatus includes a deposition module **310**, a first etching module **320** and a second etching module **330**. For illustration purposes, the apparatus **300** is described with continued reference to FIGS. **1**A-**1**D.

[0038] The apparatus **300** forms charge trap separation in a semiconductor device **100** having charge trap layers **150** formed over a top surface of a substrate **110**, as shown for example in FIG. **1**A. The charge trap layers **150** include a first oxide layer **152** that extends into isolation trenches **120** defined by vertically-extending source/drain regions **115** of the substrate **110**. The first oxide layer **152** includes substantially rectangular protrusions **153** that extend above the isolation trenches **120**. The charge trap layers **150** further include a silicon rich nitride layer **154** uniformly formed over the first oxide layer **152**, as well as a second oxide layer **156** uniformly formed over the silicon rich nitride layer **154**.

[0039] The deposition module **310** is configured to form a polymer deposition **160** on a top surface of the semiconductor device **100**, as shown for example in FIG. **1**B. The polymer deposition **160** can be formed using a formation chemistry using for example and without limitation hydrocarbon gases and/or fluorocarbon gases, such as those described above. The polymer deposition **160** is formed so as to at least substantially fill cell separation gaps **175** defined by adjacent cells **170** of the semiconductor device **100**.

[0040] The first etching module **320** is configured to etch the polymer deposition **160** using an etch chemistry, as shown for example in FIG. **1**C. The etch chemistry may include, but is not limited to, a mixture of CF_4 and O_2, and should etch the polymer deposition **160** to expose a top surface of the charge trap layers **150** without significantly removing the polymer deposition **160** from the cell separation gaps **175**.

[0041] The second etching module **330** is configured to etch the upper surface of the semiconductor **100** using the etch chemistry, as shown for example in FIG. **1**D. This second etch removes portions of the second oxide layer **156** and portions of the silicon rich nitride layer **154** so as to expose the first oxide layer **152** at each of the cells **170** of the semiconductor device **100**. In addition, the second etch removes portions of the polymer deposition **160** so as to maintain a substantially flat top surface in the resulting semiconductor device **100**. In an embodiment, the apparatus **300** is a plasma reactor.

[0042] Those skilled in the relevant art(s) will recognize that the above method can additionally or alternatively include any of the steps or substeps described above with respect to FIGS. **1**A-**1**D, as well as any of their modifications. Further, the above description of the exemplary method should not be construed to limit the description of the method depicted in FIGS. **1**A-**1**D.

CONCLUSION

[0043] It is to be appreciated that the Detailed Description section, and not the Abstract section, is intended to be used to interpret the claims. The Abstract section may set forth one or more, but not all exemplary embodiments, and thus, is not intended to limit the disclosure and the appended claims in any way.

[0044] The invention has been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries may be defined so long as the specified functions and relationships thereof are appropriately performed.

[0045] It will be apparent to those skilled in the relevant art(s) that various changes in form and detail can be made therein without departing from the spirit and scope of the disclosure. Thus, the invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

1-13. (canceled)

14. An apparatus for forming charge trap separation in a semiconductor device, the semiconductor device having a charge trap layer formed on a substrate, the apparatus comprising:

a deposition module configured to grow a polymer deposition on the charge trap layer so as to fill cell separation gaps between adjacent cells of the charge trap layer;

a first etching module configured to etch the polymer deposition to expose the charge trap layer such that an upper surface of the polymer deposition is lower than an upper surface of the charge trap layer; and

a second etching module configured to etch the polymer deposition over the cells and within the cell separation gaps together with the charge trap layer so as to expose a bottom portion of the charge trap layer within the cells and form a uniform upper surface among the cells and the cell separation gaps.

15. The apparatus of claim **14**, wherein the deposition module is configured to grow the polymer deposition using a grow chemistry, and

wherein at least one of the first etching module and the second etching module is configured to etch using an etch chemistry that is different from the grow chemistry.

16. The apparatus of claim **15**, wherein the first etching module and the second etching module are both configured to etch using the etch chemistry.

17. The apparatus of claim **15**, wherein the grow chemistry includes at least one of a hydrocarbon gas and a fluorocarbon gas.

18. The apparatus of claim **15**, wherein the etch chemistry includes a mixture of CF4 and O2.

19. (canceled)

20. The apparatus of claim **14**, wherein the first etching module is configured to remove a portion of the polymer deposition from within the cell separation gaps.

* * * * *