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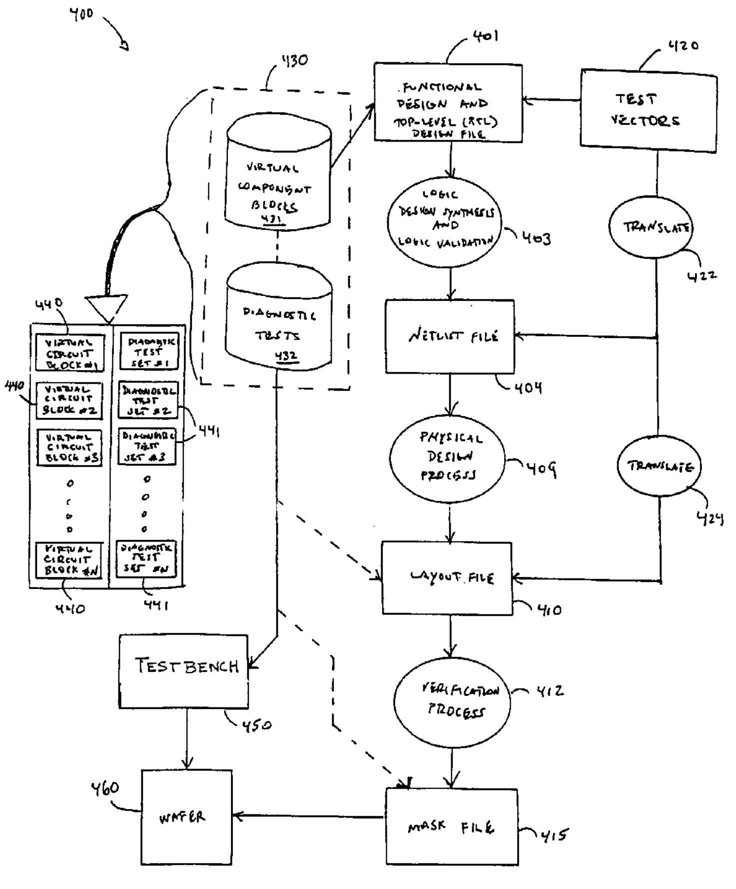
(54) Title: SYSTEM AND METHOD FOR TESTING INTEGRATED CIRCUITS



(57) Abstract: A method of testing an integrated circuit including component blocks of random logic in a manufacturing environment is disclosed. The method includes the steps of performing built-in self tests, at least in part to test memory and data paths of the integrated circuit, performing diagnostics tests, at least in part to test the component blocks of random logic individually, performing stress tests using test vectors, at least in part to test the component blocks of random logic collectively; and performing scan-based tests of the integrated circuit, at least in part to test for structural faults in the integrated circuit.

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patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 539 652 A (TEGETHOFF MAURO V) 23 July 1996 (1996-07-23) abstract; claims 1-10 -----	1-63

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5539652 A	23-07-1996	NONE	