(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 February 2012 (09.02.2012)

PCT

(10) International Publication Number
WO 2012/017227 A1

(51) International Patent Classification:
H01L 29/739 (2006.01) *H01L 29/06* (2006.01)
H01L 21/331 (2006.01)

(21) International Application Number:
PCT/GB2011/051413

(22) International Filing Date:
25 July 2011 (25.07.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1012951.8 2 August 2010 (02.08.2010) GB
1107979.5 13 May 2011 (13.05.2011) GB

(71) Applicant *(for all designated States except US)*: **THE UNIVERSITY OF WARWICK** [GB/GB]; University House, Coventry, Warwickshire CV4 8UW (GB).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **WARD, Peter** [GB/GB]; Wensum House, Hemington, Peterborough, Cambridgeshire PE8 5QJ (GB). **MAWBY, Philip** [GB/GB]; c/o Department of Engineering, The University of Warwick, Coventry, Warwickshire CV4 8UW (GB). **WESTMORELAND, Martin** [GB/GB]; c/o Department of Engineering, The University of Warwick, Coventry, Warwickshire CV4 8UW (GB).

(74) Agents: **PIOTROWICZ, Pawel** et al.; Venner Shipley LLP, Byron House, Cambridge Business Park, Cowley Road, Cambridge Cambridgeshire CB4 0WZ (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: SEMICONDUCTOR DEVICE

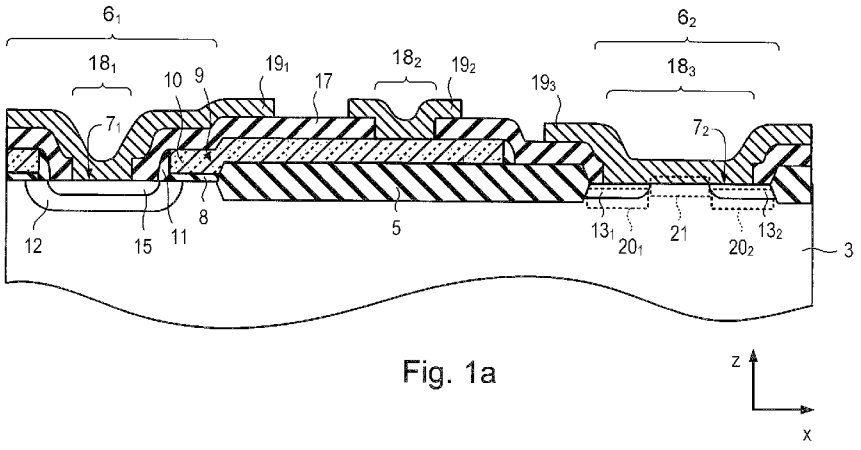

Fig. 1a

(57) **Abstract**: A semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a vertical or lateral insulated gate bipolar transistor is disclosed. The device has a Schottky-biased p-n junction.

WO 2012/017227 A1

Semiconductor device

Field of the Invention

The present invention relates to a semiconductor device and more specifically to a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor (MOSFET) and a vertical or lateral insulated gate bipolar transistor (IGBT). The present invention also relates to a semiconductor device having an integrated vertical and lateral charge balance structure.

Background

In a vertical MOSFET, current flows vertically between a source having one conductivity type and a substrate drain of the same conductivity type. The MOSFET operates based on the flow of only majority carriers through the drift region.

An IGBT has a similar structure to a vertical MOSFET, but differs in that the drain is of the opposite conductivity type. Thus, both majority and minority carriers are injected into the drift region. This has the effect of reducing the ON resistance of the IGBT compared to the MOSFET, but also has the effect of increasing the gate switching speed.

A form of vertical MOSFET device has been proposed in which a MOSFET is provided with a minority carrier injector in the form of a p-type region which forms a p-n junction with the n-type drift region so as to increase switching speed and reduce the ON resistance. Reference is made to "A novel trench-injector power device with low ON resistance and high switching speed", David K. Y. Liu and James D. Plummer, IEEE Electron Device Letters, volume 9, Issue 7, pages 321 - 323 (1988) and "Design and analysis of a new conductivity-modulated power MOSFET", David K. Y. Liu and James D. Plummer, IEEE Transactions on Electron Devices, volume 40, Issue 2, pages 428 - 438 (1993).

The device has a drawback of needing to control separately an additional terminal. However, this can be avoided by connecting the injector to the drain. However,

this arrangement presents a problem, namely that when the same bias is applied to the injector and drain, no voltage difference develops across the p-n junction and so no minority carrier injection occurs. In particular, a small voltage difference initially develops due to differing resistances between the source and the drain and the source and the injector. However, the difference in resistance is soon compensated by low-level minority carrier injection and so the effect stops.

An alternative approach is to form a hybrid vertical DMOS/lateral IGBT device and reference is made to "A new hybrid VDMOS-LIGBT transistor" T. Paul Chow & B. Jayant Baliga, IEEE Electron Device Letters, volume 9, pages 473 - 475 (1988).

This device comprises two devices in parallel, namely a p-channel vertical MOSFET DMOSFET and a p-channel lateral IGBT. However, the hybrid device needs external resistors to bias the device and, since the resistors are fixed, bipolar action is not optimized.

In lateral MOSFET devices, it has been proposed to inject minority carriers using a Schottky contact and reference is made to "The SINFET - A Schottky injection MOS-gated power transistor", Johnny K. O. Sin, C. Andre T. Salama and Li-Zhang Hou, IEEE Transactions on Electron Devices, volume ED-33, page 1940-1947 (1986).

However, the number of injected minority carriers is low. Thus, although conductivity can be modulated using minority carriers, the device falls well short of achieving full IGBT-like bipolar action.

Summary

The present invention seeks to provide an improved semiconductor device.

According to a first aspect of the present invention there is provided a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a vertical or lateral insulated gate bipolar transistor having a Schottky-biased p-n junction.

Thus, the Schottky biasing helps to ensure that the p-n junction is forward biased and continues to inject minority carriers. Therefore, the device provides an integrated vertical metal oxide semiconductor field effect transistor and vertical or lateral insulated gate bipolar transistor.

The semiconductor device may comprise a minority-carrier injector which comprises the p-n junction and a Schottky diode, wherein the Schottky diode is arranged in parallel with the p-n junction so as to provide the Schottky-biased p-n junction.

The semiconductor device may comprise a semiconductor region (for example, an epitaxial region) disposed between first and second opposite surfaces, at least a first portion of the semiconductor region comprising a semiconductor of a first conductivity type providing a drift region for majority carriers in a direction between the first and second surfaces, at least a second portion of the semiconductor region providing a body region comprising a semiconductor of a second, opposite conductivity type disposed at the first surface of the semiconductor region and at least a third portion of the semiconductor region providing a source region comprising a semiconductor of the first conductivity type disposed at the first surface of semiconductor region and within the body region. The semiconductor region may comprise the same semiconductor, such as silicon or silicon carbide, but have regions of different conductivity types, i.e. n-type and p-type regions.

The minority-carrier injector may be disposed at the first surface (e.g. top surface) of the semiconductor region laterally separated from the body region. Thus, a lateral insulated gate bipolar transistor can be formed. However, the minority-carrier injector may be disposed at the second surface (e.g. bottom surface) of the semiconductor region so as to form a vertical insulated gate bipolar transistor.

At least a fourth portion of the semiconductor region may comprise a semiconductor of the second conductivity type disposed at the first surface of the semiconductor region with a semiconductor of the first conductivity type so as to form the p-n junction. The Schottky diode may comprise a metallization in contact with the first surface of semiconductor region. The Schottky diode may have a barrier height equal to or greater than 0.7 eV. If the minority-carrier injector is disposed at the second surface, then the metallization may be in contact with the first surface of semiconductor region. A different metallization and/or process may be used to form a drain contact to the semiconductor region.

The semiconductor device may further comprise a gate structure disposed on the first surface of the semiconductor region and configured to control flow of carriers from the source region into drift region. The semiconductor device may further comprise a drain region disposed on the second surface of the semiconductor region. The drain region may include a semiconductor substrate, e.g. highly-doped substrate such as a wafer. The drain region may include a metallization, which preferably forms an ohmic contact.

The device may comprise a drain region comprising a semiconductor substrate (or layer) of a first conductivity type or a metallic layer, a drift region of the first conductivity type disposed on the drain region, a body region of a second, opposite conductivity type, for example formed in or adjacent to the drift region, and a source region of the first conductivity type disposed within the body region.

According to a second aspect of the present invention there is provided a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor, the device comprising a

semiconductor substrate drain of a first conductivity type, a drift region or epitaxial region of the first conductivity type disposed on the semiconductor substrate drain, a body region of a second, opposite conductivity type disposed within the drift region or epitaxial region, a source region of the first conductivity type disposed within the body region. The device further comprises a minority-carrier injector which comprises an injector region of the second conductivity type disposed within the drift region or epitaxial region and laterally separated from the body region, the injector region and the drift region or epitaxial region forming a p-n junction, and a metallic electrode in contact with the drift region or epitaxial region laterally adjacent to and electrically connected to the injector region, the metallic electrode and the drift region or epitaxial region forming a Schottky diode in parallel with the p-n junction.

Thus, the Schottky diode helps to ensure that the p-n junction is forward biased and continues to inject minority carriers into the drift region or epitaxial region. Therefore, the device provides an integrated vertical metal oxide semiconductor field effect transistor and lateral insulated gate bipolar transistor.

The first and second conductivity types may be n-type and p-type respectively.

The body region and the substrate (or, if no substrate is present, for example, because it has been removed or a portion of it has been removed, the second surface of the semiconductor region) may be vertically separated by a first given distance and the body region and the injector region are laterally separated by a second given distance exceeding equal to or greater than the first given distance. The second given distance may be about 6 to 12 μm.

The device may further comprise a depletion reducing region comprising a semiconductor of the first conductivity type disposed within the drift region, more highly doped than the drift region and disposed between the body region and the injector region. This can help reduce the lateral size of the device.

The body region and the substrate may be vertically separated by a first given distance and the body region and the injector region are laterally separated by a second given distance less than the first given distance.

The Schottky diode may have a barrier height equal to or greater than 0.7 eV. The metallic electrode may include a layer of platinum silicide forming the Schottky diode.

The metallic electrode and the semiconductor substrate may be coupled so as to be at substantially the same potential. The device may comprise a further, different metallic electrode in contact with the source region.

The drift region or epitaxial region may comprise silicon. Alternatively, the drift region or epitaxial region may comprise silicon carbide semiconductor. The drift region, the body region, the source region and the injector region may comprise the same semiconductor.

The device may further comprise a charge balance structure.

The charge balance structure may comprise first and second charge balance regions comprising a semiconductor of the second conductivity type, the first charge balance region extending vertically between the substrate (or bottom surface of a semiconductor region which would have been formed on a substrate) and the source region and the second charge balance region laterally spaced between the p-n junction and the first charge balance region, such that a vertical drift region comprising a semiconductor of the first conductivity type is disposed between the first and second charge balance regions. The charge balance structure may further comprise a third charge balance region comprising a semiconductor of the second conductivity type disposed under the p-n region and extending laterally to the second charge balance region, wherein a lateral drift region comprising a semiconductor of the first conductivity type is disposed over the third charge balance region. The charge balance structure may further comprise a region comprising a semiconductor of the second conductivity type linking the first and

second charge balance regions, the region configured to leave a region comprising a semiconductor of the first conductivity type linking the lateral and vertical drift regions.

According to a third aspect of the present invention there is provided a semiconductor device having an integrated vertical and lateral charge balance structure.

The semiconductor device may comprise a planar substrate, a first conductive region of a first conductivity type extending perpendicularly to the substrate between first and second ends and having at least first and second sides, first and second charge balance regions of second conductivity type disposed on the first and second sides respectively of the first conductive region, a second conductive region of the first conductivity type extending parallel to the substrate between first and second ends and having at least a first side, a third charge balance region of the second conductivity type disposed on the first side of the second conductive region, and the device may further comprise at least one region of the first conductivity type linking the first and second conductive regions so as to form a continuous region of the first conductivity type between the first end of the first conductive region to the second end of the second conductive region and at least one region of the second conductivity type linking the first, second and third charge balance regions so as to form an integrated charge balance structure.

According to a fourth aspect of the present invention there is provided an integrated circuit comprising at least one semiconductor device.

According to a fifth aspect of the present invention there is provided a method of fabricating a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a vertical or lateral insulated gate bipolar transistor, the method comprising providing the insulated gate bipolar transistor with a Schottky-biased p-n junction.

The method may comprise providing a minority-carrier injector which comprises the p-n junction and a Schottky diode, wherein the Schottky diode is arranged in parallel with the p-n junction so as to provide the Schottky-biased p-n junction.

The method may comprise providing a semiconductor region, such as an epitaxial layer of semiconductor material(s), between first and second opposite surfaces (or top and bottom surfaces or faces). The semiconductor region may be formed in stages, e.g. by growing or depositing a first layer of semiconductor material and growing or depositing one or more successive layers of semiconductor material on the first layer. At least a first portion of the semiconductor region may comprise a semiconductor of a first conductivity type, preferably n-type, providing a drift region for majority carriers in a direction between the first and second surfaces. A lateral drift region may also be provided. At least a second portion of the semiconductor region may provide a body region comprising a semiconductor of a second, opposite conductivity type, preferably p-type, disposed at the first surface of the semiconductor region. At least a third portion of the semiconductor region may provide a source region comprising a semiconductor of the first conductivity type disposed at the first surface of semiconductor region and within the body region. The semiconductor region may comprise the same semiconductor, such as silicon or silicon carbide. The minority-carrier injector may be disposed at the first surface of the semiconductor region laterally separated from the body region so as to form a lateral insulated gate bipolar transistor or disposed at the second surface of the semiconductor region vertically separated from body region so as to form a vertical insulated gate bipolar transistor.

At least a fourth portion of the semiconductor region may comprise a semiconductor of the second conductivity type disposed at the first surface of the semiconductor region with a semiconductor of the first conductivity type so as to form the p-n junction. The Schottky diode may comprise a metallization in contact with the first surface of semiconductor region.

The method may further comprise providing a gate structure on the first surface of the semiconductor region. The method may further comprise providing a drain

region on the second surface of the semiconductor region. This may comprise growing the semiconductor region on a semiconductor substrate. Additionally or alternatively, the drain region or contact may include a metallization.

The method may comprise providing a semiconductor substrate drain of a first conductivity type, a drift region of the first conductivity type disposed on the semiconductor substrate drain, a body region of a second, opposite conductivity type, for example formed in or adjacent to the drift region, and a source region of the first conductivity type disposed within the body region.

The method may comprise providing a drift region of first conductivity type on a semiconductor substrate of the first conductivity type, forming a body region of a second, opposite conductivity type within the drift region, forming a source region of the first conductivity type within the body region, and providing the Schottky-biased p-n junction may comprise forming an injector region of the second conductivity type within the drift region, laterally separated from the body region, wherein the injector region and the drift region provide a p-n junction and providing a metallic electrode in contact with the drift region laterally adjacent and electrically connected to the injector region, wherein the metallic electrode and the drain region provide a Schottky diode in parallel with the p-n junction.

According to a sixth aspect of the present invention there is provided a method of fabricating a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor, the method comprising providing a drift region of first conductivity type on a semiconductor substrate of the first conductivity type, forming a body region of a second, opposite conductivity type within the drift region, forming a source region of the first conductivity type within the body region, forming an injector region of the second conductivity type within the drift region, laterally separated from the body region, wherein the injector region and the drift region provide a p-n junction; and providing a metallic electrode in contact with the drift region laterally adjacent and electrically connected to the injector region, wherein the metallic electrode and the drain region provide a Schottky diode in parallel with the p-n junction.

The body region and the substrate may be vertically separated by a first given distance and wherein forming the injector region within the drift region comprises laterally separating the injector region from the body region by a second given distance exceeding the first given distance.

The device may further comprise a depletion reducing region comprising a semiconductor of the first conductivity type disposed within the drift region, more highly doped than the drift region and disposed between the body region and the injector region.

The body region and the substrate may be vertically separated by a first given distance and the body region and the injector region are laterally separated by a second given distance less than the first given distance.

The method may further comprise providing a charge balance structure.

According to a seventh aspect of the present invention there is provided a method of fabricating a semiconductor device, the method comprising providing an integrated vertical and lateral charge balance structure.

Providing the integrated vertical and lateral charge balance structure may comprise providing a planar substrate, providing a first conductive region of a first conductivity type extending perpendicularly to the substrate between first and second ends and having at least first and second sides, providing first and second charge balance regions of second conductivity type disposed on the first and second sides respectively of the first conductive region, providing a second conductive region of the first conductivity type extending parallel to the substrate between first and second ends and having at least a first side, providing a third charge balance region of the second conductivity type disposed on the first side of the second conductive region, providing at least one region of the first conductivity type linking the first and second conductive regions so as to form a continuous region of the first conductivity type between the first end of the first conductive region to the

second end of the second conductive region, and providing at least one region of the second conductivity type linking the first, second and third charge balance regions so as to form an integrated charge balance structure.

According to an eighth aspect of the present invention there is provided a method of operating a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a vertical or lateral insulated gate bipolar transistor having a Schottky-biased p-n junction, the metal oxide semiconductor field effect transistor and insulated gate bipolar transistor sharing a source region (or source/emitter terminal) and a drain region (or drain terminal) and wherein the Schottky-biased p-n junction has a terminal (i.e. an injector and/or collector terminal), the method comprising grounding the source region and applying given bias(es) to the injector/collector terminal and to the drain region. Preferably the same bias is applied to the injector/collector terminal and the drain region.

Brief Description of the Drawings

Certain embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a vertical section of an embodiment of a semiconductor device in accordance with the present invention;

Figure 1a is more detailed view of the semiconductor device shown in Figure 1;

Figure 2 illustrates a set of mask layers used to fabricate the semiconductor device shown in Figure 1;

Figure 3a is a schematic circuit diagram of the semiconductor device shown in Figure 1 before the onset of minority carrier injection;

Figure 3b is a schematic circuit diagram of the semiconductor device shown in Figure 1 after the onset of minority carrier injection;

Figure 4 is a vertical section of the semiconductor device shown in Figure 1 illustrating operation;

Figure 5 schematically illustrates the behaviour of the semiconductor device shown in Figure 1;

Figures 6a to 6p are vertical sections through the semiconductor device shown in Figure 1 at different stages during fabrication;

Figure 7 is a process flow diagram of a method of fabricating the device shown in Figure 1 and part of the device shown in Figure 11;

Figure 8 is a vertical section of another embodiment of a semiconductor device in accordance with the present invention;

Figure 9 is a vertical section of yet another embodiment of a semiconductor device in accordance with the present invention;

Figure 10 is a vertical section of still another embodiment of a semiconductor device in accordance with the present invention;

Figure 11 is a perspective view of a further embodiment of a semiconductor device in accordance with the present invention;

Figure 12 is a plan view of the semiconductor device shown in Figure 11;

Figure 13 is a vertical section of the semiconductor device shown in Figure 12 taken along the line B–B';

Figure 14 is a vertical section of the semiconductor device shown in Figure 12 taken along the line C–C';

Figure 15 is a vertical section of the semiconductor device shown in Figure 12 taken along the line D–D';

Figure 16 is a vertical section of the semiconductor device shown in Figure 13 taken along the line E–E';

Figure 17a is a schematic circuit diagram of the semiconductor device shown in Figure 11 before the onset of minority carrier injection;

Figure 17b is a schematic circuit diagram of the semiconductor device shown in Figure 11 after the onset of minority carrier injection;

Figure 18 schematically illustrates the behaviour of the semiconductor device shown in Figure 11;

Figure 19a to 19d are vertical sections through the semiconductor device shown in Figure 11 at different stages during fabrication of a charge balance structure; and

Figure 20 is a process flow diagram of a method of fabricating a charge balance structure.

Detailed Description of Certain Embodiments

Referring to Figures 1, 1a and 2, an embodiment of a power semiconductor device in accordance with the present invention is shown. The semiconductor device takes the form of a hybrid silicon n-channel vertical metal oxide semiconductor field effect transistor and insulated gate bipolar transistor device 1. The transistor 1 is configured to permit injection of both majority and minority carriers into a drift region.

The transistor 1 includes a heavily-doped n-type monocrystalline silicon substrate 2 which functions as a drain region. An epitaxial layer 3 of lightly-doped n-type monocrystalline silicon (herein also referred to as the "drift region") is arranged on an upper surface 4 of the substrate 2. A field oxide 5 is located at an upper surface of the epitaxial layer 3 and has first and second windows 6_1, 6_2 defining first and second laterally-separated upper surfaces 7_1, 7_2 of the epitaxial layer 3. The first and second windows 6_1, 6_2 have lengths l_1, l_2 of about 6 μm and 4.8 μm respectively and are separated by a length, l_3, of about 7 μm.

A gate oxide 8 is disposed within the first window 6_1 on the upper surface 7_1 of the epitaxial layer 3. The gate oxide 8 runs along the upper surface 7_1 of the epitaxial layer 3 and abuts the field oxide 5 thereby forming a step 9. A layer of heavily-doped n-type polycrystalline silicon 10 (which may also be referred to as the "gate poly") is disposed on the gate oxide 8 and runs over the step 9 onto the field oxide 5. Silicon dioxide spacers 11 are formed on the sides of the gate poly 10.

A p-type body 12 comprising a lightly-doped p-type diffusion well is disposed within the epitaxial layer 3 at the first upper surface 7_1. As shown in Figure 1a, the p-type body 12 extends laterally under the spacer 11 and the gate oxide 8.

First and second p-type injectors 13_1, 13_2 in the form of heavily-doped p-type diffusion wells are located within the epitaxial layer 3 at the second upper surface 7_2. The p-type injectors 13_1, 13_2 are spaced apart to leave a region 14 of the n-type epitaxial layer 3 extending up to the second upper surface 7_2 of the epitaxial layer 3.

An n-type source region 15 in the form of a heavily-doped n-type diffusion well is disposed within the p-type body 12 at the upper surface 7_1. A p-type body short (not shown) in the form of a heavily-doped p-type diffusion well is also provided at the first upper surface using a body short mask (Figure 2).

A layer 17 of silicon dioxide runs over the gate poly 10 and the field oxide 5, and has windows 18_1, 18_2, 18_3. Layers of 19_1, 19_2, 19_3 of metallization are disposed on the silicon dioxide layer 17 covering windows 18_1, 18_2, 18_3. The first metallisation layer 19_1 provides a source/emitter terminal S, the second metallisation layer 19_2 provides a gate terminal G and the third metallisation layer 19_1 provides a collector/injector terminal I. The metallization layers 19_1, 19_2, 19_3 each comprise a bi-layer comprising a high-barrier metal silicide base layer comprising, for example, platinum silicide (PtSi), and a high-conductivity overlayer comprising, for example, aluminium (Al).

As shown in Figure 1a, the third metallisation layer 19_3 is in contact with the first and second p-type injectors 13_1, 13_2 and the n-type region 14 between the p-type

injectors 13_1, 13_2. The p-type injectors 13_1, 13_2 form respective p-n junctions 20_1, 20_2 with the epitaxial layer 3 and the metallisation layer 19_3 forms a Schottky diode 21 with the epitaxial layer 3. Thus, the pair of p-n junctions 20_1, 20_2 and the Schottky diode 21 are arranged in parallel between the metallisation layer 19_3 and the epitaxial layer 3.

The high-barrier metal silicide forms a Schottky diode with the epitaxial layer 3, but forms ohmic contacts to the heavily-doped injector and source regions 13_1, 13_2, 15.

As shown in Figure 1, an inner edge 22 of the p-type body 12 and an inner edge 23 of the p-type injector 13_1 which is closest to the p-type body 12 are separated by a length, L. A bottom 24 of the p-type body 12 is separated from the highly-doped substrate 2 by a depth, d_1. The length, L, approximately equals the depth, d_1, i.e. $L \approx d$, to maintain the breakdown voltage of the device. The separation length, L, and the depth, d, are about 8 μm. As will be explained later, the length, L, can be smaller if a highly-doped field stop region or a charge balance structure is used.

Also as shown in Figure 1, a source-drain depletion region 25 having an edge 26 is formed in the epitaxial layer 3 due to the junction between the p-type body 12 and the n-type epitaxial layer 3. As will be explained in more detail later, the transistor 1 is arranged so that, in blocking mode, the edge 26 of the depletion region 25 does not reach the inner edge 23 of the first injector 13_1.

Referring to Figures 3a and 3b, schematic circuit diagrams of the transistor 1 before and after the onset of minority carrier injection are shown.

Referring in particular to Figure 3a, the transistor 1 includes a MOSFET 28.

The drain of the MOSFET 28 is connected to the drain D of the transistor 1 through a first, vertical resistive element 29_1. The drain of the MOSFET 28 is also connected to a local bias point 30 through a second, lateral resistive element 29_2. The first and second resistive elements 29_1, 29_2 are joined at node 31 at which electron current branches when flowing towards the drain D and the injector I. The

first and second resistive elements 29_1, 29_2 have values R_1 and R_2 respectively. In this example, R_1 and R_2 depend on the depth, d_1, of the epitaxial region 3 and the lateral separation of the p-body region 12 and the Schottky diode 21 respectively.

Referring in particular to Figure 3b, after the onset of minority carrier injection, minority carriers (in this example, holes) flow from the injector I through a bipolar transistor 32 to source S.

Figure 3b shows the flow of majority carriers and minority carriers through the transistor 1 which, in this example, are electrons and holes respectively. When a large minority carrier current flows through bipolar transistor 32 between emitter and collector, a parasitic bipolar transistor 33 may affect operation of the device.

Referring also to Figures 3a, 3b, 4 and 5, operation of the transistor 1 will now be described.

The transistor 1 is arranged so that the source S is grounded and that the drain D and injector I are connected together to a positive voltage V_d. The gate G is used to control the transistor 1 and if a voltage V_g is applied to the gate G and the voltage exceeds a threshold voltage V_{th}, then current flows through the transistor 1 from the source region 15 into the epitaxial region 3.

The transistor 1 can provide an integrated vertical metal oxide semiconductor field effect transistor and lateral insulated gate bipolar transistor.

At low V_d and high V_g, most of the current (which comprises majority carriers, i.e. electrons) flows to the drain D. Thus, the transistor 1 operates in a similar way to a conventional vertical MOSFET, as shown in Figure 3a.

Initially, the potential barriers of the p-n junctions 20_1, 20_2 limit or prevent the flow of majority carriers (i.e. electrons) to injector I. As V_d increases, electron charge builds up in a region 34 beneath the p-type injectors 13_1, 13_2. As charge builds up a depletion region 35 associated with the Schottky diode 21 is reduced. The depletion

region 35 of the Schottky diode 21 has a capacitance $C_{dep(Sch)}$ which varies with the thickness of the depletion region 35. As shown in Figure 3a, the capacitance is shown in series with the Schottky diode 21 which has a resistance, $R_{Schottky}$. The p-n junctions 20_1, 20_2 also have respective depletion regions 36_1, 36_2, each having a capacitance $C_{dep(p-n)}$. As V_d increases further, the depletion region 35 becomes so small that thermionic emission of electrons through the Schottky diode 21 occurs. This biases the region 34 beneath the p-type injectors 13_1, 13_2 below V_d and, thus, forward-biases the p-n junctions 20_1, 20_2. The p-n junction 20_1 forms the emitter-base junction of the bipolar transistor 32. Thus, minority carriers (i.e. holes) are injected into the portion of the epitaxial layer 3 which provides base region. Majority carriers flow through the MOSFET via node 31 to provide a base current to drive the now activated pnp bipolar transistor 32 which passes minority carriers from the injector I to the source S thereby reducing the ON-resistance. Thus, the transistor 1 starts to imitate operation of a conventional IGBT. However, the transistor 1 benefits from low loss conduction with a high saturation current level, which in turn depends on channel geometry.

The Schottky diode 21 helps to dynamically bias the p-n junctions 20_1, 20_2 and ensure that the p-n junctions 20_1, 20_2 continue to inject minority carriers into the base region provided by the epitaxial region 3 at higher V_d unlike, for example, an ohmic resistor. If an ohmic resistor is used instead of the Schottky diode, then the p-n junctions 20_1, 20_2 would initially be forward biased. However, once this occurs, the resistivity of the epitaxial region would drop, allowing the bias in region 34 to fall below that required to forward bias the p-n junctions 20_1, 20_2 resulting in termination of injection of minority carriers.

The bias level within region 34 relative to V_d can be altered depending on the choice of metallisation (which varies the barrier height), the area of the Schottky diode and the operating point of Schottky diode 21. A barrier height of at least 0.7 eV is preferred. For example, the metallization may be platinum silicide with an aluminium overlayer. Platinum silicide has a work function of about 5.2 to 5.8 eV, resulting in a barrier height of around 0.84 eV.

Referring also to Figure 1, the geometry and dimensions of the transistor 1 are chosen so that the depletion layer 25 arising from junction between the p-type body region 12 and the epitaxial layer 3 does not touch the depletion layer arising from the closest p-n junction 20_1. If the depletion layer should touch, then there is no space charge or neutral region between the source (which is at ground) and the injector (which is at V_d) leading to punch through and uncontrolled drain to source current flow. Thus, although injection start up voltage is reduced (in terms of V_d), the closer the injector is to the p-type body region 12, the lateral extent of the depletion layer 25 in blocking mode sets a minimum lateral separation, L.

For silicon, for the dimensions given earlier, the transistor 1 has a breakdown voltage of about 120 V. An array (not shown) of transistors 1 and bond pads (not shown) can be implemented in a chip having an area of about 3.3 mm^2 and can support 10 A of current comprising majority carriers and 70 A of current comprising majority and minority carriers. For silicon carbide, for the dimensions given earlier, the transistor 1 has a breakdown voltage of about 1000 V.

The transistor 1 has a further advantage that if the device heats up (e.g. to 400 K or above) due to a surge current, then this will assist the onset of minority carrier injection, thereby reducing the ON state resistance of the device and, thus lowering, power loss.

Referring to Figures 1, 1a, 2, 6a to 6p and 7, a method of fabricating the semiconductor device 1 will now be described.

Referring in particular to Figures 1 and 2, the device 1 is fabricated using a succession of masks including an active area mask for defining the extent of the field oxide 5, a gate poly mask for defining the extent of the gate poly 10, a p-body mask for defining the p-body well 12, an n-source mask for defining the n-source well 15, a body short mask for defining a body short (not shown), a contact mask for defining openings in the silicon dioxide layer 17 and a metal mask for defining metallization 19_1, 19_2, 19_3.

Referring in particular to Figure 6a, a layer 3' of lightly-doped n-type monocrystalline silicon is grown epitaxially on a highly-doped n-type monocrystalline substrate 2 (step S1). The epitaxial layer 3' is doped *in-situ* during growth with arsenic or antimony to a concentration of about 5×10^{15} cm^{-3} and has a thickness of about 8 μm. In some embodiments, a highly-doped n-type field stop region 37 (Figure 8) can be formed (step S2).

Referring in particular to Figure 6b, a field oxide 5 is formed at the surface 7' (Figure 6a) of the epitaxial layer 3' (Figure 6a) by thermal oxidation using a LOCOS process (step S3). The field oxide 5 has thickness of about 1 μm.

As shown in Figure 6b, the field oxide 5 has first and second windows 6_1, 6_2 defining first and second laterally-separated upper surfaces 7_1, 7_2 of the epitaxial layer 3.

Referring in particular to Figure 6c, a layer 8' of silicon dioxide is grown by thermal oxidation on the upper surfaces 7_1, 7_2 of the epitaxial layer 3 (step S4). The silicon dioxide layer 8' has a thickness of about 1,500 Å.

Referring in particular to Figure 6d, a layer 10' of heavily-doped n-type polycrystalline silicon is grown by chemical vapour deposition (CVD) over the silicon dioxide layer 8' and field oxide 5 (step S5). The polycrystalline layer 10' is doped *in-situ* during growth with phosphorous or arsenic to a concentration equal to or greater than about 1×10^{20} cm^{-3} and has a thickness of about 3,000 Å. Instead of *in-situ* doping, an undoped polycrystalline layer 10' can be grown and doped by ion implantation after growth.

A layer (not shown) of photoresist is applied over the polycrystalline layer 10' and is patterned to form a mask (not shown). The mask pattern is transferred to the underlying polycrystalline layer 10' and silicon dioxide layer 8' by reactive ion etching (RIE) using suitable feed gases (step S6).

Referring in particular to Figure 6e, the resulting structure includes the gate poly 10 and gate oxide 8.

Referring in particular to Figure 6f, with the mask (not shown) still in place, a further layer (not shown) of photoresist is applied and patterned so as to protect the epitaxial layer 3 in the second window 6_2. Boron ions are implanted at an energy between about 20 to 160 keV.

Referring to Figure 6g, the masks (not shown) are removed and the structure is annealed to activate the implant leaving a p-type well 12 doped to a concentration of between about 1×10^{17} cm^{-3} and about 5×10^{18} cm^{-3} and having a depth of about 0.7 to 1.2 μm (step S7).

Referring to Figure 6h, a conformal layer (not shown) of silicon dioxide is deposited and globally etched back by RIE using suitable feed gases to form a spacer 11 around the sides of the gate poly 10 (step S8).

Referring in particular to Figure 6i, a layer (not shown) of photoresist is applied and patterned so as to protect the epitaxial layer 3 in the second window 6_2. Arsenic ions are implanted into the epitaxial layer 3 in the first window 6_1 at an energy of about 40 keV.

Referring to Figure 6j, the mask (not shown) is removed and the structure is annealed to activate the implant leaving an n-type well 15 doped to a concentration of between about 1×10^{20} cm^{-3} and about 3×10^{20} cm^{-3} and having a depth of about 1,000 Å to 5,000 Å (step S9).

Referring to Figure 6k, a layer (not shown) of photoresist is applied and patterned to open a small hole over the first window 6_1 and two narrow windows (not shown) over the second window 6_2. Boron ions are implanted into the epitaxial layer 3 in the second window 6_2 at an energy of about 40 keV.

Referring to Figure 6l, the mask (not shown) is removed and the structure is annealed to activate the implant leaving an p-type body short (Figure 2) and p-type injectors 13_1, 13_2 doped to a concentration of between about 1×10^{20} cm^{-3} and about 3×10^{20} cm^{-3} and having a depth of about 1,000 Å to 5,000 Å (step S10).

Referring to Figure 6m, another layer 17' of silicon dioxide having a thickness of about 4,000 Å is deposited (step S11).

A layer (not shown) of photoresist is applied over the silicon dioxide layer 17' and is patterned to form a mask (not shown). The mask pattern is transferred to the underlying silicon dioxide layer 17' by RIE using suitable feed gases (step S12).

Referring in particular to Figure 6n, the resulting structure includes a patterned silicon dioxide layer 17 with contact windows 18_1, 18_2, 18_3.

Referring to Figure 6o, the mask (not shown) is removed and a layer 19' of a first metallization layer comprising platinum is deposited by physical vapour deposition (PVD) (step S13). The metallization is annealed using one or more rapid thermal anneals (RTA). Unreacted platinum is removed using aqua regia. A second metallization layer comprising aluminium is deposited by PVD having a thickness of about 10,000 Å.

A layer (not shown) of photoresist is applied over the metallization 19' and is patterned to form a mask (not shown). The mask pattern is transferred to the underlying metallization 19' by RIE using suitable feed gases (step S14).

Referring in particular to Figure 6p, the resulting structure comprises metallization contacts 19_1, 19_2, 19_3.

It will be appreciated that layer thicknesses and process parameters can be varied and optimised and that the fabrication process can include other steps, such as substrate thinning and depositing a metallization on the back side of the substrate.

Referring to Figure 8, another embodiment of a power semiconductor device 1' in accordance with the present invention is shown. The device 1' is shown in simplified form, for example, as can be used in numerical simulations.

The device 1' is substantially the same as the device 1 (Figure 1) hereinbefore described, but differs in that it includes a field stop region 37 and has different dimensions.

The field stop region 37 takes the form of a shallow n-type diffusion well disposed at the upper surface of the epitaxial layer 3 under the field oxide 10 between p-type body region 12 and the p-type injector 13_1. The field stop region helps to restrict the depletion layer width laterally and improve performance of the bipolar transistor 32 (Figure 3b).

This allows the lateral dimension of the device 1' to be reduced, in particular, a shorter separation length, L, of about 4 μm. The depth of the device, d_2, can have a value in a range of about 8 μm to 10 μm, although the depth can be higher or lower depending on required operating voltage. The half-cell width of the device, w_2, can be about 7 μm to 11 μm. Again, the width, w_2, can be larger or smaller depending on operating voltage.

Referring to Figure 9, yet another embodiment of a power semiconductor device 1" in accordance with the present invention is shown.

Referring to Figures 8 and 9, the device 1" is substantially the same as the device 1' hereinbefore described, but differs in that the position of the first injector 13_1 is moved away from the -type body region 12 and does not extend to the edge of the oxide 10, 17. The second injector 13_2 may be omitted. Thus, the positions of the p-n junction 20_1 and the Schottky diode 21 are swapped.

The device 1" is fabricated using a modified mask for the p-type implant at step S10 above.

Operation the device 1" is substantially the same as device 1'. In particular, there is no detrimental effect on blocking voltage. However, the onset of injection occurs at a slightly higher source-drain voltage. For example, for the device 1' shown in Figure 8, simulation shows that hole injection starts at voltage of about 1.7 V at a temperature of 300 K and, for the device 1" shown in Figure 9, simulation shows that hole injection starts at voltage of about 1.9 V at a temperature of 300 K. This is thought to be due to the slightly increased distance from the channel to the injector 13_1.

Referring to Figure 10, another embodiment of a power semiconductor device 1'" in accordance with the present invention is shown.

The device 1'" is similar to the devices hereinbefore described except that the device 1'" employs a vertical injector rather than a lateral injector. Thus, the injectors 13_1', 13_2' and Schottky diode 20' can be placed at a lower surface 38 of the epitaxial layer 3 on the underside of a thinned substrate (not shown).

The Schottky diode 20' comprises a pad 39 directly in contact with the epitaxial layer 3 adjacent to or between p-type well(s) 13_1', 13_2'. The pad 39 is formed by a layer of a first metallization, such as platinum silicide or other metallization providing a barrier height of at least 0.7 eV.

The drain contact comprises a layer 40 of a metallization in contact with the epitaxial layer 3 which forms an ohmic contact to the epitaxial layer. The metallization is preferably alloyed or annealed. The metallization may comprise aluminium or aluminium silicide. The layer 40 may run over the pad 39. Alternatively, it may laterally abut the pad 38. In some embodiments, the layers 39, 40 may not join or overlap, but may be connected in some other way, e.g. by a bond wire or high-temperature solder.

The device 1'" having a vertical injector operates in a similar way to the devices having a lateral injector. However, one difference is that the injector uses vertical

biasing. The biasing depends on the amount of electron charge in the area immediately above the Schottky diode 21'.

Using the vertical injector, there is no detrimental affect to one-dimensional (that is, doping-dependent) blocking voltage.

The blocking voltage performance is set by the drift region thickness, d_3, from the bottom of the p-body region 12 to the drain. In some embodiments, $d_3 = d_1$. Neighbouring p-body regions 12 provide mutual protection to the radius of curvature, thus minimising the electric field in that area.

The device 1''' has the advantage that, due to the position of the injector, no separate bond wire or connection is required from front to back face. It may also allow a heat sink (not shown) to be placed more easily on top of the source metallization to help dissipate heat.

The placement of the injector can allow a smaller cell width to be used and so reduce the drain-source specific resistance per unit area in a pre-injection state and in an injection state compared to the embodiments using a lateral injector.

Furthermore, injector elements can be evenly distributed across the underside of the wafer and so help to ensure an even current share across the resultant device area once injection begins.

Moreover, the use of electrons available from two voltage-controlled, gated MOS channels per injector, instead of a single channel per injector, as in transistor 1 (Figure 1) allows for an increased current saturation level.

As described earlier, a Schottky-biased injector can be used to reduce the ON resistance of a vertical MOSFET. The blocking voltage of the hybrid device depends on the thickness and doping concentration of the drift region 3, as well as the radius of curvature of the p-type body 12.

One way to increase the blocking voltage in a conventional power MOSFET is to increase the doping density of the n-type drift region and include charge compensating structure comprising regions of p-type material on either side of the drift region as described, for example, in "COOLMOS™-a new milestone in high voltage power MOS" by L. Lorenz, G. Deboy, A. Knapp and M. Marz, Proceedings of the 11th International Symposium on Power Semiconductor Devises and ICs, pages 3 to 10 (1999). Reference is also made to "Theory of Semiconductor Superjunction Devices" by T. Fujihara, Japanese Journal of Applied Physics, volume 36, part 1, number 10, pages 6254 to 6262 (1997) which introduces the use of alternatively stacked p- and n-type, heavily doped thin semiconductor layers. However, such charge compensation structures are unsuitable for a hybrid device since the charge compensation structure would restrict lateral flow of majority carriers to the injector.

However, a modified form of charge compensation structure can be used not only to allow the flow of majority carriers to the injector, but also to direct their flow. Thus, the modified charge compensation structure can be adapted to control the voltage at which IGBT-like action occurs.

Referring to Figures 11 to 16, a further embodiment of a power semiconductor device 101 in accordance with the present invention is shown. The semiconductor device 101 takes the form of a hybrid silicon n-channel vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor device comprising a combined vertical and lateral charge balance structure 131. The device 101 is also hereinreferred to as a "super junction device".

The super junction device 101 includes a heavily-doped n-type monocrystalline silicon substrate 102 which functions as a drain region. An epitaxial layer 103 of silicon is arranged on an upper surface 104 of the substrate 102. As will be explained later, the epitaxial layer 103 comprises p-type and n-type regions which provide the charge balance structure 131.

The structure of super junction device 101 at the upper surface 107 of the epitaxial layer 103 is generally the same as that of the device 1 shown in Figures 1 and 1a.

A field oxide 105_1, 105_2 is located at the upper surface 107 of the epitaxial layer 103 and has first, second and third windows (not shown) defining first, second and third laterally-separated portions of upper surfaces 107 of the epitaxial layer 103.

In the following description, a first half of a full cell is described.

A first gate oxide 108_1 is provided on the first portion of the upper surface 107 of the epitaxial layer 103. The first gate oxide 108_1 runs along the first portion of the upper surface 107 of the epitaxial layer 103 and abuts the first field oxide 105_1. A first layer of heavily-doped n-type polycrystalline silicon 110_1 is disposed on the first gate oxide 108_1.

A first p-type body 112_1 comprising a lightly-doped p-type diffusion well is disposed within the epitaxial layer 103 at the first portion of the upper surface 107. The first p-type body 112_1 extends laterally under a first spacer 111_1 and the first gate oxide 108_1.

First and second p-type injectors 113_1, 113_2 in the form of heavily-doped p-type diffusion wells are located within the epitaxial layer 103 at the second portion of the upper surface 107. The p-type injectors 113_1, 113_2 are spaced apart to leave a region 114 of n-type epitaxial layer 103 extending up to the second portion of the upper surface 107 of the epitaxial layer 103. The injectors 113_1, 113_2 straddle the centre of the cell.

A first n-type source region 115_1 in the form of a heavily-doped n-type diffusion well is disposed within the first p-type body 112_1 at the upper surface 107. A p-type body short (not shown) in the form of a heavily-doped p-type diffusion well is also provided at the first upper surface.

A layer (not shown) of silicon dioxide runs over the first gate poly 10 and the first field oxide 105 and has windows (not shown). A first metallisation layer 119_1 provides a first source/emitter terminal S1, a second metallisation layer (not shown) provides a first gate terminal G1 and a third metallisation layer 119_3 provides a collector/injector terminal I. The metallization layers 119_1, 119_3 each comprise a bi-layer comprising a high-barrier metal silicide base layer comprising, for example, platinum silicide, and a high-conductivity overlayer comprising, for example, aluminium.

Similar to the device 1 shown in Figures 1 and 1a, the third metallisation layer 119_3 is in contact with the first and second p-type injectors 113_1, 113_2 and the n-type region 114 between the p-type injectors 113_1, 113_2. The p-type injectors 113_1, 113_2 form respective p-n junctions 145_1, 145_2 (Figures 17a and 17b) with the epitaxial layer 103 and the metallisation layer 119_3 forms a Schottky diode 146 (Figures 17a and 17b) with the epitaxial layer 103. Thus, the pair of p-n junctions (not shown) and the Schottky diode (not shown) are arranged in parallel between the metallisation layer 119_3 and the epitaxial layer 103.

The high-barrier metal silicide forms a Schottky diode with the epitaxial layer 103, but forms ohmic contacts to the heavily-doped injector and source regions 113_1, 113_2, 115_1.

The second half of the cell is a mirror image of the first half and includes a second field oxide 105_2, a second gate oxide 108_2, a second p-type body 112_2, a second source region 115_2, a second source/emitter terminal S2 and a second gate terminal G2. However, as explained earlier, the first and second injectors 113_1, 113_2 straddle the centre of the cell and injector I is shared by both halves of the cell.

The epitaxial layer 103 comprises alternating stripes (or "walls" or "columns") of p-type and n-type regions 132_1, 132_2, 133_1, 133_2, 134_1, 134_2, 135 extending up from the substrate 102 (i.e. along the z-axis) and in a direction along the length of the device (i.e. along the y-axis). As will be explained later, these alternating n-type and p-type

regions 132_1, 132_2, 133_1, 133_2, 134_1, 134_2, 135 provide a first, vertical charge balance structure.

As shown particularly in Figures 13 and 14, first and second, outer p-type regions 132_1, 132_2 are disposed under the p-type body regions 112_1, 112_2. The p-type regions 132_1, 132_2 extend from the substrate 102 and reach the bottoms of the respective p-type body regions 112_1, 112_2.

Third and fourth inner p-type regions 134_1, 134_2 are disposed between the outer p-type regions 132_1, 132_2.

A first n-type region 133_1 is formed between the first and third p-type regions 132_1, 134_1. Likewise, a second n-type region 133_2 is formed between the second and fourth p-type regions 132_2, 134_2. As will be explained later, the first and second n-type regions 133_1, 133_2 form a vertical path through which majority carriers (i.e. electrons) from the source regions 115_1, 115_2 can flow to reach the substrate 102.

A third n-type region 135 is formed between the third and fourth p-type regions 134_1, 134_2. This forms a voltage sustaining region.

Referring in particular to Figures 11, 13 and 14, the p-type regions 132_1, 132_2, 134_1, 134_2 are interconnected by lateral, bridge-like, p-type linking regions 136_1, 136_2 and by a buried p-type cross layer 137 (which collectively may be referred to as "p-type ground links" as the p-type body regions 112_1, 112_2 are connected to ground). The buried p-type cross layer 137 forms part of a second, lateral charge balance structure

Referring in particular to Figure 13, the third and fourth p-type regions 134_1, 134_2 and the p-type cross layer 137 form a core structure generally having the appearance of an inverted parallel flange channel, i.e. an elongate structure which is 'n'-shaped in cross section.

Referring also to Figures 11 and 14, the outer p-type walls 132_1, 132_2 flank the core structure 134_1, 134_2, 137 and are joined to the top of the core structure at intervals

along its length by the linking regions 136_1, 136_2 which extend laterally from the p-type cross layer 137 and so form a unitary p-type region, i.e. a single continuous region of p-type semiconductor.

The first and second n-type regions 133_1, 133_2 (herein referred to as the "lower drift regions") are connected by short, vertical, column-line, n-type linking regions 141_1, 141_2 (which are also referred to as "linking drift regions") to a n-type surface layer 142 (herein referred to as the "upper drift region") and so form a unitary n-type region. The third n-type region 135 does not form part of the unitary n-type region.

The column-like, n-type linking regions 141_1, 141_2 pass between the p-type linking regions 136_1, 136_2 such that the p-type and n-type unitary regions interlock or interlace.

Referring also to Figure 13, in the interlocking arrangement, majority carriers (i.e. electrons) from the source regions 115_1, 115_2 can flow into the upper drift region 142. Majority carriers can then flow through the n-type linking drift regions 141_1, 141_2 and into the lower drift regions 133_1, 133_2 towards the drain 102. Majority carriers can also flow through the upper drift region 142 towards the injector 113_1, 113_2.

Thus, this arrangement allows a hybrid silicon n-channel vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor device to benefit from a charge balanced structure.

In particular, the charge balanced structure allows the thickness of the device (i.e. the dimension along the z-axis) to be reduced because the electric field generated by applying a source-drain voltage (with gate-source voltage of 0 V) is distributed laterally (along the x-direction), thereby driving electrons towards the n-type columns 133_1, 133_2 and holes towards the p-type columns 132_1, 132_2, 134_1, 134_2.

A space charge region (not shown) is formed which spreads out along a vertical p-n junction (not shown). The lower drift regions 133_1, 133_2 are depleted and act like the voltage sustaining layers of a PIN diode structure.

The source-drain voltage required to reach a critical electric field is now much higher than a similar device without a charge balance structure. Thus, to obtain the same blocking voltage, the length of the drift region can be reduced, which reduces the resistance of the drift region length. In addition, use of the vertical charge balance structure allows the doping of the n-type drift regions to be increased by about an order of magnitude or more, for example, from about 5×10^{15} cm^{-3} to about 5×10^{16} cm^{-3}. The higher doping concentration results in a further reduction in drift region resistance.

The reduction in the thickness of the device (i.e. along the z-axis) and the lower resistivity can help to significantly reduce the resistance of the lower drift regions, while maintaining or even increasing blocking voltage. The charge balance structure allows the device to break the so-called "silicon limit" in one dimension defined by:

$$sRon \approx 3.7\times10^{-9}.\ (BV)^{2.6} \qquad (1)$$

where sRon is the specific ON resistance (in $\Omega.cm^2$) and BV is the blocking voltage (in V). Reference is made to "On the Specific On-Resistance of High-Voltage and Power Devices", by R. Zingg, IEEE Transactions on Electron Devices, volume 51, number 3, page 492 (2004) which describes that, for the same level of current and the same active area, forward voltage drop across a charge balanced MOSFET is lower than that across a normal device, thus improving transconductance.

The super junction device 101 has a lateral charge balance structure configured such that a lateral blocking voltage for the lateral insulated-gate bipolar transistor is the same or similar to the vertical blocking voltage for vertical metal-oxide semiconductor field effect transistor. The lateral charge balance structure helps to shield the radius of curvature of the p-type body regions 112_1, 112_2.

Referring to Figure 17a, a schematic circuit diagram of the super junction device 101 prior to the onset of injection is shown. The device 101 includes a MOSFET 143, a bipolar transistor 144 which includes p-n junctions 145_1, 145_2 (forming the emitter to base junction) and a Schottky diode 146. In this example, the bipolar transistor 144 is a pnp transistor.

The drain 147 of the MOSFET 143 is connected to the drain D of the transistor 101 through a first, vertical resistive element 148_1 and to the base 149 of the bipolar transistor 144 via a second, lateral resistive element 148_2. The first and second resistive elements 148_1, 148_2 are joined at node 150 at which electron current branches. The first and second resistive elements 148_1, 148_2 have values $R_{vertical}$ and $R_{lateral}$ respectively. As shown in Figure 17a, the Schottky diode 146 has a depletion region 151 having a capacitance $C_{dep(Sch)}$ which varies with the thickness of the depletion region 151. The capacitance is shown in series with the Schottky diode 146 which has a resistance, $R_{Schottky}$. The p-n junctions 145_1, 145_2 also have respective depletion regions 152_1, 152_2, each having a capacitance $C_{dep(p-n)}$.

Figure 17b shows the flow of majority carriers and minority carriers through the transistor 101 which, in this example, are electrons and holes respectively. When a large minority carrier current flows through bipolar transistor 144, a parasitic bipolar transistor 153 may affect operation of the device.

Referring to Figures 14, 17a and 18, as explained earlier, at a low drain voltage (V_d) and a high gate voltage (V_g), the device operates principally as a MOSFET, electrons flow mainly from the source S to the drain D. However, enabled by the p-type ground links 136_1, 136_2, a small proportion of the electrons flow to the injector 113_1, 113_2 via a lateral resistance 148_2, which are used to bring about IGBT-action.

These electrons are unable to flow to the injector, I, as they are prevented by the potential barriers of the p-n junction within the base-emitter region 145_1, 145_2, 149 of the bipolar transistor 144 and by the parallel Schottky diode 146.

As the drain voltage, V_d, increases, the electron charge (and the potential) in the base 149 is increased. The width of the depletion region 151 associated with the Schottky diode 146 is reduced.

As the drain voltage, V_d, increases further, the potential barrier is overcome and thermionic emission of electrons via the Schottky diode 146 starts, thereby biasing the region 149 beneath the p-type injectors 113_1, 113_2 below V_d and, thus, forward biasing the p-n junctions 145_1, 145_2 within the base-emitter region of the bipolar transistor 144.

Referring to Figure 17b, once the p-n junctions 145_1, 145_2 are forward-biased, the Schottky diode 146 acts to maintain that bias thereby ensuring that any change in resistance of the second resistive element 149_2 due to increased electron concentration does not de-bias the emitter to base junction. Minority carriers flow via the bipolar transistor 144, p-body regions 112_1,112_2 and body short (not shown) to the source S.

By varying the number and dimensions of p-type ground links 136_1, 136_2 (Figure 15) to n-type linking regions 141_1, 141_2 (Figure 15), the charge balance structure offers a way of controlling the ratio of electrons flowing to the substrate 102 and injector 113_1, 113_2 and, thus, set the onset of IGBT-action, as well providing other benefits and features, as will now be described in more detail.

Firstly, the charge balance structure, in particular the p-type cross layer 137 and upper drift region 142, provides a reduced surface field (RESURF)-like distribution of electric field resulting in a reduction in electric field at the surface between the oxide 105_1, 105_2 and the upper drift region 142. This helps to maintain the one-dimensional (that is, doping-dependent) blocking voltage for the interface between the p-type body region 112_1, 112_2 and the upper drift region 142.

Secondly, the lateral distance, L, between the channel and injector can be reduced without the risk of punch-through, as the extent of the depletion region (not shown) from the p-body regions 112_1, 112_2 can be reduced by increasing the doping

concentration in the upper drift region 142. Furthermore, the doping concentration in the upper drift region 142 and the lower drift regions 133_1, 133_2 can be independently controlled (that is, they can have different doping concentrations). The flow of electrons from the n-type source regions115_1, 115_2 to the injectors 113_1, 113_2 and the substrate 102 can be independently controlled.

Referring also to Figures 12 and 15, the ratio, R, of the areas (in the x-y plane) of the p-type linking regions 136_1, 136_2 and the n-type linking regions 141_1, 141_2, i.e. (k×m):(k×n), can be set to control the proportion of electrons flowing laterally towards the injectors 113_1, 113_2 through the upper drift region 142, i.e. set R_1 and R_2 respectively.

This can be used to tune the device 101 to ensure that the injectors 113_1, 113_2 turn on at a given source-drain voltage.

At the onset of injection, minority carriers (i.e. holes) travel to the sources 112_1, 112_2 via the p-type linking regions 136_1, 136_2.

In this example, the ratio, R, has a value of about 1:10. However, the ratio, R, can have a value, for example, between about 1:5 to about 1:20. For a value of about 1:10, the p-type linking regions 136_1, 136_2 do not appreciably inhibit electron flow to the drain.

Referring still to Figures 13, 14, 17a, 17b and 18, since injected holes flowing to the source S via p-type body regions 112_1, 112_2 mainly take a different path to electrons flowing to the substrate 102, they do not interfere and do not recombine in the region adjacent to the channel. This leads to improved transconductance of the pnp transistor 144 characteristic once conductance begins when the electron-limited current saturated state is removed. In the devices hereinbefore described, this state tends to require further electron charge build up next to the channel to provide a potential barrier to holes before the device fully conducts via the pnp transistor 144.

In the charge balanced structure, the ability to control electrons flowing to the injector and to the base 148 of the pnp transistor 144 provides another parameter which can be controlled. Using a low contact resistance for the injector, automatic de-biasing of the pnp transistor 144 can occur which can help to avoid localisation of current and ensure that emitter current is evenly distributed.

Referring in particular to Figures 13, 14, 17a and 17b, the base region 148 of the pnp transistor 144 within the charge balanced structure is fixed by the gap having a thickness, b. The thickness of the gap can be optimised to ensure adequate effective base thickness of the pnp transistor 144 to provide improved levels of pnp emitter current gain for the limited levels of base drive available via the metal-oxide-semiconductor channel. The base thickness, b, is relatively unaffected by any growing depletion width from the p-type body regions 112_1, 112_2 as the source-drain voltage increases. In contrast, in the device 1 shown in Figures 1 and 1a, as the source-drain voltage increases, the base thickness is reduced and so pnp current gain, hFE, increases.

The behaviour of pnp gain in the transistor 1 shown in Figure 1 differs from a conventional pnp device as a conventional device is fabricated with minimum base width, whereas base region within the transistor 1 (Figure 1) is relatively large and results in low gain. The effective base width is reduces as source depletion region extends laterally towards region 13_1 (Figure 1) and so gain improves with source-drain voltage. In the super junction device 101, the base width is set by fabrication to have a high gain and the doping in the base region 149 is preferably sufficiently high so as to avoid collector to emitter punch-through.

The thickness of the p-type cross layer 137 can be adjusted for both doping density and vertical thickness, s, along the z-axis. The doping in the p-type cross layer 137 is chosen to balance the doping in the top n-type layer 142. The ability to alter the thickness of the p-type cross layer 137 allows optimisation of the charge balance structure and extent of the depletion from the p-type body regions 112_1, 112_2 into n-type regions 141_1, 141_2, 142. Furthermore this can be achieved without compromising MOSFET performance as the drift length (not shown) need not be

increased as the p-type cross layer 137 thickness, s, is increased. Any such increase in thickness, s, reduces the z-dimension of the voltage sustaining, n-type region 135, which is not critical.

In the device 1 shown in Figures 1 and 1a, the minimum lateral resistance is limited by punch-through thereby setting a minimum distance, L, between the edge 22 of the p-body 12 and the edge 23 of the injector region 13_1. The minimum lateral resistance also sets a minimum length for the drift region. This is because, if the vertical resistance is reduced, the ratio of lateral resistance to vertical resistance would be reduced below a minimum value for a sufficient proportion of electrons to reach the injector region 13_1. This can make it difficult to improve the ON state resistance prior to the onset of injection.

Assuming a fixed work function for the Schottky contact, the distance from the edge of the channel 122_1 to the edge of the injector 113_1 effectively controls the value of source-drain voltage needed bring about the onset of conductivity modulation of the drift region by the injector. Using the charge balanced structure, the lateral distance can be greatly reduced and so provide way to further reduce the injection start-up voltage. Thus, a wider range of injection start-up voltages can be used.

The charge balanced structure allows all of the channel area to participate in injecting electrons into the n-type regions 133_1, 133_2 to the drain 102.

Holes are restricted to the upper layers bounded by the p-type cross layer 137. This has the effect of reducing the switch off time as the holes can easily reach the p-type body 112_1, i.e. the collector of the bipolar transistor 144, with minimal travel. Unlike a conventional IGBT, there is no need to wait for recombination since recombination is not the only means of charge removal.

The device 1 shown in Figure 1 has been simulated in an un-clamped inductive switching test circuit and has shown to be free of latch-up. The transistor 101 also has the potential to provide latch-up-free operation as the mechanism for charge

removal from the drift region is via the p-type grounding channels 136_1, 136_2, 137 for holes to the p-type body regions 112_1, 112_2 and via the drift region to the drain 102 for electrons. Even if a parasitic npn bipolar transistor 152 started conducting, then electrons collected in the drift region (which serves as the npn collector) simply find their way to the drain 102 thereby contributing to the MOSFET current. The parasitic npn transistor 152 will therefore switch off when the channel restricts the electron base drive to the pnp transistor 144. This in turn removes any hole current to the source S via the p-type body regions 112_1, 112_2. Thus, there is no sustained base bias to the bipolar transistor 144 to cause latch-up

The devices 1 (Figure 1), 101 (Figure 11) benefit from greatly improved switch off time similar to that achieved by a conventional unipolar MOSFET. As hereinbefore described, charge storage does not occur in the devices 1 (Figure 1), 101 (Figure 11), unlike conventional IGBTs, which would otherwise have the effect of greatly increasing switch off time. The devices 1 (Figure 1), 101 (Figure 11) therefore benefit from low ON state loss, available from a source-drain voltage of ≥ 0.1 V with fast switching capability.

The devices 1 (Figure 1), 101 (Figure 11) also provide a mechanism to "self clamp" when switching inductive loads, thus preventing the device going into avalanche from which recovery times can be long.

The devices 1 (Figure 1), 101 (Figure 11) do not suffer from the so-called "snap-back" phenomenon associated with other devices capable of MOSFET-IGBT hybrid operation, for example, as described in "The Bi-mode Insulated Gate Transistor (BIGT) a potential technology for higher power applications" by M. Rahimo, A. Kopta, U. Schlapbach, J. Vobecky, R. Schnell and S.Klaka, Proceedings of the 22nd International Symposium on Power Semiconductor Devises and ICs, pages 391 to 394 (2010). In the devices 1 (Figure 1), 101 (Figure 11), the Schottky-biased injector ensures a smooth transition between MOSFET-like and IGBT-like conduction states.

Finally, with increasing ambient heat-sink temperatures, for example up to 400 K, the potential barrier between the p-type and n-type regions will decrease. This is because, as the device heats up, bipolar conduction is activated at a lower source-drain voltage. A reduction in ON state voltage with increasing temperature is helpful in a device experiencing surge current.

The device 101 is fabricated in a similar to way to the device 1 shown in Figures 1 and 1a.

However, instead of growing an epitaxial layer of lightly-doped n-type monocrystalline silicon (step S1, Figures 6a and 7), an epitaxial layer of monocrystalline silicon having appropriate n-type and p-type regions for providing the charge balance structure is formed.

Referring to Figures 19a to 19d and 20, a method of fabricating an epitaxial layer for providing the charge balance structure will now be described.

Figure 19a shows a highly-doped n-type monocrystalline substrate 103.

P-type and n-type columns 132_1', 133_1', 134_1', 135, 132_2', 133_2', 134_2' are formed (step S1A).

The columns can be formed 132_1', 133_1', 134_1', 135, 132_2', 133_2', 134_2' by growing a plurality of epitaxial layers (not shown) of lightly doped n-type, monocrystalline silicon and, for each epitaxial layer, doping regions of the epitaxial layer with acceptors to compensate for the n-type doping and to provide excess acceptors to dope the regions p-type. For example, this may be achieved by masking regions of an epitaxial layer (not shown), doping unmasked regions of the using an acceptor, such as boron. The n-type layers (not shown) are doped to a concentration of about 5×10^{16} cm^{-3}. The p-type regions are doped to a net concentration of about 5×10^{16} cm^{-3}. Alternatively, the columns can be formed by growing layers of lightly doped p-type silicon may be deposited and, for each epitaxial layer, doping regions of the epitaxial layer with donors. In some embodiments, the columns can be

formed by growing undoped layers and, for each epitaxial layer, selectively doping respective regions of the epitaxial layer with acceptors and donors. Doping can be performed by ion implantation. The structure is annealed to activate the implants. The process can be repeated for each epitaxial layer until the columns can have a suitable thickness, d_3, e.g. between about 10 and 50 μm. Between 2 and 10 or more epitaxial layers can be used.

Alternatively, the columns 132_1', 133_1', 134_1', 135, 132_2', 133_2', 134_2' can be formed by growing an epitaxial layer of lightly-doped n-type monocrystalline silicon. The epitaxial layer (not shown) can be doped *in-situ* during growth with a donor to a concentration of about 5×10^{16} cm^{-3} and has a thickness of between about 10 and 50 μm. A dielectric layer (not shown) is formed on the epitaxial layer (not shown) and it patterned to form an etch mask. Then, trenches (not shown) are formed by dry etching which reach the substrate 102. The trenches (not shown) can be filled by epitaxially growing lightly-doped p-type monocrystalline silicon. In some embodiments, more than one epitaxial layer can be deposited, etched and filled.

As shown in Figure 19b, the outer, p-type columns 132_1', 132_2' have length (along the x-axis), q_1, of between about 0.5 μm to about 5 μm. The n-type columns 133_1', 133_2' can have a length, q_2, of between about 0.5 μm to about 5 μm. The inner p-type columns 134_1', 134_2' can have a length, q_3, of between about 0.5 μm to about 5 μm. The central, n-type column 135 can have a length of about 0.5 μm to about 30 μm.

Referring in particular to Figure 19c, the p-type cross layer 137 and the rest of the outer p-type columns 132_1, 132_2, the p-type linking regions 136_1, 136_2 (Figure 14), the n-type linking regions 141_1, 141_2 (Figure 13) are formed (step S1B). A similar process to one of those described earlier for forming the columns can be used. The regions are doped to a concentration of about 5×10^{16} cm^{-3}. The thickness, s, of the p-type cross layer 137 can be between about 0.5 μm to about 5 μm.

Referring in particular to Figure 19d, a layer 154 of lightly doped n-type monocrystalline silicon is epitaxially grown (step S1C). The epitaxial layer 154 can

be doped *in-situ* during growth with a donor to a concentration of about 5×10^{16} cm^{-3} and can have a thickness, t, of between about 1 and 2 μm.

The values of lengths q_1, q_2, q_3, q_4 and values of thicknesses d_3, s, b and t can be found by routine experiment and/or by computer simulation using, for example, a bespoke or commercially-available Poisson solver. Different p-type and n-type doping concentrations may be used. The doping concentrations can differ between the lower drift regions 133_1, 133_2 and the upper drift region 142. The doping concentrations can differ between the inner p-type columns 134_1, 134_2 and the buried p-type cross layer 137.

The rest of the device can be fabricated in substantially the same way as that described earlier using steps S3 to S14 (Figure 7).

It will be appreciated that many modifications may be made to the embodiments hereinbefore described.

The semiconductor device may be a p-channel device. Thus, the drift region, the body region, the source region and injector regions may take the form of a lightly-doped p-type semiconductor material, lightly-doped n-type semiconductor material, heavily-doped p-type semiconductor material and heavily-doped n-type semiconductor material respectively. Thus, the majority carriers may be holes instead of electrons and the minority carriers may be electrons instead of holes.

The semiconductor device may be based on silicon carbide. For example, the substrate may comprise 4H or 3C polytypes. The drift region and the body, source and injector regions may comprise silicon carbide. Other elemental or compound semiconductors, such as GaN, can be used.

Other metallizations can be used to provide the high Schottky barrier.

A single continuous metallization forming a Schottky contact and an ohmic contact to the p-n junctions need not be used. Separate layers of metallization (which may

comprise different materials) can be used and may be connected, for example, by an overlayer or by a bond wire.

Processing steps and process parameters may be altered and optimised. For example, doping concentrations, dopant ions, ion-implant energies can be varied. Methods of deposition and methods of etching can also be varied. Also, dielectric materials can be altered. For example, silicon dioxide need not be used and can be replaced, for example, by silicon oxynitride or high-k dielectrics.

A gate metallization may be used instead of gate poly, for example, comprising tungsten (W).

Claims

1. A semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a vertical or lateral insulated gate bipolar transistor having a Schottky-biased p-n junction (20_1; 145_1).

2. A semiconductor device according to claim 1, comprising:

a minority-carrier injector which comprises:

the p-n junction (20_1; 145_1); and

a Schottky diode (21; 146);

wherein the Schottky diode is arranged in parallel with the p-n junction so as to provide the Schottky-biased p-n junction.

3. A semiconductor device according to claim 2, comprising:

a semiconductor region (3; 133_1 141_1, 142) disposed between first and second opposite surfaces,

at least a first portion of the semiconductor region comprising a semiconductor of a first conductivity type providing a drift region for majority carriers in a direction between the first and second surfaces,

at least a second portion of the semiconductor region providing a body region (12; 112_1) comprising a semiconductor of a second, opposite conductivity type disposed at the first surface of semiconductor region; and

at least a third portion of the semiconductor region providing a source region (15; 115_1) comprising a semiconductor of the first conductivity type disposed at the first surface of semiconductor region and within the body region.

4. A semiconductor device according to claim 3 wherein the minority-carrier injector is disposed at the first surface of the semiconductor region laterally separated from the body region.

5. A semiconductor device according to claim 4, wherein at least a fourth portion of the semiconductor region comprises a semiconductor of the second

conductivity type disposed at the first surface of the semiconductor region with a semiconductor of the first conductivity type so as to form a p-n junction.

6. A semiconductor device according to claims 4 or 5, wherein the Schottky diode (21; 146) comprises a metallization in contact with the first surface of semiconductor region.

7. A semiconductor device according to claim 6, wherein the Schottky diode (21; 146) has a barrier height equal to or greater than 0.7 eV

8. A semiconductor device according to any one of claims 3 to 7, further comprising a gate structure disposed on the first surface of the semiconductor region and configured to control flow of carriers from the source region into drift region.

9. A device according to claim 1, comprising:

a semiconductor substrate (2; 102) of a first conductivity type;

a drift region (3; 133_1 141_1, 142) comprising a semiconductor of the first conductivity type disposed on the semiconductor substrate;

a body region (12; 112_1) comprising a semiconductor of a second, opposite conductivity type;

a source region (15; 115_1) comprising a semiconductor of the first conductivity type disposed within the body region;

the device further comprising:

a minority-carrier injector which comprises:

an injector region (13_1; 113_1) comprising a semiconductor of the second conductivity type disposed within the drift region and laterally separated from the body region, the injector region and the drift region forming a p-n junction (20_1; 145_1); and

a metallic electrode (19_3; 119_3) in contact with the drift region laterally adjacent and electrically connected to the injector region, the metallic electrode and the drift region forming a Schottky diode (21; 146) in parallel with the p-n junction to provide the Schottky-biased p-n junction.

10. A semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor, the device comprising:

a semiconductor substrate (2; 102) of a first conductivity type;

a drift region (3; 133_1 141_1, 142) comprising a semiconductor of the first conductivity type disposed on the semiconductor substrate;

a body region (12; 112_1) comprising a semiconductor of a second, opposite conductivity type;

a source region (15; 115_1) comprising a semiconductor of the first conductivity type disposed within the body region;

the device further comprising:

a minority-carrier injector which comprises:

an injector region (13_1; 113_1) comprising a semiconductor of the second conductivity type disposed within the drift region and laterally separated from the body region, the injector region and the drift region forming a p-n junction (20_1; 145_1); and

a metallic electrode (19_3; 119_3) in contact with the drift region laterally adjacent and electrically connected to the injector region, the metallic electrode and the drift region forming a Schottky diode (21) in parallel with the p-n junction.

11. A device according to claim 9 or 10, wherein the body region (12) and the substrate (2) are vertically separated by a first given distance and the body region (12) and the injector region (13_1) are laterally separated by a second given distance equal to or greater than the first given distance.

12. A device according to claim 11, wherein the second given distance is about 6 to 12 μm.

13. A device according to claim 9 or 10, further comprising:

a depletion reducing region (35) comprising a semiconductor of the first conductivity type disposed within the drift region (3), more highly doped than the drift region and disposed between the body region (12) and the injector region (13_1).

14. A device according to claim 13, wherein the body region (12) and the substrate (2) are vertically separated by a first given distance and the body region (12) and the injector region (13_1) are laterally separated by a second given distance less than the first given distance.

15. A device according to any one of claims 9 to 14, wherein the Schottky diode (21; 146) has a barrier height equal to or greater than 0.7 eV.

16. A device according to any one of claims 9 to 15, wherein the metallic electrode (19_3; 119_3) includes a layer of platinum silicide forming the Schottky diode (21; 146).

17. A device according to any one of claims 9 to 16, wherein the metallic electrode (19_3; 119_3) and the semiconductor substrate (2) are coupled so as to be at the same potential.

18. A device according to any one of claims 9 to 17, wherein the drift region (3; 133_1 141_1, 142) comprises silicon.

19. A device according to any one of claims 9 to 17, wherein the drift region (3; 133_1 141_1, 142) comprises silicon carbide semiconductor.

20. A device according to any preceding claim, further comprising:
a charge balance structure (131).

21. A device according to claim 20, wherein the charge balance structure (131) comprises:
first and second charge balance regions (132_1, 134_1) comprising a semiconductor of the second conductivity type, the first charge balance region (132_1) extending vertically between the substrate and the body region (112_1) and the second charge balance region (134_1) laterally spaced between the p-n junction (113_1) and the first charge balance region (132_1), such that a vertical drift region (133_1)

comprising a semiconductor of the first conductivity type is disposed between the first and second charge balance regions.

22. A device according to claim 21, wherein the charge balance structure (131) further comprises:

a third charge balance region (137) comprising a semiconductor of the second conductivity type disposed under the p-n junction (145_1) and extending laterally to the second charge balance region (134_1), wherein a lateral drift region (142) comprising a semiconductor of the first conductivity type is disposed over the third charge balance region.

23. A device according to claim 22, wherein the charge balance structure (131) further comprises:

a region (136_1) comprising a semiconductor of the second conductivity type linking the first and second charge balance regions (132_1, 134_1), the region configured to leave a region (141_1) comprising a semiconductor of the first conductivity type linking the lateral and vertical drift regions.

24. A semiconductor device having an integrated vertical and lateral charge balance structure.

25. A semiconductor device according to claim 24, wherein the semiconductor device comprises:

a planar substrate (102);

a first conductive region (133_1) of a first conductivity type extending perpendicularly to the substrate between first and second ends and having at least first and second sides;

first and second charge balance regions (132_1, 134_1) of second conductivity type disposed on the first and second sides respectively of the first conductive region;

a second conductive region (142) of the first conductivity type extending parallel to the substrate between first and second ends and having at least a first side;

a third charge balance region (137) of the second conductivity type disposed on the first side of the second conductive region;

the device further comprising:

at least one region (141_1) of the first conductivity type linking the first and second conductive regions so as to form a continuous region of the first conductivity type between the first end of the first conductive region to the second end of the second conductive region; and

at least one region (136_1) of the second conductivity type linking the first, second and third charge balance regions so as to form an integrated charge balance structure.

26. An integrated circuit comprising at least one semiconductor device according to any preceding claim.

27. A method of fabricating a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor, the method comprising:

providing a Schottky-biased p-n junction.

28. A method according to claim 27, further comprising:

providing a drift region of first conductivity type on a semiconductor substrate of the first conductivity type;

forming a body region of a second, opposite conductivity type within the drift region;

forming a source region of the first conductivity type within the body region;

wherein providing the Schottky-biased p-n junction comprises:

forming an injector region of the second conductivity type within the drift region, laterally separated from the body region, wherein the injector region and the drift region provide a p-n junction; and

providing a metallic electrode in contact with the drift region laterally adjacent and electrically connected to the injector region, wherein the metallic electrode and the drift region provide a Schottky diode in parallel with the p-n junction.

29. A method of fabricating a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a lateral insulated gate bipolar transistor, the method comprising:

providing a drift region of first conductivity type on a semiconductor substrate of the first conductivity type;

forming a body region of a second, opposite conductivity type within the drift region;

forming a source region of the first conductivity type within the body region;

forming an injector region of the second conductivity type within the drift region, laterally separated from the body region, wherein the injector region and the drift region provide a p-n junction; and

providing a metallic electrode in contact with the drift region laterally adjacent and electrically connected to the injector region, wherein the metallic electrode and the drift region provide a Schottky diode in parallel with the p-n junction.

30. A method according to claim 29, wherein the body region and the substrate are vertically separated by a first given distance and wherein forming the injector region within the drift region comprises laterally separating the injector region from the body region by a second given distance exceeding the first given distance.

31. A device according to claim 29, further comprising:

a depletion reducing region comprising a semiconductor of the first conductivity type disposed within the drift region, more highly doped than the drift region and disposed between the body region and the injector region.

32. A method according to claim 31, wherein the body region and the substrate are vertically separated by a first given distance and the body region and the injector region are laterally separated by a second given distance less than the first given distance.

33. A method according to any one of claims 27 to 32, further comprising:

providing a charge balance structure.

34. A method of fabricating a semiconductor device, the method comprising:

providing an integrated vertical and lateral charge balance structure.

35. A method according to claim 34, wherein providing the integrated vertical and lateral charge balance structure comprises:

providing a planar substrate;

providing a first conductive region of a first conductivity type extending perpendicularly to the substrate between first and second ends and having at least first and second sides;

providing first and second charge balance regions of second conductivity type disposed on the first and second sides respectively of the first conductive region;

providing a second conductive region of the first conductivity type extending parallel to the substrate between first and second ends and having at least a first side;

providing a third charge balance region of the second conductivity type disposed on the first side of the second conductive region;

providing at least one region of the first conductivity type linking the first and second conductive regions so as to form a continuous region of the first conductivity type between the first end of the first conductive region to the second end of the second conductive region; and

providing at least one region of the second conductivity type linking the first, second and third charge balance regions so as to form an integrated charge balance structure

36. A method of operating a semiconductor device operable as a vertical metal oxide semiconductor field effect transistor and a vertical or lateral insulated gate bipolar transistor having a Schottky-biased p-n junction, the metal oxide semiconductor field effect transistor and insulated gate bipolar transistor sharing a source region and a drain region and wherein the Schottky-biased p-n junction has a

terminal, the method comprising grounding the source region and applying given bias(es) to terminal and the drain region.

37. A method according to claim 36, wherein the drain region comprises a semiconductor substrate of a first conductivity type or metallic region, and the device further comprises a drift region of the first conductivity type disposed on the semiconductor substrate or metallic region, a body region of a second, opposite conductivity type disposed within the drift region, a source region of the first conductivity type disposed within the body region, an injector region of the second conductivity type disposed within the drift region and laterally separated from the body region, the injector region and the drift region forming a p-n junction and a metallic electrode in contact with the drift region laterally adjacent and electrically connected to the injector region, the metallic electrode and the drift region forming a Schottky diode in parallel with the p-n junction.

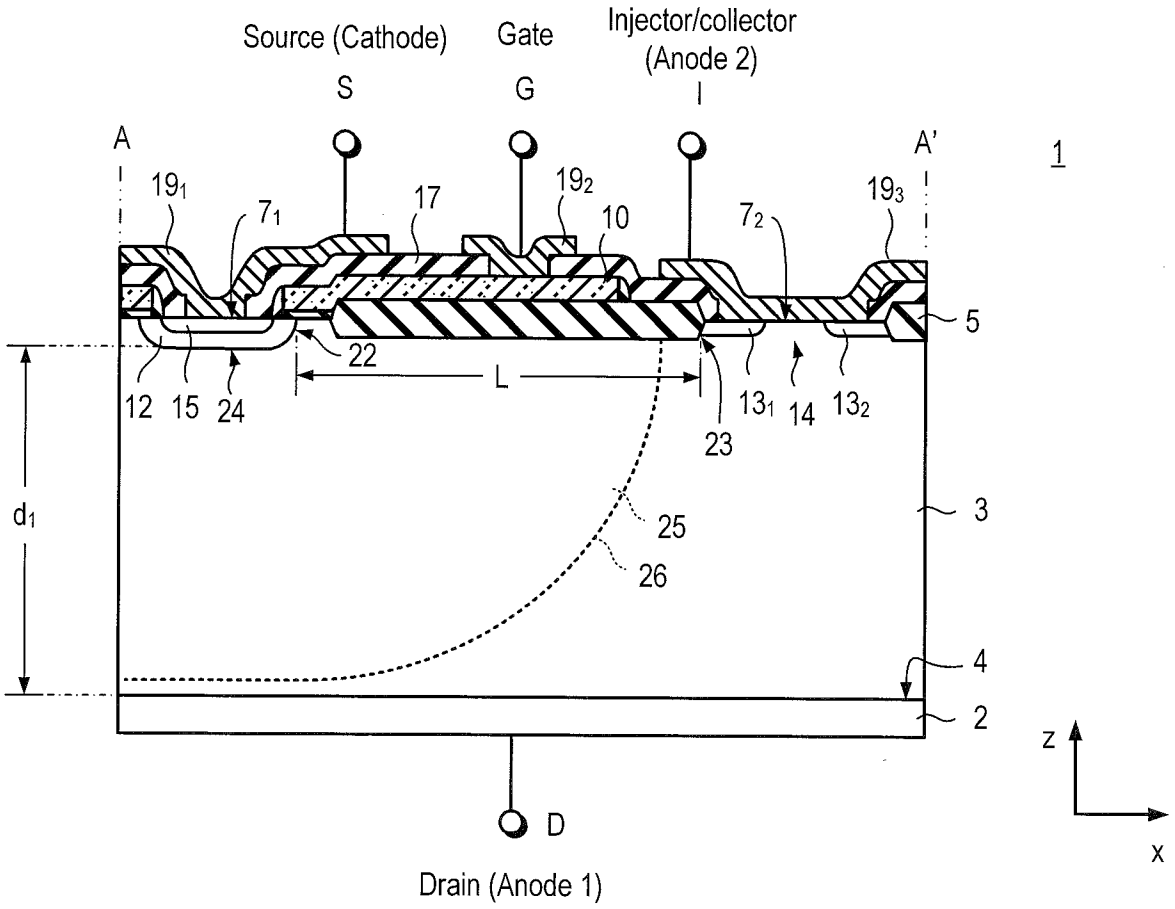
Source (Cathode)
S
Gate
G
Injector/collector
(Anode 2)
I
A
A'
1
19_1
7_1
17
19_2
10
7_2
19_3
5
22
L
12
15
24
23
13_1
14
13_2
d_1
25
26
3
4
2
z
x
D
Drain (Anode 1)

Fig. 1

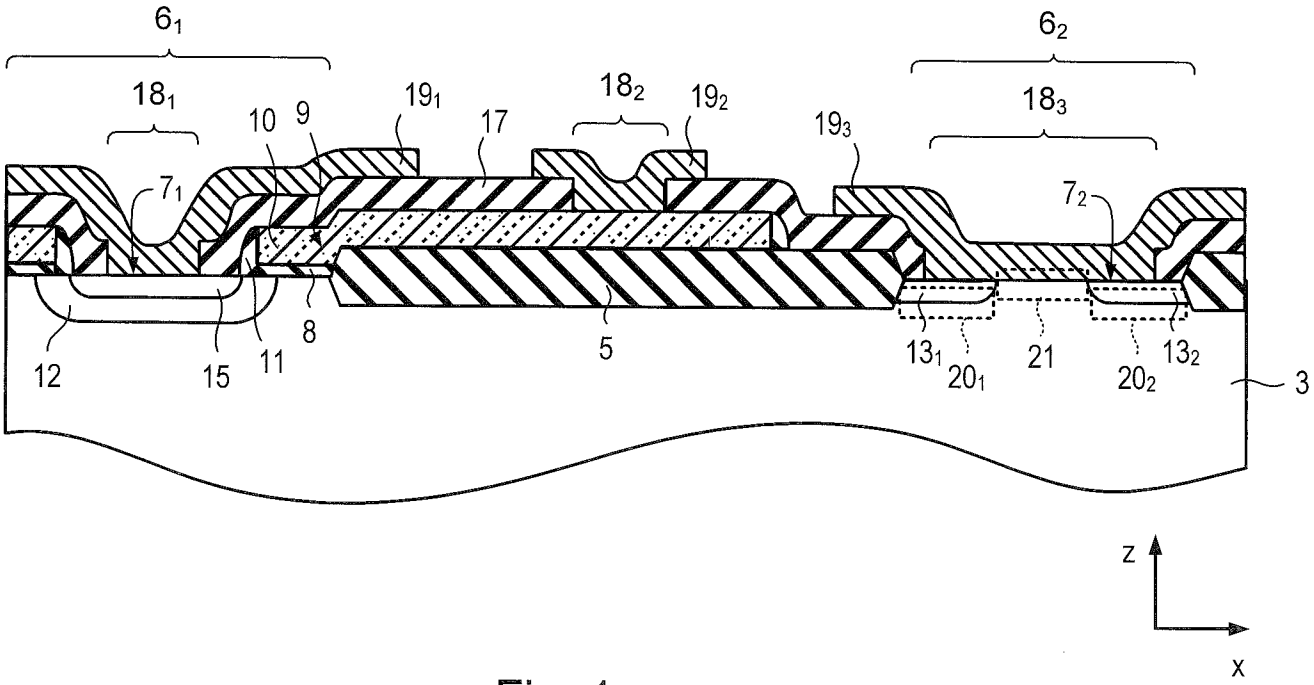
6_1
6_2
18_1
18_2
18_3
19_1
19_2
19_3
10
9
17
7_1
7_2
12
15
11
8
5
13_1
20_1
21
20_2
13_2
3
z
x

Fig. 1a

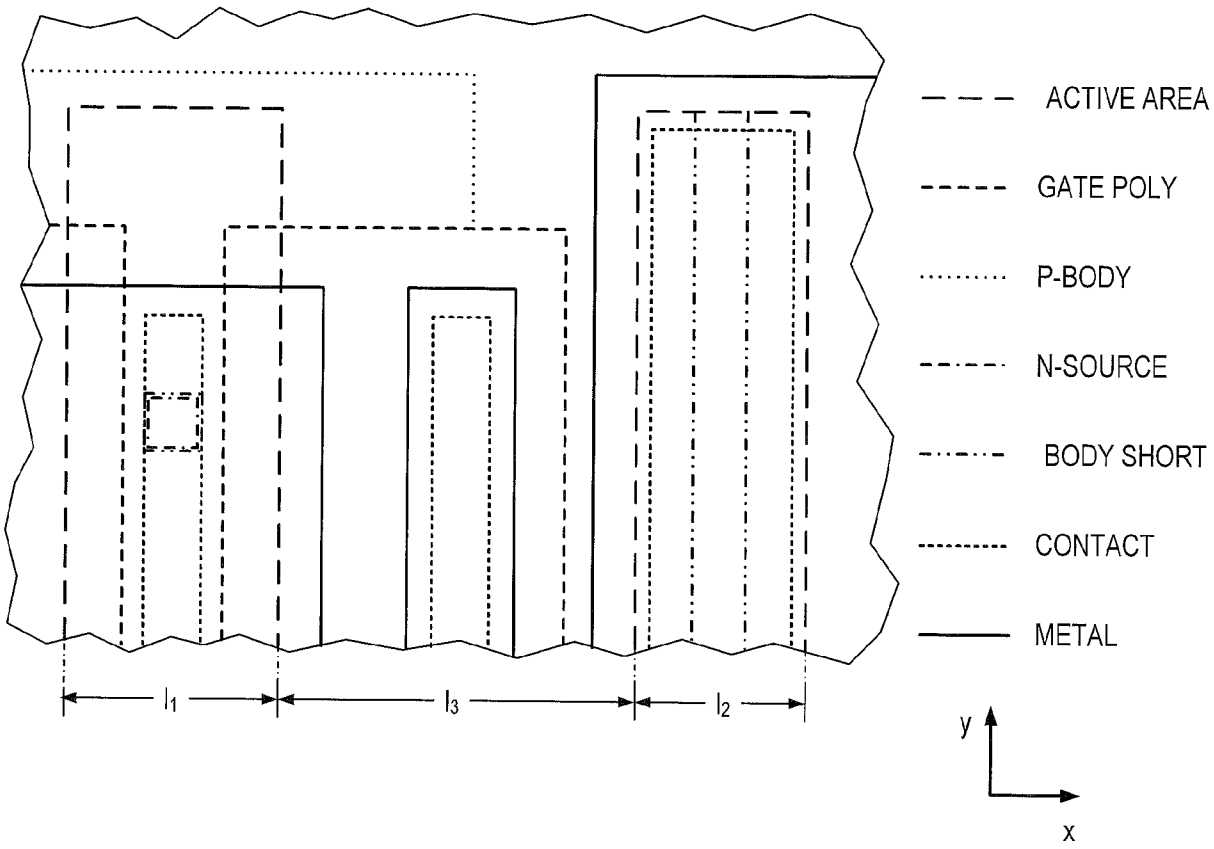
ACTIVE AREA
GATE POLY
P-BODY
N-SOURCE
BODY SHORT
CONTACT
METAL
l1
l3
l2
y
x

Fig. 2

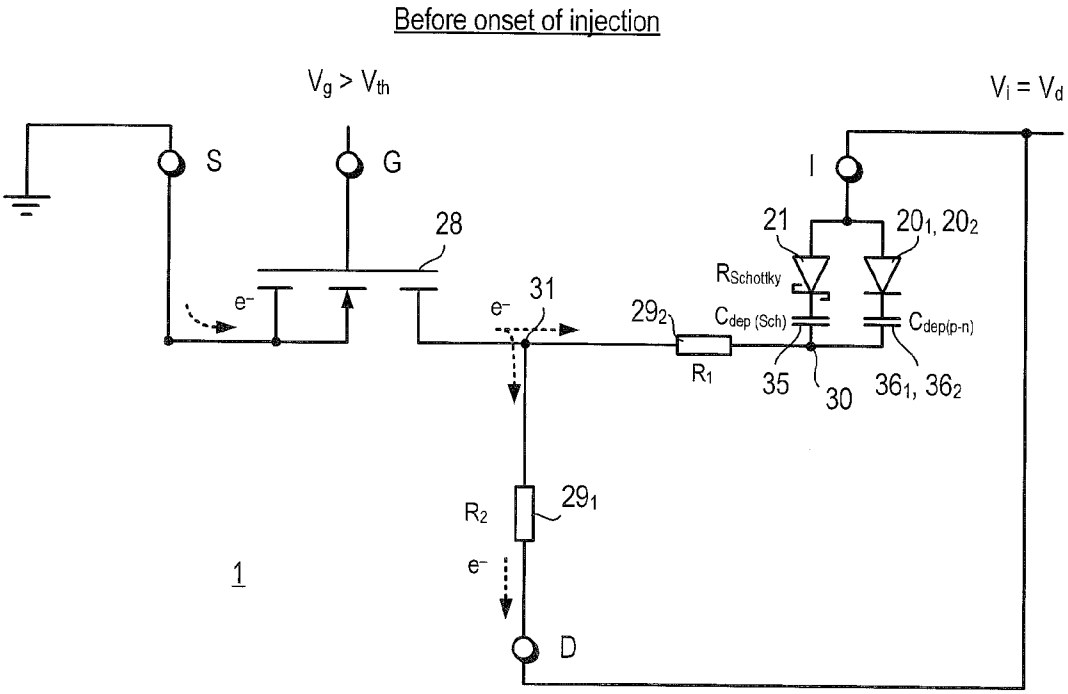
Before onset of injection
Vg > Vth
Vi = Vd
S
G
I
28
21
20₁, 20₂
RSchottky
e⁻
31
29₂
Cdep (Sch)
Cdep(p-n)
R1
35
30
36₁, 36₂
R2
29₁
1
D

Fig. 3a

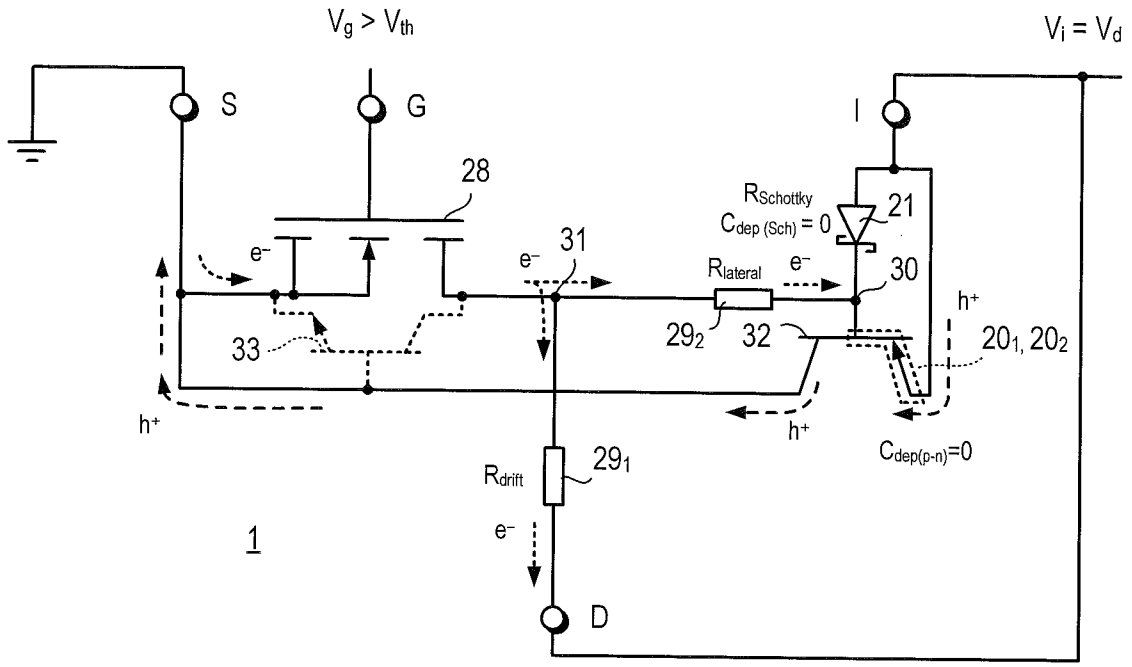
After onset of injection
$V_g > V_{th}$
$V_i = V_d$
S
G
I
28
$R_{Schottky}$
$C_{dep\ (Sch)} = 0$
21
e⁻
31
e⁻
$R_{lateral}$
e⁻
30
h⁺
33
29_2
32
$20_1, 20_2$
h⁺
h⁺
$C_{dep(p-n)}=0$
R_{drift}
29_1
e⁻
1
D

Fig. 3b

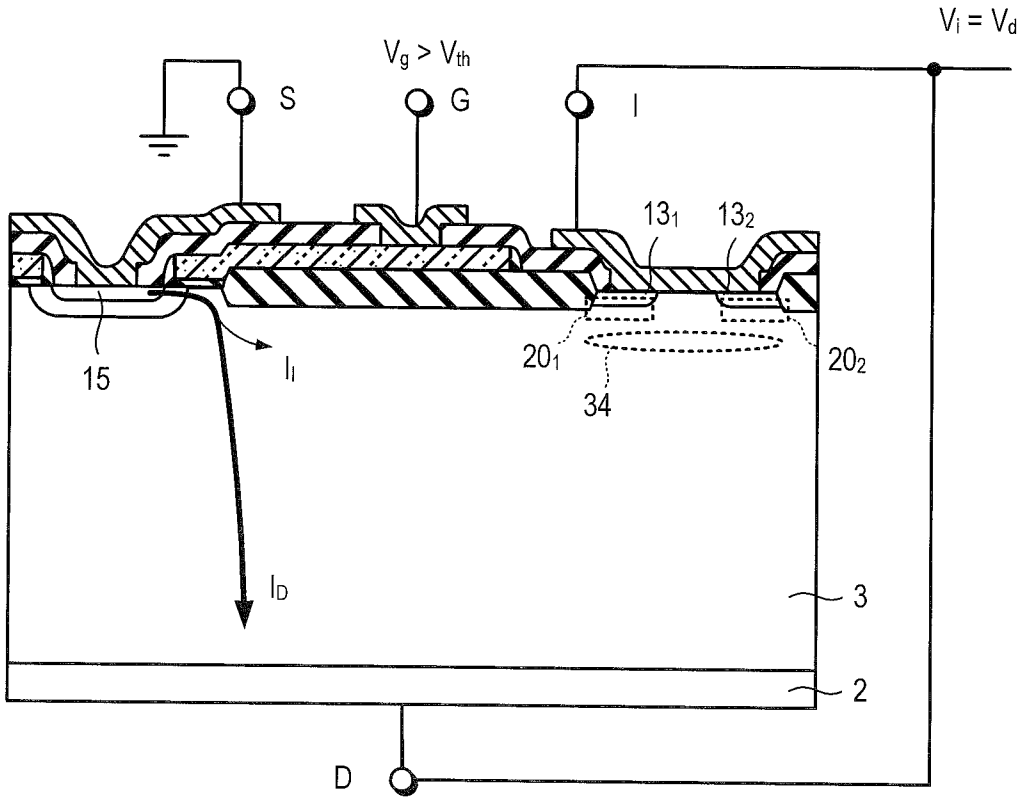
$V_i = V_d$
$V_g > V_{th}$
S
G
I
13_1
13_2
15
I_I
20_1
20_2
34
I_D
3
2
D

Fig. 4

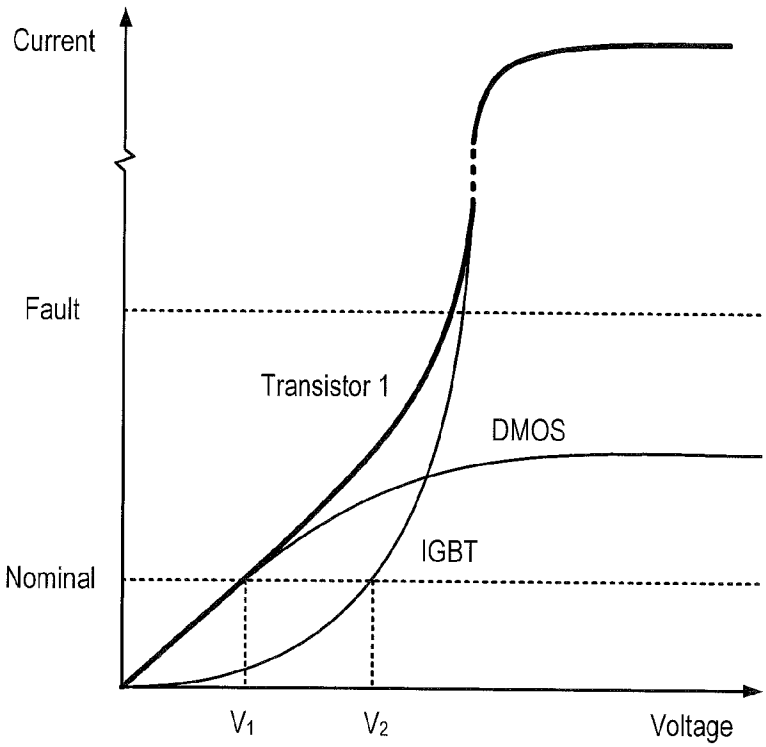
Current
Fault
Transistor 1
DMOS
IGBT
Nominal
V1
V2
Voltage

Fig. 5

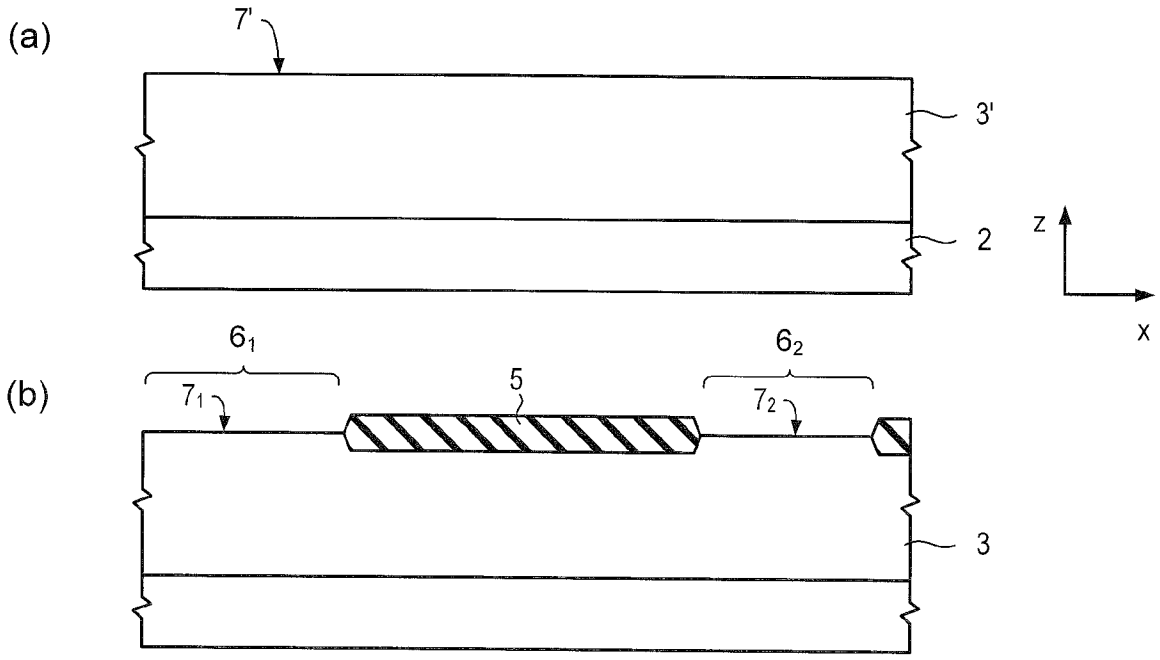
(a)
7'
3'
2
z
x
(b)
61
62
71
5
72
3

Fig. 6

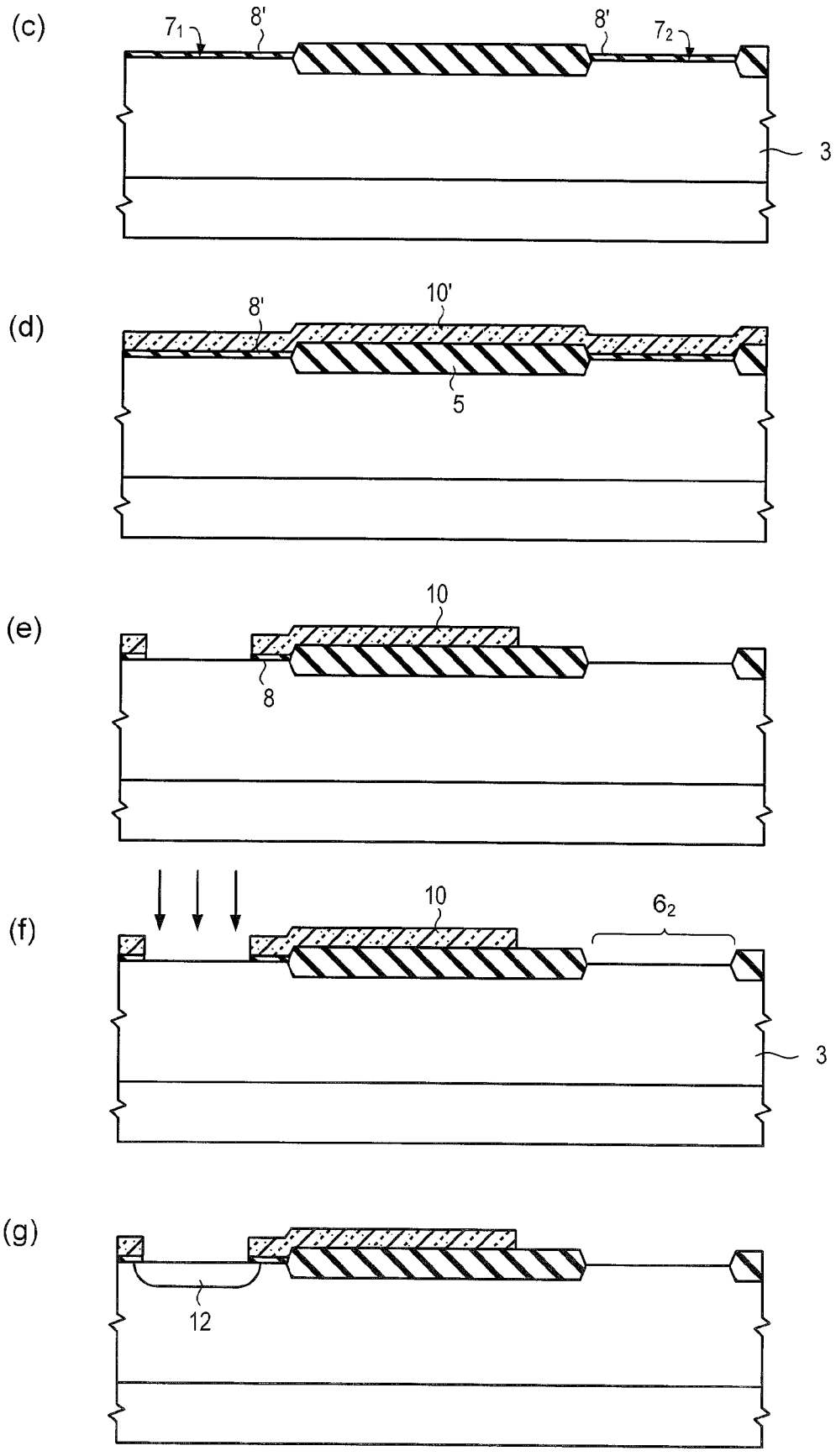

Fig. 6

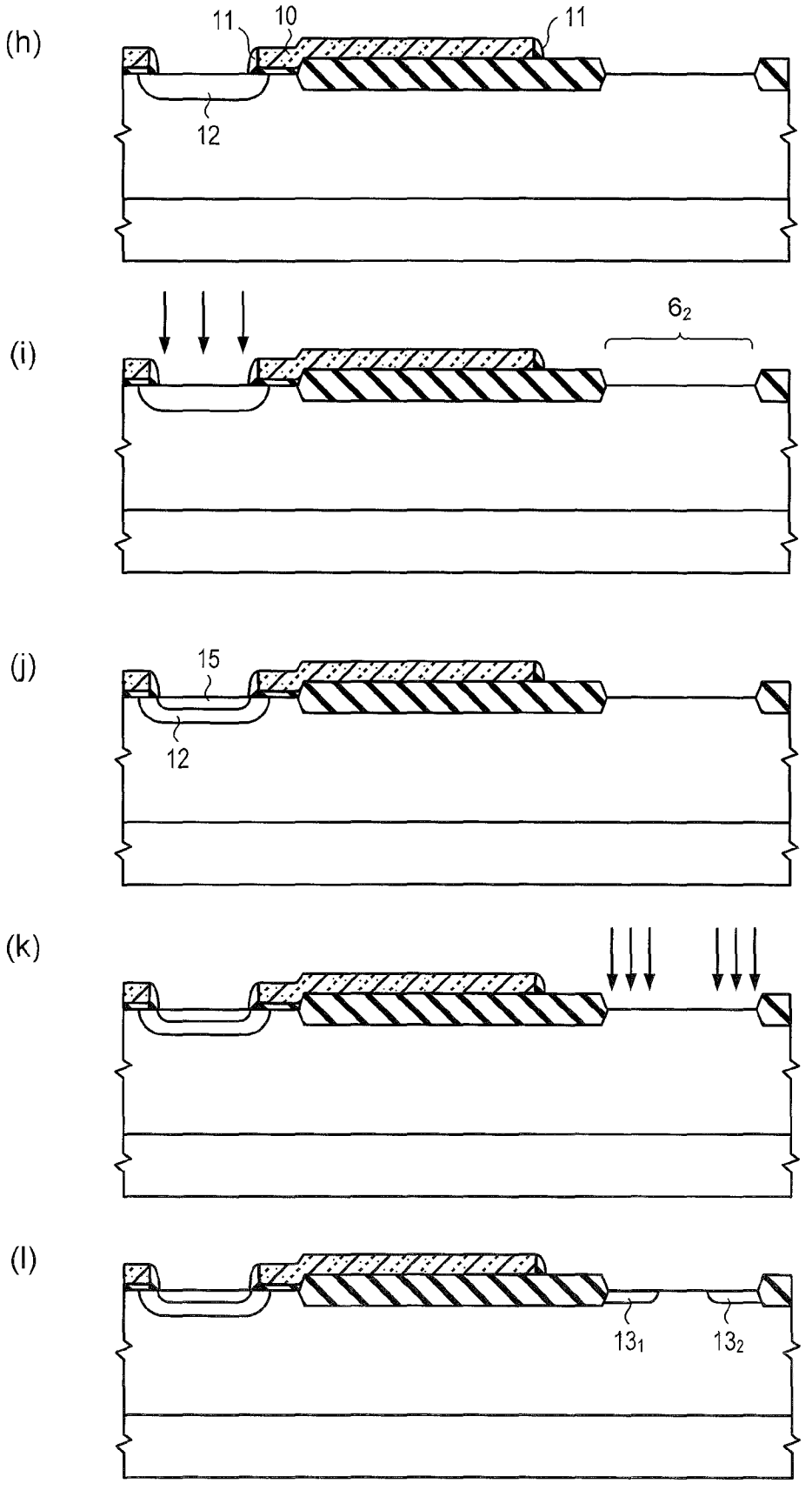

Fig. 6

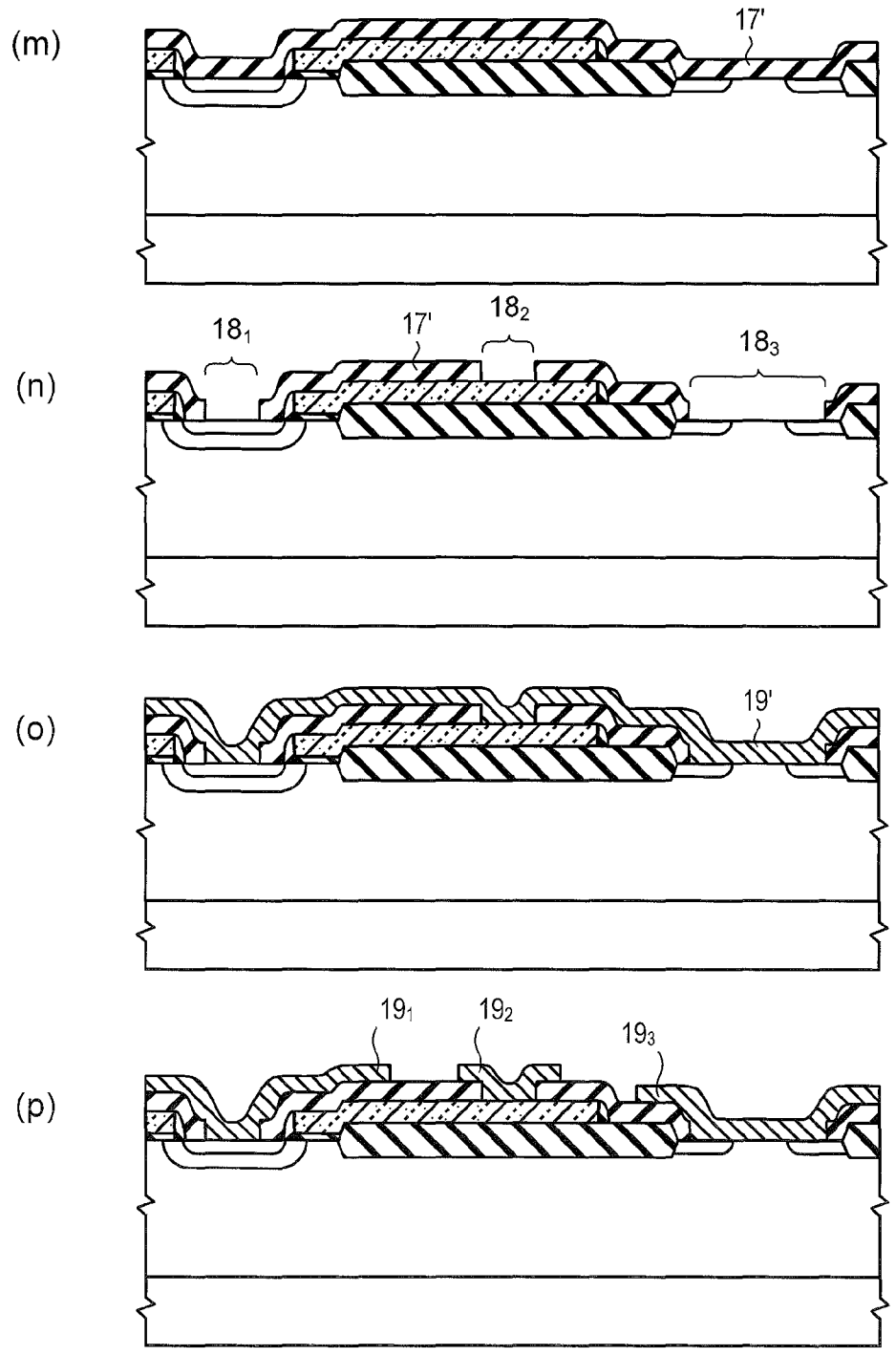

Fig. 6

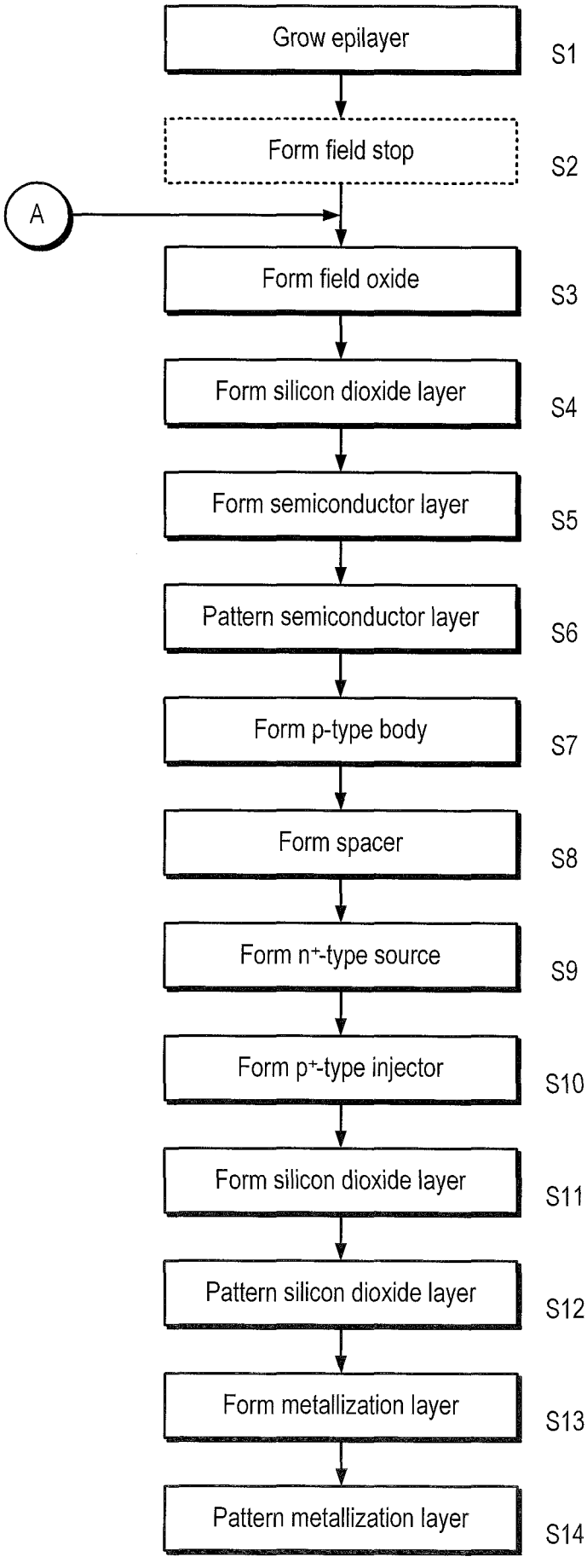
Grow epilayer
S1
Form field stop
S2
A
Form field oxide
S3
Form silicon dioxide layer
S4
Form semiconductor layer
S5
Pattern semiconductor layer
S6
Form p-type body
S7
Form spacer
S8
Form n+-type source
S9
Form p+-type injector
S10
Form silicon dioxide layer
S11
Pattern silicon dioxide layer
S12
Form metallization layer
S13
Pattern metallization layer
S14

Fig. 7

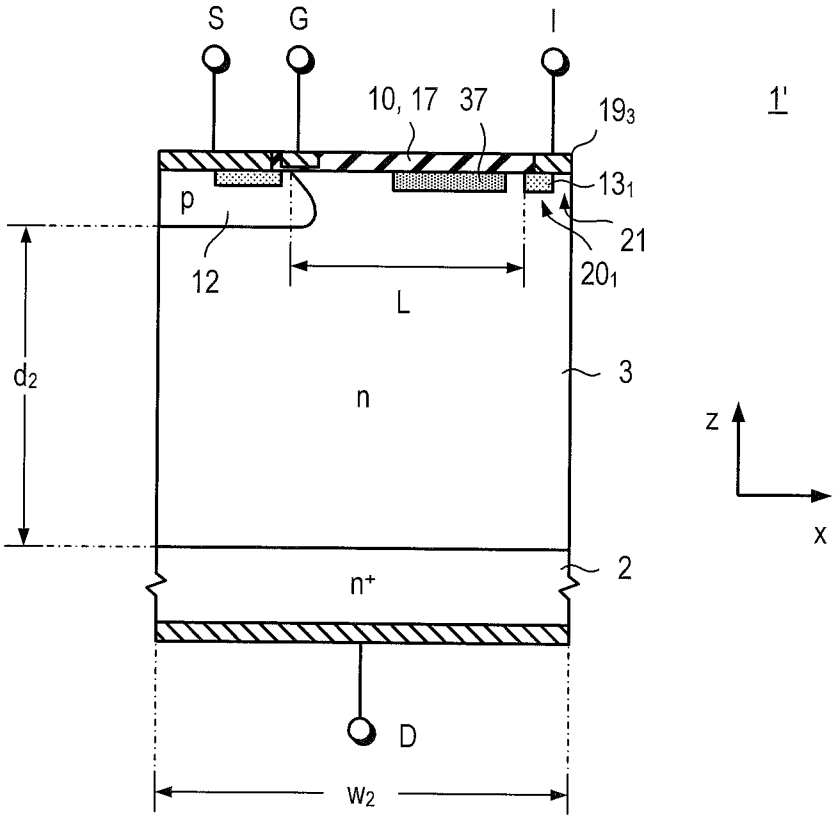
S
G
I
10, 17
37
19₃
1'
13₁
p
21
12
20₁
L
d₂
3
n
z
x
n+
2
D
w₂

Fig. 8

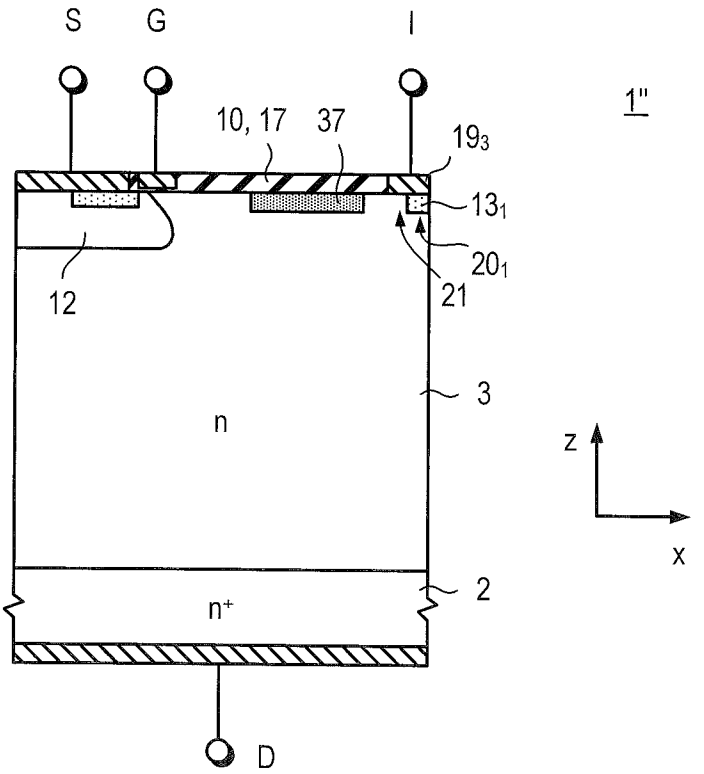
S
G
I
10, 17
37
19₃
1"
13₁
20₁
12
21
3
n
z
x
n+
2
D

Fig. 9

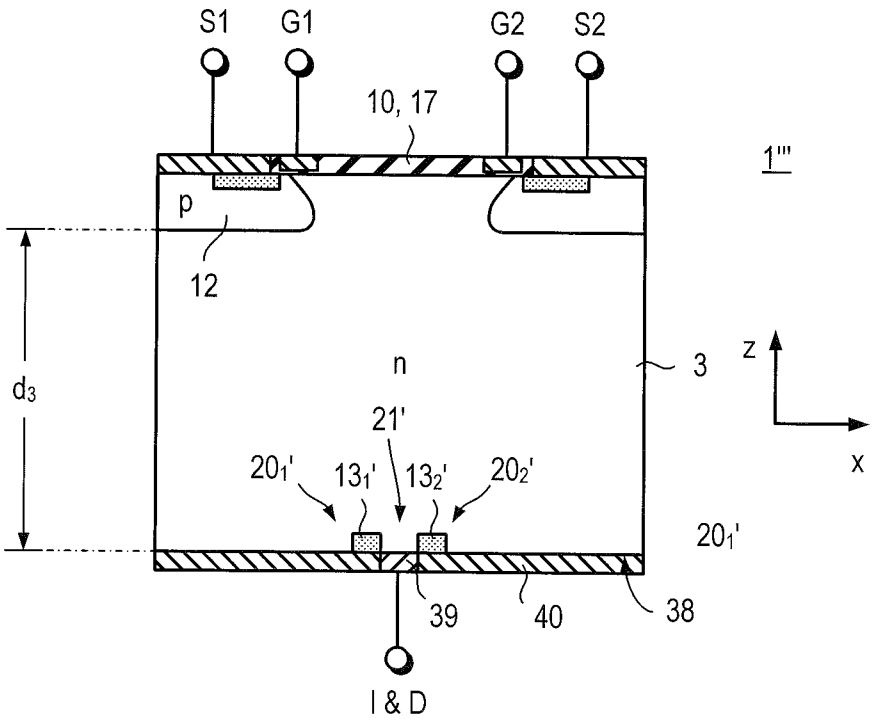

Fig. 10

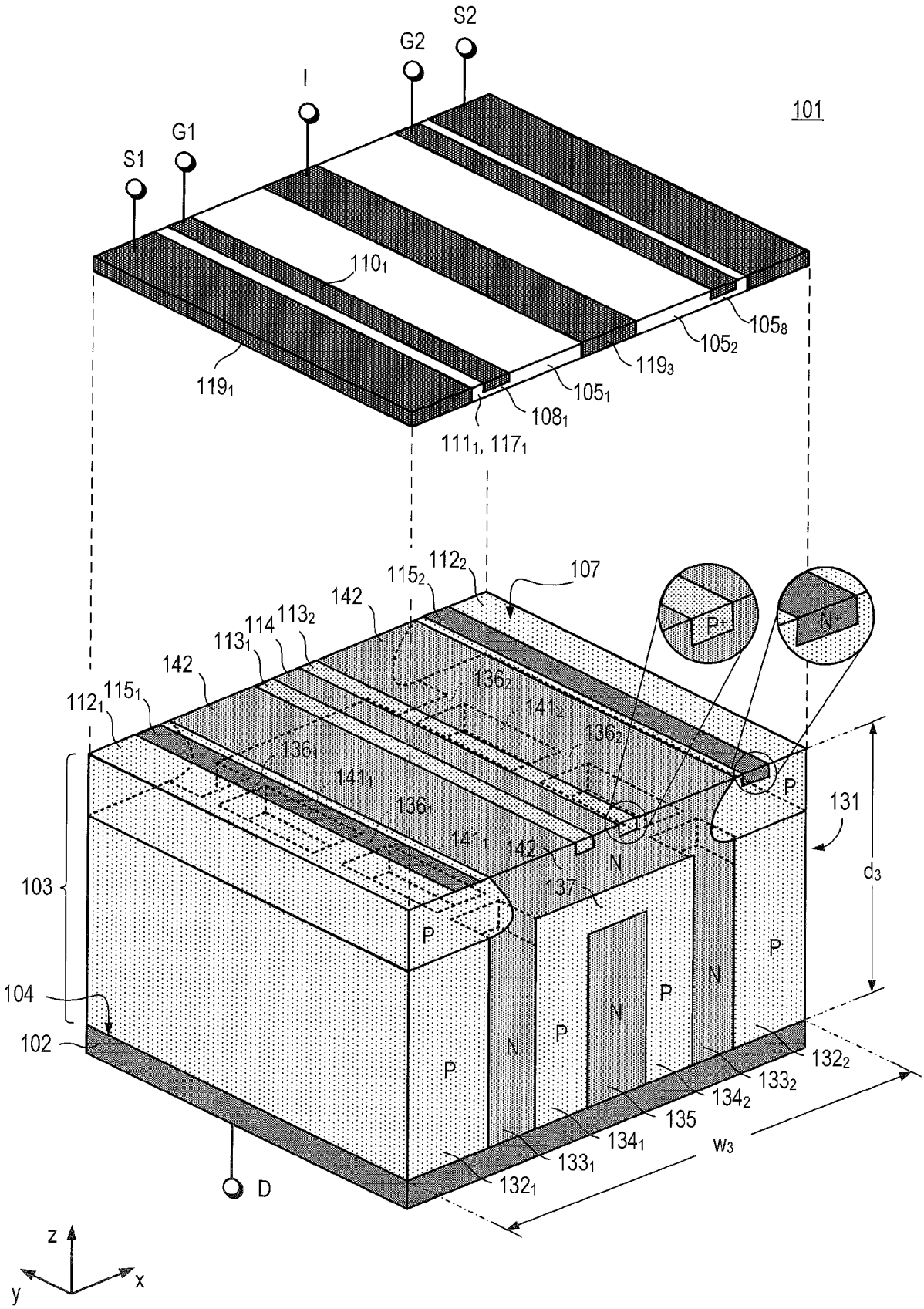
S2
G2
I
G1
S1
101
110₁
105₈
105₂
119₃
119₁
105₁
108₁
111₁, 117₁
112₂
115₂
107
142
113₂
114
113₁
142
112₁
115₁
136₂
141₂
136₁
141₁
136₁
141₁
142
137
131
103
104
102
d₃
w₃
P
N
P+
N+
D
z
y
x
132₂
133₂
134₂
135
134₁
133₁
132₁

Fig. 11

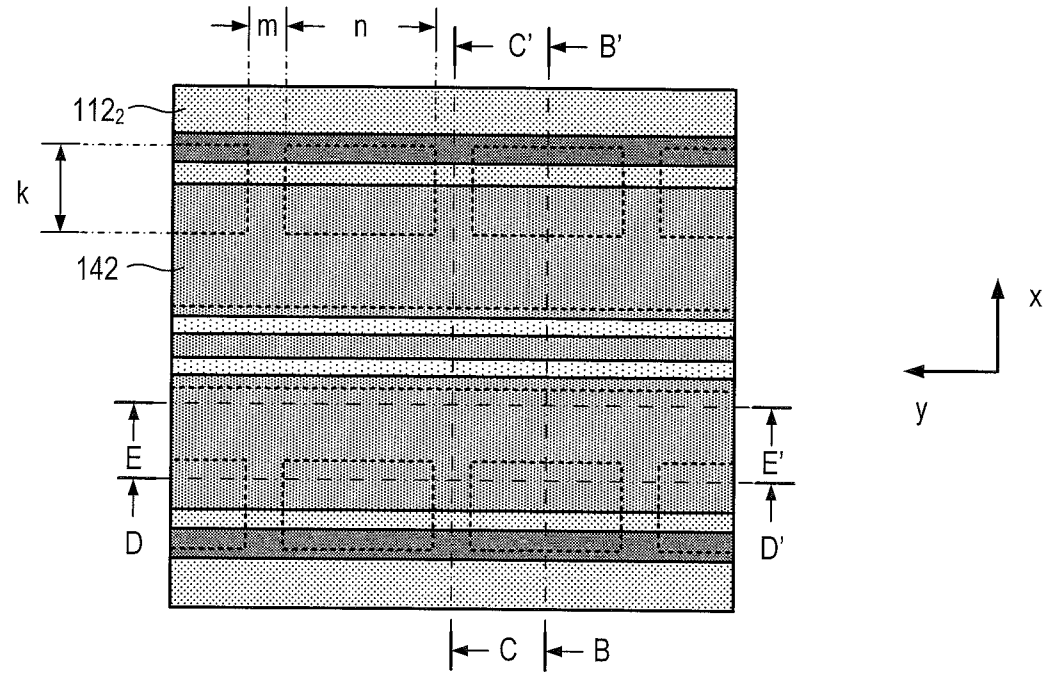

Fig. 12

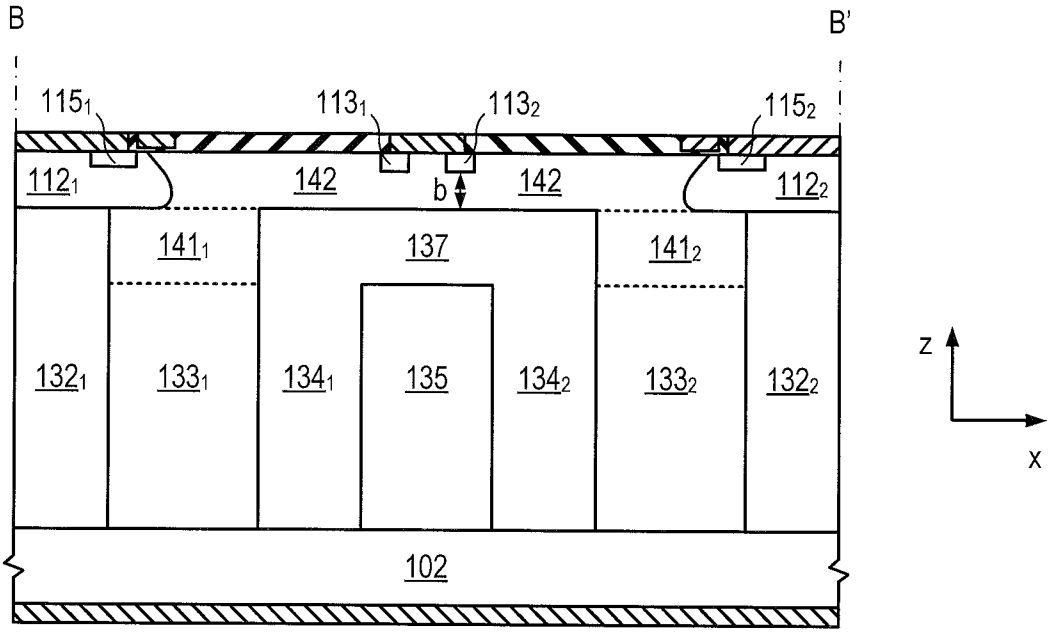
B
B'
115_1
113_1
113_2
115_2
112_1
142
b
142
112_2
141_1
137
141_2
132_1
133_1
134_1
135
134_2
133_2
132_2
102
z
x

Fig. 13

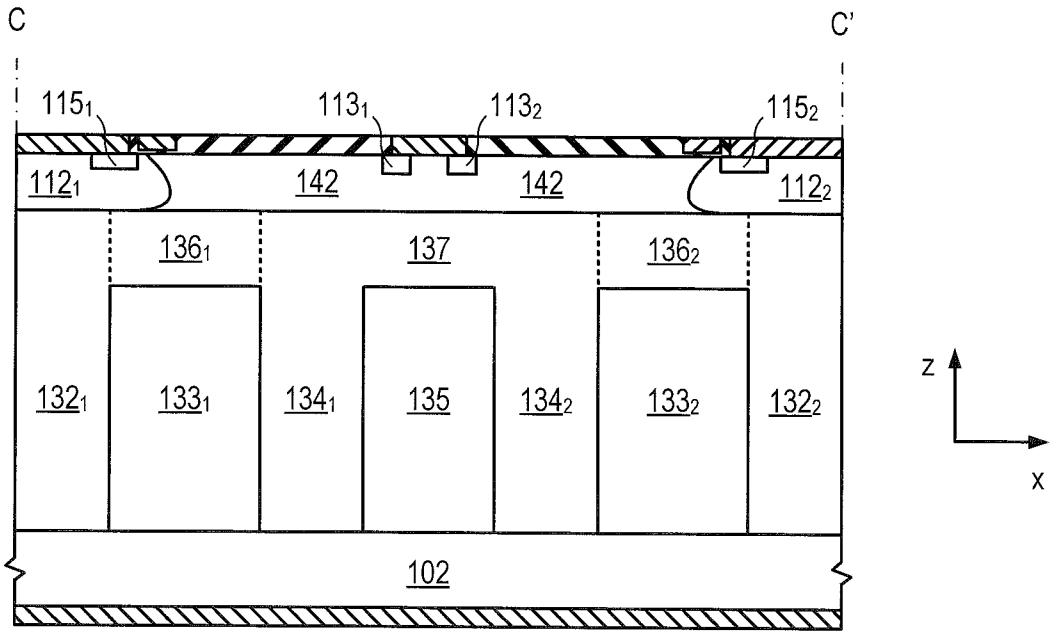
C
C'
115_1
113_1
113_2
115_2
112_1
142
142
112_2
136_1
137
136_2
132_1
133_1
134_1
135
134_2
133_2
132_2
102
z
x

Fig. 14

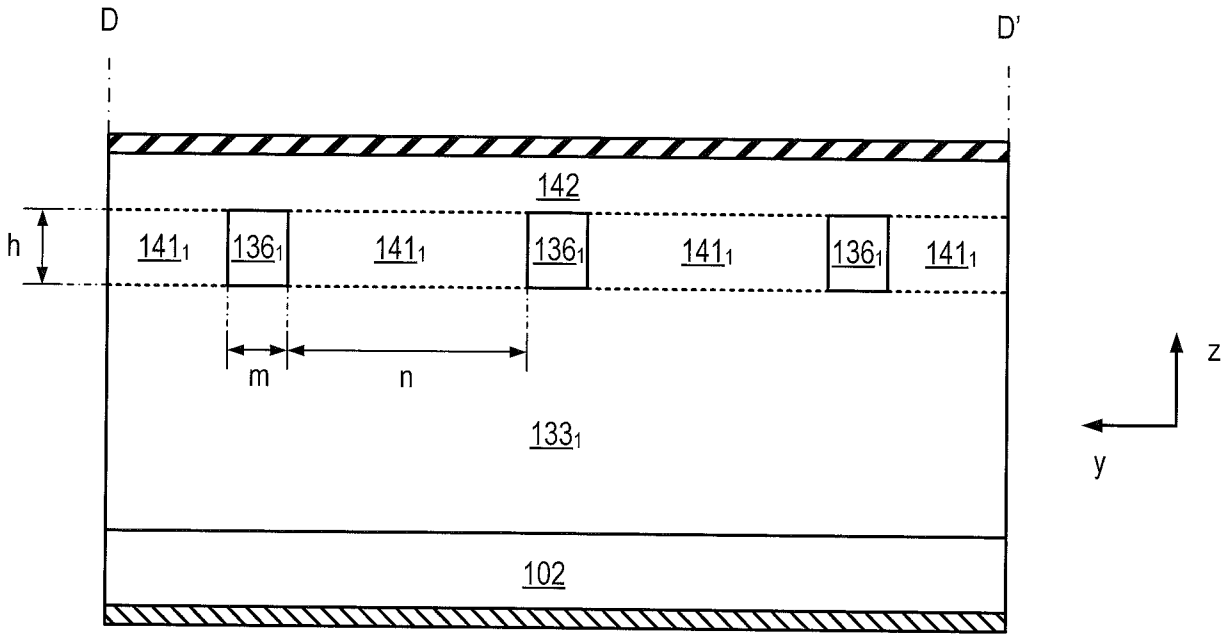
D
D'
142
h
141_1
136_1
141_1
136_1
141_1
136_1
141_1
m
n
133_1
z
y
102

Fig. 15

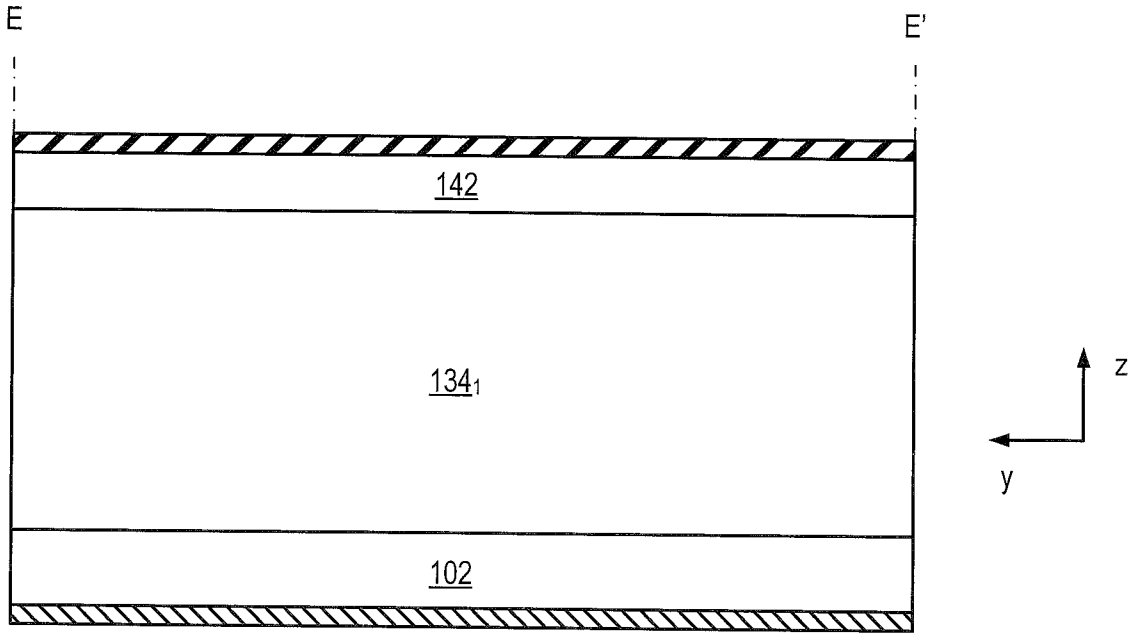
E
E'
142
134_1
z
y
102

Fig. 16

Before onset of injection

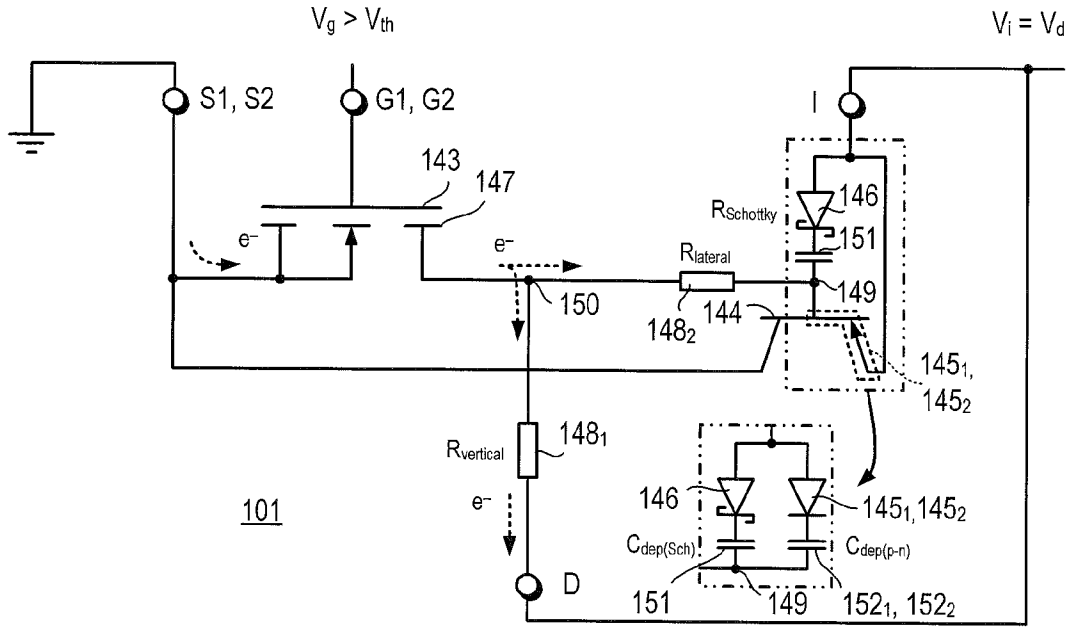

Fig. 17a

After onset of injection

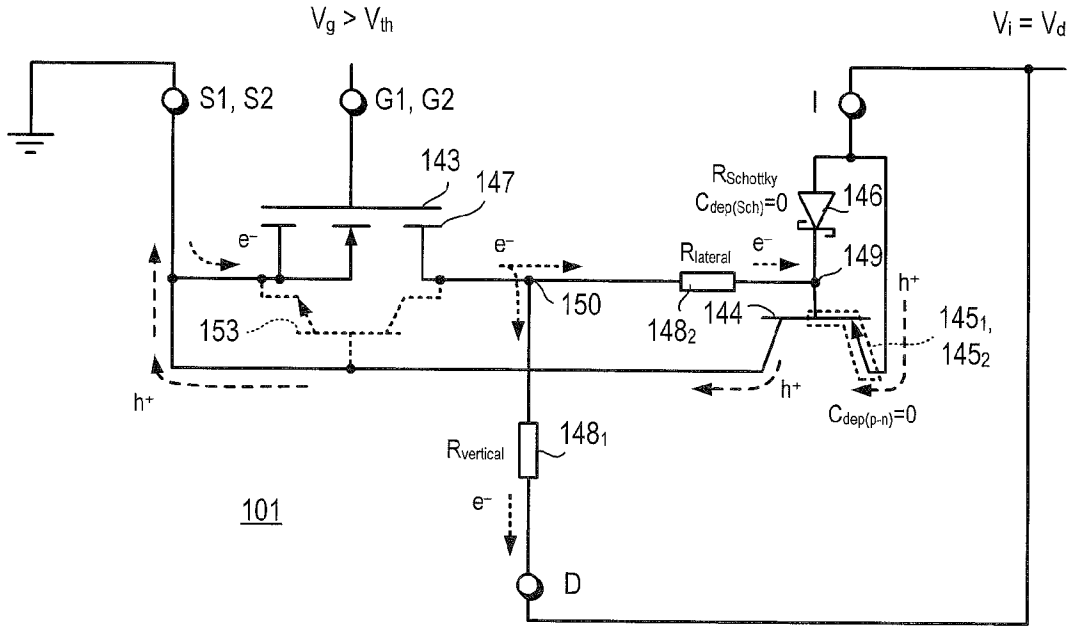

Fig. 17b

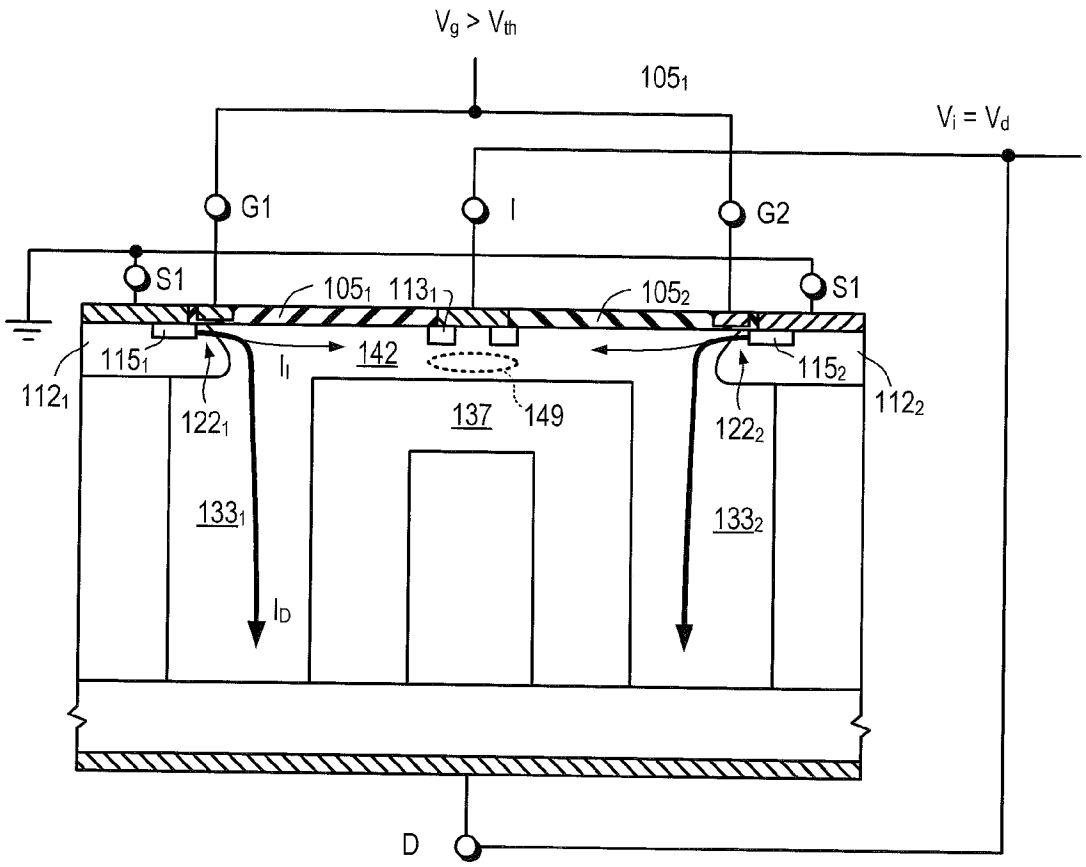
$V_g > V_{th}$
105_1
$V_i = V_d$
G1
I
G2
S1
S1
105_1 113_1
105_2
115_1
I_I
142
115_2
112_1
122_1
137
149
122_2
112_2
133_1
133_2
I_D
D

Fig. 18

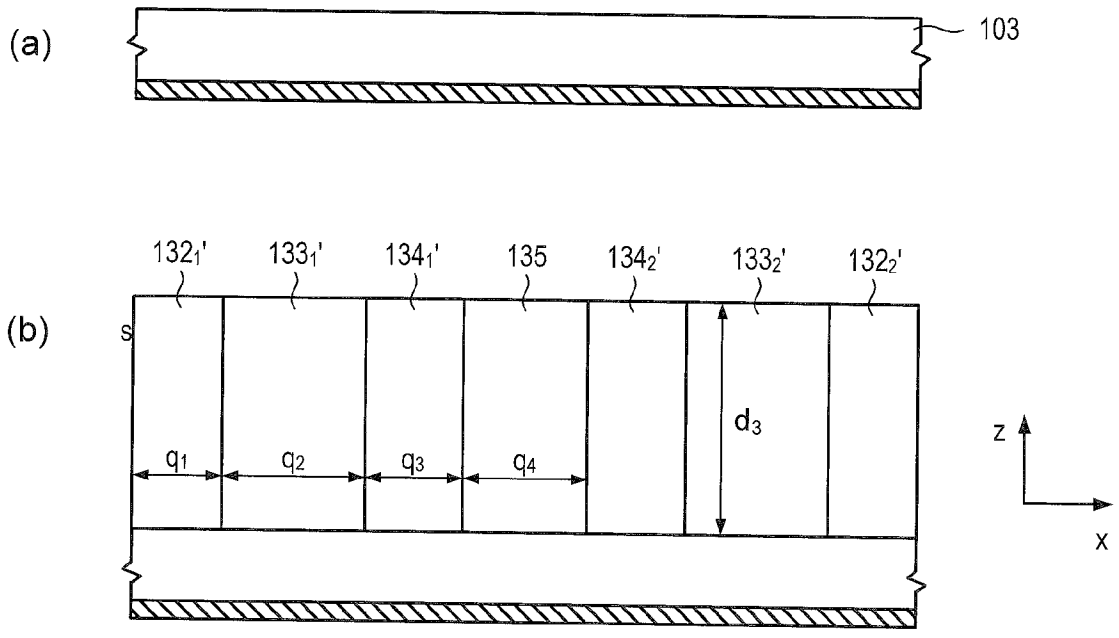
(a)
103
(b)
$132_1'$
$133_1'$
$134_1'$
135
$134_2'$
$133_2'$
$132_2'$
S
d_3
q_1
q_2
q_3
q_4
z
x

Fig. 19

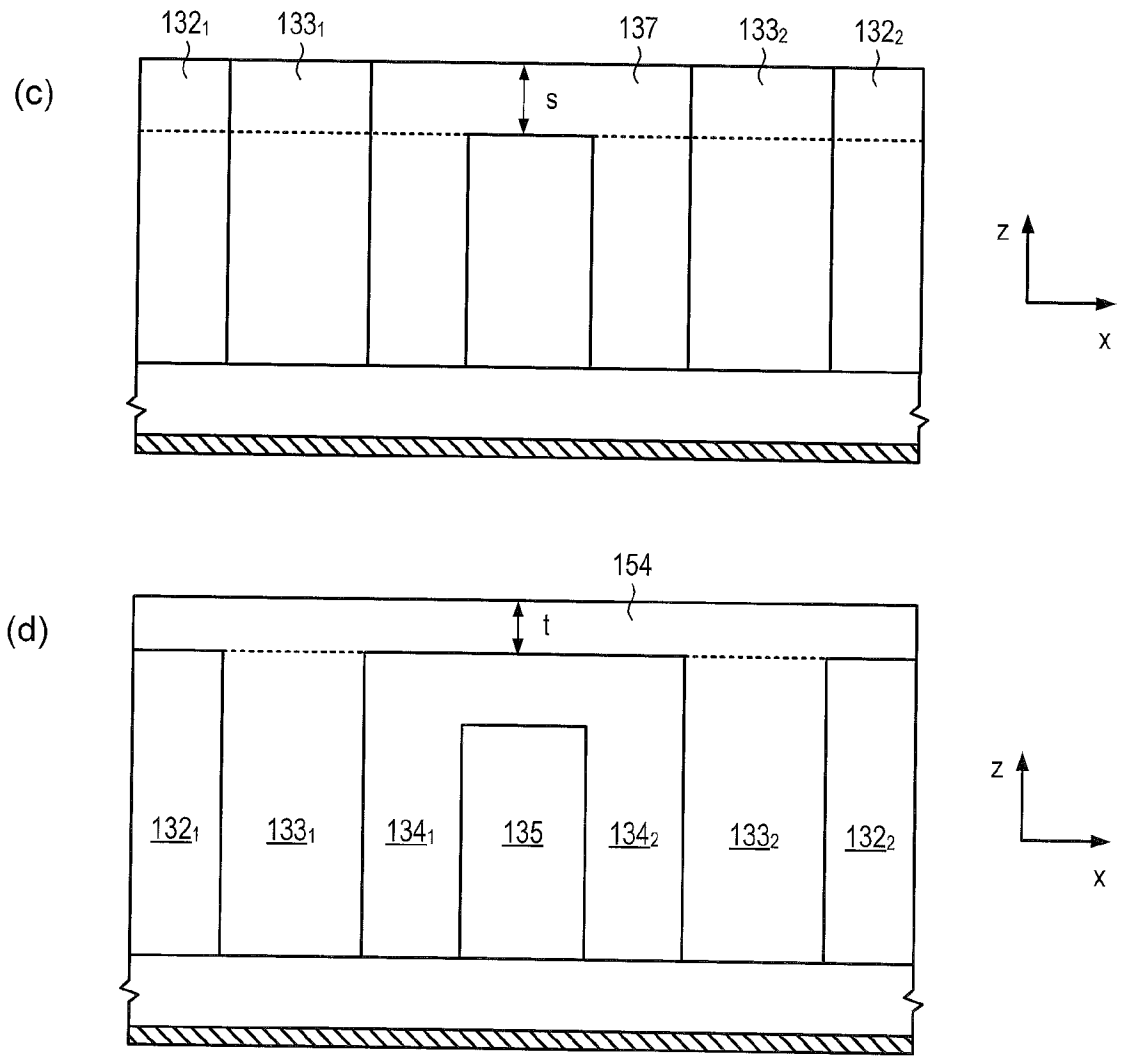
(c)
132_1
133_1
137
133_2
132_2
s
z
x
(d)
154
t
132_1
133_1
134_1
135
134_2
133_2
132_2
z
x

Fig. 19

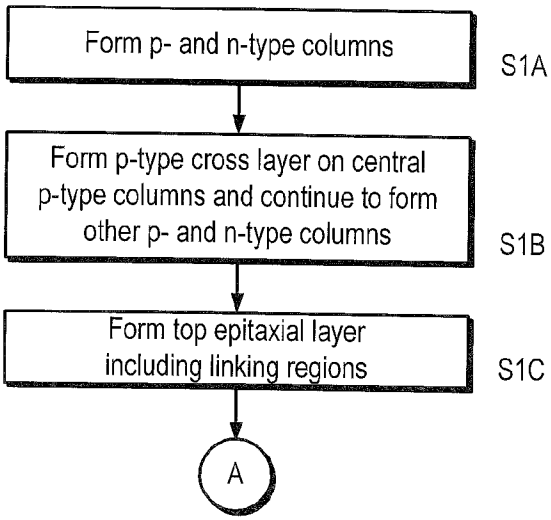
Form p- and n-type columns
S1A
Form p-type cross layer on central p-type columns and continue to form other p- and n-type columns
S1B
Form top epitaxial layer including linking regions
S1C
A

Fig. 20

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2011/051413

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/739 H01L21/331 H01L29/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	WO 2008/035134 A1 (FREESCALE SEMICONDUCTOR INC [US]; REYNES JEAN-MICHEL [FR]; LANCE PHILI) 27 March 2008 (2008-03-27) Figs.1 and 5 and corresponding text -----	1-19, 26-33, 36,37 20-23 24,25, 34,35
A	SIN J K O ET AL: "Hybrid Schottky injection MOS-gated power transistor", ELECTRONICS LETTERS, IEE STEVENAGE, GB, vol. 22, no. 19, 11 September 1986 (1986-09-11), pages 1003-1005, XP009151680, ISSN: 0013-5194, DOI: 10.1049/EL:19860686 Fig.1 and corresponding text -----	1-37

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 November 2011	09/11/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kusztelan, Leonard

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2011/051413

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/211189 A1 (SIEMIENIEC RALF [AT] ET AL) 21 September 2006 (2006-09-21) Abs.Fig. and corresponding text	1-37
A	US 2004/212011 A1 (RYU SEI-HYUNG [US]) 28 October 2004 (2004-10-28) Abs.Fig. and corresponding text	1-37
X	US 2003/011039 A1 (AHLERS DIRK [DE] ET AL) 16 January 2003 (2003-01-16) Figs.4 and 5 and corresponding text	24,25, 34,35
X	US 2006/284248 A1 (SAITO WATARU [JP] ET AL) 21 December 2006 (2006-12-21)	24,25, 27,28
Y	Fig.17 and corresponding text	20-23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2011/051413

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-23, 26-33, 36, 37

   device, method of fabrication and method of operation concerning a vertical MOSFET and an vertical or lateral IGBT injector including a combined schottky biassed pn junction. The latter injects minority carriers to the MOSFET drift region, the pn junction being clamped by the schottky limiting carrier number.

   ---

2. claims: 24, 25, 34, 35

   Integrated device and method of fabrication comprising vertically and perpendicularly disposed integrated regions conductively linked to form a charge compensated or superjunction device. The charge compensation reduces ON-voltage

   ---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2011/051413

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2008035134 A1	27-03-2008	CN 101512738 A	19-08-2009
		EP 2067164 A1	10-06-2009
		US 2009267112 A1	29-10-2009
US 2006211189 A1	21-09-2006	DE 102005009020 A1	31-08-2006
US 2004212011 A1	28-10-2004	EP 1616356 A2	18-01-2006
		JP 2006524432 A	26-10-2006
		WO 2004097944 A2	11-11-2004
US 2003011039 A1	16-01-2003	DE 10132136 C1	13-02-2003
US 2006284248 A1	21-12-2006	NONE	