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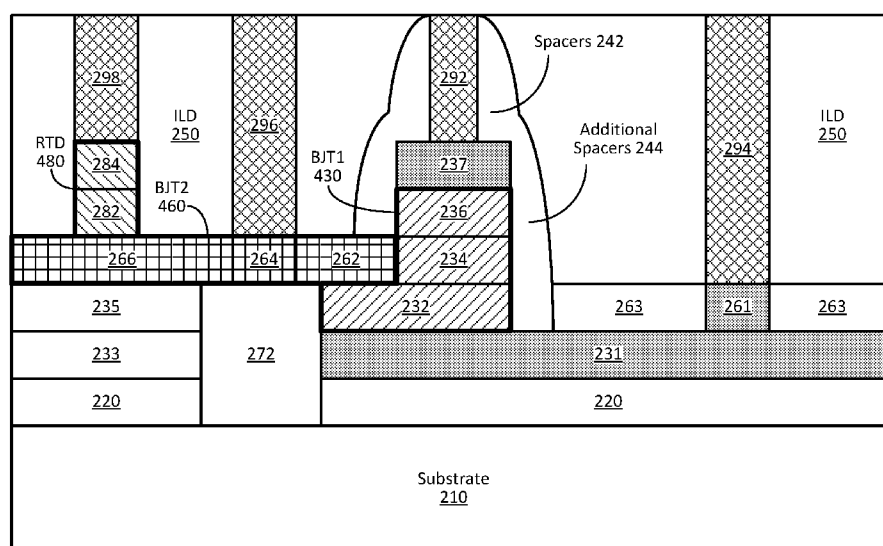


FIG. 4



(57) Abstract: Techniques are disclosed for forming a cell for an N-NDR latch. Such a cell may include two bipolar junction transistors (BJTs) and a resonant-tunneling diode (RTD) in what is referred to herein as a dual BJT plus RTD cell. In some cases, a latch configuration can be achieved using two of the dual BJT plus RTD cells (for a total of four BJTs and two RTDs) to enable storage of a bit of data (e.g., a '1' or a '0'), which can be used for memory applications (e.g., for SRAM applications). For example, both a pull-up network (PUN) and a pull-down network (PDN) can be formed using the dual BJT plus RTD cell disclosed herein, such that the two cells can be coupled into a latch design having a pull-up and pull-down network. Other embodiments may be described and/or disclosed.

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## CELL FOR N-NEGATIVE DIFFERENTIAL RESISTANCE (NDR) LATCH

## BACKGROUND

5 In circuits and electronics, a latch is an example of a bistable multivibrator. In other words, a latch is a device with two stable states, which may represent a high-output (e.g., '1') and a low-output (e.g., '0'). A latch has a feedback path, so information can be retained by the device such that the device can be used as a data storage element. Thus, latches can be used for memory applications, as they can store a bit of data (e.g., a '1' or a '0') for as long as the device  
10 is receiving power. Latches are similar to flip-flops, where they can both be used as data storage elements; however, latches are not synchronous devices and do not operate on clock edges, as flip-flops do. Instead, latches are typically classified as simple, transparent, opaque, or asynchronous.

Numerous types of semiconductor memory currently exist. The primary objectives in  
15 manufacturing many such devices include obtaining a device that occupies as small an area as possible and consumes low levels of power using low supply levels, while performing at speeds comparable to speeds realized by larger devices. The construction and formation of such memory circuitry typically involves forming at least one storage element and circuitry designed to read and write the stored information. In applications where circuit space, power  
20 consumption, and circuit speed are primary design goals, the formation and layout of memory devices can be very important. Typical random access memory (RAM) devices, such as static RAM (SRAM) and dynamic RAM (DRAM), often make compromises for these primary design goals. SRAMs, for example, are typically based on a four-transistor ("4T") cell (e.g., including four n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) and two polycrystalline-silicon (poly-Si) load resistors) or a six-transistor ("6T") cell (e.g., including four  
25 n-channel MOSFETs and two p-channel MOSFETs). Such cells are compatible with CMOS technology, consume relatively low levels of standby power, operate at relatively low voltage levels, and perform at relatively high speeds. However, the 4T and 6T cells are typically implemented using a large cell area, which significantly limits the maximum density of such  
30 SRAM devices.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an example method of forming an integrated circuit (IC) including a dual bipolar junction transistor (BJT) plus resonant-tunneling diode (RTD) cell for an N-negative differential resistance (NDR) latch, in accordance with some embodiments of the present disclosure.

Figures 2A-R illustrate example IC structures formed when carrying out the method of Figure 1, in accordance with some embodiments of the present disclosure. Note that the structures of Figures 2A-R are cross-sectional views taken along what will eventually be the layers of the dual BJT plus RTD cell.

Figure 2R' illustrates a blown-out view of an example alternative structure for the RTD portion of the dual BJT plus RTD cell of Figure 2R, in accordance with an embodiment of the present disclosure.

Figures 3A-B illustrate the example structure of Figure 2R, including visual patterning of some of the features or layers to help illustrate example material and/or doping schemes, in accordance with some embodiments of the present disclosure.

Figure 4 illustrates the example structure of Figure 2R, including visual patterning and shading of some of the features and layers to help illustrate the dual BJT plus RTD cell structure, in accordance with some embodiments of the present disclosure.

Figure 5A is a circuit diagram of an example pull-up network including a dual BJT plus RTD cell, in accordance with an embodiment of the present disclosure.

Figure 5B is a circuit diagram of an example pull-down network including a dual BJT plus RTD cell, in accordance with an embodiment of the present disclosure.

Figure 5C is a circuit diagram including the pull-up network of Figure 5A and the pull-down network of Figure 5B in a memory latch configuration, in accordance an embodiment of the present disclosure.

Figure 6 is a chart of output current ( $I_{out}$ ) versus output voltage ( $V_{out}$ ) illustrating example current-voltage (IV) characteristics of the circuit diagram of Figure 5C, in accordance with an embodiment of the present disclosure.

Figure 7 illustrates an example computing system implemented with the integrated circuit structures and/or techniques disclosed herein, in accordance with some embodiments of the present disclosure.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the

drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines and right angles, and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. Further still, some of the features in the drawings may include a patterned and/or shaded fill, which is primarily provided to assist in visually differentiating the different features. In short, the figures are provided merely to show example structures.

## DETAILED DESCRIPTION

Techniques are disclosed for forming a memory device configured with an N-NDR latch. In some embodiments, the techniques are implemented as an integrated (IC) circuit configuration that includes two bipolar junction transistors (BJTs) and a resonant-tunneling diode (RTD) in what is referred to herein as a dual BJT plus RTD cell. The cell can be used in a latch configuration that exhibits N-NDR current-voltage (IV) curves with relatively high peak-to-valley (PVR) ratio. The IV curves intersect and create two stable points in the IV profile. These points can be used as the “0” and “1” in a memory cell, such as an SRAM cell. For NDR devices, the current first increases with increasing applied voltage, reaching a peak value, then decreases with increasing applied voltage over a range of applied voltages, thereby exhibiting negative differential resistance (NDR) over this range of applied voltages and reaching a minimum (‘valley’) value. At even higher applied voltages, the current again increases with increasing applied voltage. Thus, the current-versus-voltage characteristic of an NDR device is shaped like the letter “N”, resulting in such devices being referred to as N-NDR devices. As will be appreciated in light of this disclosure, such an NDR-based memory cell has a cell area smaller than typical 4T and 6T SRAM cells, because of the smaller number of included active devices and interconnections, according to some embodiments.

In general, BJTs can use either electrons or holes as the charge carriers and include three semiconductor regions: the emitter region (or emitter), the base region (or base), and the collector region (or collector). These regions are typically respectively doped with p-type, n-type, and p-type dopants in a PNP transistor configuration or respectively doped with n-type, p-type, and n-type dopants in an NPN transistor configuration. Further, each region (the emitter,

base, and collector) may be electrically connected to a corresponding terminal or contact. The base is physically located between the emitter and collector, in a similar manner that the channel of a MOSFET is located between the source and drain. An RTD is a diode that has a resonant-tunneling structure in which electrons can tunnel through resonant states at different energy levels. The current-voltage (IV) characteristic often exhibits NDR regions. The PVR of RTDs is typically not high enough to make them practical for low-power memory applications, because in order for the RTDs to have sufficient current drive, the valley current is too large, causing large static power dissipation. However, the dual BJT plus RTD cells described herein enable N-NDR IV characteristics with a high peak-to-valley ratio (PVR) and relatively low valley currents, making such cells suitable for various memory (e.g., SRAM) applications.

A memory can be implemented using dual BJT plus RTD cells in a number of ways. In some example embodiments, a latch configuration can be achieved using two of the dual BJT plus RTD cells (for a total of four BJTs and two RTDs) to enable storage of a bit of data (e.g., a '1' or a '0'), which can be used for memory cell applications (e.g., for SRAM cell applications). For example, both a pull-up network (PUN) and a pull-down network (PDN) can be formed using the dual BJT plus RTD cell disclosed herein, such that the two cells can be coupled into a latch design having a pull-up and pull-down network. Further, in some embodiments, use of the dual BJT plus RTD cell can enable a relatively small circuit footprint and also provide positive feedback to store a memory state. As can be understood based on this disclosure, the dual BJT and RTD cell can be formed to be relatively smaller than typical SRAM cells due to, for example, the use of vertical integration for the dual BJT and RTD cell. As will be apparent in light of this disclosure, techniques and a process flow for formation of the dual BJT plus RTD cell are provided. However, the present disclosure is not intended to be limited to any particular formation techniques or end structure for a dual BJT plus RTD cell, unless otherwise stated.

Use of the techniques and structures provided herein may be detectable using tools such as: electron microscopy including scanning/transmission electron microscopy (SEM/TEM), scanning transmission electron microscopy (STEM), and reflection electron microscopy (REM); composition mapping; x-ray crystallography or diffraction (XRD); energy-dispersive x-ray spectroscopy (EDS); secondary ion mass spectrometry (SIMS); time-of-flight SIMS (ToF-SIMS); atom probe imaging or tomography; local electrode atom probe (LEAP) techniques; 3D tomography; or high resolution physical or chemical analysis, to name a few suitable example analytical tools. In particular, in some embodiments, such tools may indicate a dual BJT plus RTD cell as variously described herein. Further, in some such embodiments, two of the dual BJT plus RTD cells may be used in a memory latch structure, such as where one of the cells

forms a pull-up network and the other of the cells forms a pull-down network, for example. Thus, as can be understood based on this disclosure, the dual BJT plus RTD cells variously described herein may be used for memory applications, such as for applications where SRAM is being used. In some embodiments, the techniques and structures described herein may be detected based on the benefits derived from using a dual BJT plus RTD cell, such as the relatively high PVR values for such a cell and/or the IC footprint benefits achieved from using such a cell (e.g., compared to typical SRAM cells). Numerous configurations and variations will be apparent in light of this disclosure.

#### Methodology and Architecture

Figure 1 illustrates an example method 100 of forming an integrated circuit (IC) including a dual bipolar junction transistor (BJT) plus resonant-tunneling diode (RTD) cell for an N-negative differential resistance (NDR) latch, in accordance with some embodiments of the present disclosure. Figures 2A-R illustrate example IC structures formed when carrying out the method 100 of Figure 1, in accordance with some embodiments of the present disclosure. Note that the structures of Figures 2A-R are cross-sectional views taken along what will eventually be the layers of the dual BJT plus RTD cell. However, in some embodiments, all of the layers of the three devices (two BJTs and one RTD) need not be visible in a single cross-sectional view, as there may be an offset of one or more of the layers in a Z direction (the direction going into or coming out of the page). Therefore, in some embodiments, more than one cross-sectional view may be required to identify the dual BJT plus RTD cells variously described herein. As can be understood based on this disclosure, the dual BJT plus RTD cell formed using method 100 can be used for a pull-up network (PUN) and/or a pull-down network (PDN) of a memory cell (e.g., an SRAM cell). Method 100 and the structures of Figures 2A-R are provided as examples to help illustrate techniques for forming a dual BJT plus RTD cell and are not intended to limit the present disclosure. Note that the BJT devices are primarily referred to herein as a first BJT (or BJT1) and a second BJT (or BJT2) for ease of reference. However, the designation of first (or 1) and second (or 2) for the BJTs is not intended to designate any preference, order, or any other limiting characteristic. In some embodiments, the techniques may be used to benefit devices of varying scales, such as IC devices having critical dimensions in the micrometer range or in the nanometer range (e.g., formed at the 32, 22, 14, 10, 7, or 5 nm process nodes, or beyond).

Method 100 of Figure 1 includes forming 110 a stack of layers for a first BJT on a substrate to form the example structure of Figure 2A, in accordance with some embodiments. Method 100 may also include a preliminary process of providing the substrate, for example. As shown in Figure 2A, six layers are formed on and above substrate 210, in this example

embodiment. As will be apparent in light of this disclosure, the layers formed on substrate 210 will be used to form a first BJT (BJT1) device. The stack of layers formed on and/or above substrate 210 in the example structure of Figure 2A include isolation layer 220, the BJT1 collector contact layer 231, BJT1 collector layer 232, BJT1 base layer 234, BJT1 emitter layer 236, and BJT1 emitter contact layer 237. In some embodiments, the stack of layers (220, 231, 232, 234, 236, and 237) on/above substrate 210 may be formed using any suitable techniques, such as depositing the layers as shown in Figure 2A using, for example, metal-organic chemical vapor deposition (MOCVD), molecular-beam epitaxy (MBE) chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), and/or any other suitable processes as will be apparent in light of this disclosure. In some embodiments, the stack of layers (220, 231, 232, 234, 236, and 237) may be blanket deposited on the substrate 210 or the stack of layers may be selectively deposited/grown in desired locations on substrate 210, for example. Note that in the figures and the disclosure included herein, one or more of the layers may be described based on the end use for the layer in the dual BJT plus RTD cell, for clarity of disclosure. However, the present disclosure is not intended to be so limited unless otherwise stated.

Substrate 210, in some embodiments, may include: a bulk substrate including a group IV material, such as silicon (Si), germanium (Ge), silicon germanium (SiGe), or silicon carbide (SiC), and/or at least one group III-V material and/or sapphire and/or any other suitable material(s) as will be apparent in light of this disclosure; an X on insulator (XOI) structure where X is one of the aforementioned materials (e.g., group IV and/or group III-V and/or sapphire) and the insulator material is an oxide material or dielectric material or some other electrically insulating material; or some other suitable multilayer structure where the top layer includes one of the aforementioned materials (e.g., group IV and/or group III-V and/or sapphire). Note that group IV material as used herein includes at least one group IV element (e.g., carbon, silicon, germanium, tin, lead), such as Si, Ge, SiGe, or SiC to name some examples. Note that group III-V material as used herein includes at least one group III element (e.g., aluminum, gallium, indium, boron, thallium) and at least one group V element (e.g., nitrogen, phosphorus, arsenic, antimony, bismuth), such as gallium arsenide (GaAs), gallium nitride (GaN), indium gallium arsenide (InGaAs), indium gallium nitride (InGaN), aluminum gallium arsenide (AlGaAs), aluminum gallium nitride (AlGaN), and indium phosphide (InP), to name some examples. In some embodiments, substrate 210 may be doped with one or more materials, such as including p-type or n-type impurity doping of any suitable concentration, for example. In some embodiments, substrate 210 may include a surface crystalline orientation described by a Miller

Index of  $\langle 100 \rangle$ ,  $\langle 110 \rangle$ , or  $\langle 111 \rangle$ , or its equivalents, as will be apparent in light of this disclosure. Although substrate 210, in this example embodiment, is shown as having a thickness T1 (the dimension in the Y direction) similar to the other layers for ease of illustration, in some instances, substrate 210 may be much thicker than the other layers, such as having a thickness in the range of 50 to 950 microns, for example. In some embodiments, substrate 210 may be used for one or more other IC devices, such as various diodes (e.g., light-emitting diodes (LEDs) or laser diodes), various transistors (e.g., MOSFETs and/or TFETs), various capacitors (e.g., MOSCAPs), various microelectromechanical systems (MEMS), various nanoelectromechanical systems (NEMS), various sensors, or any other suitable semiconductor or IC devices, depending on the end use or target application. Accordingly, in some embodiments, the structures described herein may be included in a system-on-chip (SoC) application, as will be apparent in light of this disclosure.

Isolation layer 220, in some embodiments, may be formed to assist with electrically insulating the overlying layers (and the subsequently formed overlying dual BJT plus RTD cell) from substrate 210, for example. In some embodiments, isolation layer 220 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, isolation layer 220 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than  $1\text{E}15$ ,  $1\text{E}16$ ,  $1\text{E}17$ ,  $1\text{E}18$ ,  $1\text{E}19$ ,  $1\text{E}20$ , or  $1\text{E}21$  per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layer 220 may be in the range of  $1\text{E}15$  to  $7\text{E}21$  per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than  $1\text{E}18$  per cubic cm, for example. In some embodiments, isolation layer may include any suitable material to help to electrically insulate the overlying layers (such as the immediately overlying BJT1 collector contact layer 231, in this example embodiment) from substrate 210. For instance, in some embodiments, BJT1 collector contact layer 231 may be doped with an n-type or p-type dopant (e.g., n-type doped or p-type doped Si or SiGe), and in such embodiments, isolation layer 220 may be doped with the opposite type dopant of immediately overlying layer 231. For example, in some such embodiments, if BJT1 collector contact layer 231 is an n-type doped layer (e.g., n-type doped Si), then isolation layer 220 may include p-type doped material (e.g., p-type doped Si), such that the n/p interface of layers 231/220 forms a diode to provide electrical isolation from substrate 210. However, in some embodiments, isolation layer 220 need not be present and is thus an optional layer, as can

be understood based on this disclosure. For instance, in the previous example where BJT1 collector contact layer 231 is an n-type doped layer (e.g., n-typed doped Si), then substrate 210 may include p-type doped material (e.g., p-type doped Si) to assist with electrical isolation. In some embodiments, optional isolation layer 220, when present, may have any suitable thickness T2 (dimension in the Y direction), such as a thickness of 10 to 100 nm (e.g., 20 to 50 nm), or any other suitable thickness as will be apparent in light of this disclosure.

BJT1 collector contact layer 231, in some embodiments, may be formed to be used as a contact layer for the collector or collector region of the first BJT in the dual BJT plus RTD cell, for example. In some embodiments, BJT1 collector contact layer 231 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT1 collector contact layer 231 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layer 231 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than 1E18 per cubic cm, for example. In some embodiments, BJT1 collector contact layer 231 may have any suitable thickness T3 (dimension in the Y direction), such as a thickness of 10 to 100 nm (e.g., 20 to 50 nm), or any other suitable thickness as will be apparent in light of this disclosure.

BJT1 collector layer 232, in some embodiments, may be formed to be used as the collector or collector region for the first BJT in the dual BJT plus RTD cell, for example. In some embodiments, BJT1 collector layer 232 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT1 collector layer 232 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layer 232 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively low, such as less than 1E18 per cubic cm, for example. In some embodiments, BJT1 collector layer 232 may have any suitable thickness T4 (dimension in the Y direction), such as a thickness of 10 to

50 nm (e.g., 20 to 40 nm), or any other suitable thickness as will be apparent in light of this disclosure.

BJT1 base layer 234, in some embodiments, may be formed to be used as the base or base region for the first BJT in the dual BJT plus RTD cell, for example. In some embodiments, BJT1 base layer 234 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT1 base layer 234 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layer 234 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than 1E18 per cubic cm, for example. In some embodiments, BJT1 base layer 234 may have any suitable thickness T5 (dimension in the Y direction), such as a thickness of 10 to 50 nm (e.g., 20 to 40 nm), or any other suitable thickness as will be apparent in light of this disclosure.

BJT1 emitter layer 236, in some embodiments, may be formed to be used as the emitter or emitter region for the first BJT in the dual BJT plus RTD cell, for example. In some embodiments, BJT1 emitter layer 236 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT1 emitter layer 236 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layer 236 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively low, such as less than 1E18 per cubic cm, for example. In some embodiments, BJT1 emitter layer 236 may have any suitable thickness T6 (dimension in the Y direction), such as a thickness of 10 to 50 nm (e.g., 20 to 40 nm), or any other suitable thickness as will be apparent in light of this disclosure.

BJT1 emitter contact layer 237, in some embodiments, may be formed to be used as a contact layer for the emitter or emitter region of the first BJT in the dual BJT plus RTD cell, for example. In some embodiments, BJT1 emitter contact layer 237 may include any suitable

material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT1 emitter contact layer 237 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layer 237 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than 1E18 per cubic cm, for example. In some embodiments, BJT1 emitter contact layer 237 may have any suitable thickness T7 (dimension in the Y direction), such as a thickness of 10 to 100 nm (e.g., 20 to 50 nm), or any other suitable thickness as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with patterning 112 (or otherwise forming) a dummy gate (DG) 240 for the first BJT (BJT1) and forming spacers 242 on both sides of the dummy gate, to form the example structures of Figures 2B and 2C, in accordance with an embodiment. In some embodiments, dummy gate 240, formed above substrate 210 and on the stack of layers in the example structure of Figure 2A, may be formed using any suitable techniques, such as depositing the dummy gate material and patterning it to the shape shown in Figure 2B. Dummy gate 240 may include any suitable thickness (dimension in the Y direction) and any suitable width (dimension in the X direction), as can be understood based on this disclosure. In some embodiments, dummy gate 240 is formed to be layer removed and replaced with interconnect material for making electrical contact to BJT1 emitter contact layer 237 (and thereby being electrically connected to BJT1 emitter layer 236), for example. In some embodiments, dummy gate 240 may include any suitable materials, and may even include a dummy gate dielectric (e.g., dummy oxide material) and a dummy gate electrode (e.g., dummy poly-silicon material), for example. Formation of spacers 242 shown in the example structure of Figure 2C may be performed using any suitable techniques, such as depositing the spacer material and performing a spacer etch to form the structure shown. Spacers 242 (also referred to as gate spacers or sidewall spacers) may include any suitable material, such as any suitable electrical insulator, dielectric, oxide (e.g., silicon oxide), and/or nitride (e.g., silicon nitride) material, as will be apparent in light of this disclosure. As can be understood based on this disclosure, dummy gate 240 may be considered a hardmask feature to be later removed and replaced with a metal feature, for example.

Method 100 of Figure 1 continues with etching 114 the emitter layers 236, 237 and base layer 234 of the first BJT to form the example structure of Figure 2D, in accordance with an embodiment. In some embodiments, etch 114 may be performed using any suitable techniques, such as any suitable wet and/or dry etch processes, and gate 240 and spacers 242 may serve as a mask for the etch process(es), for example. For instance, in an example embodiment, layer 234 may include different material, such as doped SiGe, relative to layers 232, 236, and 237, which may include doped Si. In such an example embodiment, a wet etch may be performed to remove BJT1 emitter contact layer 237 and BJT1 emitter layer 236, where the etchant used selectively removes the material of layers 237 and 236 relative to layer 234 (where selectively removes includes removing the material at a rate of at least 2, 3, 4, 5, 10, 15, 20, or 25 times faster, for example) such that the underlying layer 234 can act as an etch stop layer. Then, in such an example embodiment, another wet etch may be performed to remove BJT1 base layer 234, using an etchant that selectively removes the material of layer 234 relative to layer 232, such that the underlying layer 232 can act as an etch stop layer. As can be understood based on this disclosure, where gate 240 and spacers 242 act as a mask for the etch 114 process(es), the width (dimension in the X direction) of those features may approximate the width (dimension in the X direction) of the resulting BJT1 emitter contact layer 237, BJT1 emitter layer 236, and BJT1 base layer 234, for example. Thus, in such cases, the gate 240 and spacers 242 may be formed with a desired width to achieve a desired resulting width of layers 237, 236, and 234, as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with asymmetric patterning 116 (or otherwise forming) of hardmask 252 material and etching to expose the BJT1 collector layer 232 on one side of the BJT1 stack of layers, such as is shown in the example structures of Figures 2E and 2F, in accordance with an embodiment. In some embodiments, hardmask (HM) 252 may be formed using any suitable techniques, such as an asymmetric patterning technique (e.g., angled implant process) that only masks off one side of the structure, as shown in Figure 2E, for example. In some embodiments, hardmask 252 may include any suitable material, such as a dielectric material, for example. Continuing from the example structure of Figure 2E, an etch process can be performed to remove the BJT1 collector layer 232 from one side of BJT1 stack of layers (the right side, in this example case, as the left side is masked off), to form the example structure of Figure 2F, in this example embodiment. The etch process may include any suitable techniques, such as a wet and/or dry etch process, or any other suitable process as will be apparent in light of this disclosure. As a result of the etch process performed on only one side of the structure (due

to asymmetric hardmask 252), BJT1 collector contact layer 231 is exposed on that side, as shown in Figure 2F.

Method 100 of Figure 1 continues with removing 118 the asymmetric hardmask 252 and forming additional spacers 244 to form the example structure of Figure 2G, in accordance with an embodiment. As shown in the example structure of Figure 2G, asymmetric hardmask 252 present in the structure of Figure 2F was removed (e.g., using a suitable etch process), and then additional spacers 244 were deposited on both sides of the BJT1 stack of layers, in this example embodiment. In some cases, additional spacers 242 may be formed using any suitable techniques, such as performing an angled deposition or implant process, or any other suitable process as will be apparent in light of this disclosure. In some embodiments, additional spacers 244 may be formed using asymmetric hardmask 252, such that the hardmask 252 material is not removed prior to forming additional spacers 244 or such hardmask 252 material may be a part of additional spacers 244, for example. In some such embodiments, only the right side of additional spacers 244 may be formed, as the left side may be formed from hardmask 252. In some embodiments, additional spacers 244 may include any suitable material, such as any suitable electrical insulator, dielectric, oxide (e.g., silicon oxide), and/or nitride (e.g., silicon nitride) material, as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with depositing 120 the second BJT (BJT2) layer 260 to form the example structure of Figure 2H, in accordance with an embodiment. As shown in the example structure of Figure 2H, BJT2 layer 260 was formed on the left side of the structure of Figure 2G on BJT1 collector layer 232, in contact with BJT1 base layer 234, and under additional spacers 242, and BJT2 layer 260 was also formed on the right side of the structure of Figure 2G, on BJT1 collector contact layer 231. In some embodiments, BJT2 layer 260 may be formed using any suitable techniques, such using any of the aforementioned deposition techniques (e.g., MOCVD, MBE, CVD, ALD, PVD) and/or any other suitable process(es) as will be apparent in light of this disclosure. In some embodiments, BJT2 layer 260 may be blanket deposited or may be selectively deposited/grown in desired locations, for example. In some embodiments, BJT2 layer 260 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT2 layer 260 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than  $1\text{E}15$ ,  $1\text{E}16$ ,  $1\text{E}17$ ,  $1\text{E}18$ ,  $1\text{E}19$ ,  $1\text{E}20$ , or  $1\text{E}21$  per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this

disclosure. In other words, the dopant level for layer 260 may be in the range of  $1\text{E}15$  to  $7\text{E}21$  per cubic cm, for example. In some embodiments, the doping level may be relatively low, such as less than  $1\text{E}18$  per cubic cm, for example. In some embodiments, BJT2 layer 260 may have any suitable thickness T8 (dimension in the Y direction), such as a thickness of 10 to 50 nm (e.g., 20 to 40 nm), or any other suitable thickness as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with depositing 122 interlayer dielectric (ILD) 250 material and polishing the structure to form the example structure of Figure 2I, in accordance with an embodiment. In some embodiments, ILD 250 may be deposited 122 and polished/planarized using any suitable techniques, and in some embodiments, the polishing/planarization process need not be performed. In some embodiment ILD 250 may include any suitable electrical insulator, dielectric, oxide (e.g., silicon oxide), and/or nitride (e.g., silicon nitride) material, as will be apparent in light of this disclosure. As can be understood based on this disclosure, the ILD 250 material shown may be at metallization layer 0 (M0) as shown; however, the present disclosure need not be so limited (e.g., if one or more of the devices of the dual BJT plus RTD cell are formed at a back end location of the integrated circuit).

Method 100 of Figure 1 continues with forming 124 vias 253, 255 in the ILD material 250 at first BJT collector contact location and second BJT base location to form the example structure of Figure 2J, in accordance with an embodiment. In some embodiments, vias 253, 255 may be formed using any suitable techniques, such as any suitable wet and/or dry etching processes, as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with patterning 126 (or otherwise forming) implant material and activating the same to form BJT1 collector contact portion 261 and second BJT base 264, shown in the example structure of Figure 2K, in accordance with an embodiment. In some embodiments, patterning 126 implant and activating the same may include any suitable techniques, such as depositing material in vias 253 and 255, annealing the structure to drive dopants from the material into the underlying layer 260 at both locations, and etching to remove the material after the dopants have been driven into the locations indicated as 261 and 264 in Figure 2K, for example. In some embodiments, features 261 and 264 may include any suitable impurity dopants as a result of process 126, such as n-type and/or p-type dopant, for example. As can be understood based on this disclosure, in this example embodiment, BJT1 collector contact portion 261 and second BJT base 264 includes the material of layer 260, with the addition of dopant material. However, in some other embodiments, feature 261 and/or 264 may be formed by removing/etching those portions of layer 260 from the structure of Figure 2J and replacing the material with substitute material. In any such embodiments, features 261 and 264

may include any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, BJT1 collector contact portion 261 and second BJT base 264 may be doped with a suitable n-type or p-type dopant, as will be apparent in light of this disclosure. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for features 261 and 264 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than 1E18 per cubic cm, for example. In some embodiments, the dopant may be of opposite type than that of original BJT2 layer 260. For instance, in an example embodiment, if BJT2 layer 260 was originally doped with a p-type dopant, then BJT base 264 may be doped with an n-type dopant, and vice versa. In this example embodiment, the formation of BJT2 base 264 also assists with establishing the location of BJT2 collector 262 and BJT2 emitter 266, as shown in Figure 2K. In this manner, in some embodiments, BJT2 layer 260 on the left side of the BJT1 stack of layers has been converted into an NPN or PNP BJT including collector 262, base 264, and emitter 266, for example. In addition, layer 260 on either side of BJT1 collector contact portion 261 has been relabeled as portions 263, for ease of reference. Note that BJT1 collector contact portion 261 is in physical contact with BJT1 collector contact layer 231, in this example embodiment, and in some embodiments, BJT1 collector contact portion 261 and BJT1 collector contact layer 231 may include the same type of dopants (e.g., both n-type or both p-type).

Method 100 of Figure 1 continues with asymmetric patterning 128 (or otherwise forming) hardmask 254 material over BJT1, and specifically, over BJT1 contact portion 261 in via 253, to form example structure 2L, in accordance with an embodiment. In some embodiments, hardmask (HM) 254 may be formed using any suitable techniques, such as an asymmetric patterning technique that only deposits the hardmask material in via 253 and not in via 255, as shown in Figure 2L, for example. In some embodiments, hardmask 254 may include any suitable material, such as a dielectric material, for example.

Method 100 of Figure 1 continues with selectively etching 130 layers under the second BJT base 264 to form gap (or air gap) 270, and to form the example structure of Figure 2M, in accordance with an embodiment. In some embodiments, selective etch 130 may be performed using any suitable techniques, such as performing a wet etch process including an etchant that removes the material of layers 232, 231, and 220 relatively faster than the etchant removes the material of BJT2 base 264, such as at a relative rate of at least 2, 3, 4, 5, 10, 15, 20, or 25 times

faster, for example. For instance, in an example embodiment, layers 232, 231, and 220 may all include Si and BJT2 base 264 may include SiGe, such that selective etch 130 can be performed using an etchant that selectively removes Si material relative to SiGe material to form gap 270. Note that selective etch may be performed in via 255, in some embodiments. Also note that gap 270 has separated layer 231 into BJT1 collector contact layer 231 and remnants of layer 231 now labeled as portion 233 and also separated layer 232 into BJT1 collector layer 232 and remnants of layer 232 now labeled as portion 235, in this example embodiment. Further note that although gap 270 is wider (dimension in the X direction) than BJT2 base 264, the present disclosure is not intended to be so limited.

Method 100 of Figure 1 continues with optionally depositing 132 electrically insulating material 272 in gap 270 and patterning 134 (or otherwise forming) hardmask 256 over second BJT base 264, followed by a polish or planarization process, to form the example structure of Figure 2N, in accordance with an embodiment. In some embodiments, air gap 270 need not be filled with electrically insulating material 272, as the air gap 270 itself may serve as a suitable electrical insulator. However, in some embodiments, insulator material 272, such as any suitable electrical insulator, dielectric, oxide (e.g., silicon oxide), and/or nitride (e.g., silicon nitride) material, may be deposited to form the example structure of Figure 2N. In some such embodiments, filling (or substantially filling) air gap 270 with insulator material 272 may assist with providing structural support for the dual BJT plus RTD structure (as opposed to having an air gap under at least a portion of BJT2), for example. Regardless of whether feature 272 remains an air gap or is filled with insulator material, in this example embodiment, the process continues with patterning 134 hardmask 256, which results in via 255 of the structure of Figure 2M being filled with hardmask material 256 as shown in Figure 2N. In some embodiments, hardmask 256 may be patterned, deposited, or otherwise formed using any suitable techniques. In some embodiments, hardmask 256 may include any suitable material, such as a dielectric material, for example.

Method 100 of Figure 1 continues with forming 136 a via 257 in the ILD material 250 at the RTD contact location to form the example structure of Figure 2O, in accordance with an embodiment. In some embodiments, via 257 may be formed using any suitable techniques, such as any suitable wet and/or dry etching processes, as will be apparent in light of this disclosure. Note that via 257 is formed over BJT2 emitter 266, as the RTD is to be in contact with BJT2 at that location, as can be understood based on this disclosure.

Method 100 of Figure 1 continues with forming 138 resonant tunneling-diode (RTD), which includes layers 282 and 284, as shown in the example structure of Figure 2P, in

accordance with an embodiment. In some embodiments, RTD layers 282 and 284 may be formed using any suitable techniques, such using any of the aforementioned deposition techniques (e.g., MOCVD, MBE, CVD, ALD, PVD) and/or any other suitable process(es) as will be apparent in light of this disclosure. In some embodiments, RTD layers 282 and 284 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, the RTD layers 282 and 284 may include an n-type layer and a p-type layer, to create a p-n junction, for example. In some such embodiments, the dopant levels may be selected to be greater than 1E15, 1E16, 1E17, 1E18, 1E19, 1E20, or 1E21 per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layers 282 and 284 may be in the range of 1E15 to 7E21 per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than 1E18 per cubic cm, for example. In such embodiments, layers 282 and 284 may be heavily doped to achieve an NDR IV characteristic, as can be understood based on this disclosure. In an example embodiment, layer 282 may be a highly p-type doped material, such as highly p-type doped SiGe, and layer 284 may be a highly n-type doped material, such as highly n-type doped SiGe. In some embodiments, RTD layers 282 and 284 may have any suitable thicknesses T9 and T10 (dimensions in the Y direction), respectively such as a thickness of 10 to 100 nm (e.g., 20 to 50 nm), or any other suitable thickness as will be apparent in light of this disclosure. Note that although this example embodiment includes an Esaki diode (or simply, a tunnel diode) for RTD, which includes a heavily doped p-n junction, in other embodiments, the RTD may include a double barrier, triple barrier, quantum well, or quantum wire structure, or any other suitable RTD structure, as will be apparent in light of this disclosure.

Method 100 of Figure 1 continues with removing 140 hardmask 254 and 256 and dummy gate 240 material to form the example structure of Figure 2Q and forming metal features 292, 294, 296, and 298 to form the example structure of Figure 2R, in accordance with an embodiment. In some embodiments, removal of hardmask 254 and 256 and dummy gate 240 may be performed using any suitable techniques, such as using one or more wet and/or dry etch processes, for example. As shown in Figure 2Q, removal of the hardmask and dummy gate material forms vias, including via 251 over (and exposing) BJT1 emitter contact layer 237, via 253 over (and exposing) BJT1 collector contact portion 261, and via 255 over (and exposing) BJT2 base 264, for example. As is also shown, via 257 is over (and exposes) RTD layer 284, in this example embodiment. As shown in Figure 2R, metal features 292, 294, 296, and 298 were

formed in vias 251, 253, 255, and 257, respectively, in this example embodiment. In some embodiments, metal features 292, 294, 296, and 298 may be considered interconnects and may be formed using any suitable techniques, such as depositing the material in the vias and optionally planarizing and/or polishing the structure, and/or any other suitable process(es) as will be apparent in light of the present disclosure. In some embodiments, metal features 292, 294, 296, and 298 may include any suitable electrically conductive material, such as any suitable metal or metal alloy, such as copper (Cu), cobalt (Co), molybdenum (Mo), rhodium (Rh), beryllium (Be), chromium (Cr), manganese (Mn), aluminum (Al), silver (Ag), gold (Au), titanium (Ti), indium (In), ruthenium (Ru), palladium (Pd), tungsten (W), and/or nickel (Ni), to name a few examples. In some embodiments, the material of features 292, 294, 296, and 298 need not include metal, such as where one or more of the features includes graphene, for example. Accordingly, any suitable electrically conductive material can be used, in some embodiments.

Figure 2R' illustrates a blown-out view of an example alternative structure for the RTD portion of the dual BJT plus RTD cell of Figure 2R, in accordance with an embodiment of the present disclosure. As shown, Figure 2R' (located above Figure 2R) illustrates an alternative to the RTD stack formed for the dual BJT plus RTD cell structure. More specifically, in this example embodiment, the alternative structure includes layer 281 at the bottom of the RTD stack of layers, which may be used as a contact layer for the RTD device. In other words, RTD contact layer 281 may be located between RTD layer 282 and BJT2 emitter 266, for example. In embodiments where present, RTD contact layer 281 may be formed using any suitable techniques, such using any of the aforementioned deposition techniques (e.g., MOCVD, MBE, CVD, ALD, PVD) and/or any other suitable process(es) as will be apparent in light of this disclosure. In some such embodiments, RTD contact layer 281 may include any suitable material, such as any suitable group IV semiconductor material (e.g., Si, SiGe, Ge, SiGeC) and/or any suitable group III-V semiconductor material (e.g., AlGaAs, GaAs, InP, InGaAs, GaN, InGaN). In some embodiments, the RTD contact layer 281 may include an n-type or p-type dopants, for example. In some such embodiments, the dopant levels may be selected to be greater than  $1\text{E}15$ ,  $1\text{E}16$ ,  $1\text{E}17$ ,  $1\text{E}18$ ,  $1\text{E}19$ ,  $1\text{E}20$ , or  $1\text{E}21$  per cubic cm, or some other suitable minimum threshold amount of doping as will be apparent in light of this disclosure. In other words, the dopant level for layers 282 and 284 may be in the range of  $1\text{E}15$  to  $7\text{E}21$  per cubic cm, for example. In some embodiments, the doping level may be relatively high, such as greater than  $1\text{E}18$  per cubic cm, for example. In embodiments where RTD contact layer 281 is present, it may be doped of an opposite type relative to overlying RTD layer 282. For instance, in an

example embodiment where RTD layer 282 is to be n-type doped, RTD contact layer may be p-type doped, and vice versa. In some embodiments, where RTD contact layer 281 is present, it may have any suitable thicknesses (dimension in the Y direction), such as a thickness of 10 to 100 nm (e.g., 20 to 50 nm), or any other suitable thickness as will be apparent in light of this disclosure.

Figures 3A-B illustrate the example structure of Figure 2R, including visual patterning of some of the features or layers to help illustrate example material and/or doping schemes, in accordance with some embodiments of the present disclosure. As can be understood, the previous relevant disclosure with respect to Figures 2A-R is equally applicable to the example structures of Figures 3A-B. As shown in Figures 3A-B, features or layers that include diagonal patterning from the bottom left to the top right (e.g., similar to slashes) may include one of n-type and p-type doping, while the features or layers that include diagonal patterning from the bottom right to the top left (e.g., similar to backslashes) may include the other of n-type and p-type doping. For instance, in the example structure of Figure 3B, it can be seen that the features or layers including diagonal patterning from the bottom left to the top right are p-type doped and the features or layers including diagonal patterning from the bottom right to the top left are n-type doped. Further, in some such embodiments, the density of the diagonal patterning (e.g., the number of slashes or backslashes in a given area) may correspond with the amount of doping, with relatively lower density patterning (e.g., layer 263) indicating relatively lower doping concentrations (e.g., amounts less than  $1\text{E}18$  per cubic cm) and with relatively higher density patterning (e.g., layer 234) indicating relatively higher doping concentrations (e.g., amounts greater than  $1\text{E}18$  per cubic cm), for example. Also note, for completeness of description, the metal features (292, 294, 296, 298) are filled with crosshatch patterning. Although substrate 210 is not shown with a pattern, in some embodiments, it may include doping, for example.

Example materials are indicated for the features and layers of the structure of Figure 3A in the structure of Figure 3B, where 'P-' indicates relatively low p-type doping (relative to the 'P+' features/layers) of the material following the designation (e.g., Si or SiGe), 'P+' indicates relatively high p-type doping (relative to the 'P-' features/layers) of the material following the designation, 'N-' indicates relatively low n-type doping (relative to the 'N+' features/layers) of the material following the designation, and 'N+' indicates relatively high n-type doping (relative to the 'N-' features/layers) of the material following the designation, to provide one specific example. However, note that such example structures are provided for illustration purposes and are not intended to limit the present disclosure. As can be understood based on this disclosure, either of BJT1 and BJT2 may have an NPN or PNP configuration and the RTD may have a PN

or NP configuration. In the example embodiment of Figure 3B, BJT1 has an NPN configuration, where collector 232 is n-type doped, base 234 is p-type doped, and emitter 236 is n-type doped, BJT2 has a PNP configuration, where collector 262 is p-type doped, base 264 is n-type doped, and emitter 266 is p-type doped, and the RTD has a PN configuration, where the first RTD layer 282 is p-type doped, and the second RTD layer 284 is n-type doped. However, in another example embodiment Numerous material and doping scheme variations and configurations for a dual BJT plus RTD cell will be apparent in light of this disclosure.

Figure 4 illustrates the example structure of Figure 2R, including visual patterning and shading of some of the features and layers to help illustrate the dual BJT plus RTD cell structure, in accordance with some embodiments of the present disclosure. As can be understood, the previous relevant disclosure with respect to Figures 2A-R is equally applicable to the example structure of Figure 4. As shown in Figure 4, the features/layers of BJT1 430 (which includes layers 232, 234, and 236, in this example case) are indicated with diagonal patterning that goes from the bottom left to the top right (e.g., similar to slashes) of the structure shown, the features/layers of BJT2 460 (which includes features 262, 264, and 266, in this example case) are indicated with grid-like patterning that includes vertical and horizontal lines, and the features/layers of RTD 480 (which includes layers 282 and 284, in this example case) are indicated with diagonal patterning that goes from the bottom right to the top left (e.g., similar to backslashes) of the structure shown, for example. In addition, each of BJT1 430, BJT2 460, and RTD 480 include a thicker outline to help visually identify the three components of an example dual BJT plus RTD cell. For completeness of description, BJT1 contact features/layers are indicated with grey shading and the metal features are filled with crosshatch patterning, in this example structure. Figure 4 helps illustrate that the base 234 of BJT1 430 is in physical contact with and thus directly electrically connected to the collector 262 of BJT2 460, and also illustrates that the emitter 266 of BJT2 460 is in physical contact with and thus directly electrically connected to the first RTD layer 282 of RTD 480, in this example embodiment.

In some embodiments, the widths of the features/layers (dimension in the X direction) of BJT1 430, BJT2, 460, and RTD 480 may include any suitable width, such as 5 to 200 nm (e.g., 10 to 40 nm), or any other suitable widths as will be apparent in light of this disclosure. For instance, in an example embodiment, BJT2 460 may be formed such that collector 262, base 264, and emitter 266 each have a width (dimension in the X direction) of approximately 10 to 20 nm, to provide one example set of dimensions for one of the devices. As can be understood based on this disclosure, and as seen in Figure 4, the dual BJT plus RTD structure utilizes vertical integration (in the Y direction) for BJT1 430 and RTD 480, while BJT2 460 is formed in a

horizontal configuration (in the X direction), in this example embodiment. In some such embodiments, use of vertical integration for one or more of the components of the dual BJT plus RTD cell can reduce the IC footprint of the cell, for example. Numerous variations and configurations will be apparent in light of this disclosure.

5        Circuit Diagrams and Latch Structure

Figure 5A is a circuit diagram of an example pull-up network 510 including a dual BJT plus RTD cell, in accordance with an embodiment of the present disclosure. Figure 5B is a circuit diagram of an example pull-down network 520 including a dual BJT plus RTD cell, in accordance with an embodiment of the present disclosure. Figure 5C is a circuit diagram including the pull-up network 510 of Figure 5A and the pull-down network 520 of Figure 5B in a memory latch configuration, in accordance an embodiment of the present disclosure. Figure 6 is a chart of output current ( $I_{out}$ ) versus output voltage ( $V_{out}$ ) illustrating example current-voltage (IV) characteristics of the circuit diagram of Figure 5C, in accordance with an embodiment of the present disclosure. A pull-up network provides a low resistance path to  $V_{dd}$  (the positive supply voltage) when output logic is in a high state ('1') and provides a high resistance to  $V_{dd}$  otherwise. A pull-down network provides a low resistance path to  $V_{ss}$  (negative supply or ground) when output logic is in a low state ('0') and provides a high resistance to  $V_{ss}$  otherwise. Thus, a pull-up network can be coupled with a pull-down network to form a memory latch configuration.

20        As shown in Figure 5A, the circuit diagram of the pull-up network 510 includes positive voltage supply  $V_{dd}$  electrically connected to the emitter of BJT1 532, where BJT1 532 has a PNP configuration, in this example embodiment. Further, the base of BJT1 532 is electrically connected to the collector of BJT2 562 (where BJT2 562 has an NPN configuration), the base of BJT2 is electrically connected to a first input current  $I_1$ , and the emitter of BJT2 562 is electrically connected to the anode (and/or p-type portion) of RTD1 582, as shown. In addition, the collector of BJT1 532 and the cathode (and/or n-type portion) of RTD1 582 are electrically connected to the output voltage  $V_{out}$ , as shown. As shown in Figure 5B, the circuit diagram of the pull-down network 520 includes negative supply or ground  $V_{ss}$  electrically connected to the emitter of BJT3 534, where BJT1 534 has an NPN configuration, in this example embodiment. Further, the base of BJT3 534 is electrically connected to the collector of BJT4 564 (where BJT4 546 has a PNP configuration), the base of BJT4 564 is electrically connected to a second input current  $I_2$ , and the emitter of BJT2 564 is electrically connected to the cathode (and/or n-type portion) of RTD2 584, as shown. In addition, the collector of BJT3 534 and the anode (and/or p-type portion) of RTD2 584 are electrically connected to the output voltage  $V_{out}$ , as shown.

Figure 5C illustrates the circuit diagrams of Figures 5A and 5B combined into one circuit diagram to illustrate pull-up network 510 coupled with pull-down network 520 in a memory latch configuration. The IV characteristics of the memory latch configuration of Figure 5C are shown in Figure 6, where the pull-up network 510 has an N-NDR IV characteristic illustrated by pull-up loadline 610 and the pull-down network 520 has an N-NDR IV characteristic illustrated by pull-down loadline 620, in this example embodiment. As shown in Figure 6, the loadlines 610 and 620 intersect and create two stable points in the IV plot, which correspond to a low state (or a '0') and a high state (or a '1') for a memory cell (e.g., an SRAM cell).

As can be understood based on this disclosure, the dual BJT plus RTD cell illustrated in Figures 2R, 3A, and 4 can be used to form both the pull-up network 510 of Figure 5A and the pull-down network of Figure 5B, in accordance with some embodiments. For instance, matching up the integrated circuit devices with those in the circuit diagrams (using Figure 4 for ease of reference), for pull-up network 510, BJT1 430 can be used for BJT1 532, BJT2 460 can be used for BJT2 562, and RTD 480 can be used for RTD1 582, for example. Further, interconnect 292 can be electrically connected to V<sub>dd</sub>, interconnect 294 can be electrically connected to V<sub>out</sub>, interconnect 296 can be electrically connected to I<sub>1</sub>, and interconnect 298 can be electrically connected to V<sub>out</sub>, for example. In addition, for pull-down network 520, BJT1 430 can be used for BJT3 534, BJT2 460 can be used for BJT4 564, and RTD 480 can be used for RTD2 584, for example. Further, interconnect 292 can be electrically connected to V<sub>ss</sub>, interconnect 294 can be electrically connected to V<sub>out</sub>, interconnect 296 can be electrically connected to I<sub>2</sub>, and interconnect 298 can be electrically connected to V<sub>out</sub>, for example. As can also be understood based on this disclosure, the doping scheme illustrated in Figure 3A may be used for either dual BJT plus RTD cell, i.e., for either the pull-up network 510 cell or the pull-down network 520 cell. For instance, the example doping scheme illustrated in Figure 3B could be used for pull-down network 520, as it is labeled with appropriate p-type and n-type doping for the features/layers of the components of the dual BJT plus RTD cell that could be used for pull-down network 520, as can be understood based on this disclosure. For example, as shown in Figure 3B (using the component labels of Figure 4), BJT1 430 includes an NPN configuration, BJT2 460 includes a PNP configuration, and RTD 480 includes an NP configuration. As can also be understood based on this disclosure, a dual BJT plus RTD cell suitable for pull-up network 510 would have an opposite type doping scheme for the features/layers of the components of the dual BJT plus RTD cell, such that BJT1 430 would include a PNP configuration, BJT2 460 would include an NPN configuration, and RTD 480 would include a PN

configuration. Numerous variations and configurations will be apparent in light of the present disclosure.

### Example System

Figure 7 illustrates an example computing system 1000 implemented with the integrated circuit structures and/or techniques disclosed herein, in accordance with some embodiments of the present disclosure. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc.

Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM, SRAM, dual BJT plus RTD cell-based memory), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G,

and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term “processor” may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices formed using the disclosed techniques as variously described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

#### Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit (IC) including: a substrate; a first bipolar junction transistor (BJT) at least one of on and above the substrate, wherein the first BJT includes a first

collector, a first base, and a first emitter; a second BJT at least one of on and above the substrate, wherein the second BJT includes a second collector, a second base, and a second emitter; and a resonant-tunneling diode (RTD) at least on of on and above the substrate, wherein the RTD includes a first RTD layer doped one of n-type and p-type and a second RTD layer doped the  
5 other of n-type and p-type; wherein the first base is electrically connected to the second collector; and wherein the second emitter is electrically connected to the first RTD layer.

Example 2 includes the subject matter of Example 1, wherein the first BJT has an NPN configuration, the second BJT has a PNP configuration, the first RTD layer is n-type doped, and the second RTD layer is p-type doped.

10 Example 3 includes the subject matter of Example 1, wherein the first BJT has a PNP configuration, the second BJT has an NPN configuration, the first RTD layer is p-type doped, and the second RTD layer is n-type doped.

Example 4 includes the subject matter of any of Examples 1-3, wherein the first BJT, second BJT, and RTD each include at least one of silicon (Si) and silicon germanium (SiGe).

15 Example 5 includes the subject matter of any of Examples 1-4, wherein at least one of the first BJT, second BJT, and RTD include group III-V semiconductor material.

Example 6 includes the subject matter of any of Examples 1-5, wherein the first base is between the first collector and the first emitter, and wherein one of the first collector and the first emitter are above the first base.

20 Example 7 includes the subject matter of any of Examples 1-6, wherein the second RTD layer is above the first RTD layer.

Example 8 includes the subject matter of any of Examples 1-7, wherein the second base is between the second collector and the second emitter, such that the second collector and the second emitter are both adjacent to the second base.

25 Example 9 includes the subject matter of any of Examples 1-8, wherein the RTD is above the second emitter.

Example 10 includes the subject matter of any of Examples 1-9, wherein the second collector is adjacent to the first base.

30 Example 11 includes the subject matter of any of Examples 1-10, further including at least one of an air gap and a dielectric material between the second base and the substrate.

Example 12 includes the subject matter of any of Examples 1-11, further including one or more contact layers at least one of above and below the first BJT, the one or more contact layers including dopant concentrations of at least  $1E18$  per cubic cm.

5 Example 13 includes the subject matter of any of Examples 1-12, wherein the first base, the second base, the first RTD layer, and the second RTD layer each include dopant concentrations of at least  $1E18$  per cubic cm.

Example 14 includes the subject matter of any of Examples 1-13, wherein the first BJT, second BJT, and RTD are included in one of a pull-up network and a pull-down network for a memory cell.

10 Example 15 is a memory latch including the subject matter of any of Examples 1-14.

Example 16 is a computing system including the subject matter of any of Examples 1-15.

Example 17 is a memory latch including: a first cell including a first bipolar junction transistor (BJT), a second BJT, and a first resonant-tunneling diode (RTD); and a second cell including a third BJT, a fourth BJT, and a second RTD.

15 Example 18 includes the subject matter of Example 17, wherein one of the first and the second cells is used for a pull-up network and the other of the first and second cells is used for a pull-down network.

Example 19 includes the subject matter of any of Examples 17-18, wherein the first BJT has a PNP configuration, the second BJT has an NPN configuration, the third BJT has an NPN  
20 configuration, and the fourth BJT has a PNP configuration.

Example 20 includes the subject matter of any of Examples 17-19, wherein a base of the first BJT is in physical contact with a collector of the second BJT and wherein a base of the third BJT is in physical contact with a collector of the fourth BJT.

25 Example 21 includes the subject matter of any of Examples 17-20, wherein the first RTD is in physical contact with a base of the second BJT and wherein the second RTD is in physical contact with a base of the fourth BJT.

Example 22 includes the subject matter of any of Examples 17-21, further including a substrate common to both the first and second cells.

30 Example 23 includes the subject matter of any of Examples 17-22, wherein the second BJT is adjacent to the first BJT and the fourth BJT is adjacent to the third BJT.

Example 24 is a computing system including the subject matter of any of Examples 17-23.

Example 25 is a method of forming an integrated circuit (IC), the method including: providing a substrate; forming a first bipolar junction transistor (BJT) at least one of on and above the substrate, wherein the first BJT includes a first collector, a first base, and a first emitter; forming a second BJT at least one of on and above the substrate, wherein the second  
5 BJT includes a second collector, a second base, and a second emitter; and forming a resonant-tunneling diode (RTD) at least one of on and above the substrate, wherein the RTD includes a first RTD layer doped one of n-type and p-type and a second RTD layer doped the other of n-type and p-type.

Example 26 includes the subject matter of Example 25, further including removing  
10 material under the second base to form an air gap.

Example 27 includes the subject matter of Example 26, further including forming dielectric material in the air gap.

Example 28 includes the subject matter of any of Examples 25-27, wherein the first BJT has an NPN configuration, the second BJT has a PNP configuration, the first RTD layer is n-type  
15 doped, and the second RTD layer is p-type doped.

Example 29 includes the subject matter of any of Examples 25-27, wherein the first BJT has a PNP configuration, the second BJT has an NPN configuration, the first RTD layer is p-type doped, and the second RTD layer is n-type doped.

Example 30 includes the subject matter of any of Examples 25-29, wherein the first BJT,  
20 second BJT, and RTD each include at least one of silicon (Si) and silicon germanium (SiGe).

Example 31 includes the subject matter of any of Examples 25-30, wherein at least one of the first BJT, second BJT, and RTD include group III-V semiconductor material.

Example 32 includes the subject matter of any of Examples 25-31, wherein the first base is formed between the first collector and the first emitter, and wherein one of the first collector and  
25 the first emitter are formed above the first base.

Example 33 includes the subject matter of any of Examples 25-32, wherein the second RTD layer is formed above the first RTD layer.

Example 34 includes the subject matter of any of Examples 25-33, wherein the second base is formed between the second collector and the second emitter, such that the second collector and  
30 the second emitter are both adjacent to the second base.

Example 35 includes the subject matter of any of Examples 25-34, wherein the RTD is formed above the second emitter.

Example 36 includes the subject matter of any of Examples 25-34, wherein the RTD is formed adjacent to the second emitter.

Example 37 includes the subject matter of any of Examples 25-36, wherein the second collector is formed adjacent to the first base.

5        Example 38 includes the subject matter of any of Examples 25-37, further including forming one or more contact layers at least one of above and below the first BJT, the one or more contact layers including dopant concentrations of at least  $1\text{E}18$  per cubic cm.

10        Example 39 includes the subject matter of any of Examples 25-38, wherein the first base, the second base, the first RTD layer, and the second RTD layer each include dopant concentrations of at least  $1\text{E}18$  per cubic cm.

Example 40 includes the subject matter of any of Examples 25-39, further including forming a memory latch including the first BJT, the second BJT, and the RTD.

15        The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit this disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of this disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future filed applications claiming priority to this application may claim the disclosed subject matter in a different manner, and may generally include any set of one or more limitations as variously disclosed or otherwise  
20        demonstrated herein.

## CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:  
a substrate;  
5 a first bipolar junction transistor (BJT) at least one of on and above the substrate, wherein the first BJT includes a first collector, a first base, and a first emitter;  
a second BJT at least one of on and above the substrate, wherein the second BJT includes a second collector, a second base, and a second emitter; and  
a resonant-tunneling diode (RTD) at least on of on and above the substrate, wherein the  
10 RTD includes a first RTD layer doped one of n-type and p-type and a second RTD layer doped the other of n-type and p-type;  
wherein the first base is electrically connected to the second collector; and  
wherein the second emitter is electrically connected to the first RTD layer.
2. The IC of claim 1, wherein the first BJT has an NPN configuration, the second  
15 BJT has a PNP configuration, the first RTD layer is n-type doped, and the second RTD layer is p-type doped.
3. The IC of claim 1, wherein the first BJT has a PNP configuration, the second BJT has an NPN configuration, the first RTD layer is p-type doped, and the second RTD layer is n-type doped.
- 20 4. The IC of claim 1, wherein the first BJT, second BJT, and RTD each include at least one of silicon (Si) and silicon germanium (SiGe).
5. The IC of claim 1, wherein at least one of the first BJT, second BJT, and RTD include group III-V semiconductor material.
6. The IC of claim 1, wherein the first base is between the first collector and the first  
25 emitter, and wherein one of the first collector and the first emitter are above the first base.
7. The IC of claim 1, wherein the second RTD layer is above the first RTD layer.

8. The IC of claim 1, wherein the second base is between the second collector and the second emitter, such that the second collector and the second emitter are both adjacent to the second base.

9. The IC of claim 1, wherein the RTD is above the second emitter.

5 10. The IC of claim 1, wherein the second collector is adjacent to the first base.

11. The IC of claim 1, further comprising at least one of an air gap and a dielectric material between the second base and the substrate.

12. The IC of claim 1, further comprising one or more contact layers at least one of above and below the first BJT, the one or more contact layers including dopant concentrations of  
10 at least  $1E18$  per cubic cm.

13. The IC of claim 1, wherein the first base, the second base, the first RTD layer, and the second RTD layer each include dopant concentrations of at least  $1E18$  per cubic cm.

14. The IC of claim 1, wherein the first BJT, second BJT, and RTD are included in one of a pull-up network and a pull-down network for a memory cell.

15 15. A memory latch comprising the IC of any of claims 1-14.

16. A computing system comprising the IC of any of claims 1-14.

17. A memory latch comprising:

a first cell including a first bipolar junction transistor (BJT), a second BJT, and a first resonant-tunneling diode (RTD); and

20 a second cell including a third BJT, a fourth BJT, and a second RTD.

18. The memory latch of claim 17, wherein one of the first and the second cells is used for a pull-up network and the other of the first and second cells is used for a pull-down network.

19. The memory latch of claim 17, wherein the first BJT has a PNP configuration, the  
25 second BJT has an NPN configuration, the third BJT has an NPN configuration, and the fourth BJT has a PNP configuration.

20. The memory latch of claim 17, wherein a base of the first BJT is in physical contact with a collector of the second BJT and wherein a base of the third BJT is in physical contact with a collector of the fourth BJT.

21. The memory latch of claim 17, wherein the first RTD is in physical contact with a base of the second BJT and wherein the second RTD is in physical contact with a base of the fourth BJT.

22. The memory latch of any of claims 17-21, further comprising a substrate common to both the first and second cells.

23. A method of forming an integrated circuit (IC), the method comprising:  
providing a substrate;  
forming a first bipolar junction transistor (BJT) at least one of on and above the substrate, wherein the first BJT includes a first collector, a first base, and a first emitter;  
forming a second BJT at least one of on and above the substrate, wherein the second BJT includes a second collector, a second base, and a second emitter; and  
forming a resonant-tunneling diode (RTD) at least one of on and above the substrate, wherein the RTD includes a first RTD layer doped one of n-type and p-type and a second RTD layer doped the other of n-type and p-type.

24. The method of claim 23, further comprising removing material under the second base to form an air gap.

25. The method of claim 24, further comprising forming dielectric material in the air gap.

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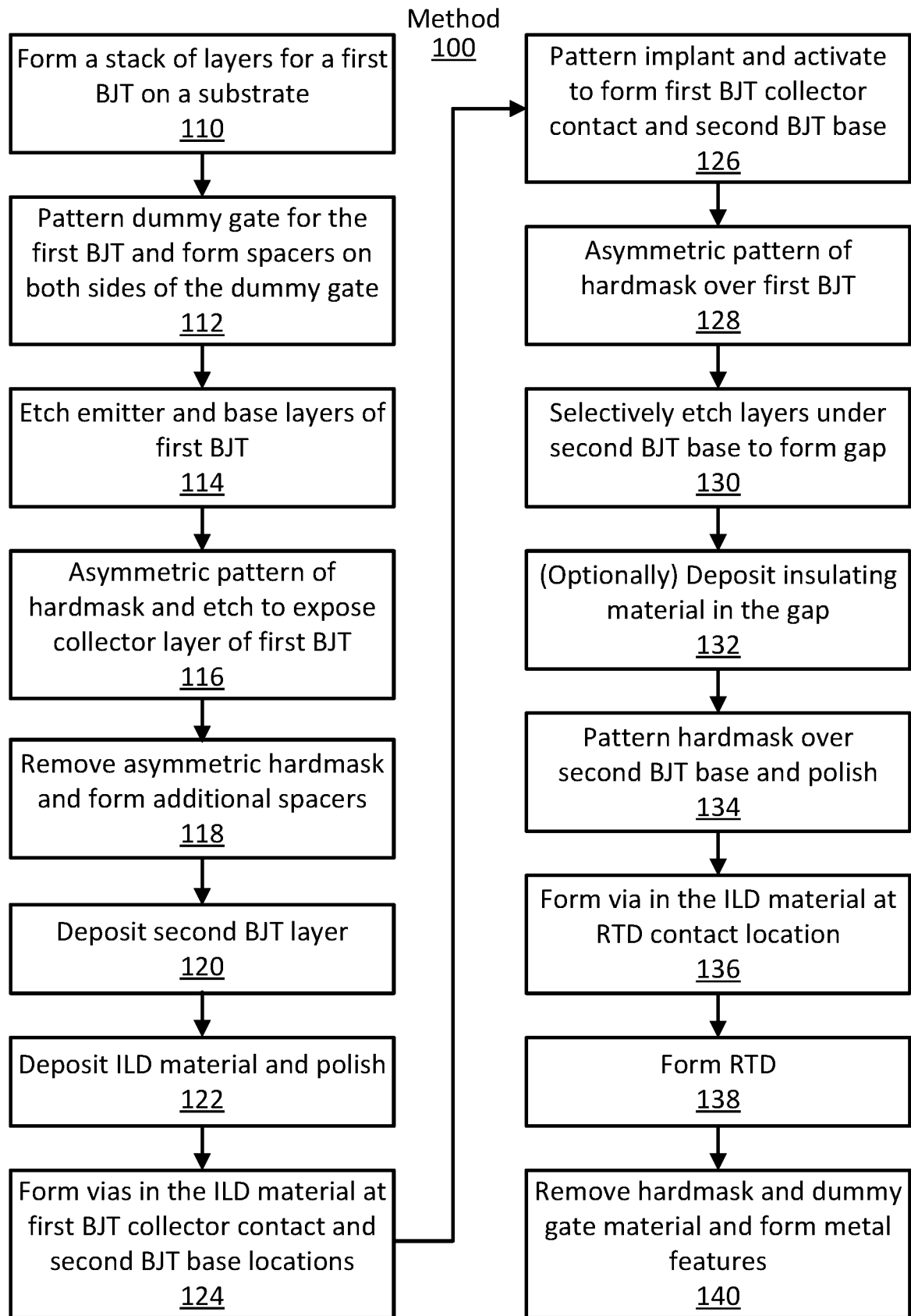


FIG. 1

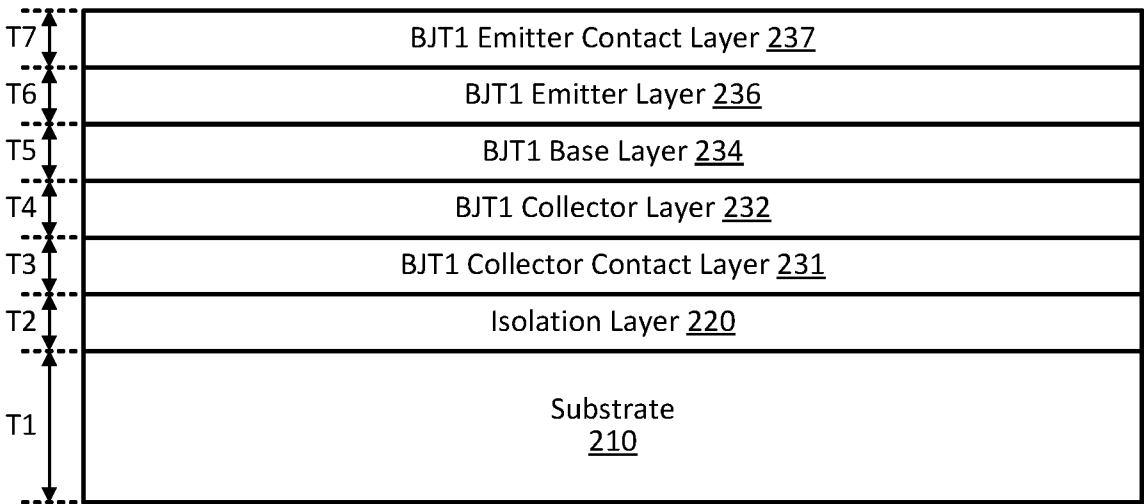


FIG. 2A

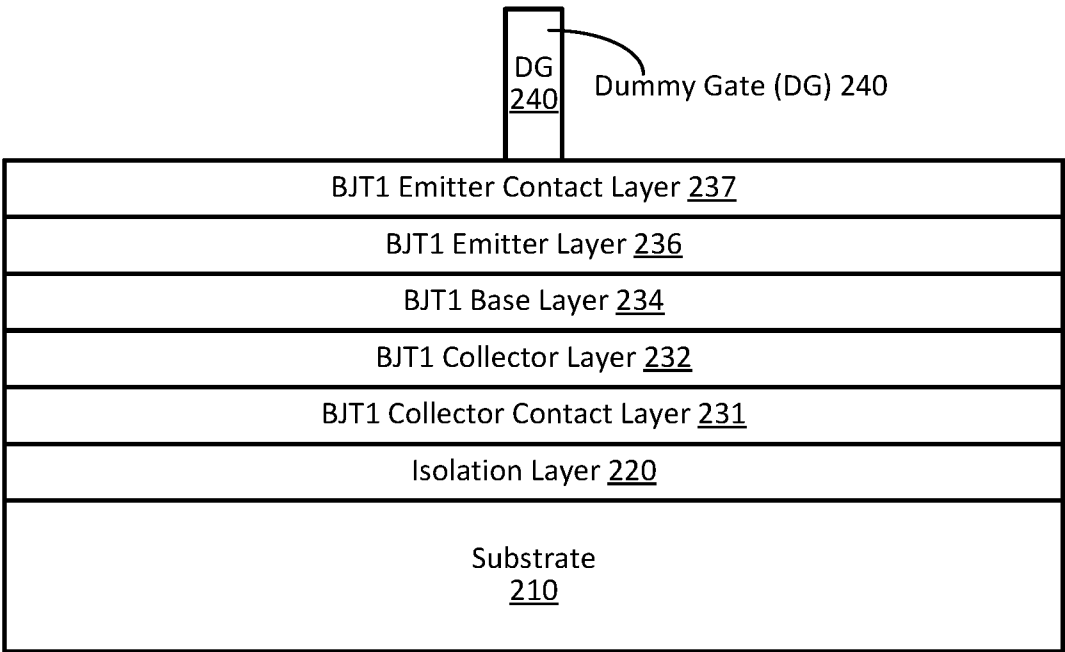
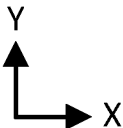


FIG. 2B



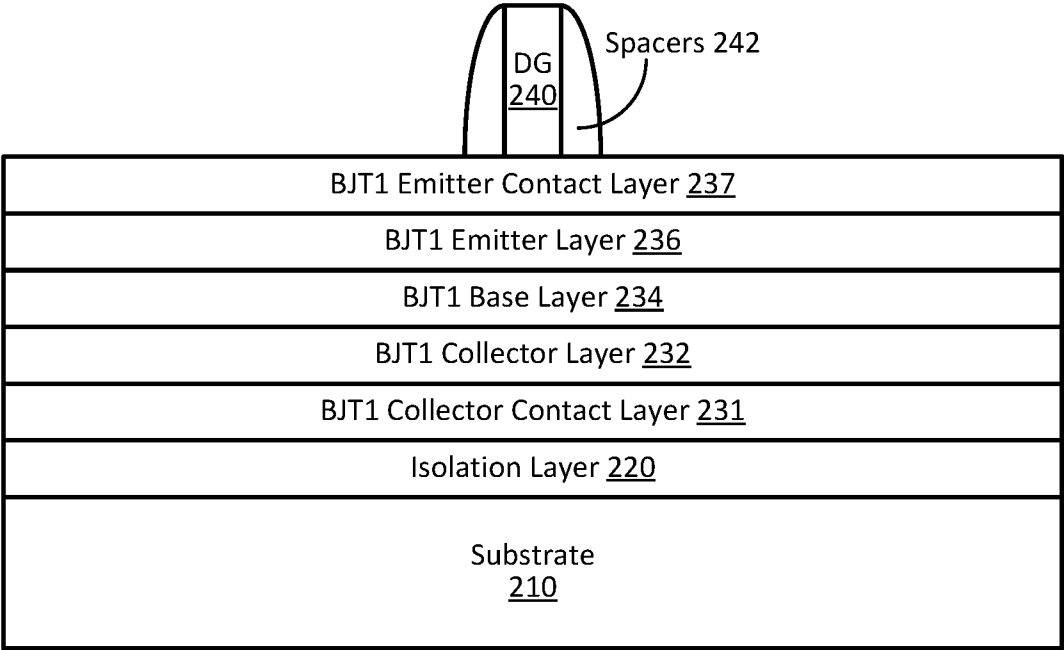


FIG. 2C

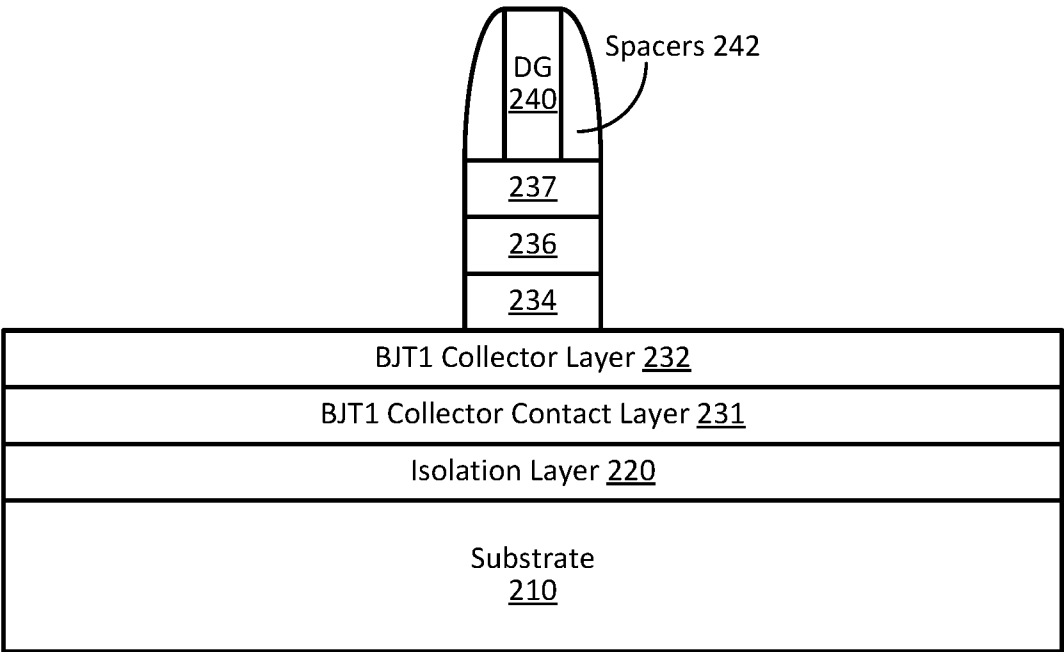
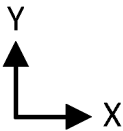


FIG. 2D



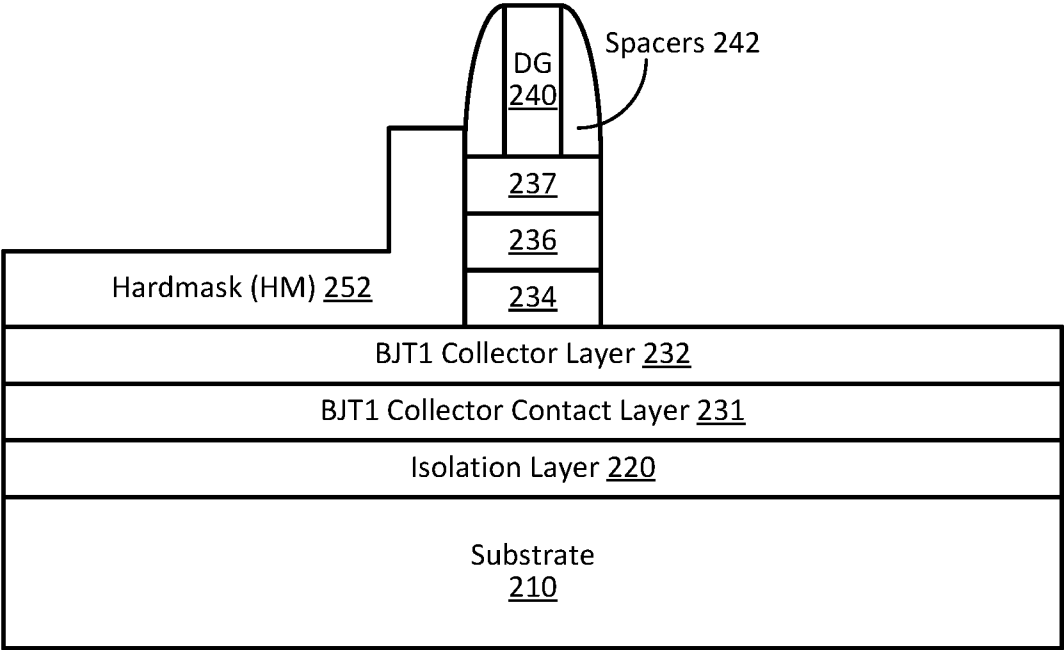


FIG. 2E

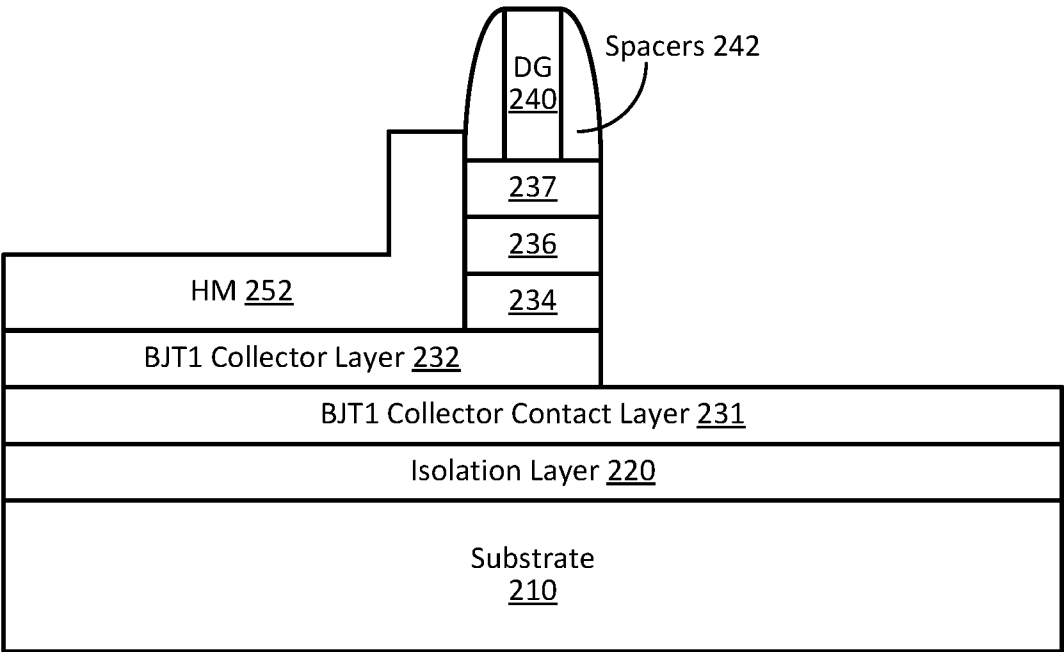
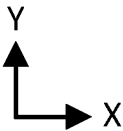


FIG. 2F



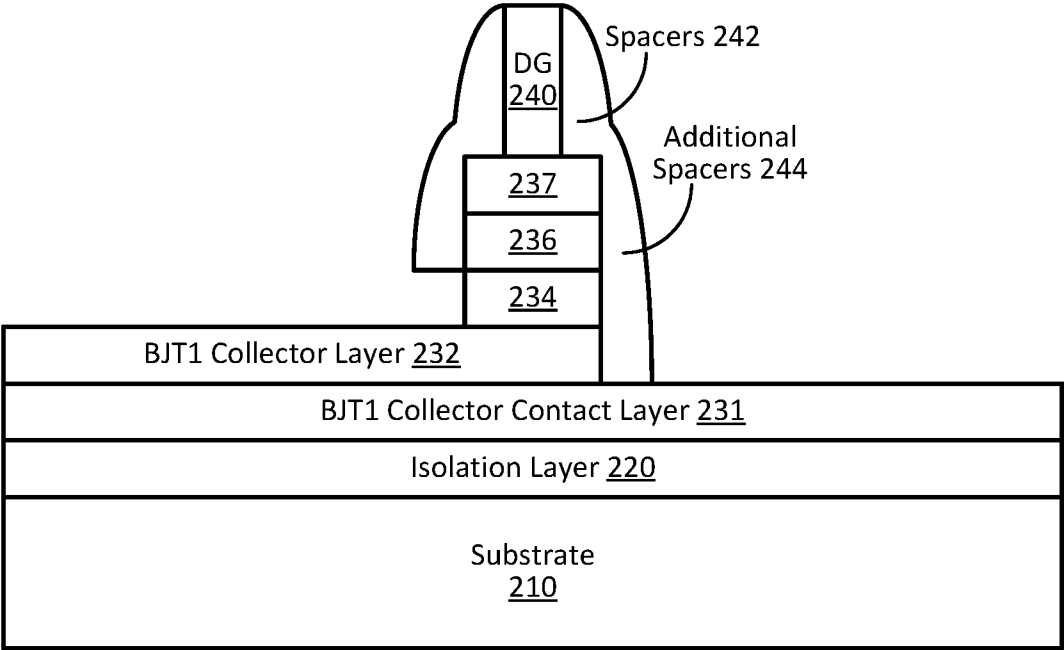


FIG. 2G

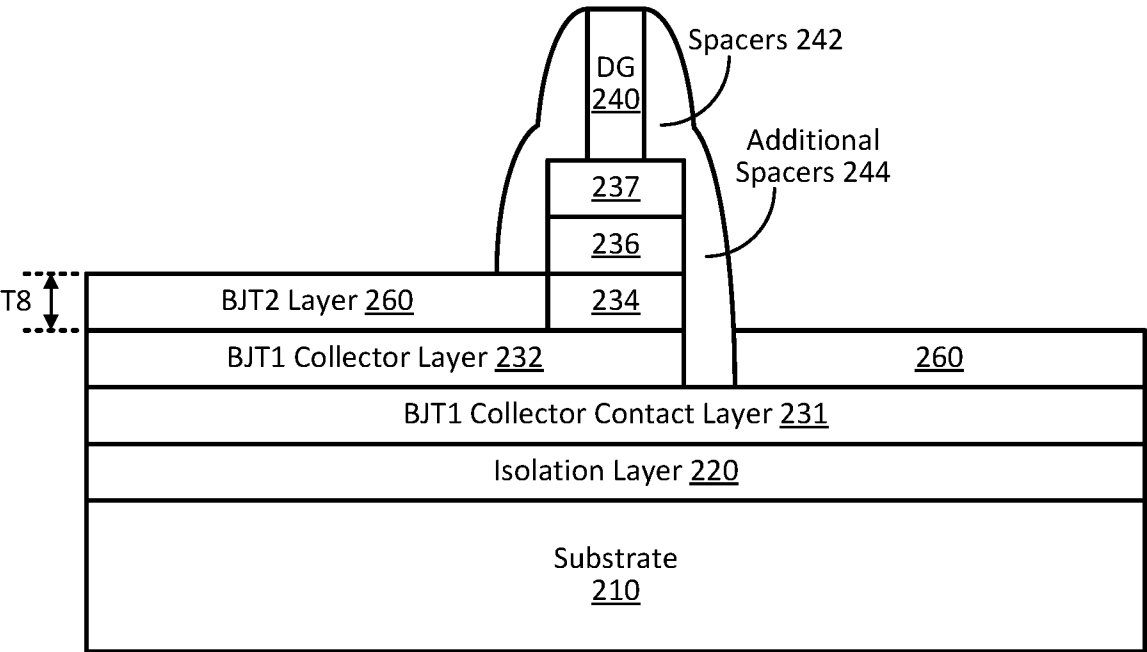
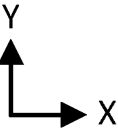


FIG. 2H



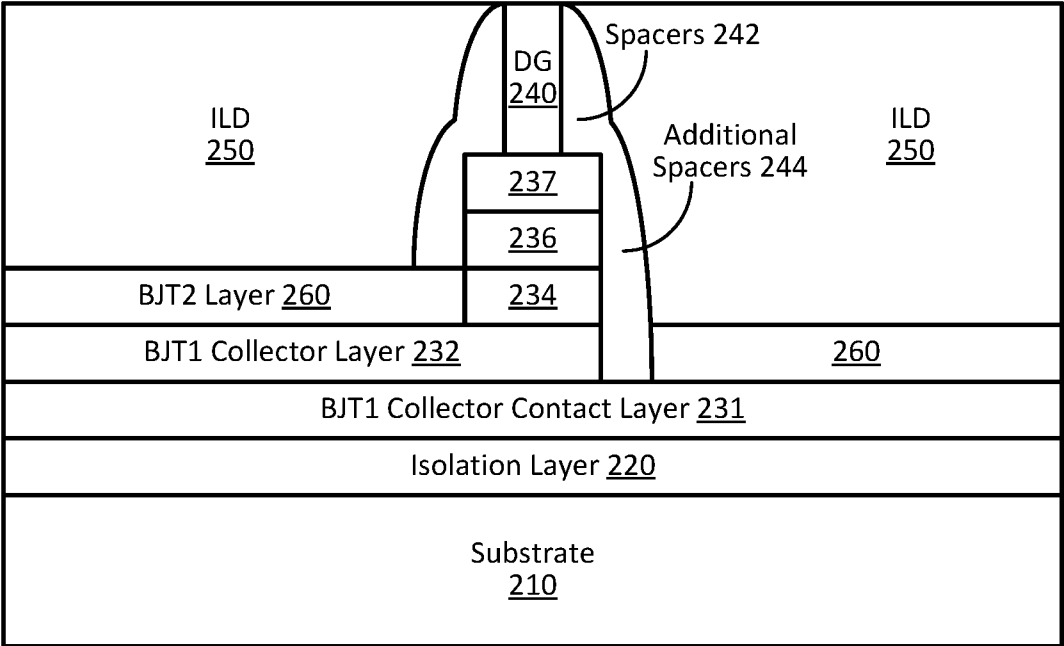


FIG. 2I

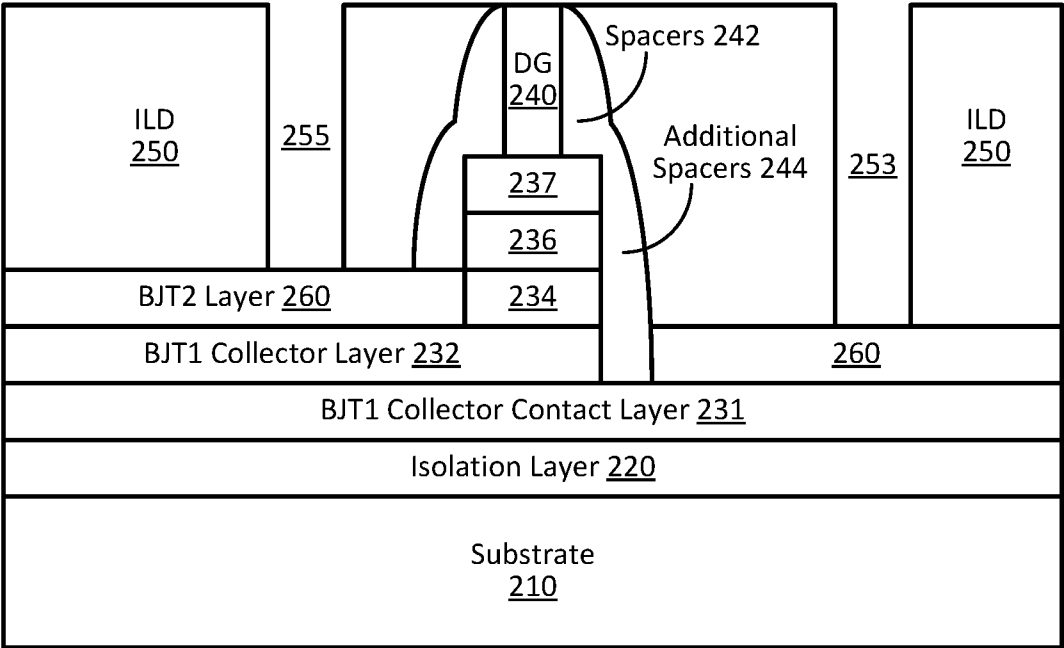
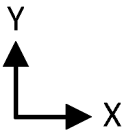


FIG. 2J



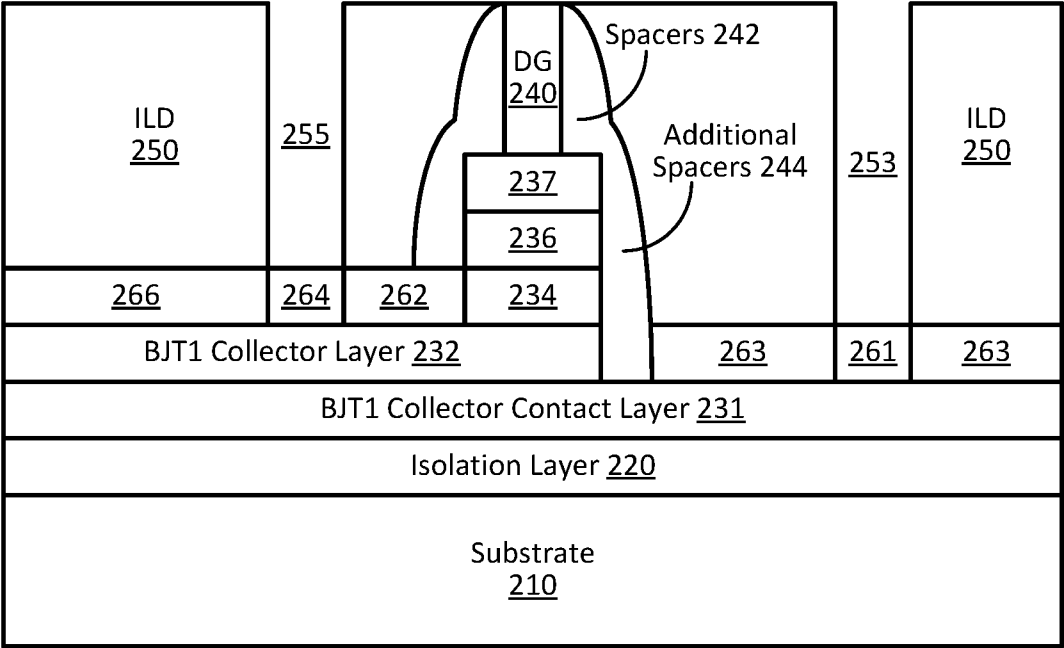


FIG. 2K

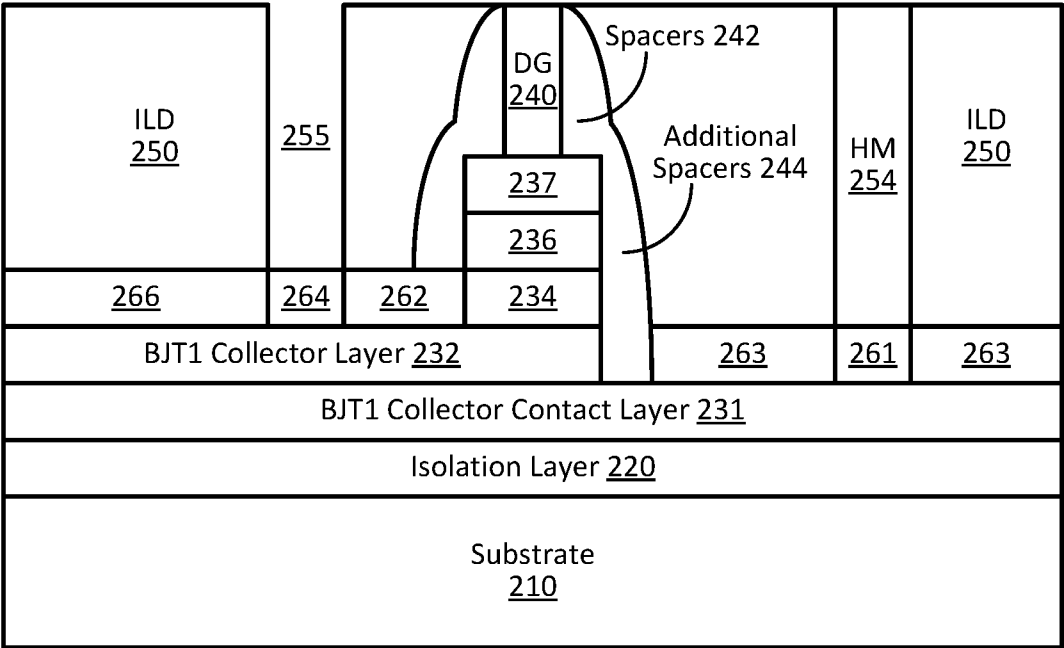
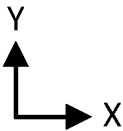


FIG. 2L



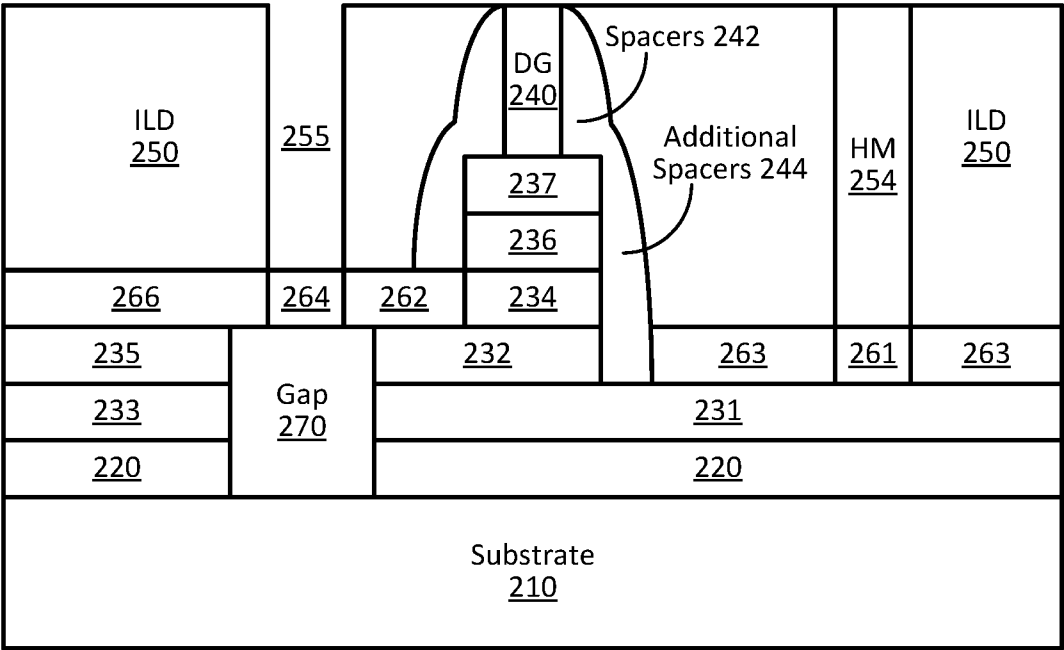


FIG. 2M

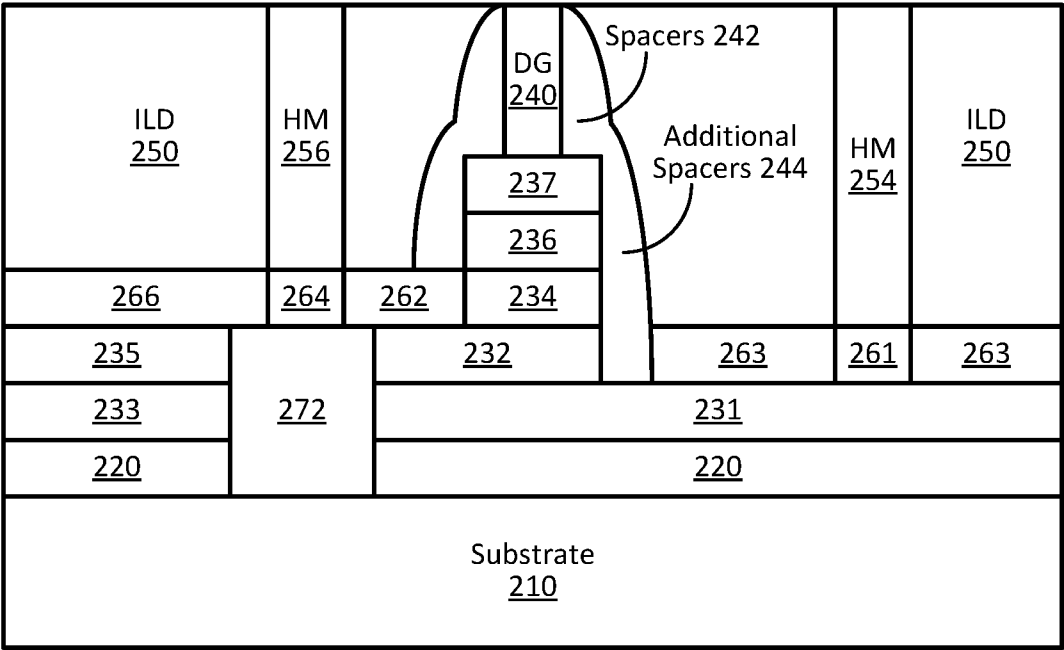
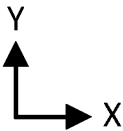


FIG. 2N



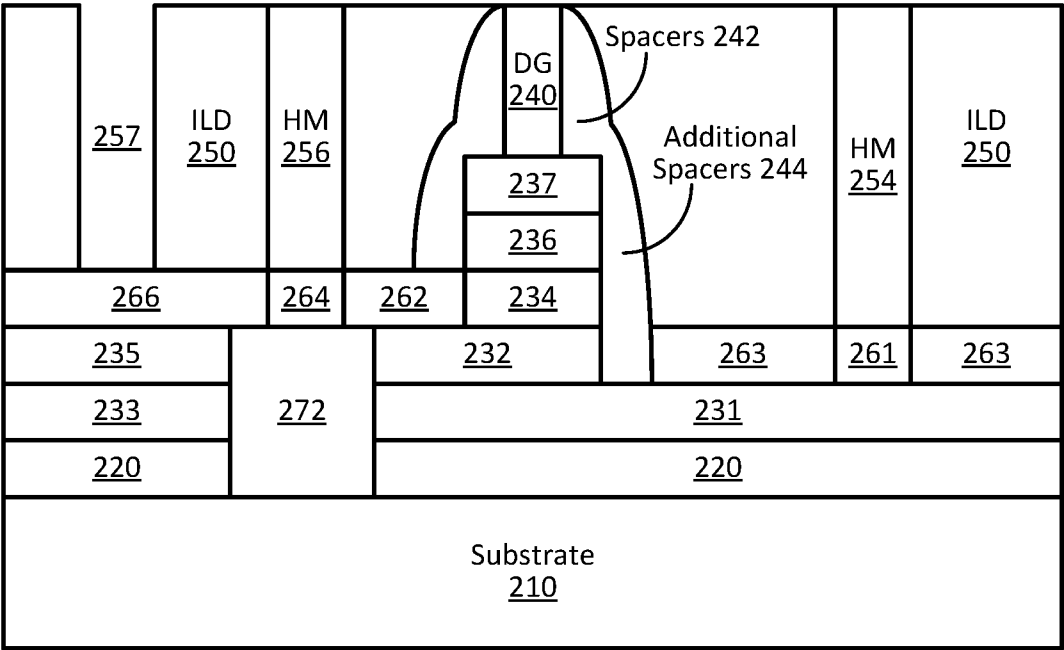


FIG. 20

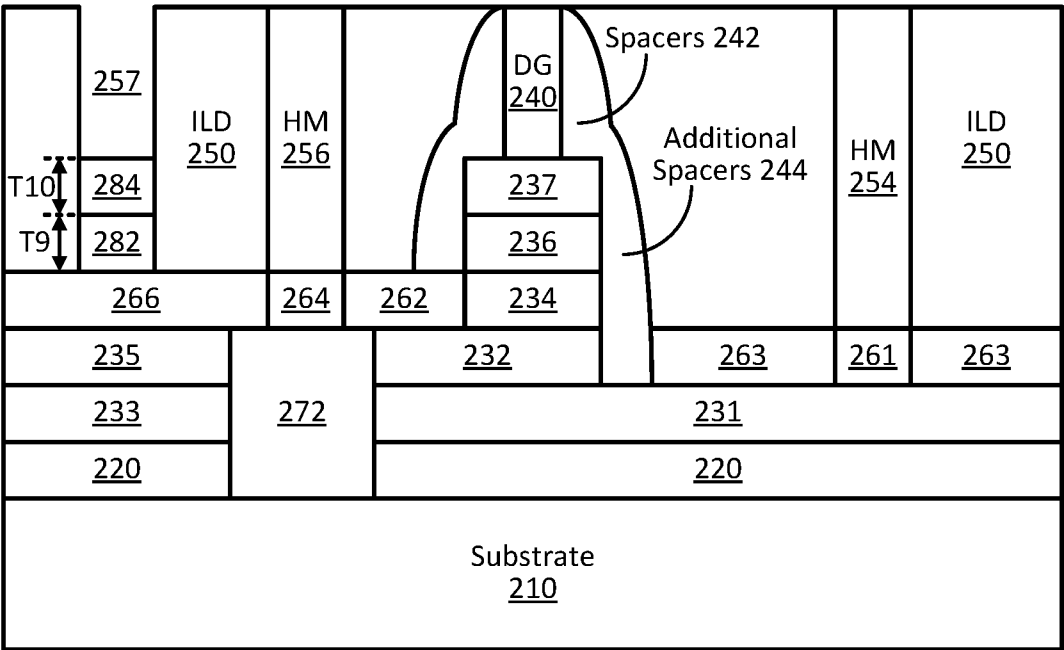
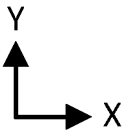


FIG. 2P



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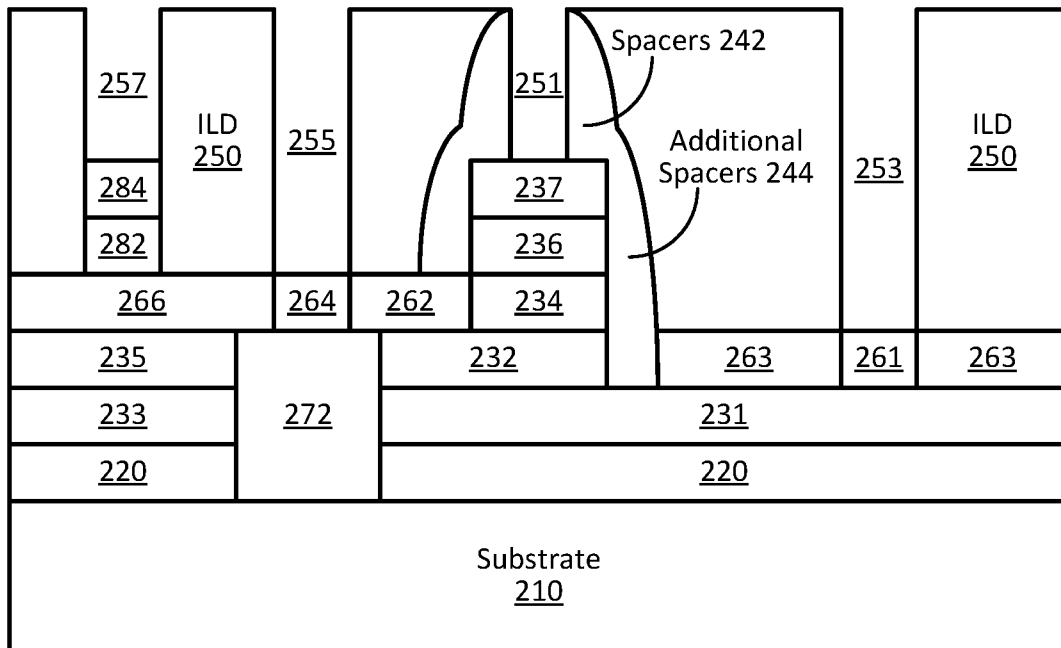


**FIG. 2Q**

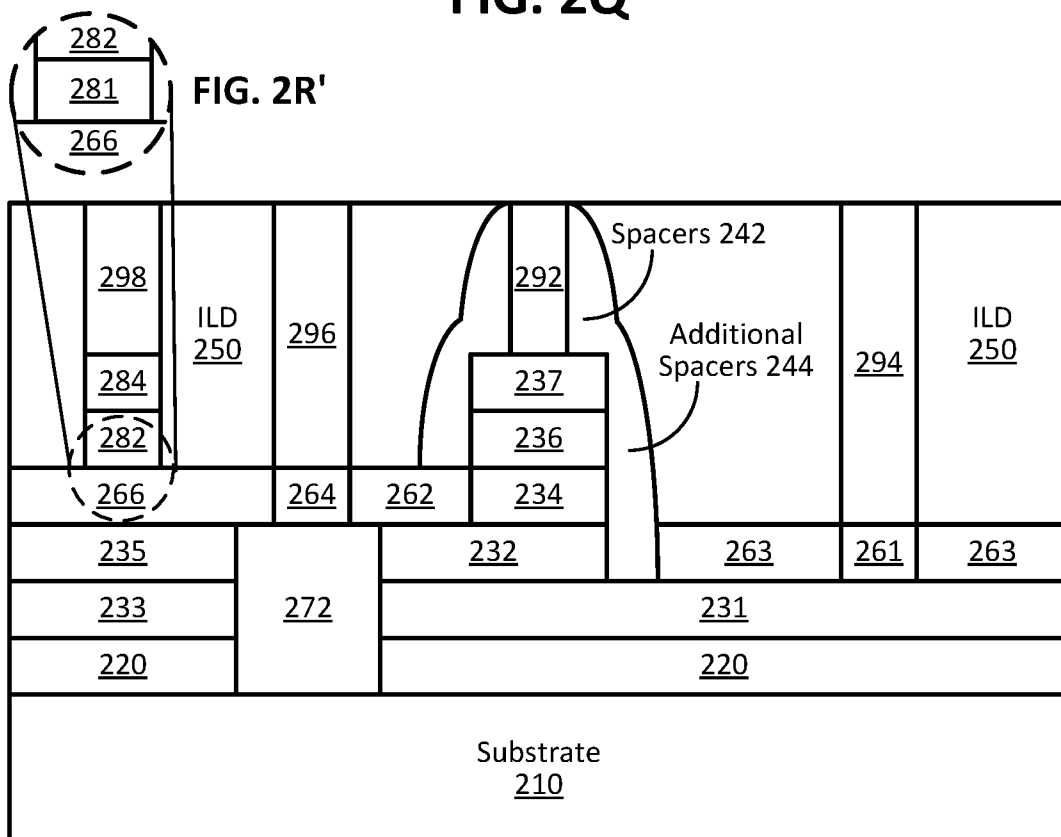
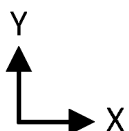


**FIG. 2R**



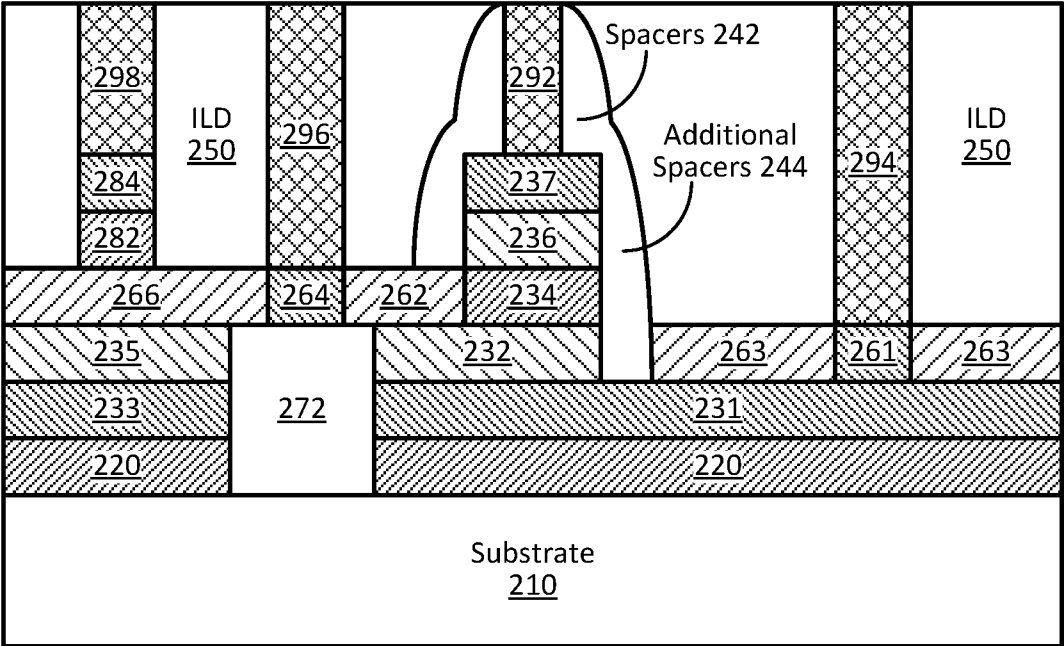


FIG. 3A

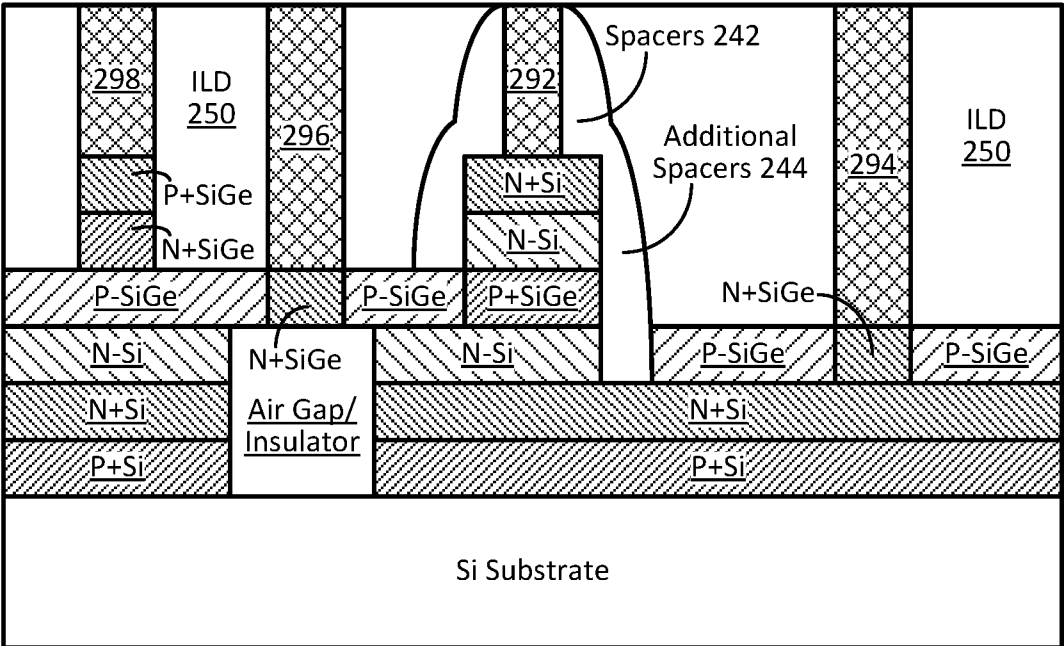
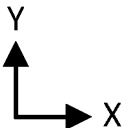


FIG. 3B



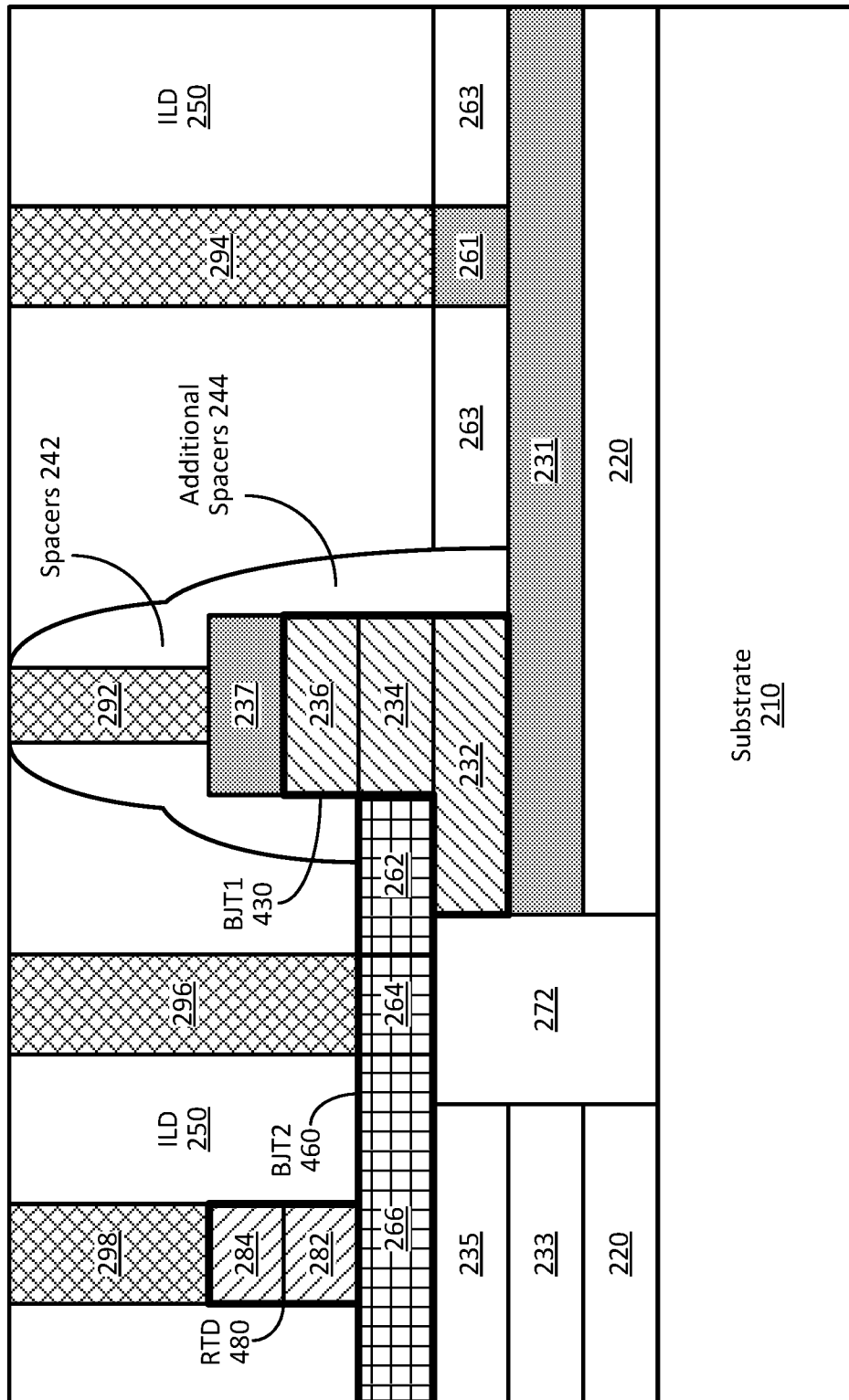
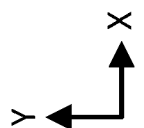


**FIG. 4**



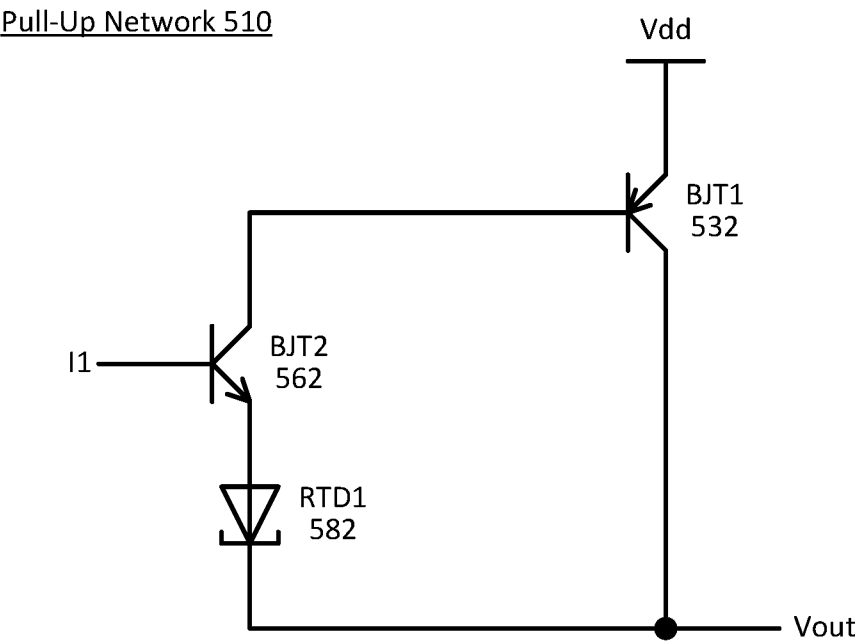


**FIG. 5A**

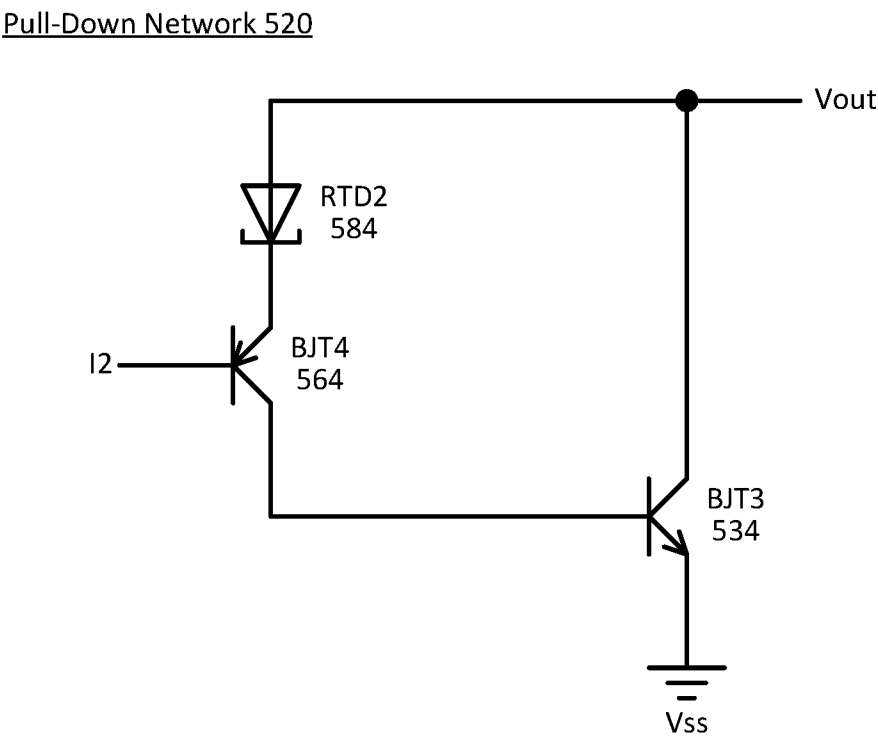


**FIG. 5B**

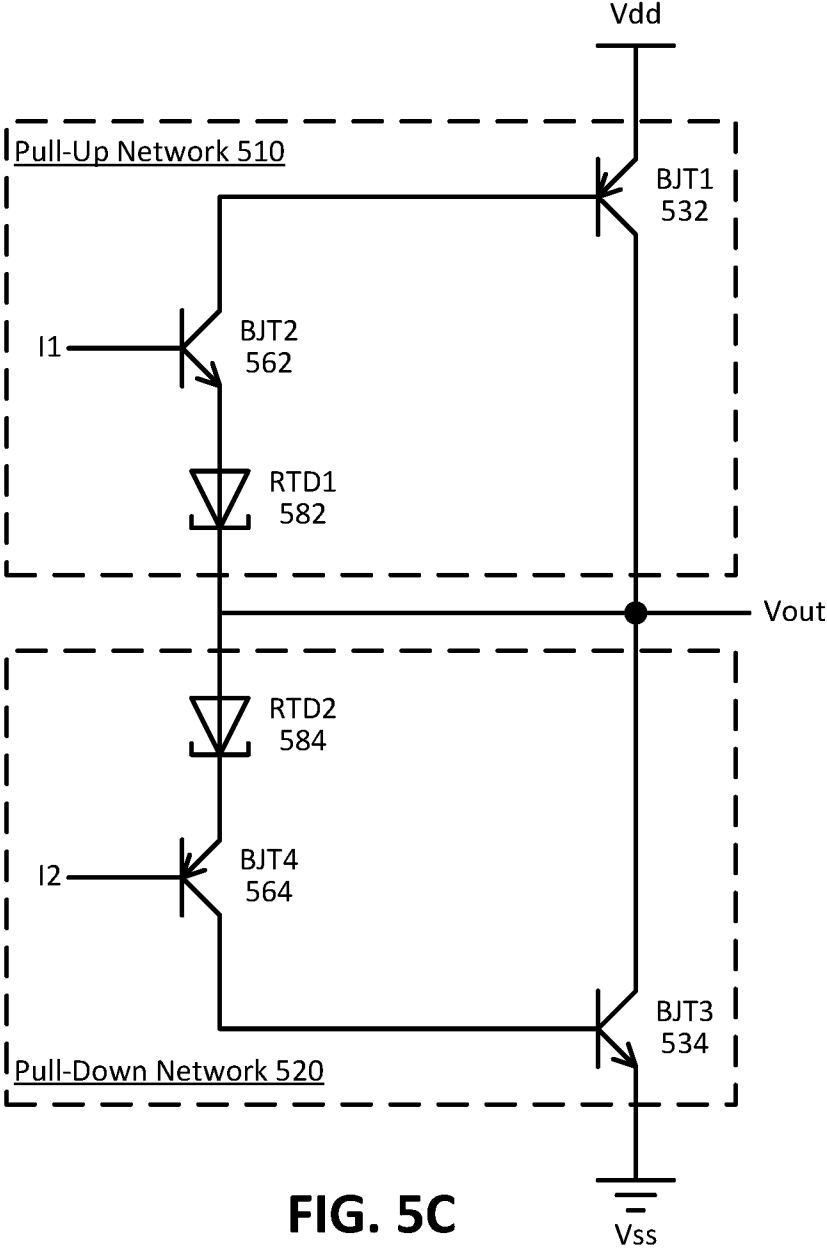


FIG. 5C

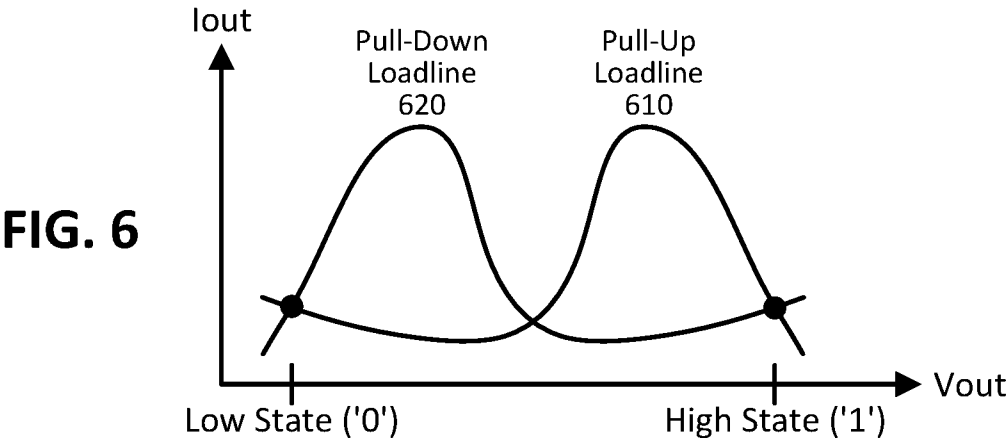


FIG. 6

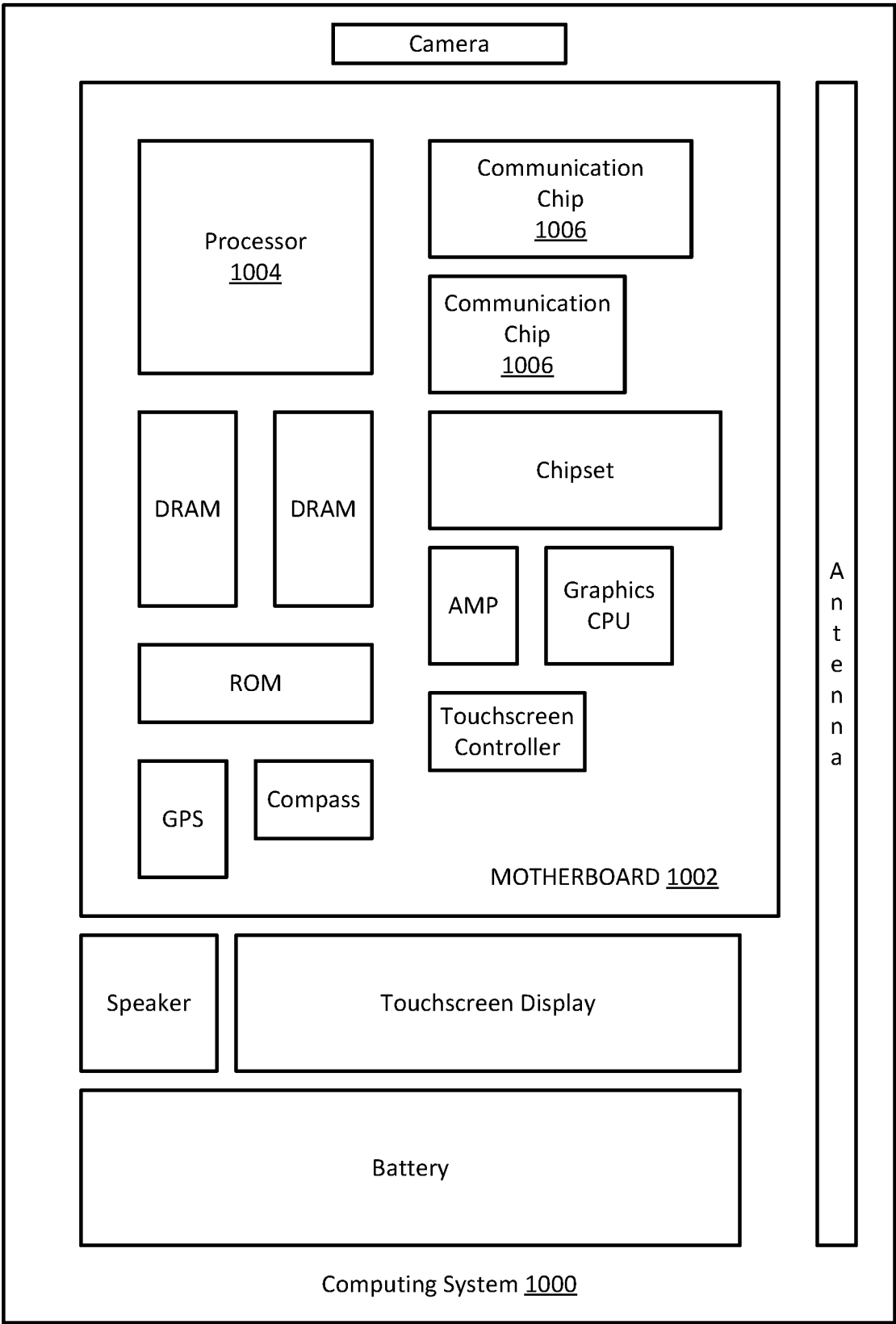


FIG. 7

**A. CLASSIFICATION OF SUBJECT MATTER****H01L 27/26(2006.01)i, H01L 29/88(2006.01)i, H01L 29/66(2006.01)i, H01L 27/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/26; H01L 21/20; H01L 21/28; G11C 11/40; H03B 7/08; H01L 21/338; H01L 29/06; H01L 27/12; H01L 29/88; H01L 29/66; H01L 27/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; keywords: bipolar junction transistor, BJT, resonant tunneling diode, RTD, first, second

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                         | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 4396999 A (SHASHI D. MALAVIYA) 02 August 1983<br>See abstract, column 4, lines 38-41, column 8, line 29 - column 9, line 28, claims 10-12 and figure 6. | 1-16, 23-25           |
| Y         |                                                                                                                                                            | 17-22                 |
| Y         | US 2006-0202720 A1 (LOUIS LUH et al.) 14 September 2006<br>See claims 1-2 and figure 3.                                                                    | 17-22                 |
| A         | US 2008-0042762 A1 (KYOUNG-HOON YANG et al.) 21 February 2008<br>See paragraphs [0007]-[0008] and figure 4.                                                | 1-25                  |
| A         | US 2006-0220127 A1 (SIEGFRIED MANTL) 05 October 2006<br>See paragraph [0145] and figure 9.                                                                 | 1-25                  |
| A         | US 2003-0116782 A1 (HIROSHI MIZUTANI) 26 June 2003<br>See paragraphs [0009]-[0013] and figure 20.                                                          | 1-25                  |



Further documents are listed in the continuation of Box C.



See patent family annex.

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"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

27 March 2017 (27.03.2017)

Date of mailing of the international search report

**27 March 2017 (27.03.2017)**

Name and mailing address of the ISA/KR

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2016/039738**

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s)                                                                                                                                                                                             | Publication<br>date                                                                                                                                                  |
|-------------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| US 4396999 A                              | 02/08/1983          | EP 0068164 A2<br>EP 0068164 A3<br>EP 0068164 B1<br>JP 02041834 B2<br>JP 58-006587 A                                                                                                                                    | 05/01/1983<br>06/11/1985<br>13/09/1989<br>19/09/1990<br>14/01/1983                                                                                                   |
| US 2006-0202720 A1                        | 14/09/2006          | CA 2600411 A1<br>CA 2600411 C<br>EP 1941613 A1<br>EP 1941613 B1<br>JP 04741672 B2<br>JP 2008-537457 A<br>KR 10-2007-0100926 A<br>NO 20075081 A<br>TW 200703907 A<br>TW I318054 B<br>US 7202708 B2<br>WO 2007-030134 A1 | 15/03/2007<br>03/01/2012<br>09/07/2008<br>14/07/2010<br>03/08/2011<br>11/09/2008<br>12/10/2007<br>08/10/2007<br>16/01/2007<br>01/12/2009<br>10/04/2007<br>15/03/2007 |
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| US 2003-0116782 A1                        | 26/06/2003          | EP 1109226 A2<br>EP 1109226 A3<br>JP 2001-177060 A<br>US 2001-0016377 A1<br>US 6525346 B2                                                                                                                              | 20/06/2001<br>14/01/2004<br>29/06/2001<br>23/08/2001<br>25/02/2003                                                                                                   |