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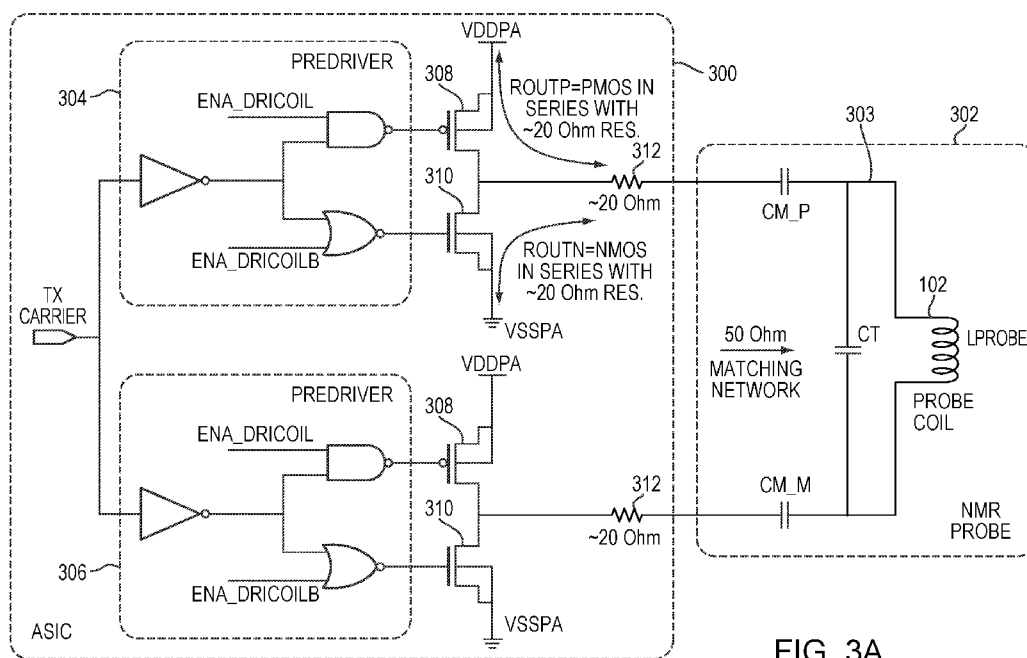


FIG. 3A

(57) Abstract: Systems and methods for reducing variability in the output impedance of an integrated switch-mode power amplifier (PA) split the output impedance between passive resistor, which may be on-chip, and a MOSFET switch of the amplifier. The PA may have a single-ended configuration or a differential configuration having two single-ended structures operating with opposite phases. In one implementation, the size of the MOSFET switch is larger than that of the MOSFET switch implemented in a conventional PA, but the size is still acceptable to operate the PA at a desired frequency. In addition, a calibration approach may be utilized to ensure that the MOSFET switch has a controlled and calibrated ON resistance, thereby providing stable output power levels of the PA and ensuring consistency and repeatability in NMR measurements.



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INTEGRATED SWITCHED-MODE POWER AMPLIFIERS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of, U.S. Provisional Patent Application Nos. 62/477,009 and 62/477,014, both filed on March 27, 2017.

FIELD OF THE INVENTION

[0002] The field of the invention relates, generally, to nuclear magnetic resonance (NMR) equipment, and in particular to managing output impedance and/or power levels in such equipment.

BACKGROUND

[0003] Nuclear magnetic resonance (NMR) is a well-known analytic technique that has been used in a number of fields, such as spectroscopy, bio-sensing and medical imaging. In general, an NMR device includes transceiver circuits to transmit signals to a test sample and receive echo signals therefrom. For example, with reference to FIG. 1, the basic components a conventional NMR system 100 include an NMR coil 102 surrounding a sample 104 being analyzed, a magnet 106 for generating a static magnetic field B_0 across the sample 104 and the coil 102, a duplexer 108 coupled to the NMR coil 102, and a controller 110 for controlling operation of the various components. Typically, the duplexer 108 includes a transmitter (Tx) portion for delivering RF signals to the NMR coil 102 and a receiver (Rx) portion for receiving echo signals from the sample 104 vis the NMR coil 102.

[0004] NMR coil 102 and transceiver 108 are commonly known as an “NMR probe,” which operates with large electromagnets or superconducting permanent magnets in conventional NMR systems. The NMR probe is typically included in an environment having a 50 Ω impedance because of a long interconnection required between the probe and NMR instrument.

[0005] The RF signals delivered by the duplexer 108 originate with an RF frequency source 115 and a pulse sequence generator 117. A modulator circuit 120 modulates the RF signal

from the RF frequency source 115 in accordance with the pulse sequence supplied by the pulse sequence generator 117. The modulated RF signal is amplified by a power amplifier 122.

[0006] During NMR measurements, the modulated RF signal having a Larmor frequency ω_0 is delivered to the coil 102 via the duplexer 108; the coil 102 generates an RF magnetic field B_1 (which is typically orthogonal to the static magnetic field B_0) that resonantly excites nuclei spins within the sample 104. After a time duration, Δt , the RF excitation signal is stopped and the controller 110 causes the duplexer 108 to receive the echo signals from the sample 104. Upon stopping the RF excitation, the nuclear spins within the sample 104 precess around the B_0 -axis at the Larmor frequency ω_0 . The nuclear spins slowly lose phase coherence via spin-spin interactions, which manifest themselves in a macroscopic average as an exponential relaxation or damping signal in the precession of the net magnetic moment. This NMR signal relaxation can be detected by the coil 102. Because the spin-spin interactions are peculiar to the material of the sample 104 being tested, the characteristic time, commonly referred to as T_2 , of the relaxation signal is material specific.

[0007] The duplexer 108 directs the received echo signals, representing the signal output of the NMR probe, to an amplification block including a pre-amplifier (e.g., a low-noise amplifier 125) and a programmable gain amplifier 127. The signal is ultimately converted to digital form by an analog-to-digital converter (ADC) 130 for processing. But the frequency of the “raw” NMR signal received by the pre-amplifier 125 is too high for the ADC 130, and is therefore “down-converted” through comparison with the signal supplied by the RF frequency source 115. A mixer 135 combines the amplified NMR signal, which oscillates at the Larmor frequency, with the reference signal from the RF frequency source to generate a new signal that oscillates at a lower “relative Larmor frequency.” Following filtering by a low-pass filter 137, the signal varies slowly enough to be handled by the ADC 130 but nonetheless retains the essential frequency characteristics of the received echo signals.

[0008] Thus, by measuring the Larmor frequency ω_0 described above (e.g., for spectroscopy) and characteristic time T_2 (e.g., for relaxometry), NMR techniques can be used as an analytic tool in a number of fields, including but not limited to chemical composition analysis, medical imaging, and bio-sensing.

[0009] Significant efforts have been devoted to miniaturizing traditional NMR systems. For example, the entire NMR electronics, including the power amplifier (PA) 122, may be integrated on a single semiconductor device. The numerous advantages of miniaturization include low cost, portability, and the fact that a micro-coil tightly surrounding a small sample

increases the signal quality. In addition, reducing the size of the magnet 106 allows use of a much smaller power to excite (or polarize) the sample 104 than in a conventional system.

[0010] FIG. 2A depicts a traditional class-D PA 200 implemented in a miniaturized NMR system; the input signal V_S to the PA 200 is typically a square-wave signal having low and high amplitudes between the ground (V_{SSPA}) and the PA source voltage (V_{DDPA}). The input signal is used to close and open switches 202, 204 in an alternating fashion for connecting an output load 206 to either V_{DDPA} or V_{SSPA} . The power transferred to the load 206 depends on the output impedance of the amplifier 200, the input signal amplitude V_S , and the load impedance R_L . In a single-ended PA as depicted in FIG. 2, the delivered power can be represented as:

$$P_L = \frac{1}{2} \frac{|V_S|^2 R_L}{(R_{Out} + R_L)^2} \quad Eq. (1).$$

When the duty cycle of the input switching bipolar square-wave signal is not 50%, the total average power at the fundamental frequency supplied by the PA can be computed as:

$$P_{Av} \cong \frac{\left(\frac{4}{\pi} \times V_{DDPA} \times \sin(\pi \times DUTYCYCLE)\right)^2}{2 \times (2R_{OUT} + R_L)} \quad Eq. (2).$$

where DUTYCYCLE is the positive duty cycle of the waveform expressed as a decimal fraction in the range from 0 to 0.5. Thus, the total average power is a direct function of the supply voltage V_{DDPA} , the duty cycle of the input square-wave signals, the output impedance of the PA, and the impedance of the load R_L .

[0011] The traditional class-D PA typically delivers a power ranging from watts to kilowatts. The power may be adjusted by changing the supply voltage V_{DDPA} while maintaining the duty cycle of the switching waveform at 50% (DUTYCYCLE = 0.5) corresponding to the maximum total average power of the fundamental. In addition, the output impedance R_{OUT} and load impedance R_L are generally kept constant so as to ensure impedance matching between the PA and the load resistor 206.

[0012] Recent developments in class-D amplifier technology have been exploited to integrate the PA on a semiconductor device and generate excitation signals suitable for NMR measurements, particularly in low-field time-domain NMR relaxometry. Controlling the available power of the integrated class-D PA via adjustment of the supply voltage, V_{DDPA} ,

however, is not desirable. This is because such adjustment ordinarily requires implementation of an additional power domain and associated pin(s) dedicated exclusively to the PA output drivers; this introduces extra system complexity.

[0013] Alternatively, the total available power may be adjusted via changing the duty cycle of the PA switching waveform as shown in FIG. 2B and Eq. (2). In this case a duty cycle control block is inserted between RF signal source 115 and modulator 120 in FIG. 1

[0014] Efforts have been made to use analog duty-cycle-control circuits to adjust the duty cycle of the input signals to an integrated PA. Conventional approaches, however, tend to suffer from a high degree of variability and poor control of accuracy when environmental conditions, such as a manufacturing process, supply voltage and operating temperature (PVT) vary. Accordingly, there is a need for an approach that reliably and accurately controls the total available power of the PA by adjusting the duty cycle of the switching input signals. The approach should desirably account for effects resulting from various environmental conditions (e.g., PVT), thereby ensuring repeatably stable power levels during NMR measurements.

[0015] In addition, the traditional class-D PA typically has a somewhat limited bandwidth (usually much less than 1 MHz). To make NMR measurements, the PA, however, requires a wide bandwidth (e.g., between 10 MHz and 60 MHz). Further, because the output impedance of the traditional class-D amplifier is fixed, the available power setting is also fixed for the fixed power-supply voltage V_{DDPA} . In other words, the power and output impedance of the amplifier are not separable. Because of this constraint, it is difficult to adjust the power available from the amplifier in order to optimize the excitation parameters (such as magnetization flipping angles and NMR excitation pulse spacing) of an NMR measurement. Another challenge of implementing the traditional class-D amplifier in NMR applications is that it is hard to achieve impedance matching (compared to classic audio or power applications) for optimizing the power delivery (as shown by Eq. (1) above) and maintain PA power levels with accuracy and consistency for repeatable NMR measurements.

[0016] Various strategies to address these difficulties have been proposed, generally involving the use of discrete components for the PA and assuming the ON resistance of the switches 202, 204 to be negligible. This allows the output impedance of the PA to be set by an external precision resistor. When integrating the PA and other NMR electronics on a single semiconductor device — resulting in an integrated “switch-mode” power amplifier — the switch devices 202, 204 are typically implemented using MOSFETs whose gates are

controlled by an input RF signal having a square wave form with an amplitude of $V_{DDPA} - V_{SSPA}$.

[0017] In a typical NMR application, the PA drives a 50Ω load impedance. This means that for the case of a differential class-D PA, each PA driver has an output impedance of 25Ω for an optimal, reflection-free power delivery to the load. The ON resistance of the MOS device, however, varies with manufacturing processes, supply voltage and temperature. In addition, the highly nonlinear behavior for large voltages across the device makes it extremely challenging to implement a basic MOSFET switch having a constant ON resistance of 25Ω .

[0018] Accordingly, there is a need for an approach that reduces the variability of the output impedance of an integrated switch-mode power amplifier in order to maintain consistent power levels repeatably during NMR measurements.

SUMMARY

[0019] Embodiments of the present invention provide an approach for reducing variability in the output impedance of an integrated switch-mode power amplifier by splitting the output impedance between passive resistor, which may be on-chip, and a MOSFET switch of the amplifier. The PA may have a single-ended configuration or a differential configuration having two single-ended structures operating with opposite phases. In one implementation, the size of the MOSFET switch is larger than that of the MOSFET switch implemented in a conventional PA, but the size is still acceptable to operate the PA at a desired frequency. In addition, a calibration approach may be utilized to ensure that the MOSFET switch has a controlled and calibrated ON resistance, thereby providing stable output power levels of the PA and ensuring consistency and repeatability in NMR measurements.

[0020] In various embodiments, a replica circuit of a class-D PA-driver sensor is utilized to monitor the output impedance of the matched replica switch devices; a software (and/or hardware) implemented state-machine algorithm may then be utilized to automatically adjust the output impedance of the PA to achieve a target value set by a pair of externally matched precision resistors. Implementation of the resistor on-chip may advantageously eliminate the need for an external resistor component and, at the same time, reduce voltage swings across the MOSFET switch device, thereby increasing the linearity thereof.

[0021] Another embodiment of the present invention provides an approach for accurately setting a duty cycle of PA switching waveforms using an all-digital PVT sensor circuit. In various embodiments, the all-digital PVT sensor circuit measures a pulse width of a periodic reference signal using digital delay line, and subsequently, implements an off-chip digital calculation to program the digital delay line to delay this periodic reference signal so that, when the delayed periodic reference signal is combined with the original (undelayed) reference via a logical AND operation, the resulting signal conforms to a desired duty cycle. In one implementation, the PA is a class-D PA, which may have a single-ended configuration or a differential configuration having two single-ended structures operating in opposite phases.

[0022] Accordingly, in a first aspect, the invention relates to circuitry for reducing variability of an output impedance of an integrated switch-mode PA. In various embodiments, the circuitry comprises a PA driver; a pre-driver for facilitating activation and deactivation of the PA driver; and a passive resistor coupled to the PA driver so as to split the output impedance between the PA driver and the passive resistor. The PA driver may comprise or consist of a PMOS device and an NMOS device. Typically, the on-chip passive resistor has an impedance that substantially does not depend on temperature or voltage.

[0023] In various embodiments, the circuitry further comprises a calibration circuit for calibrating an ON resistance of the PA driver so as to provide stable output power levels. The calibration circuit may comprise a replica circuit of the PA driver and a load resistor, and may further comprise an on-chip voltage divider for generating a reference voltage. In some embodiments, the calibration circuit further comprises a comparator for comparing the reference voltage with an output voltage of the replica circuit and the load resistor. The passive resistor may be on-chip or off-chip.

[0024] In another aspect, the invention pertains to an NMR apparatus comprising an NMR coil configured to enclose a sample, an integrated switch-mode PA coupled to the NMR coil, and circuitry for reducing variability of an output impedance of the PA. In various embodiments, the circuitry includes (i) a PA driver, (ii) a pre-driver for facilitating activation and deactivation of the PA driver; and (iii) an on-chip passive resistor coupled to the PA driver for splitting the output impedance between the PA driver and the passive resistor. The circuitry may include one or more of the features described above.

[0025] Another aspect of the invention relates to a method of reducing variability of an output impedance of an integrated switch-mode PA. In various embodiments, the method comprises providing a PA driver having at least one MOS device; providing a pre-driver for

facilitating activation and deactivation of the PA driver; and adjusting the number of stripes of the MOS device(s) so to provide a desired impedance.

[0026] In yet another aspect, the invention pertains to circuitry for adjusting a duty cycle of an RF carrier input signal to a PA. In various embodiments, the circuitry comprises a digital delay line, comprising a plurality of digital delay elements, for receiving the input signal; a time-to-digital converter for measuring a number of the digital delay elements required for generating a desired duty cycle; and circuitry for selecting the number of delay elements of the digital delay line required to generate a desired duty cycle and receiving an output signal therefrom, the output signal having the adjusted duty cycle. In some embodiments, the circuit further comprises a processor having a control register for enabling a HIGH-power mode or a LOW-power mode of the circuitry. For example, the control register may have a value of 1 for enabling the LOW-power mode and a value of 0 for enabling the HIGH-power mode. The control register may select the HIGH-power mode when the desired duty cycle has a value between 25% and 50% and the LOW-power mode when the desired duty cycle has a value between 5% and 25%.

[0027] In various embodiments, the circuitry further comprises a processor having a register for bypassing the digital delay line. The digital delay line may comprise a plurality of delay elements. Each one of the delay elements may comprise one input and three outputs. For example, a first one of the outputs may be coupled to an input of a successive delay element; a second one of the outputs to an input of a multiplexer; and a third one of the outputs to an input of the time-to-digital converter.

[0028] In some embodiments, the circuitry further comprises a processor configured to determine the number of the delay elements required for generating the desired duty cycle based on a measurement of the time-to-digital converter. The processor may be implemented on a chip integrating the digital delay line and time-to-digital converter, or off a chip integrating the digital delay line and time-to-digital converter; in the latter case, the circuitry may further comprise a communication module for allowing signal communication between the processor and the chip.

[0029] Still another aspect of the invention relates to an NMR apparatus comprising an NMR coil configured to enclose a sample; an integrated switch-mode PA coupled to the NMR coil; and circuitry for adjusting a duty cycle of an input signal to a power amplifier (PA). In various embodiments, the circuitry includes (i) a digital delay line having a plurality of delay elements, and (ii) a time-to-digital converter for measuring a number of the delay

elements required for generating a desired duty cycle. The circuitry may include one or more of the features described above.

[0030] In general, as used herein, the term “substantially” means $\pm 10\%$, and in some embodiments, $\pm 5\%$. In addition, reference throughout this specification to “one example,” “an example,” “one embodiment,” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the example is included in at least one example of the present technology. Thus, the occurrences of the phrases “in one example,” “in an example,” “one embodiment,” or “an embodiment” in various places throughout this specification are not necessarily all referring to the same example.

Furthermore, the particular features, structures, routines, steps, or characteristics may be combined in any suitable manner in one or more examples of the technology. The headings provided herein are for convenience only and are not intended to limit or interpret the scope or meaning of the claimed technology.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, with an emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[0032] FIG. 1 schematically illustrates a conventional NMR device.

[0033] FIG. 2A schematically illustrates a conventional class-D power amplifier.

[0034] FIG. 2B is a timing diagram illustrating the definition of duty cycle.

[0035] FIG. 3A schematically illustrates a circuit comprising an exemplary class-D PA interface coupled to an NMR probe in accordance with various embodiments of the present invention.

[0036] FIG. 3B schematically illustrates an exemplary circuit for adjusting ON resistance.

[0037] FIG. 4 schematically illustrates a calibration circuit in accordance with various embodiments of the present invention.

[0038] FIG. 5 is a flow chart illustrating a representative approach for calibrating PA output impedance.

[0039] FIG. 6A schematically illustrates the relationship between the duty-cycle controller shown in FIG. 6B and other components of an NMR system.

[0040] FIG. 6B schematically illustrates an exemplary circuit for duty-cycle control.

[0041] FIG. 6C schematically illustrates generation of quadrature phase inputs to the duty-cycle controller shown in FIG. 6B.

[0042] FIG. 7 schematically illustrates, in greater detail, a time-to-digital converter in accordance with embodiments of the invention.

[0043] FIG. 8 is a timing diagram.

DETAILED DESCRIPTION

[0044] Refer first to FIG. 3A, which depicts an exemplary differential class-D PA interface 300 coupled to an NMR probe 302 in accordance with various embodiments of the present invention. The PA is implemented as a part of a CMOS (Complementary Metal Oxide Semiconductor) application-specific integrated circuit (ASIC) chip. The NMR probe 302 includes a coil 102 and capacitors CM_P, CM_M, CT. Capacitor CT in combination with inductance of coil 102 creates a parallel resonant circuit 303. Capacitor CM_P and CM_M provide a matching network that transforms the impedance of parallel resonant circuit 303 to the passive differential impedance R_T at the excitation frequency at the output of the PA. The PA 300 is implemented as a discrete chip or a part of a larger application specific integrated circuit (ASIC) including a pair of pre-drivers 304, 306, each coupled to output driver P-type and N-type MOSFET devices 308, 310, which are connected in series with an on-chip resistor 312 having a resistance R_D and function as the PA circuit. The pre-drivers 304, 306 receive, respectively, the pulse sequence, its inverse and the carrier signal, and include logical NAND and NOR gates. In a typical switched-mode power amplifier, the sizes of the PMOS device 308 and NMOS device 310 are chosen to produce a desired PA output power for operation at a target frequency. A fundamental tradeoff exists between the amount of power provided by such PA and its bandwidth due to the parasitic capacitances of devices 308, 310, which reduce the PA bandwidth as their sizes are increased to boost output PA power and vice versa.

[0045] In CMOS manufacturing process, ON resistances (R_{ON}) – i.e., the resistance across the drain/source path of the MOSFET with the gate terminal configured to operate the MOSFET in a strong inversion linear regime – is a function of many parameters, such as

supply voltage, operating temperature, variations in manufacturing parameters including lithography, chemical etching, and electron mobility (among others). As a result, a switching-mode power amplifier using MOSFET devices 308, 310 as switches in the in configuration shown in FIG. 3A will exhibit a large variation of up to 30% in both output power and bandwidth due to variation in the MOSFET ON resistance from one instance of circuit 300 to another and over the full range of environmental conditions. To minimize this variation a calibration approach, as further described below, is utilized to adjust the ON resistance of the PMOS device 308 and NMOS device 310 and keep it at a constant value suited to the particular application.

[0046] Because the devices 308, 310 are each connected in series with the resistor 312, the target ON resistance of devices 308, 310 is $R_{ON} \Omega$ so as to provide a combined differential PA output impedance of $R_T = 2 \times (R_{ON} + R_D)$. In a typical NMR instrument, NMR probe 302 presents a passive 50Ω load to the PA that is expected to have an output impedance of the same value. This promotes optimal power delivery from the PA to probe 302 and avoids electrical reflections that can damage the PA. Without loss of generality, other interface impedance values can be chosen; for example, smaller interface impedance values will result in larger power delivery by the PA. In this case, the value of resistor 312 is reduced and the values of matching capacitors CM_P, CM_M are adjusted appropriately to satisfy the power-matching condition and the lower interface impedance.

[0047] FIG. 3B illustrates a circuit for adjusting the ON resistance by changing the total width of the output MOSFET devices 308, 310 driving the output of the PA. In one embodiment, PA output devices are configured as a parallel connection of plurality of MOSFET devices ("stripes") each having a width equal to the total desired width of the MOSFET device divided by the chosen number of parallel devices. Without loss of generality, in the embodiment shown in FIG. 3B, the number of parallel MOSFET devices is indicated as NSTRIPES. In some embodiments, the number of stripes in PMOSFET devices can differ from the number of stripes in NMOSFET devices to accommodate different variabilities of P-type and N-type MOSFETs. Unlike the conventional class-D PA illustrated in FIG. 3A, the gate terminals of the output MOSFETS shown in FIG. 3B can be individually controlled using the illustrated stripe-selection logic circuits 320, 322. In particular, the desired number of stripes is selected by driving HI the appropriate number of bits in the digital control signals SELECT_P_STRIPES and SELECT_N_STRIPES, which are digital signals of width NSTRIPES bits. The value of NSTRIPES is chosen in such that when all

stripes of the output MOSFET device are selected, the ON resistance of the MOSFET device is less than the target R_{ON} value for the worst-case manufacturing variation, resulting in lowest ON resistance of the typical MOSFET in the chosen manufacturing process, lowest desired operating temperature and highest operating power supply voltage.

[0048] The resistance R_D of the on-chip resistors 312 typically does not depend significantly on temperature and voltage, but may vary in a range of $\pm 15\%$ as a result of the manufacturing process variations. Thus, total single-ended output impedance of the PA, $R_{ON} + R_D$, may vary in the range of $\pm 30\%$; this necessitates a calibration approach to provide stable PA output power levels to ensure consistency and repeatability during NMR measurements.

[0049] FIG. 4 illustrates a calibration circuit 400 in accordance with various embodiments of the present invention. The calibration circuit 400 utilizes sensors integrated on the same chip as the PA circuit 300 to accurately measure a DC ON resistance of the switch MOSFET devices of the PA. In various embodiments, the ON resistance is measured using a PA driver replica circuit 402 having PMOSFET and NMOSFET switches 404, 406 with on-chip resistors R_D and loaded with external resistors 408, 410, respectively; each of the resistors 408, 410 has an impedance of R_{CAL} precisely. Devices 404, 406 have identical total width and length and have the same number of stripes (NSTRIPES) as devices 308, 310 shown in FIG. 3A. In various embodiments, the calibration approach implements an on-chip voltage reference 412 for generating a reference voltage and a comparator 414 for comparing the reference voltage with the output voltage of the sense PMOSFET or NMOSFET 404, 406 generated by a resistive divider from V_{DDPA} to V_{SSPA} . The resistive dividers may be formed by the resistors 408, 410, which have a precise impedance of R_{CAL} , resistors R_D connected in series with the drain terminal of the PMOSFET and NMOSFET sensors of the calibration circuit, and the ON resistance of the MOSFET devices 404, 406.

[0050] In various embodiments, a decision value of the comparator 414 is stored in one of a bank of control registers 416, which are accessible to a digital interface 418. (All of these components may reside on the ASIC 300 shown in FIG. 3A.) In addition, a finite state machine may be utilized to adjust the corresponding ON resistance of the replica half driver 402 until the output voltage of the sense PMOSFET or NMOSFET crosses a threshold voltage corresponding to a target value of the ON resistance. For the PMOSFET sensor circuit, the comparator threshold voltage is chosen to be $(2/3) \times V_{DDPA}$ where V_{DDPA} is the PA supply voltage. For the NMOSFET sensor circuit, comparator threshold voltage is chosen to be $(1/3) \times V_{DDPA}$. The finite state machine may be implemented on or outside the chip 300

in hardware and/or software. In some embodiments, the threshold voltages can be generated internally on the chip using the resistive divider string formed by three identical resistors connected in series from V_{DDPA} to V_{SSPA} . Given the generated threshold voltages, the comparator output will change when the following condition is met for either one of the MOSFET sensors: $R_{ON} + R_D = (R_{CAL}/2)$.

[0051] In various embodiments, the PA half-replica impedance sensor 402 is controlled by two control registers (e.g., CENSN and CENSP in a Model WG1000 provided by WaveGuide Corporation). Writing logic 1 to either one of these registers may enable one or both sense devices 404, 406. In addition, two registers (e.g., CDSN and CDSP) may be used to drive the gates of the MOS sensor devices 404, 406 to an appropriate value required for the calibration approach. In some embodiments, a register (e.g., SELCALREF) is used to select which one of the sense PMOSFET and NMOSFET devices and which reference voltages are connected to the inputs of the decision comparator 414. For example, writing logic 0 may select the output from the sense PMOS 404 and $(2/3) \times V_{DDPA}$ reference voltage, whereas writing logic 1 may select the output from the sense NMOS 406 and $(1/3) \times V_{DDPA}$ reference voltage.

[0052] FIG. 5 illustrates a representative flow chart 500 illustrating operation of the calibration circuit 400 for calibrating a PA output impedance. In a preferred embodiment, the output impedance of the PA is calibrated, before each NMR experiment, during the so called “recycle delay” or after the chip is powered up. While no specific algorithm update rate is specified for the steps of the flow chart 500, it is expected that a minimal progression time interval in the finite state machine is determined based on the settling time constants of capacitors in a low-pass filter that are used to remove high-frequency noise at the inputs of the decision comparator 414 arising during switching between different comparison thresholds.

[0053] With reference to FIGS. 3B, 4 and 5, in a first step 502, the circuit 400 is enabled. The NMOSFET leg 406 of the circuit 400 is disabled and the comparator reference 412 is set to $(2/3) \times V_{DDPA}$ reference voltage (step 504). At this point, no stripes of the PMOSFET sense circuit 404 are selected (step 506). If the output of the comparator 414 is low, additional stripe is enabled in the PMOSFET sense circuit 404 (step 508). If the output of the comparator 414 is high and the procedure 500 has just been entered, an error condition exists where either target R_{ON} value of the PMOSFET device is too large and cannot be achieved by selecting even single stripe of the calibration sensor PMOSFET 404 or comparator threshold value was chosen incorrectly for the target R_{ON} value; otherwise, the current number of

stripes is written the register bank 416 (step 510). At this point the PMOSFET leg 404 of the circuit 400 is disabled and the NMOSFET leg 406 is enabled, and the comparator reference 412 is set to $(1/3) \times V_{DDPA}$ reference voltage (step 512). All 15 stripes of the NMOS sense circuit are selected (step 514). If the output of the comparator 414 is now low, the number of stripes selected for the NMOS sense circuit is progressively decremented until the comparator output is high (step 516). Once again, if the comparator output is high and the procedure 500 has just been entered, an error condition exists where either target R_{ON} value of the NMOSFET device is too small (i.e., cannot be achieved by selecting all stripes of the calibration sense NMOSFET 406) or the comparator threshold value was chosen incorrectly for the target R_{ON} value; otherwise, the current number of stripes is written the register bank 416 (step 518) and the procedure ends. The target value of the ON resistances having thus been established and set, the NMR circuit is ready for operation.

[0054] The calibration method 500 may be implemented in the controller 110. Controller 110 may be implemented in hardware, software or a combination of the two. For embodiments in which the functions of the controller are provided as one or more software programs, the programs may be written in any of a number of high level languages such as PYTHON, PASCAL, JAVA, C, C++, C#, BASIC, various scripting languages, and/or HTML. Additionally, the software can be implemented in an assembly language directed to the microprocessor resident on a target computer; for example, the software may be implemented in Intel 80x86 assembly language if it is configured to run on an IBM PC or PC clone. The software may be embodied on an article of manufacture including, but not limited to, a floppy disk, a jump drive, a hard disk, an optical disk, a magnetic tape, a PROM, an EPROM, EEPROM, field-programmable gate array, or CD-ROM. Embodiments using hardware circuitry may be implemented using, for example, one or more FPGA, CPLD or ASIC processors. Controller 110 may be implemented in hardware, software or a combination of the two. For embodiments in which the functions are provided as one or more software programs, the programs may be written in any of a number of high level languages such as PYTHON, PASCAL, JAVA, C, C++, C#, BASIC, various scripting languages, and/or HTML. Additionally, the software can be implemented in an assembly language directed to the microprocessor resident on a target computer; for example, the software may be implemented in Intel 80x86 assembly language if it is configured to run on an IBM PC or PC clone. The software may be embodied on an article of manufacture including, but not limited to, a floppy disk, a jump drive, a hard disk, an optical disk, a magnetic tape, a PROM, an EPROM, EEPROM, field-programmable gate array, or CD-

ROM. Embodiments using hardware circuitry may be implemented using, for example, one or more FPGA, CPLD or ASIC processors.

[0055] Approaches described herein may be particularly suitable for implementation in a low-field NMR system where multiple transceivers are integrated on the same semiconductor substrate such that multiple simultaneous NMR measurements can be performed at once. A single replica half circuit described above may be used to independently calibrate all on-chip PAs without the need for providing numerous external resistors to match the impedance of each individual PA.

[0056] In addition, approaches described herein may be suitable for implementation in a low-field NMR system where an NMR coil is integrated on the same silicon substrate as the NMR transceiver, or on a separate silicon substrate but is encapsulated in the same package. In this situation, the calibration techniques described herein may provide precise and robust power delivery to the NMR coil without directly accessing and configuring the interface between the PA and NMR coil.

[0057] An additional benefit is that this technique may also allow class-D PAs to be used with NMR probes having a significantly lower impedance. The ability to precisely control the output impedance at lower absolute impedance values is important because the same absolute variations of PA output impedance may result in larger relative variations of the delivered output power. In micro-NMR, it is desirable to shift from a 50 Ω system to a lower-impedance system so as to increase the total available PA and delivered power for the same supply voltage V_{DDPA} .

[0058] In various embodiments, with reference to FIGS. 6A and 6B, duty-cycle-control (DCC) circuitry 600 may be implemented to reliably and accurately set a duty cycle of PA switching waveforms so as to control the total available power of the PA. The DCC circuitry 600 includes two main components: a time-to-digital converter logic (TDC LOGIC) block 602 and a digital delay line (DDL) 604. Together, block 602 and DDL 604 form a time-to-digital converter (TDC). DDL 604 includes N digital-delay elements 605 connected in series, where the output of each delay element is connected to the input of the next delay element and is also connected to one of the inputs of the TDC LOGIC block 602. The total number of delay elements N and the delay T_d through each individual delay element 605 of the DDL are chosen to ensure that under all PVT conditions, DDL will provide an accurate measurement of 1/4 of the TX carrier period (in units of T_d) with the resolution required for a desired accuracy of duty-cycle programming. The TDC is a sensor that measures the number of delay elements 605 in the DDL 604 required to delay the rising edge of the input TX carrier

signal TXRF_IN with a 50% duty cycle by 1/4 of the period of the TX carrier signal (which corresponds to the output of the RF frequency source 115 shown in FIG. 1 and labeled TXRF_IN in FIG. 6A).

[0059] This number of delay elements, designated as DNUMTXCK, represents the measurement of 1/4 of the TX_carrier period in units of Td and is used to compute the required number of delay-line elements 605 for generating a DCC_OUT (indicated as TXRF_OUT signal in FIG. 6A) signal with a specific duty cycle as a fraction of DNUMTXCK. This signal is provided to the modulator 120 as the duty-cycle-controlled RF frequency source. The value of DNUMTXCK is always less than or equal to the total number of delay elements N.

[0060] With reference to FIGS. 6A-6C and 7, programming the duty cycle of the DCC_OUT signal involves two sequential operations as shown in FIG. 8. First, the TDC circuit comprising the DDL 604 and the TDC LOGIC block 602 measures the TX carrier period, expressed as the closest integer number DNUMTXCK, of the delays Td required to span exactly 1/4 of the TX carrier clock period. And second, the target duty cycle of DCC_OUT is programmed by selecting the required number of delays Td — i.e., DNUMDCC — in the DDL 604 to represent the desired duty cycle of the signal DCC_OUT after the delayed signal DELAYED_REF is combined with signal UNDELAYED_REF via a logical AND operation as shown in FIG. 6B.

[0061] In various embodiments, in order to reduce the length of the DDL 604 and the TDC LOGIC block 602 required to measure the period of the TX carrier signal, the DCC circuitry 600 uses an input clock pulse having a duration of exactly 1/4 of the period of TXRF_IN. This clock pulse corresponds to a 25% duty cycle of the TXRF_IN signal and can be generated by performing logic operations on the quadrature phases of the input clock TXRF_IN. In particular, quadrature components TX_CLK0, TX_CLK90, TX_CLK180 and TX_CLK270 of the clock signal TXRF_IN are generated by block TX_CKGEN (as shown in FIG. 6C) placed at the output of the RF frequency source 115. The quadrature components TX_CK0, TX_CK90, TX_CK180 and TX_CK270 are then provided to a 25% duty cycle generator (DCG) 606 that generates 25% duty cycle waveforms of the quadrature phases of the input signal TXRF_IN. Multiplexer 608 is then used to select between the quadrature phases of TXRF_IN that have a 50% and a 25% duty cycle.

[0062] The DCC circuitry 600 may have a HIGH-power mode and a LOW-power mode corresponding to the 50% and 25% duty cycle of the output signal DCC_OUT. These modes are accessible via an internal configuration and/or control registers 620. Specifically, when

an internal register corresponding to the multiplexer 608 select signal SDCC is written HI, a low-power mode is enabled by selecting one of the quadrature components of the signal TXRF_IN with the 25% duty cycle to propagate through to the input of the modulator 120. Alternatively, when signal SDCC is driven LOW, one of the 50% duty cycle quadrature components of signal RF_CLKIN will propagate to the input of the modulator 120.

[0063] A second multiplexer 615 is employed during the first operation of the duty cycle programming. It is used to select a single 25% duty cycle clock pulse of the RF_CLKIN signal with quadrature phase 90 degrees to perform TDC measurements. The signals and sequence of logic operations during the first operation (TDC measurement) are shown in FIG. 8. Prior to the TDC measurement signals SEL_DCC_CK, DCC_MEASURE, DCC_MEASURE_START, DCC_CK_IN, DCC_CAPTURE — also labeled CONTROL SIGNALS in FIG. 6A — are driven LOW by resetting all associated configuration registers that are used to control these signals via a digital interface. To initiate TDC measurement, signal SEL_DCC_CK is driven HIGH by writing to the associated control register to select DCC_CKIN input of the multiplexer 615 to propagate to the DDL 604 and TDC LOGIC 602. When the signal DCC_MEASURE is asserted HIGH by writing corresponding internal register, duty cycle control/pulse generation block 610 drives HIGH the signal DCC_MEASURE START on the second detected rising edge of the signal CK_PH0_DC25. The rising edge of the signal DCC_MEASURE START then enables propagation of the signal CK_PH0_DC25 to the output DCC_CK_IN of the block 610 to the DLL 604 and TDC LOGIC BLOCK 602. Consequently, the DCC_CAPTURE signal is driven HIGH on the third detected rising edge of the signal CK_PH0_DC25 to capture TDC measurement results, TDCOUT, in capture registers 707 (see FIG. 7) as a digital word DELLENGTH of length M bits, where M is equal or less than the length N of the DDL. At this point, the signal SEL_DCC_CK is driven LOW by writing the corresponding control register in block 620. This disables DCC pulse generation block 610 and completes first operation in the DCC programming sequence. It should be noted that the timing between steps in the sequence of operations may not be critical and thus may be set based on application requirements.

[0064] The signal DELLENGTH is a temperature-encoded measurement of exactly 1/4 of the TXRF_IN carrier period with the number of non-zero least-significant bits corresponding to the number DNUMTXCK. In some embodiments, the DCC circuitry 600 may be bypassed by writing 1 into a DCC_BPS_SELECT register of block 620 and selecting bypassing input to the multiplexer 627. The DCC_BPS_SELECT register may have a default state set as 0.

[0065] Block 620 communicates with the interface block 630, which implements an off-chip communications protocol and the physical layer. The interface block 630, in turn, communicates with the processor block 640. The processor block 640 includes a conventional central processing unit, memory, and control registers, and may be implemented on a chip integrating various parts of the DCC circuitry 600 or off the chip as an external device.

[0066] In the second operation of duty cycle programming sequence, the lower M bits of the TDC 602 output TDCOUT are written into the register block 620 as signal DELLENGTH, and are forwarded to the processor block 640 via the interface 630. The processor block 640 is a priori provided with information about the desired duty cycle value (DCTARGET), which it stores in an internal memory device. Based on that stored value and the information provided by signal DELLENGTH, the processor block 640 computes the required number of delay elements to generate signal DELAYED_REF. This signal, in turn, is used to generate the output signal DCC_OUT with the target duty cycle by performing logic AND operation on the signals DELAYED_REF and UNDELAYED_REF. The required number of delay elements is binary-encoded and written to the register block 620 as the signal SELDELAY of length S via interface 630. The multiplexer 625 then decodes binary signal SELDELAY and selects the output of the appropriate delay line element to generate signal DELAYED_REF. The output DCC_OUT of the multiplexer 625 is TXRF_OUT, the carrier signal of the DCC controller 600 with the target duty cycle value. The DCC controller 600 produces the TXRF_OUT carrier signal with duty cycle that is greater than zero and less than or equal to 50%. For applications where lower jitter and low phase noise are required, a “clean” 50% or 25% duty cycle waveform is obtained by bypassing DDL and AND gate 628 by writing 1 in register DCC_BPS_SELECT as shown in FIG. 6B.

[0067] In various embodiments, for a target duty cycle having a value between 0% and 25%, signal SDCC is driven HIGH to select one of the 25% duty cycle quadrature phases to propagate to the output of the multiplexer 615, DDL 604, multiplexer 625 and AND gate 628. The number DNUMDCC of required selected delay elements of DDL for the DCTARGET value is expressed as:

$$DNUMDCC = \text{floor} \left(DNUMTXCK \cdot \left(1 - 4 \cdot \left(\frac{DCTARGET}{100} \right) \right) \right) \quad \text{Eq. (3).}$$

For a target duty cycle having a value between 25% and 50%, the signal DCC is driven LOW to select one of the 50% duty cycle quadrature phases to propagate to the output of the multiplexer 615, DDL 604, multiplexer 625 and AND gate 628. The corresponding computation for number DNUMDCC is expressed as:

$$\text{DNUMDCC} = \text{floor} \left(\text{DNUMTXCK} \cdot \left(1 - 4 \cdot \frac{\text{DCTARGET} - 0.25}{100} \right) \right) \quad \text{Eq. (4).}$$

[0068] FIG. 7 illustrates the TDC 602 and support circuitry in greater detail. Each delay element 605 in the DDL 604 may have one input and two outputs; delays from the input to any of the outputs may be matched. In one embodiment, one of the outputs is connected to the input of the successive delay element in the DDL chain 604 and to one of the inputs of the multiplexer 625 that is used to select one of the DLL outputs to generate a TX carrier signal having a desired duty cycle. The second output is directed to a D input of one of a chain of TDC flip-flops 703 that collectively provide the lower 24 bits of the output of the TDC 602. The flip-flops 703 are clocked on the rising edge of the signal CLKREFB that itself is an inverted copy of the signal UNDELAYED_REF. As such, each input of each of the flip-flops 703 is captured on the falling edge of signal UNDELAYED_REF. As the signal UNDELAYED_REF propagates through delay elements 605, it reaches the condition where a setup HIGH time violation will occur at some flip-flop, where all downstream flip-flops capturing outputs of delay elements 605 will capture logic value LOW and all upstream flip-flops will capture logic value HI. The captured logic values in all flip-flops 703 then form the digital signal TDCOUT of length N.

[0069] The minimally supported duty cycle may depend on the period of the TX carrier; that period, however, is generally limited by the shortest controlled pulse width for any operating condition. This limit is set by a mismatch in the signal paths of two PA drivers as well as any variation in propagation delays for the pull-up and pull-down drivers that reduce the accuracy of the DCC circuitry 600. This limitation thus results in reduced control over the range of the duty cycle at a lower TX carrier frequency. Accordingly, while the duty cycle control is optimal for the NMR application (or any suitable application), implementing this feature may result in either reduced accuracy in determining the desired duty cycle of the TX carrier at higher frequencies or a reduced control range of the duty cycle at lower frequencies. This can be mitigated by choosing a smaller unit delay T_d and/or a larger number of DDL delay elements N.

[0070] In various embodiments, a smaller amount of power may be required for excitation of a sample at a lower TX carrier frequency. The availability of the low-power mode with a 25% duty cycle and below the control range may address this requirement. At a higher frequency, more power is required and a TX carrier having a 50% duty cycle is used almost exclusively.

[0071] In sum, various embodiments of the present invention provide an all-digital, on-chip duty-cycle control mechanism for accurately setting the duty cycle of PA switching waveforms; this ensures power control with predictable accuracy.

[0072] The central processing unit of the processor block 640 may be a general-purpose processor and, in some embodiments, may be implemented in the controller 110. Alternatively, the central processing unit of the processor block 640 may utilize any of a wide variety of other technologies including special-purpose hardware, a microcomputer, minicomputer, mainframe computer, programmed microprocessor, microcontroller, peripheral integrated circuit element, a CSIC (customer-specific integrated circuit), ASIC (application-specific integrated circuit), a logic circuit, a digital signal processor, a programmable logic device such as an FPGA (field-programmable gate array), PLD (programmable logic device), PLA (programmable logic array), RFID processor, smart chip, or any other device or arrangement of devices that is capable of implementing the steps of the processes of the invention.

[0073] The terms and expressions employed herein are used as terms and expressions of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described or portions thereof. In addition, having described certain embodiments of the invention, it will be apparent to those of ordinary skill in the art that other embodiments incorporating the concepts disclosed herein may be used without departing from the spirit and scope of the invention. Accordingly, the described embodiments are to be considered in all respects as only illustrative and not restrictive.

[0074] What is claimed is:

CLAIMS

1. Circuitry for reducing variability of an output impedance of an integrated switch-mode power amplifier (PA), the circuitry comprising:
 - a PA driver;
 - a pre-driver for facilitating activation and deactivation of the PA driver; and
 - a passive resistor coupled to the PA driver so as to split the output impedance between the PA driver and the passive resistor.
2. The circuitry of claim 1, wherein the PA driver comprises a PMOS device and an NMOS device.
3. The circuitry of claim 1, wherein the on-chip passive resistor has an impedance that does not depend on temperature or voltage.
4. The circuitry of claim 1, further comprising a calibration circuit for calibrating an ON resistance of the PA driver so as to provide stable output power levels.
5. The circuitry of claim 4, wherein the calibration circuit comprises a replica circuit of the PA driver and a load resistor.
6. The circuitry of claim 4, wherein the calibration circuit further comprises an on-chip voltage divider for generating a reference voltage.
7. The circuitry of claim 6, wherein the calibration circuit further comprises a comparator for comparing the reference voltage with an output voltage of the replica circuit and the load resistor.
8. The circuitry of claim 1, wherein the passive resistor is on-chip.
9. The circuitry of claim 1, wherein the passive resistor is off-chip.
10. An NMR apparatus comprising:
 - an NMR coil configured to enclose a sample;

an integrated switch-mode PA coupled to the NMR coil; and
circuitry for reducing variability of an output impedance of the PA;
wherein the circuitry comprises (i) a PA driver, (ii) a pre-driver for facilitating
activation and deactivation of the PA driver; and (iii) an on-chip passive resistor coupled to
the PA driver for splitting the output impedance between the PA driver and the passive
resistor.

11. The NMR apparatus of claim 10, wherein the PA driver comprises a PMOS device
and an NMOS device.

12. The NMR apparatus of claim 10, wherein the on-chip passive resistor has an
impedance that does not depend on temperature or voltage.

13. The NMR apparatus of claim 10, further comprising a calibration circuit for
calibrating an ON resistance of the PA driver so as to provide stable output power levels.

14. The NMR apparatus of claim 13, wherein the calibration circuit comprises a replica
circuit of the PA driver and a load resistor.

15. The NMR apparatus of claim 13, wherein the calibration circuit further comprises an
on-chip voltage divider for generating a reference voltage.

16. The NMR apparatus of claim 15, wherein the calibration circuit further comprises a
comparator for comparing the reference voltage with an output voltage of the replica circuit
and the load resistor.

17. A method of reducing variability of an output impedance of an integrated switch-
mode power amplifier (PA), the method comprising:
providing a PA driver having at least one MOS device;
providing a pre-driver for facilitating activation and deactivation of the PA driver; and
adjusting a number of stripes of the at least one MOS device so to provide a desired
impedance.

18. Circuitry for adjusting a duty cycle of an RF carrier input signal to a power amplifier (PA), the circuitry comprising:
 - a digital delay line, comprising a plurality of digital delay elements, for receiving the input signal;
 - a time-to-digital converter for measuring a number of the digital delay elements required for generating a desired duty cycle; and
 - circuitry for selecting the number of delay elements of the digital delay line required to generate a desired duty cycle and receiving an output signal therefrom, the output signal having the adjusted duty cycle.
19. The circuitry of claim 18, further comprising a processor having a control register for enabling a HIGH-power mode or a LOW-power mode of the circuitry.
20. The circuitry of claim 19, wherein the control register has a value of 1 for enabling the LOW-power mode and a value of 0 for enabling the HIGH-power mode.
21. The circuitry of claim 19, wherein the control register selects the HIGH-power mode when the desired duty cycle has a value between 25% and 50% and the LOW-power mode when the desired duty cycle has a value between 5% and 25%.
22. The circuitry of claim 18, further comprising a processor having a register for bypassing the digital delay line.
23. The circuitry of claim 18, wherein the digital delay line comprises a plurality of delay elements.
24. The circuitry of claim 18, wherein each one of the delay elements comprises one input and three outputs.
25. The circuitry of claim 24, wherein a first one of the outputs is coupled to an input of a successive delay element; a second one of the outputs is coupled to an input of a multiplexer; and a third one of the outputs is coupled to an input of the time-to-digital converter.

26. The circuitry of claim 18, further comprising a processor configured to determine the number of the delay elements required for generating the desired duty cycle based on a measurement of the time-to-digital converter.
27. The circuitry of claim 26, wherein the processor is implemented on a chip integrating the digital delay line and time-to-digital converter.
28. The circuitry of claim 26, wherein the processor is implemented off a chip integrating the digital delay line and time-to-digital converter and the circuitry further comprises a communication module for allowing signal communication between the processor and the chip.
29. An NMR apparatus comprising:
an NMR coil configured to enclose a sample;
an integrated switch-mode PA coupled to the NMR coil; and
circuitry for adjusting a duty cycle of an input signal to a power amplifier (PA);
wherein the circuitry comprises: (i) a digital delay line having a plurality of delay elements, and (ii) a time-to-digital converter for measuring a number of the delay elements required for generating a desired duty cycle.
30. The NMR apparatus of claim 29, wherein the circuitry further comprises a processor having a control register for enabling a HIGH-power mode or a LOW-power mode of the circuitry.
31. The NMR apparatus of claim 30, wherein the control register has a value of 1 for enabling the LOW-power mode and a value of 0 for enabling the HIGH-power mode.
32. The NMR apparatus of claim 30, wherein the control register selects the HIGH-power mode when the desired duty cycle has a value between 25% and 50% and the LOW-power mode when the desired duty cycle has a value between 5% and 25%.
33. The NMR apparatus of claim 29, wherein the circuitry further comprises a processor having a register for bypassing the digital delay line.

34. The NMR apparatus of claim 29, wherein the digital delay line comprises a plurality of delay elements.
35. The NMR apparatus of claim 29, wherein each one of the delay elements comprises one input and three outputs.
36. The NMR apparatus of claim 35, wherein a first one of the outputs is coupled to an input of a successive delay element; a second one of the outputs is coupled to an input of a multiplexer; and a third one of the outputs is coupled to an input of the time-to-digital converter.
37. The NMR apparatus of claim 29, wherein the circuitry further comprises a processor configured to determine the number of the delay elements required for generating the desired duty cycle based on a measurement of the time-to-digital converter.
38. The NMR apparatus of claim 37, wherein the processor is implemented on a chip integrating the digital delay line and time-to-digital converter.
39. The NMR apparatus of claim 37, wherein the processor is implemented off a chip integrating the digital delay line and time-to-digital converter and the circuitry further comprises a communication module for allowing signal communication between the processor and the chip.

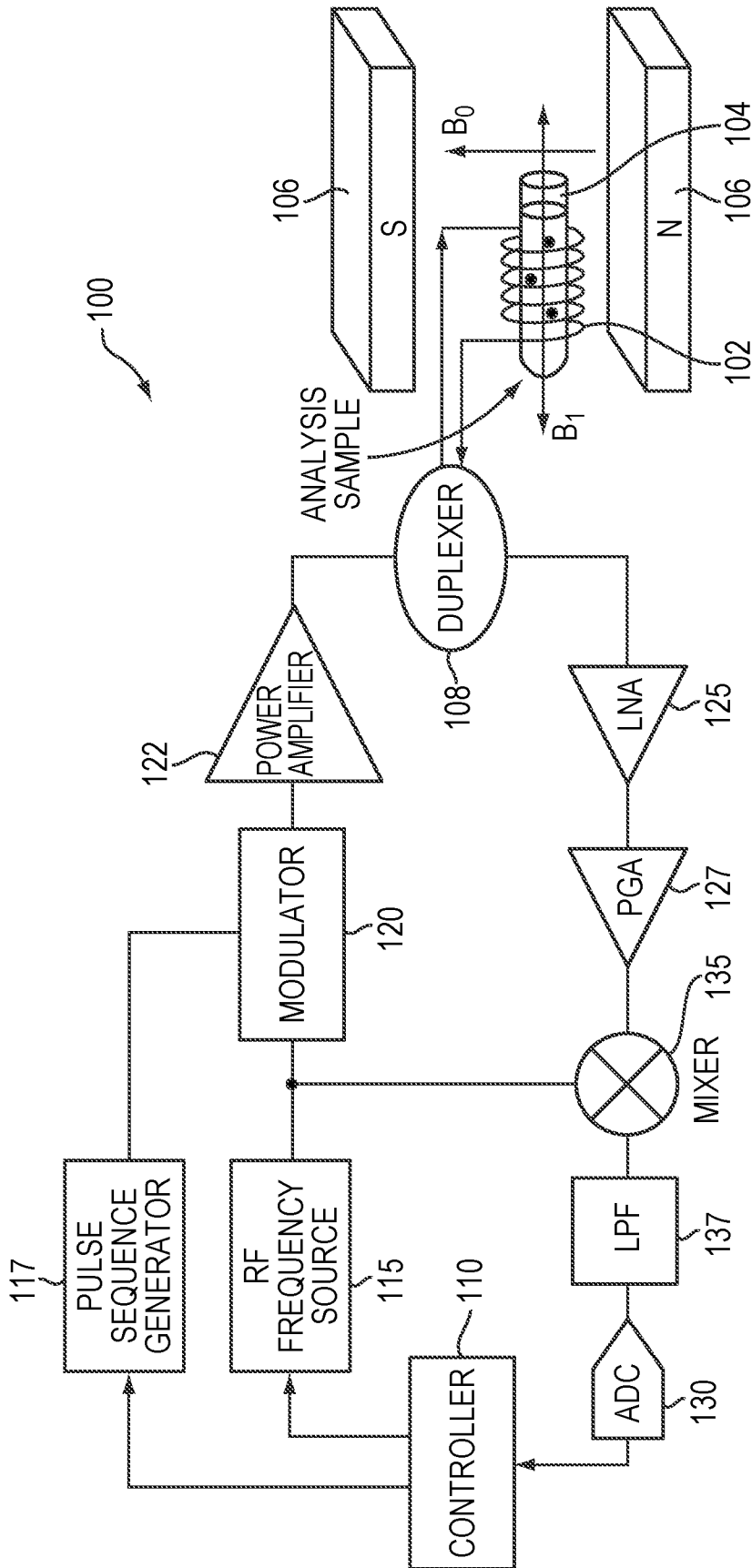


FIG. 1
(PRIOR ART)

2/10

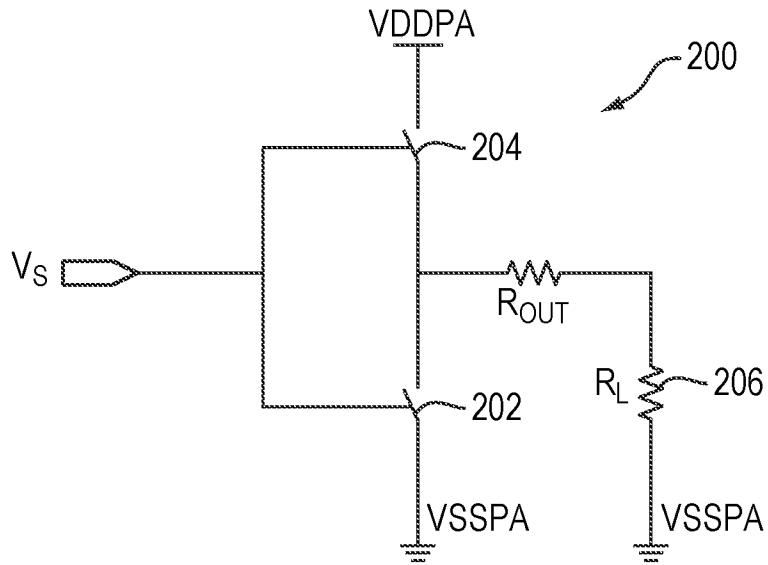
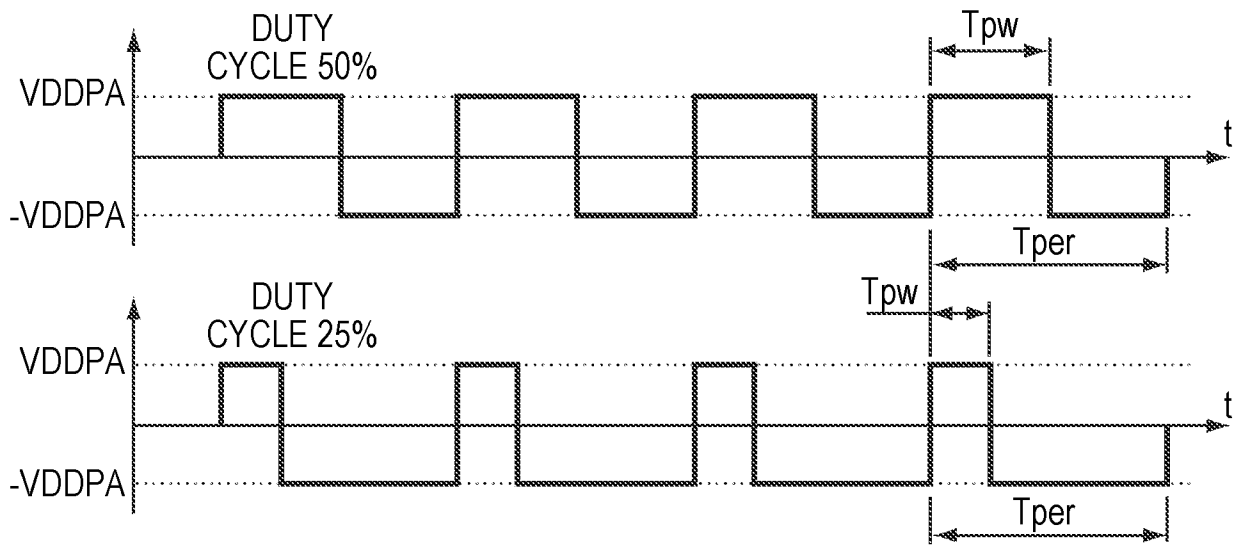


FIG. 2A
(PRIOR ART)



$$DC = T_{pw} / T_{per}$$

FIG. 2B

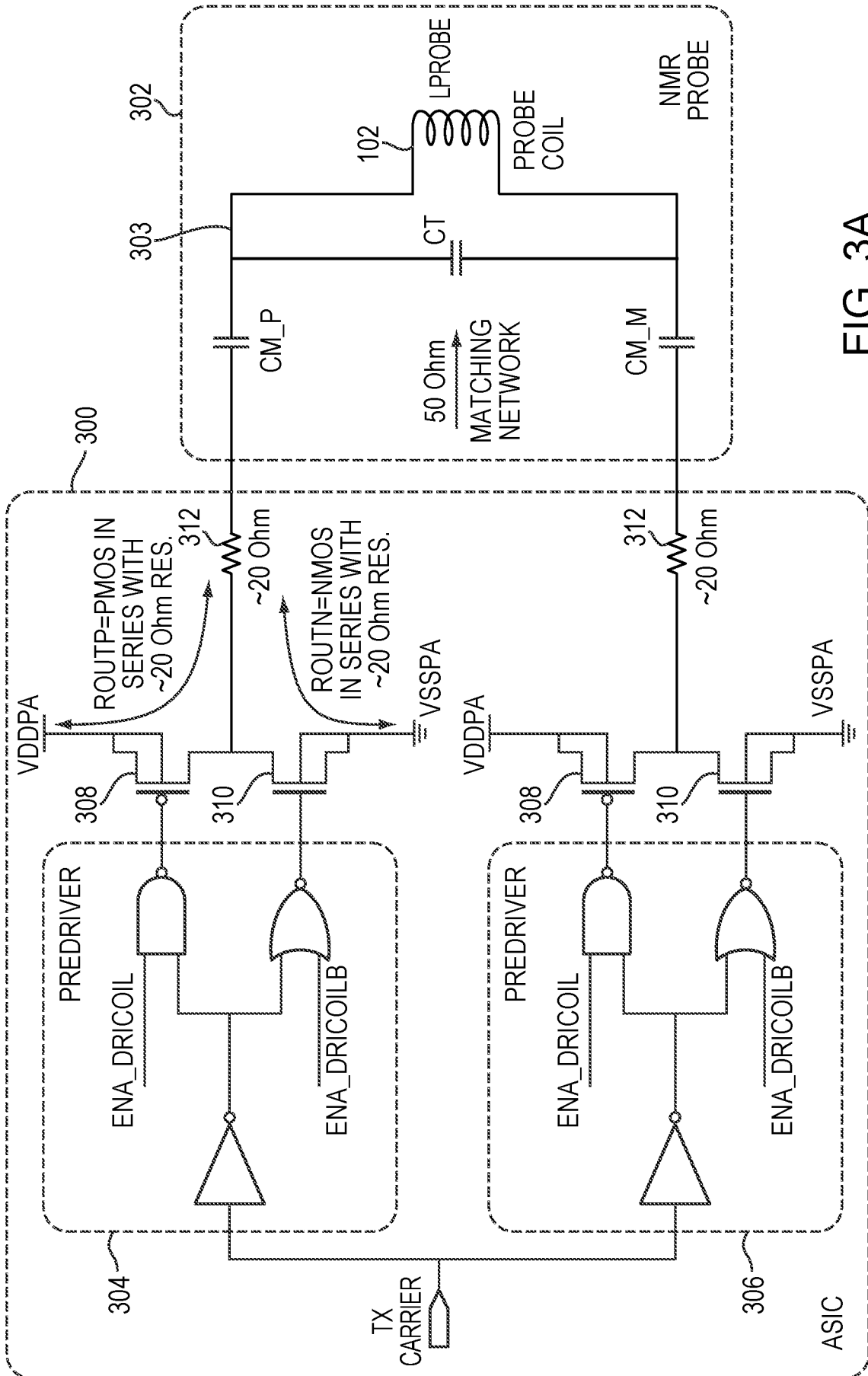


FIG. 3A

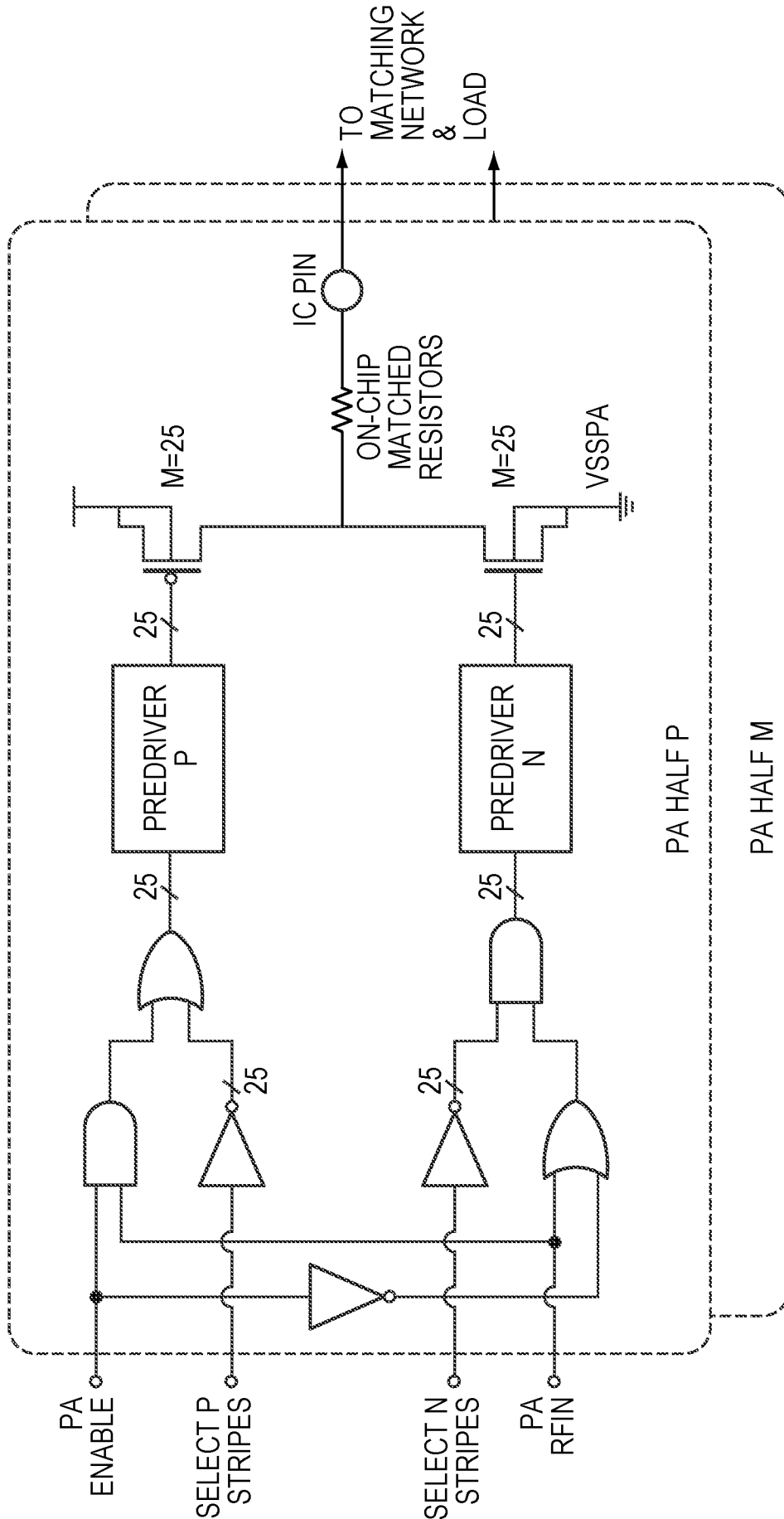


FIG. 3B

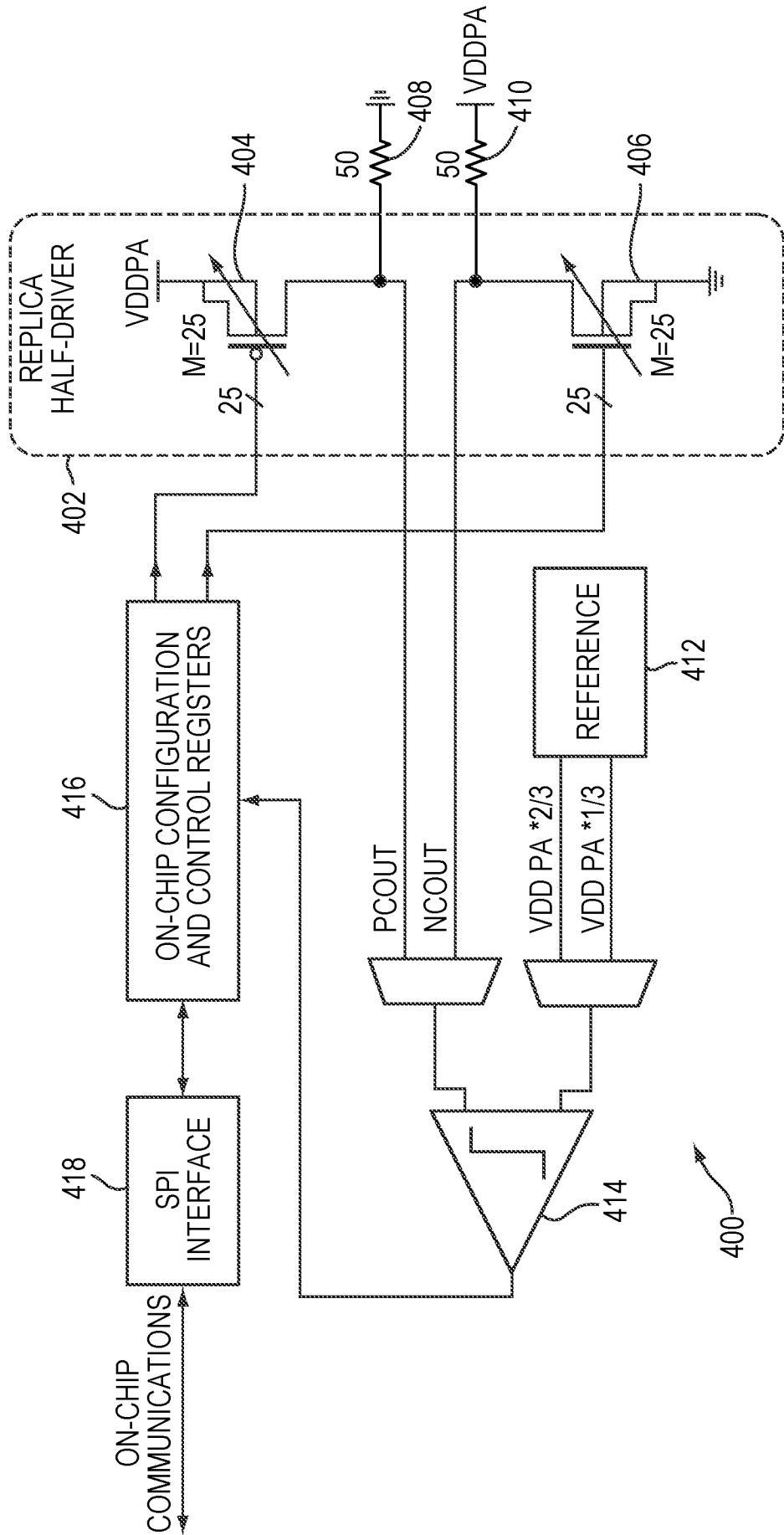


FIG. 4

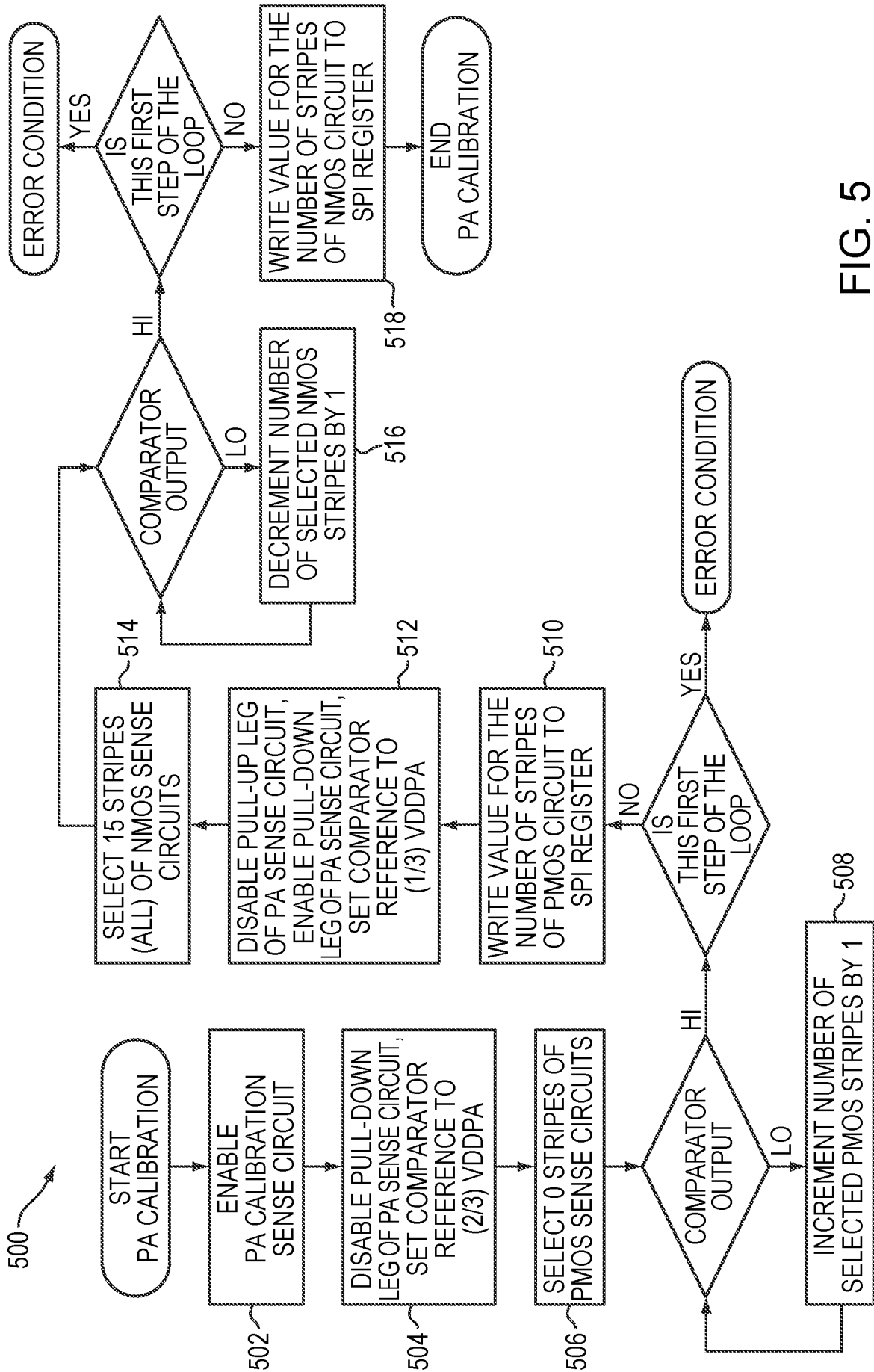


FIG. 5

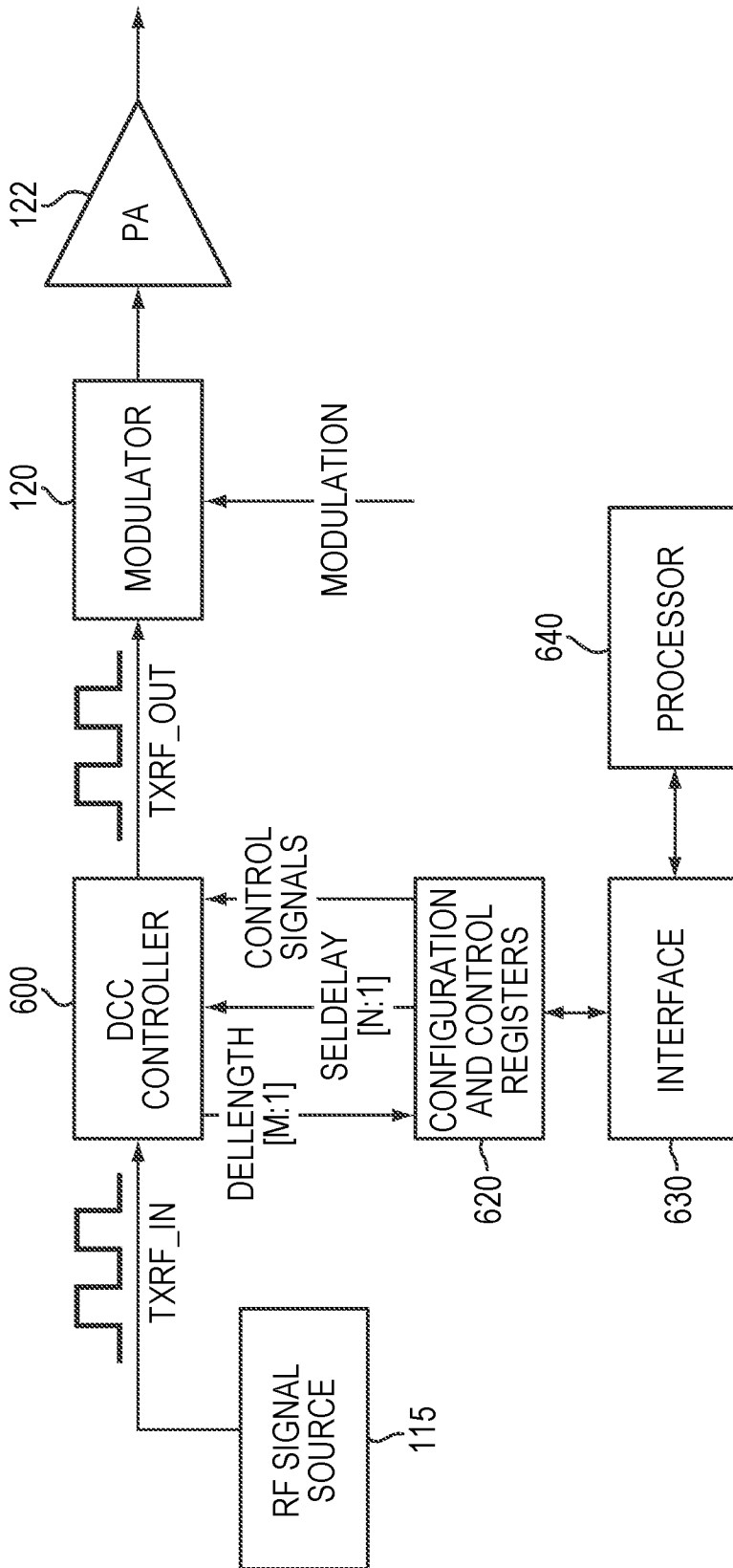


FIG. 6A

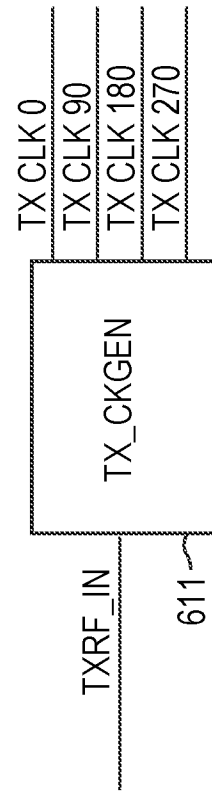


FIG. 6C

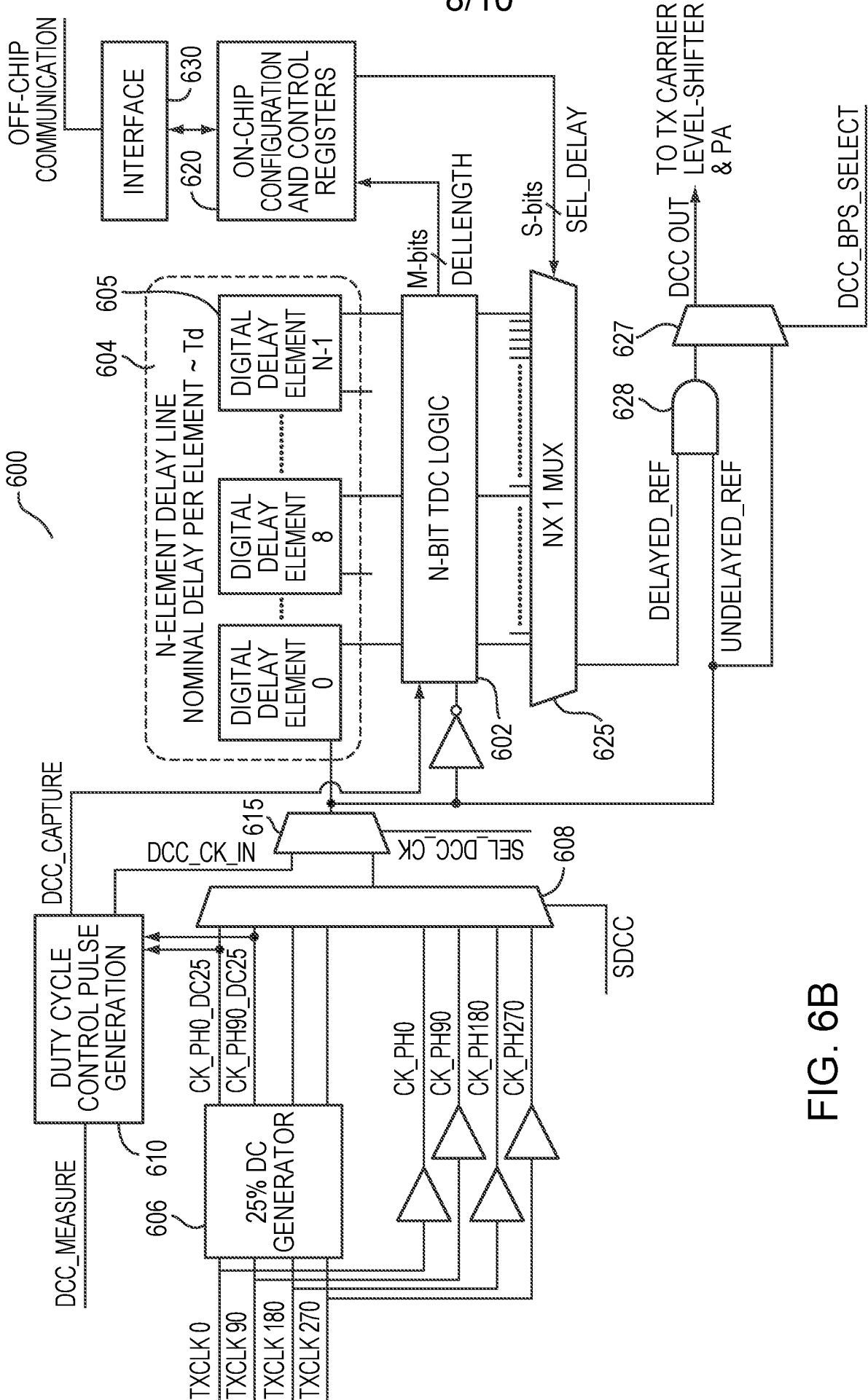


FIG. 6B

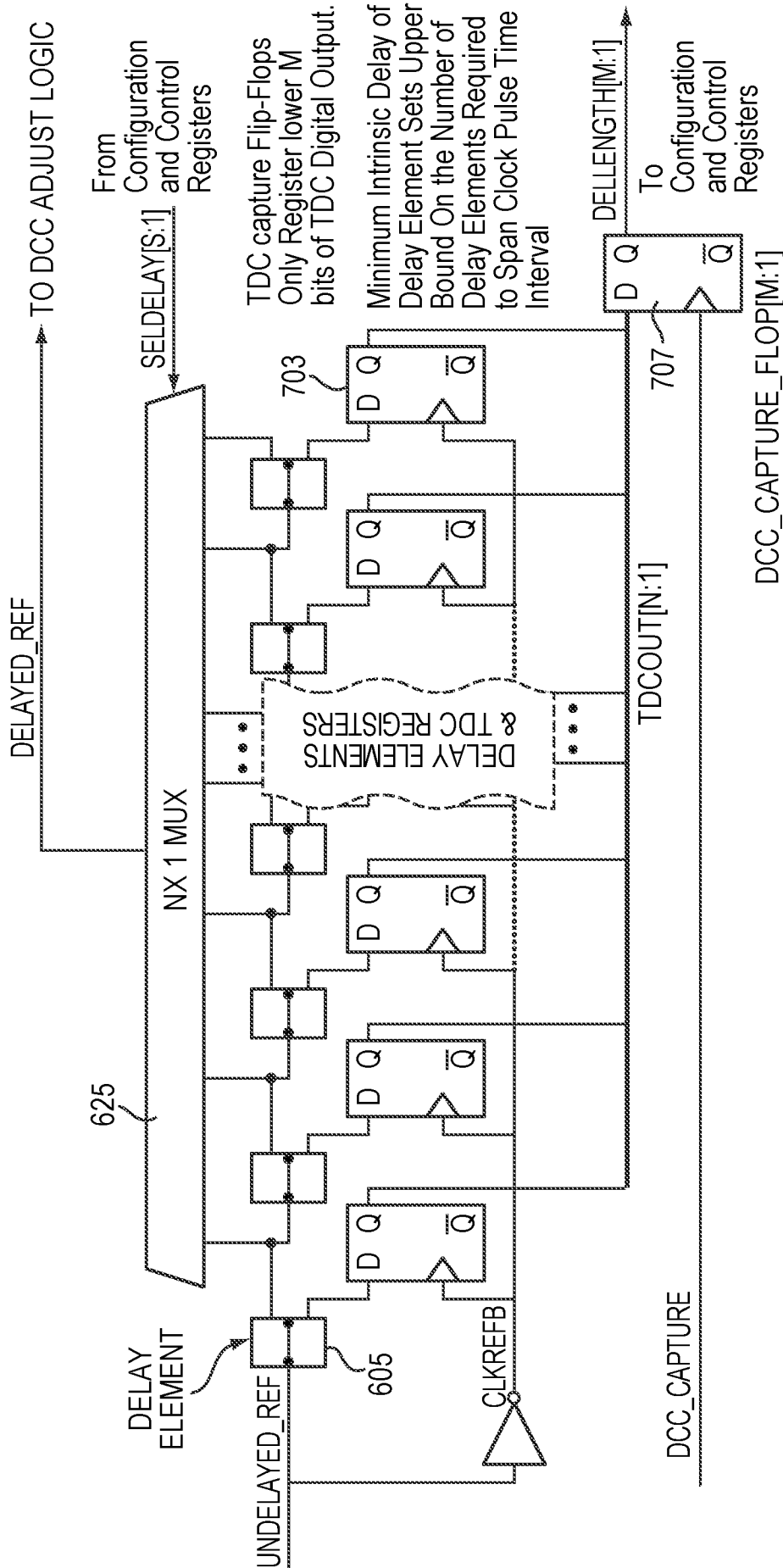


FIG. 7

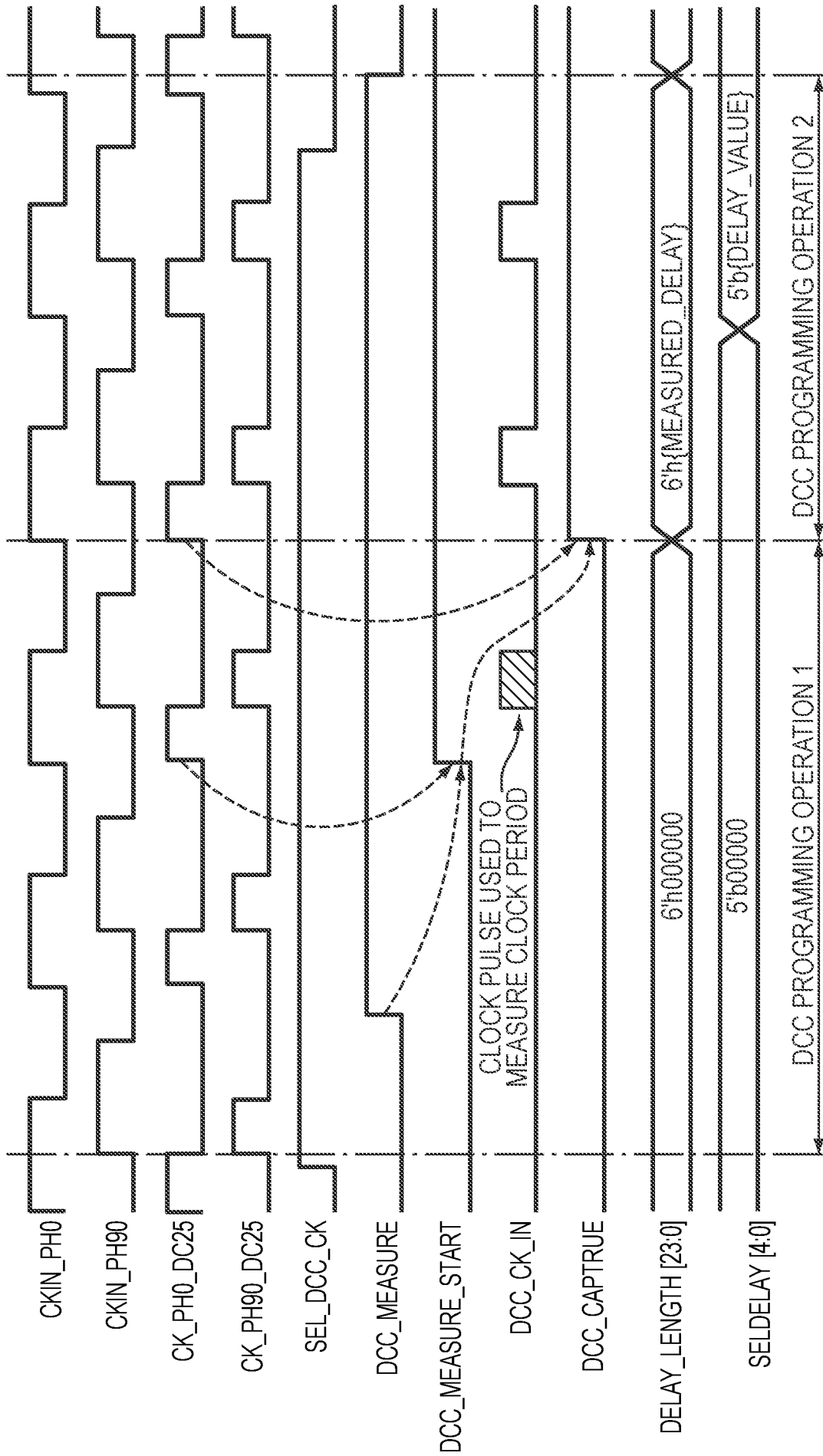


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2018/024333**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group I, claims 1-17, drawn to a technical feature(a system/an apparatus) for reducing variability of an output impedance of an integrated switch-mode power amplifier (PA).

Group II, claims 18-39, drawn to a technical feature(a system/an apparatus) for adjusting a duty cycle of an RF carrier input signal to a power amplifier (PA).

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-17

- Remark on Protest**
- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/024333**A. CLASSIFICATION OF SUBJECT MATTER****H03F 1/56(2006.01)i, H03F 3/193(2006.01)i, H03F 3/217(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
H03F 1/56; H03K 19/0175; H03F 3/38; H03K 19/094; H03F 3/217; G01R 33/38; H03F 3/193Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: NMR apparatus, switch-mode power amplifier (PA), output impedance, PA driver, resistor**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6087853 A (CAROL A. HUBER et al.) 11 July 2000 See column 2, line 26 - column 8, line 8 and figures 5-9.	1-9, 17
Y		10-16
Y	US 2014-0176135 A1 (CASE WESTERN RESERVE UNIVERSITY) 26 June 2014 See claims 1, 6 and figures 2, 7.	10-16
A	US 2006-0214688 A1 (DONG PAN et al.) 28 September 2006 See paragraphs [0024]-[0025] and figure 3.	1-17
A	WO 2008-105592 A1 (UBI SOUND CO., LTD.) 04 September 2008 See paragraphs [0042]-[0050] and figure 8.	1-17
A	WO 2006-107815 A2 (INTERNATIONAL RECTIFIER CORPORATION) 12 October 2006 See paragraphs [0014]-[0021] and figures 2A-4D.	1-17

 Further documents are listed in the continuation of Box C. See patent family annex.

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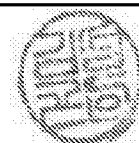
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/024333

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