May 12, 1970 A. D. SCARBROUGH 3,512,158

INFRA-RED PRINTER

Filed May 2, 1968 6 Sheets-Sheet 1

Fig. 1

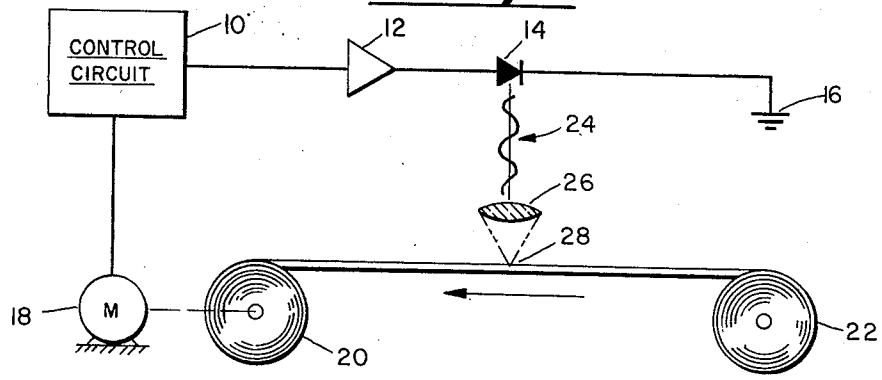

Fig. 2

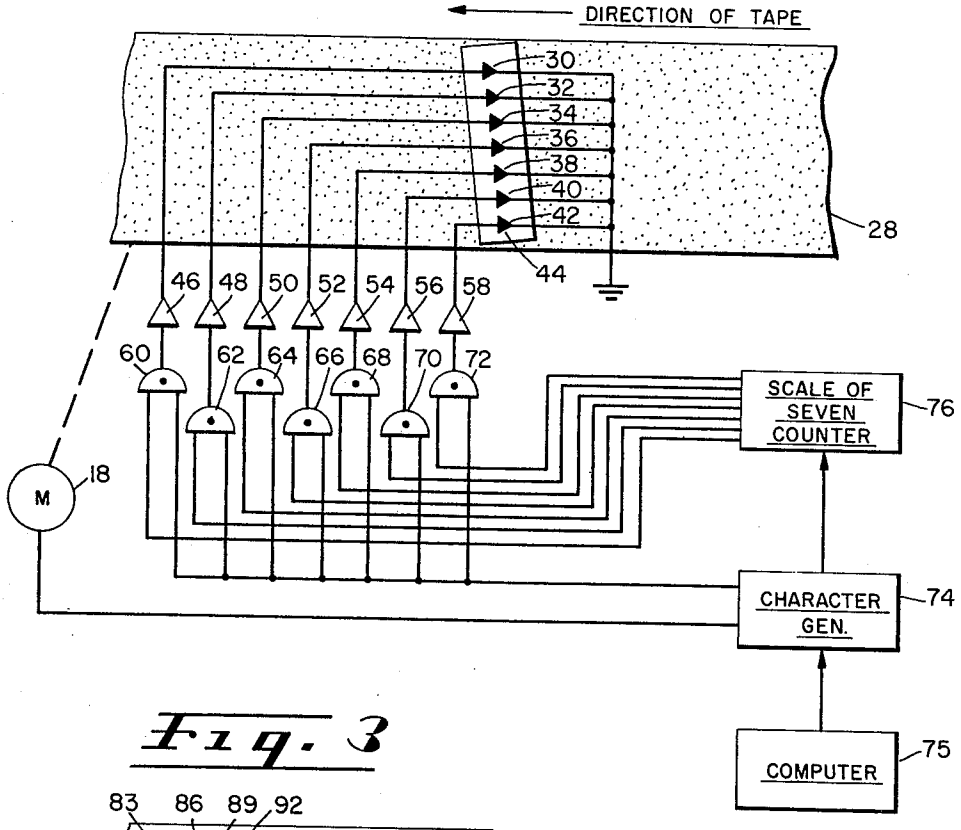

Fig. 3

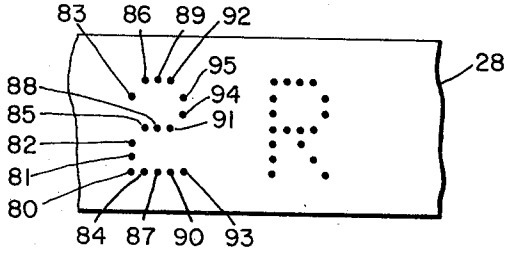

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Fig. 4

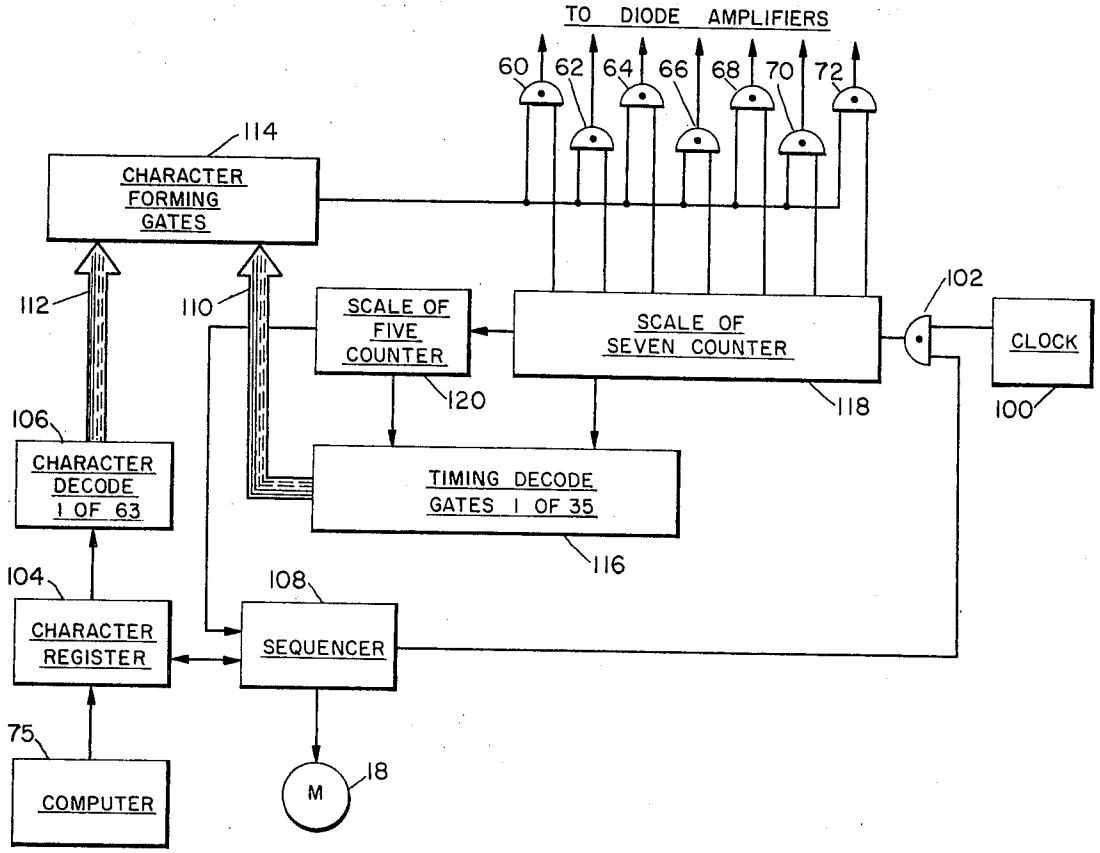

Fig. 5

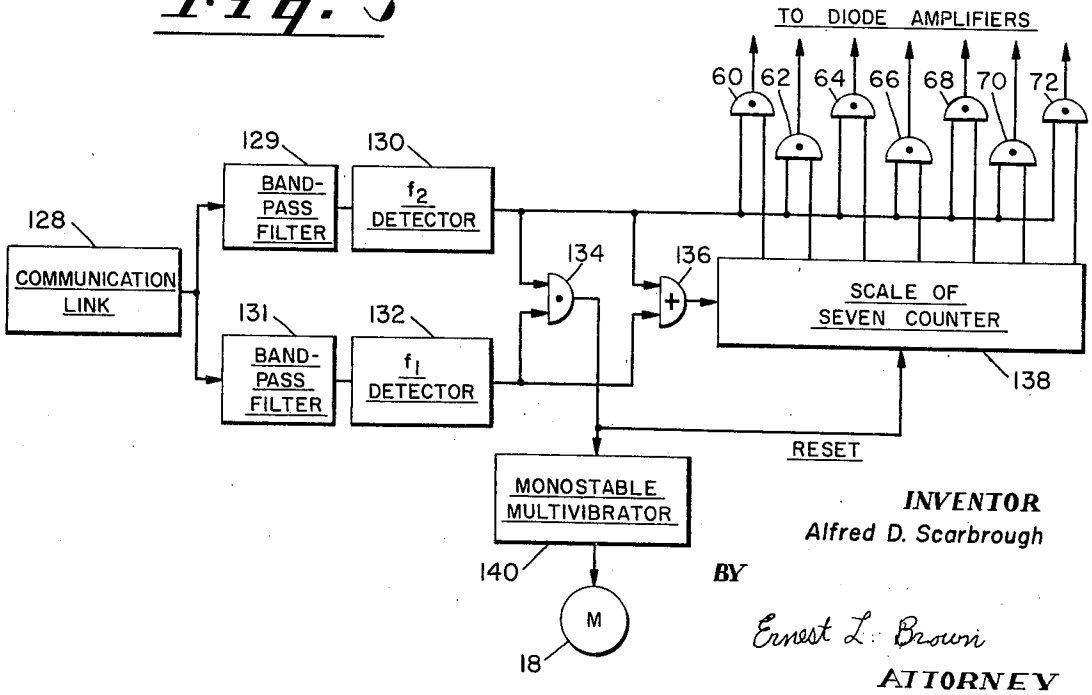

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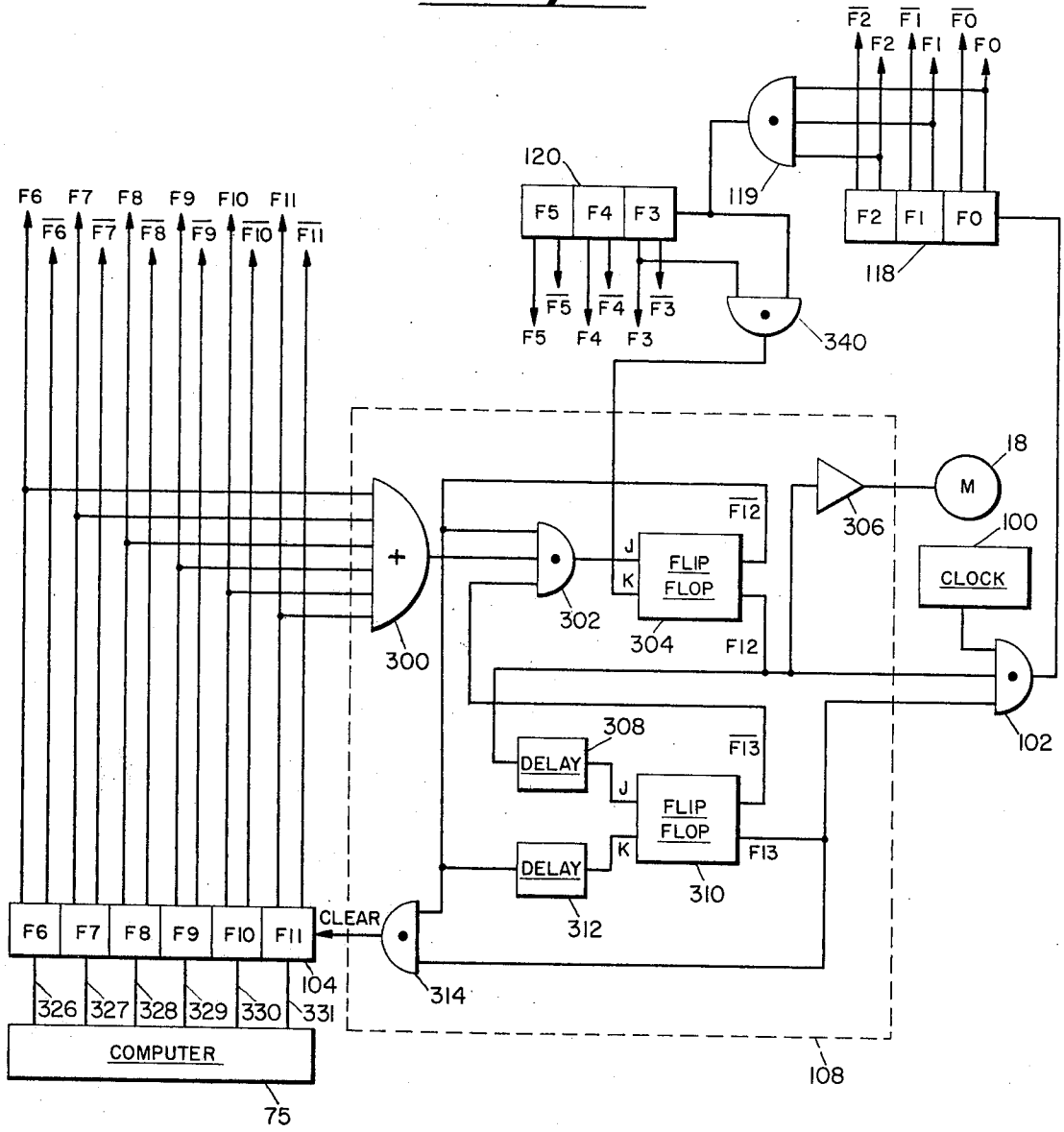
Fig. 6



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INFRA-RED PRINTER

Filed May 2, 1968 6 Sheets-Sheet 4

Fig. 1

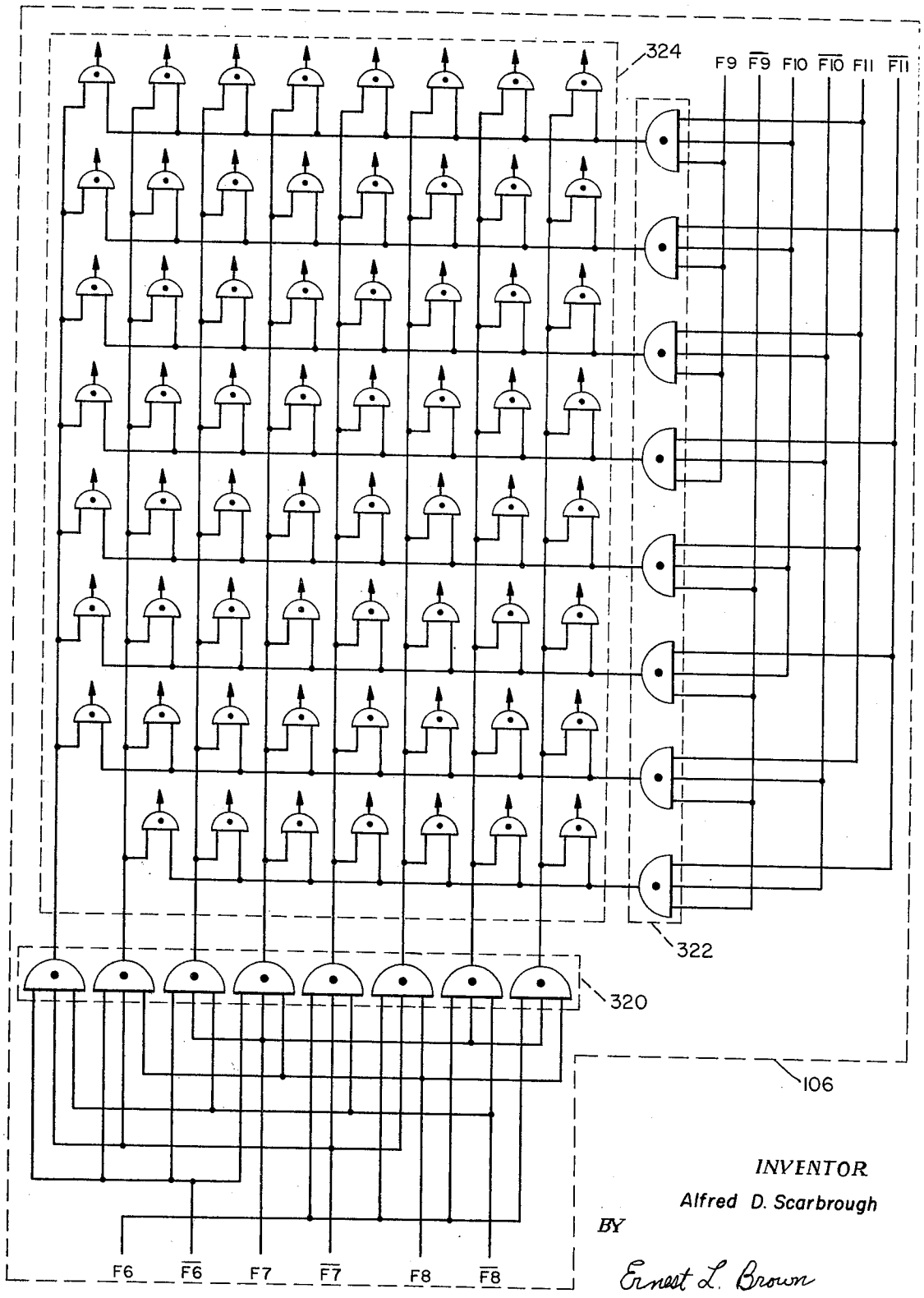

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Fig. 8

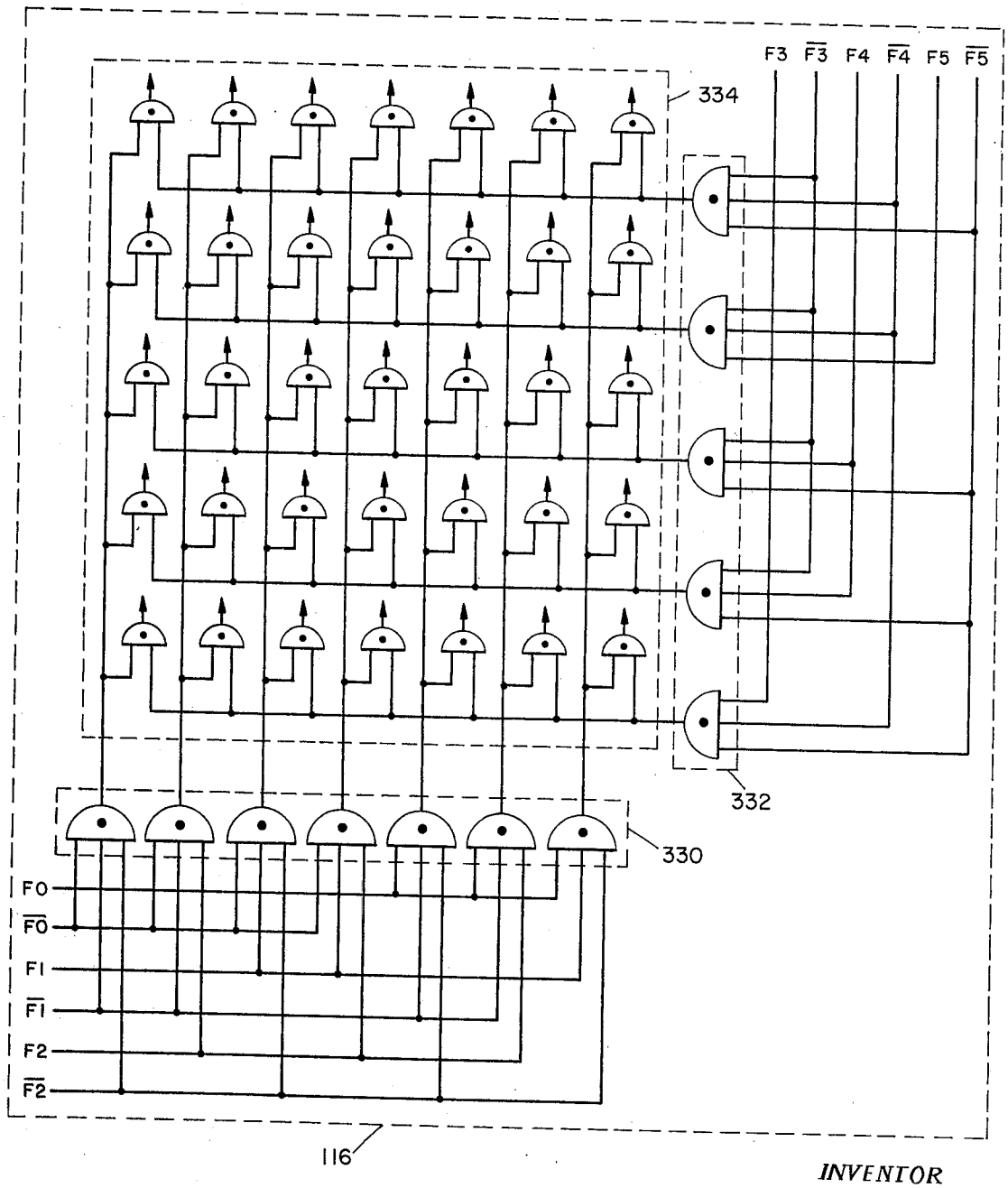

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Fig. 9

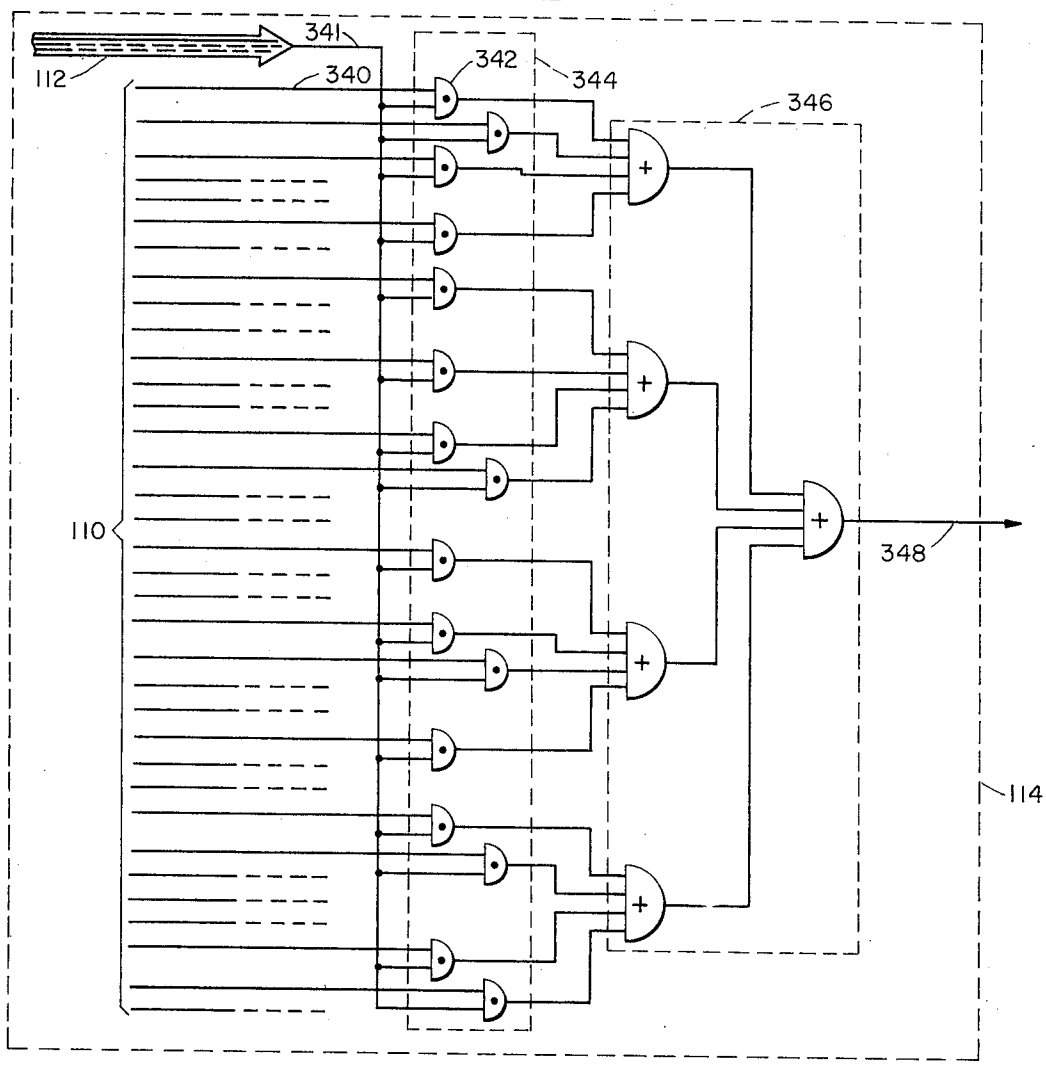
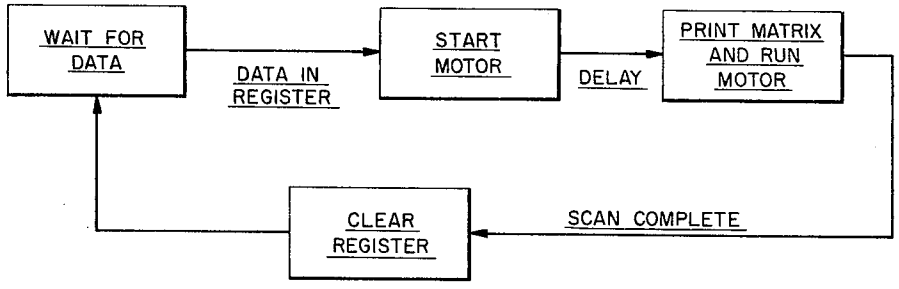


Fig. 10



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United States Patent Office 3,512,158 Patented May 12, 1970

3,512,158

INFRA-RED PRINTER

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Filed May 2, 1968, Ser. No. 726,110
Int. Cl. G01d 15/14; G06k 15/02
U.S. Cl. 346—76 15 Claims

ABSTRACT OF THE DISCLOSURE

The invention comprises an infra-red printer using infra-red emitters, such as infra-red emitting diodes, as a source of heat to produce printing or graphical characters on heat-sensitive paper. In one embodiment, a heat-sensitive paper strip is pulled past seven infra-red diodes arranged in a line across the paper to correspond to the seven vertical positions of a character matrix such as that used in display equipment. Selective energizing of the diodes irradiates the paper to correspond to a sequence of characters that can be constructed from a dot matrix. Typically the diodes are pulsed, although they may be driven for longer durations to print lines on the paper either by moving the paper past the diodes or by moving the diodes relative to the paper.

Short description of the invention

Prior art printers use heated wires or resistance elements to apply heat to heat-sensitive paper. For example, the U.S. Pat. No. 3,145,071 for a "High Speed Thermal Contact Printer," patented by Arthur W. Vance, uses heated wires, such as silver wires, to apply heat to a thermo-sensitive paper. The apparatus of the U.S. Pat. No. 3,161,457 for "Thermal Printing Units," issued to Hans Schroeder et al., uses small resistors to generate heat and to apply the heat to the paper.

An example of commercially available thermally-sensitive material which may be marked by heat is the paper manufactured by Minnesota Mining and Manufacturing Company which are marked under the trademark "Thermo-Fax" paper.

With modern high speed computers, the speed at which the computers may be read is limited by the speed at which the information may be printed. Infra-red emitting diodes have substantially no thermal inertia and they can be turned on and off very rapidly. Consequently, because they may be turned on and off very rapidly, the thermo-sensitive paper may be moved rapidly past the emitting diodes to generate information on the paper indicative of the information read out of the computer.

Infra-red emitting diodes, such as gallium arsenide diodes, are efficient and therefore generate little spurious heat. The heat generated is concentrated into a substantially monochromatic ray of high intensity infra-red radiation. The diode itself does not get hot because the generated energy is substantially all radiated.

Because the generated rays are monochromatic, they can easily be focused. Thus, for example, they may be focused into a beam of high intensity which prints the paper at a very rapid rate compared to printers wherein the heat energy is spread over a wider spectrum and has less intensity.

Some infra-red emitters emit parallel light beams in small concentrated bundles of energy, whereby no lens system is needed.

Infra-red emitters operate from relatively low power and voltage sources. Because of the low power and voltage requirements of the infra-red emitters, they may be driven by transistorized circuitry.

Because of the high efficiency of the infra-red emitters and because they operate at a cool temperature, they have an inherently long life.

It is therefore an object of this invention to print on heat-sensitive paper with infra-red radiation originating from a controlled infra-red source.

It is a more particular object of this invention to achieve the above object with infra-red emitting diodes.

It is still a more particular object of this invention to achieve the above objects with infra-red emitters which are adapted to be controlled in response to electrical signals.

It is even a more particular object of this invention to control such infra-red emitters with transistorized circuitry.

It is another object of this invention to drive infra-red emitters with circuitry arranged to produce pulses appropriate to generate recognizable characters.

It is yet another object of this invention to achieve the above-enumerated objects with transistorized circuitry which is adapted to be responsive to logical signals.

It is a specific object of this invention to provide apparatus and circuitry which is adapted to achieve the above-enumerated objects.

Other objects will become apparent from the following description, taken in connection with the accompanying drawings in which:

Brief description of drawings

FIG. 1 is a diagram of a rudimentary device of this invention;

FIG. 2 is a diagram of a device of this invention adapted to be controlled by a character generator;

FIG. 3 is a sample of typical symbols in a 7 x 5 matrix which may be printed by the device of this invention;

FIG. 4 is a more detailed block diagram of typical driving circuitry for infra-red emitters, according to this invention;

FIG. 5 is a detailed block diagram of a typical frequency-shift keying driving circuitry for driving infra-red emitters;

FIG. 6 is a specific embodiment of the character register, sequencer, and counters of FIG. 4;

FIG. 7 is a specific embodiment of the character decode means of FIG. 4;

FIGURE 8 is a specific embodiment of the timing decode gates of FIG. 4;

FIG. 9 is a specific embodiment of the character forming gates of FIG. 4; and

FIG. 10 is a block diagram of the operation sequence of the apparatus of FIG. 4.

Detailed description of invention

Typically, characters are printed out in a 7 x 5 matrix of dots as shown, for example, in FIG. 3. The driving circuitry shown herein is adapted to produce such characters. However, it should be stressed that the 7 x 5 dot matrix is shown for convenience only and that the invention is not to be limited to producing such characters.

In FIG. 1, a control circuit **10**, through an amplifier **12**, drives an infra-red emitter **14**. The return circuit typically is through a common terminal **16**. Concurrently with the energizing of emitter **14**, the control circuitry energizes the motor **18**. Motor **18** drives a reel or spindle **20**, winding heat-sensitive paper or tape off of the supply reel **22**.

The control circuit may—for example—be a computer-controlled character generator with associated equipment as shown in FIG. 2. Alternatively it may be a paper or magnetic tape reader. Other examples of information sources, such as memory drums, telemetering links, or electric typewriters may be used.

The motor **18** may be a continuously energized motor, a stepping solenoid, or other intermittent motor.

The infra-red emitter **14** may, for example be a gallium arsenide diode.

The emitter **14**, when energized, emits infra-red energy **24** which is focused by a lens system **26** onto the heat-sensitive paper **28**. It should be emphasized that the lens system **26** need not be used when the emission of the emitter **14** produces the appropriate concentrated energy without such a lens system.

The lens system **26** may be a single or multiple lens. It need not be spherical. The criterion is that the radiation **24** be focused at the desired point on the paper.

In FIG. 2, seven infra-red emitting diodes **30**, **32**, **34**, **36**, **38**, **40**, and **42** are shown above the heat-sensitive paper **28**. Radiation from these diodes is shown focused onto the paper **28** by the cylindrical lens **44**.

The diodes are driven, respectively, by amplifiers such as transistorized amplifiers **46**, **48**, **50**, **52**, **54**, **56**, and **58** which, in turn, are excited by the outputs of AND distributing gates **60**, **62**, **64**, **66**, **68**, **70**, and **72**.

The output signals of character generator **74** are channeled to the distributing gates. Timing signals are channeled from generator **74** into a scale-of-seven counter **76** and are thence channeled to the distributing gates. Computer **75** is shown connected to determine the particular character chosen by generator **74**.

The character generator **74** is also shown controlling the motor **18**, and hence the movement of the heat-sensitive tape **28**.

Details of specific embodiments of the character generator connections are reserved for the discussion of FIGS. 4–10.

Typical figures printed onto tape **28** in a 7 x 5 dot matrix are shown in FIG. 3. Notice that the dots are arranged in seven rows and five columns. For convenience of description, number the columns from left to right, "columns **1** through **5**." Number the rows, consecutively, from bottom to top of the figure, "rows **1** through **7**."

In the described embodiments, the dot positions are scanned one-at-a-time, starting with column **1**, row **1**; thence proceeding up column **1** to row **7**; thence to column **2**, row **1**, up column **2** to row **7**; thence through columns **3**, **4**, and **5**, in order, from row **1** to row **7** in the same fashion as in columns **1** and **2**.

During movement of tape **28**, the positions of the dot matrix come under the infra-red diodes in the above-described order. Should a signal be transmitted to the proper diode, a dot is produced on the tape. For example, the position of column **1**, row **1**, first moves into position under diode **42**. Should a pulse of energy be received by diode **42** at that moment, a dot is produced in the column **1**, row **1** position. A moment later the tape **28** has advanced so that the column **1**, row **2** position of the dot matrix has advanced under diode **40**. Should a pulse of energy be received by diode **40** at that moment, a dot is produced in the column **1**, row **2** position. The tape then advances to place, consecutively, the column **1**, row **3** under diode **38**; column **1**, row **4** under diode **36**; column **1**, row **5** under diode **34**; column **1**, row **6** under diode **32**; column **1**, row **7** under diode **30**; column **2**, row **1** under diode **42** . . . . Note that the row of diodes is turned slightly from a position directly across the tape **28**, toward the direction of motion of the tape so that the diode **42** is in position to produce a dot in row **1** of the next column of the dot matrix immediately after the diode **30** is in position to produce a dot in row **7**.

Since the order of production of the dots in the dot matrix is known, each character which may be produced may be represented by a thirty-five bit binary numeral in which, for example, the "1" indicates that a dot is formed in the consecutively indexed position, while the numeral "0" indicates that a dot is omitted in a particular position. Referring to FIG. 3, in which the numbers **80–95** indicate the consecutive dots to be produced in

the dot matrix, to print out the numeral "2" the print-out command can be represented by the binary sequence:

11100101001001100100110010011000110

To print out a character, the character generator **74** sends a series of timed pulses to the scale-of-seven counter **76**, causing the counter **76** to distribute the timing pulses to the gate amplifiers in the following order: **72**, **70**, **68**, **66**, **64**, **62**, **60**, **72** . . . .

Signals are also channeled from the character generator **74** to the motor **18** to synchronize the tape movement with the timing signals.

A series of intermittent pulses are transmitted from generator **74** to all of the gates in synchronism with the timing signals. For example, when the numeral "2" is to be printed out, the pulses transmitted to all of the gates are intermittent in the above-mentioned pattern, i.e.:

11100101001001100100110010011000110

wherein a "1" represents a pulse coinciding with a timing pulse, and a "0" represents the absence of a pulse coinciding with a timing pulse.

There are many variations in the character generator. Obviously, if desired, thirty-five diodes could be positioned over the heat-sensitive paper in the positions of the dots in the dot matrix. All of the appropriate diodes corresponding to the positions of desired dots could then simultaneously be energized.

One of the embodiments which prints the dots serially is shown in FIG. 4. The computer **75** produces command signals indicating the character to be written out. A typical output of computer **75** might be six channels in parallel adapted to set a register means such as the character register **104**. Typically, the character register cells are flip flops wherein the output signals, F and $\overline{F}$ represent two complementary outputs, e.g. F is true and $\overline{F}$ is false when the flip flop stores a "1," and F is false and $\overline{F}$ is true when the flip flop stores a "0." A six channel computer output is shown, for example, in FIG. 6 in which the six signals are designated by the lines **326**, **327**, **328**, **329**, **330**, and **331**. The signals **326–331** are connected to the character register **104** which generates twelve signals, F6, $\overline{F6}$, F7, $\overline{F7}$, F8, $\overline{F8}$, F9, $\overline{F9}$, F10, $\overline{F10}$, F11, and $\overline{F11}$. The signals F6-F11 are channeled into a sequencer means such as the sequencer **108** which starts the motor **18** when any signal other than $\overline{(F6)\,(F7)\,(F8)\,(F9)\,(F10)\,(F11)}$ is sensed, such term being true only when the register **104** stores only zeros. All of the output signals of register **104** are channeled into a decoding means such as the character decode means **106**. The output signal of the sequencer **108** is connected to AND gate **102** to control the channeling of clock pulses from a timing means such as the clock **100** into a counter means such as the scale-of-seven counter **118**. When the desired character is completely printed, a "clear" signal is delivered from the sequencer **108** to clear the character register **104**.

The timing pulses delivered by clock **100**, through gate **102** to the scale-of-seven counter causes the scale-of-seven counter to index through its seven states.

The scale-of-seven counter **118** may, for example, comprise three flip flops producing outputs designated F0, $\overline{F0}$, F1, $\overline{F1}$, F2, $\overline{F2}$. Any seven states of these signals may be used as the outputs of the scale-of-seven counter **118**. For explanation purposes, as shown in FIG. 8, the following codes have been chosen as outputs of the counter **118**:

F0	F1	F2
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

The binary output **110** of the counter **118** is connected to reset counter **118** into its 000 state and to send a pulse to the scale-of-five counter **120**. Counters **118** and **120**, together, may be considered to be a counter means.

The scale-of-five counter **120** may, for example, comprise three flip flops producing outputs F3, $\overline{F3}$, F4, $\overline{F4}$, F5, $\overline{F5}$. Any five states of these signals may be used as the outputs of the scale-of-five counter **120**. For explanation purposes, as shown in FIG. 8, the following codes have been chosen as outputs of the counter **120**:

F3	F4	F5
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

The binary output **100** of counter **120** is connected to reset counter **120** into its 000 state.

The scale-of-seven counter **118** may be adapted, as in FIG. 4, to produce seven signals which are produced in ordered sequence in synchronism with the timing pulses of clock **100**. Alternatively, as shown in the specific embodiment of the timing decode gates of FIG. 8, the same signals may be produced in the timing decode gates **116** (also considered to be part of the counter means).

The timing decode gates **116** are adapted to produce thirty-five timed signals, distributed in sequence upon thirty-five conductors shown generally at **110**. That is, the first signal in the sequence is channeled to the first conductor, the second signal to the second conductor, and so on through the thirty-five signals and conductors.

The character decode means **106** is adapted to produce a signal on only one of the sixty-three conductors shown generally at **112**. That is, the presence of a signal upon a particular conductor of the set **112** acts as a command signal to the character forming gates **114** to control the particular sequence of signals produced by gates **114** to cause the infra-red emitters to produce a particular character upon tape **28** in the dot matrix shown in FIG. 3.

The combination of signals from conductors **110** and **112** causes a permanent storage means such as the character forming gates **114** to produce a timed sequence of signals such as that needed to form the character "2," i.e.: 11100101001001100100110010011000110.

The signals delivered by the scale-of-seven counter **118** (or alternatively by the timing decode gate **116**) to the distributing gates **60–72**, are connected so that the first timing signal in each set of seven sequenced timing signals is channeled to gate **72**, the second to gate **70**, the third to gate **68**, and the fourth, fifth, sixth, and seventh to gates **66**, **64**, **62**, and **60**, respectively.

The basic operation diagram is shown in FIG. 10. The apparatus of FIG. 4 first waits for data from the computer **75**. The data is placed into the register **104** and the motor **18** is started. After a short delay, caused by the sequencer **108**, signals are sent to the gate **102** (the motor **18** is then up to speed and running) to cause the circuitry to drive the infra-red emitters to print the desired character. When the print out of the character is complete, the register **104** is cleared by the sequencer **108** and the apparatus again waits for data from the computer **75**.

Referring now to FIG. 6, there is shown a typical sequencer **108**. In sequencer **108**, the JK flip flops **304** and **310** have outputs which, for convenience, are designated F12, $\overline{F12}$, F13, $\overline{F13}$. The presence of a signal on the "J" input of flip flop **304** sets flip flop **304** into its F12 state (i.e. F12 true and $\overline{F12}$ false). The presence of a signal on the "K" input sets flip flop **304** into its $\overline{F12}$ state. Similarly, the presence of a signal on the "J" input of flip flop **310** sets that flip flop into its F13 state. A signal on the "K" input sets the flip flop into its $\overline{F13}$ state.

The F6–F11 signals from the register **104** are connected to the input terminals of an OR gate **300**. The output of gate **300** is connected through AND gate **302** to the "J" input of flip flop **304**. The "K" input of flip flop **304** is connected to AND gate **340** which has a true output when the end of a matrix scan is reached.

The F12 output of flip flop **304** is connected to the input of AND gate **102**, to amplifier **306**, and through time delay means **308** to the "J" input of flip flop **310**. The $\overline{F12}$ output of flip flop **304** is connected to the inputs of AND gates **302** and **314**, and through time delay means **312** to the "K" input of flip flop **310**.

The F13 output of flip flop **310** is connected to the inputs of AND gates **102** and **314**. The $\overline{F13}$ output of flip flop **310** is connected to the input of gate **302**.

When the register **104** is set into any condition except 000000, the gate **300** delivers a signal to gate **302**. Provided the flip flops are in their zero or false state, i.e. provided $\overline{F12}$ and $\overline{F13}$ signals exist, the gate **302** delivers a signal to the J input of flip flop **304** setting it into its one or true state, i.e. an F12 signal is produced.

The production of an F12 signal causes the motor **18** to be actuated by the amplifier **306**. After a short delay, by means **308**, to allow the motor to accelerate, the F12 signal appears on the J input of flip flop **310** which sets flip flop **310** into its F13 state. With flip flops **304** and **310** producing signals F12 and F13, gate **102** is opened to allow timing signals from clock **100** to be channeled to counter **118**. When thirty-five pulses have been delivered by clock **100** to register **118**, a signal appears on AND gate **340** which sets flip flop **304** into its $\overline{F12}$ state.

The setting of flip flop **304** into its $\overline{F12}$ state causes gate **314** (because an F13 signal is still present) to deliver a clearing signal to register **104**.

After a short delay to allow the clearing signal, time delay means **312** allows the $\overline{F12}$ signal to reset flip flop **310** into its $\overline{F13}$ state. The sequencer **108** is then ready to receive the next signal from register **104** and to repeat the operation.

A typical character decode means **106** is shown in FIG. 7. In FIG. 7, eight AND gates, shown at **320**, are each adapted to receive three inputs of different permutations of F6 or $\overline{F6}$, F7 or$\overline{F7}$, and F8 or $\overline{F8}$. Thus the gates **320**, from left to right in FIG. 7 are responsive, respectively to the following inputs

F6	F7	F8
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

The eight AND gates, shown at **322**, are each adapted to receive three inputs of different permutations of F9 or $\overline{F9}$, F10 or $\overline{F10}$, F11 or $\overline{F11}$. Thus the gates **322**, from bottom to top in FIG. 7, are responsive, respectively to the following inputs:

F9	F10	F11
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

The output of each of gates **320**, except the gate having input signals $\overline{(F6)}$ $\overline{(F7)}$ $\overline{(F8)}$, is connected to eight AND gates of a matrix **324** of sixty-three AND gates. Each of the eight AND gates also has connected to its input terminals an output connection of a different one of the eight gates in the set **322**. The left hand gate of gates **320**, having input signals $\overline{(F6)}$ $\overline{(F7)}$ $\overline{(F8)}$, is connected to

seven AND gates of the matrix **324**. Each of the seven AND gates also has connected to its input terminals an output connection of a different one of the set for gates **322**, except for the bottom gate which has input signals $\overline{(F9)}$ $\overline{(F10)}$ $\overline{(F11)}$. Thus for each combination of F6 or $\overline{F6}$, F7 or $\overline{F7}$, F8 or $\overline{F8}$, F9 or $\overline{F9}$, F10 or $\overline{F10}$, F11 or $\overline{F11}$, except $\overline{(F6)}$ $\overline{(F7)}$ $\overline{(F8)}$ $\overline{(F9)}$ $\overline{(F10)}$ $\overline{(F11)}$, there exists an AND gate in the matrix **324** which produces a signal. For any particular signal on register **104**, except 000000, there is one and only one of the conductors **112** energized.

A typical timing decode gate matrix **116** is shown in FIG. 8. In FIG. 8, seven AND gates, shown at **330**, are each adapted to receive three inputs of different permutations of F0 or $\overline{F0}$, F1 or $\overline{F1}$, F2 or $\overline{F2}$. The gates **330**, from left to right in FIG. 8, are responsive respectively to the following inputs:

F0	F1	F2
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

The five AND gates, shown at **332**, are each adapted to receive three inputs of different permutations of F3 or $\overline{F3}$, F4 or $\overline{F4}$, F5 or $\overline{F5}$. The gates **332**, from top to bottom in FIG. 8, are responsive, respectively, to the following inputs:

F3	F4	F5
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

The output of each of the gates **330** is connected to five AND gates of a matrix **334** of thirty-five AND gates. Each of the five AND gates also has connected to its input terminals an output connection of a different one of the five gates in the set **332**. Thus for each combination of F0 or $\overline{F0}$, F1 or $\overline{F1}$, F2 or $\overline{F2}$, F3 or $\overline{F3}$, F4 or $\overline{F4}$, F5 or $\overline{F5}$ (except those of the form 111xxx, xxx101, xxx110, and xxx111, where "x" is a "1" or "0") there exists an AND gate in the matrix **334** which produces a signal. The outputs of the matrix **334** are thirty-five conductors **110**. The thirty-five conductors **110** are consecutively energized in synchronism with the clock pulses delivered from clock **100**.

It is apparent that the gates **330** could have been part of the scale-of-seven counter **118**, with the outputs of gates **330** connected, respectively, to the gates **60–72** (FIG. 4).

It is also apparent that the gates **332** could have been part of the scale-of-five counter **120**. Instead of connecting the counters **118** and **120** with an AND gate **119** (see FIG. 6), the output of the right hand gate of gates **330** could have delivered pulses to counter **120**.

A typical character forming gate circuit **114** is shown in FIG. 9. In FIG. 9, the conductors **110** are displayed or ordered so that the conductor receiving the first timing pulse is at the top, the conductor receiving the second pulse is next, and so on down the column of conductors until the last conductor receives the last pulse.

Only a single conductor **341** of the conductors **112** is shown, carrying a control signal to print out the character "2." The first conductor **340** of conductor set **110** is connected to an AND gate **342**. The gate **342** is also connected to the conductor **341** of the set of conductors **112**. The conductor **341** is also connected to other AND gates shown generally at **344**. The set of gates **344** has a number of gates equal to the number of dots in the character "2." The gates of the set **344** are connected to the sequentially pulsed conductors **110** so that a pulse is delivered at the proper time to cause the infra-red emitters to print out the dots of the character "2."

The outputs of the gates **344** are connected to a bank of OR gates **346** so that whenever one of the gates **344** is energized, a signal appears at the output terminal **348**.

Each of the other conductors (not shown) of the set of conductors **112** is typically connected to a set of gates similar to the set **344**. The number of gates in a particular set depends upon the number of dots of the character to be printed out. The conductors of set **110** corresponding to the time-sequenced dot positions in the particular chosen character to be printed are connected to the AND gates.

It is apparent that other gate configurations could be used to reduce the number of gates.

It is also apparent that should there be dot positions in the dot matrix described in connection with FIG. 3 which are never printed, the particular conductors of set **110** corresponding to those dot positions may be omitted.

An alternative embodiment of the invention which is adapted to receive dot commands, for example, over a communication channel or link **128** is shown in FIG. 5. The particular circuit of FIG. 5 is adapted to receive print out commands from a frequency-shift-keying modulated signal. The frequency-shift-keying (FSK) signal comprises signals of two frequencies, *f*1 and *f*2. In the shown embodiment, a frequency of *f*2 corresponds to a command to print out a dot. A frequency of *f*1 corresponds to a command not to print out a dot. The communication link may comprise a radio link, or an audio link. The signal may be an amplitude modulated signal, a pulse width modulated signal, a frequency modulated signal, a pulse amplitude modulated signal, a pulse code modulated signal, or any other signal carrying the required information in FSK form.

The communication link **128** is connected to two filters **129** and **131** to separate the f2 and f1 signals. The filters transmit signals to the detectors **130** and **132** which change the signals into substantially constant amplitude signals (of short duration, i.e. a pulse). The outputs of both detectors **130** and **132** are connected to an AND gate whose output is connected to control a monostable multivibrator and to reset counter **138** into its "zero" condition. The reception of a signal having both f1 and f2 components at the beginning of a character, triggers the multivibrator, sending a pulse to the motor **18** of sufficient time duration to allow the dot matrix to be printed out. The outputs of detectors **130** and **132** are connected to the inputs of the OR gate **136** whose output drives the scale-of-seven counter **138**. Thus whenever a signal f2 (for a dot) or f1 (to skip a dot) are received, the counter **138** indexes. The output of detector **130** is connected to the inputs of distributing gates **60–72** to print a dot. The scale-of-seven counter **138** energizes only one of the gates **60–72** at a time in the sequence **72, 70, 68, 66, 64, 62, 60, 72, . . .**

Thus, when both f1 and f2 are simultaneously received, the motor **18** is started and the counter **138** is reset. The next signals received index the counter, and if they are f2 signals, they command the particular gate which is momentarily energized by counter **118** to send a signal to its infra-red emitting device to print out a dot.

It should be noted that variations of this embodiment are practical and contemplated by this invention. For example, counter **138** may be reset by the absence of both F1 and F2, and the motor **18** may be driven if either F1 or F2 is present. This could be accomplished by changing gate **134** to a NOR gate and constructing the mono-

stable multivibrator **140** so that it is triggered by the transition from true to false of the output of gate **134**.

In summary, the device of this invention is a printer using highly efficient infra-red emitters producing a maximum of radiation with little retained heat, whereby long life is assured. The emitters have insignificant thermal inertia, whereby they may rapidly be pulsed. Because of the concentrated power in the short-duration beams, low energy is required. Further, the emitters match the voltages and currents of transistorized or solid state driving circuitry.

There has also been provided by this invention, particular combinations of driving circuitry which are particularly adapted for driving the infra-red emitters.

What is claimed is:

1. In combination:

a movable strip of heat-sensitive material;

a plurality of infra-red emitters, adapted to emit infra-red radiation;

means for directing infra-red radiation from said emitters onto predetermined portions of said material;

emitter energizing means responsive to control signals, for energizing said emitters in a predetermined manner, said emitter energizing means comprising;

means for receiving and storing said control signals;

means for storing character programs;

means for converting said stored control signal into a command signal adapted to extract a predetermined character signal sequence from said permanent storage means;

timing means;

distributing means, connected to receive said character signal sequence and to deliver said signals to said emitters;

means connected to receive signals from said timing means and to deliver signals to said permanent storage means to time the production of said character signal sequence, and to said distributing means to distribute said character signal sequence consecutively, in predetermined order to said emitters; and

motor means responsive to said emitter energizing means for driving said material in synchronism with the energizing of said emitters to print out characters upon said material in response to said control signals.

2. In combination:

a movable strip of heat-sensitive material;

a plurality of infra-red emitters, adapted to emit substantially monochromatic infra-red radiation, arranged in a row which is tilted from a direction normal to the direction of motion of said material, toward said direction of motion;

means for directing infra-red radiation from said emitters onto predetermined portions of said material;

emitter energizing means responsive to control signals, for consecutively energizing said emitters in a predetermined sequence, said emitter energizing means comprising;

register means for receiving and storing said control signals;

permanent storage means for storing character programs;

decoding means for converting said stored control signal into a command signal adapted to extract a predetermined character signal sequence from said permanent storage means;

timing means;

distributing means, connected to receive said character signal sequence and to deliver said signals to said emitters;

counter means, connected to receive signals from said timing means and to deliver signals to said permanent storage means to time the production of said character signal sequence, and to said distributing means to distribute said character signal sequence consecutively, in predetermined order to said emitters; and

motor means responsive to said emitter energizing means for driving said material in synchronism with the energizing of said emitters to print out characters upon said material in response to said control signals.

3. Apparatus according to claim **2** and further comprising:

sequencer means, connected to receive signals from said register means to start said motor means, to delay delivery of said timing signals, and to reset said register means into a state ready to receive a new control signal.

4. Apparatus according to claim **3** in which:

said permanent storage means comprises a plurality of character forming gates responsive to predetermined ones of signals from said timing means, and responsive to command signals from said decoding means.

5. Apparatus according to claim **3** in which:

said decoding means comprises a gate matrix adapted to receive binary signals from said register means and to produce a signal upon a unique output conductor for predetermined ones of the binary combinations received.

6. Apparatus according to claim **3** in which:

said timing means comprises a gated clock.

7. Apparatus according to claim **3** in which:

said distributing means comprises a plurality of distributing gates, connected to receive signals from said permanent storage means, and from said counter means to distribute said signals from said storage means to said emitters in response to said signals from said counter means.

8. Apparatus according to claim **3** in which:

said counter means comprises a counter, and a plurality of timing decode gates arranged to deliver signals in sequence to a first plurality of conductors connected to said permanent storage means, and to deliver signals in sequence to a second plurality of conductors connected to said distributing means.

9. Apparatus according to claim **3** in which:

said sequencer means comprises a pair of JK flip flops, the first said flip-flop being responsive to a non-zero signal in said register means to produce a signal to start said motor means, the second said flip-flop being responsive to a delayed signal from said first flip flop to gate pulses from said timing means to said counter means, said first flip flop being responsive to said counter means to reset at the end of the count of said counter and to deliver a reset signal to said register means and a delayed reset signal to said second flip flop.

10. In combination:

a movable strip of heat-sensitive material;

a plurality of infra-red emitters, adapted to emit infra-red radiation, arranged in a row which is tilted from a direction normal to the direction of motion of said material, toward said direction of motion;

means for directing infra-red radiation from said emitters onto predetermined portions of said material;

means, responsive to control signals, for consecutively energizing said emitters in a predetermined sequence; and

motor means responsive to said means responsive to control signals for driving said material in synchronism with the energizing of said emitters to print out characters upon said material in response to said control signals,

said means responsive to control signals comprising:

means for separating control signals of a first frequency from control signals of a second frequency;

detector means for detecting said first and second frequencies and for producing first and second detected

signals indicative of the presence of said first and second frequencies, respectively;

counter means, connected to be reset to its initial condition by signals chosen from the class consisting of the simultaneous reception of both said detected signals, and of the absence of reception of either of said detected signals, and connected to count upon reception of only one of said detected signals;

a monostable multivibrator, connected to be actuated by signals chosen from the class consisting of the simultaneous reception of both said detected signals, and of the reception of the first of a group of said detected signals, and connected to deliver an energizing signal to said motor means, the dwell time of said multivibrator in its unstable condition being predetermined to allow complete print out of one character; and

a plurality of distributing AND gates, connected to receive a predetermined one of said detected signals, and connected so that said gates are consecutively gated by said counter means, said distributing gates channeling signals to said infra-red emitters.

11. Apparatus according to claim **10** and further comprising:

a communication link, connected to receive said control signals and to deliver them to said means for separating control signals, and adapted to transmit frequency-shift-keying signals.

12. Apparatus according to claim **11** in which said means for separating control signals comprises:

a first and a second filter, connected to receive signals from said communication link and to deliver signals to said first and second detector means, respectively.

13. Apparatus according to claim **12** in which:

said detected signals are channeled through an AND gate to the input terminal of said multivibrator and to the reset terminal of said counter means;

and in which said detected signals are channeled through an OR gate to the counting terminal of said counter means.

14. Apparatus according to claim **13** in which said counter means is a scale-of-seven counter, said distributing gates are seven in number, a signal is delivered by said counter to a different said distributing gate for each condition of said counter, and said predetermined one of said detected signals is channeled to all of said distributing gates.

15. Apparatus according to claim **12** in which:

said detected signals are channeled through a NOR gate to the input terminal of said multivibrator and to the reset terminal of said counter means, said multivibrator being responsive to be triggered by the transition from true to false by the output signal of said NOR gate; and in which said detected signals are channeled through an OR gate to the counting terminal of said counter means.

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U.S. Cl. X.R.

178—30; 250—65