

[54] ELECTRICAL FUEL CONTROL SYSTEM FOR INTERNAL COMBUSTION ENGINES

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[73] Assignee: **Nippondenso Kabushiki Kaisha**, Kariya-shi, Japan

[22] Filed: **Jan. 26, 1973**

[21] Appl. No.: **327,603**

Related U.S. Application Data

[63] Continuation of Ser. No. 126,830, March 22, 1971, abandoned.

[30] Foreign Application Priority Data

Mar. 26, 1970	Japan.....	45-25681
Apr. 7, 1970	Japan.....	45-29684
Apr. 10, 1970	Japan.....	45-30951
Apr. 15, 1970	Japan.....	45-32103
Apr. 15, 1970	Japan.....	45-32106
Apr. 22, 1970	Japan.....	45-34606

[52] U.S. Cl. **235/150.21**, 123/32 EA, 235/150.1, 235/150.53, 235/164

[51] Int. Cl. **F02d 5/00**, F02d 37/02, G05b 15/02

[58] Field of Search..... 235/150.21, 150.1, 151, 235/151.1; 123/32 EA

[56] References Cited

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Williams: Electronic Fuel Injection Reduces Automotive Pollution. Electronics Sept. 1972 Vol. 45 No. 19, p. 121-125.

Primary Examiner—Felix D. Gruber

Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57]

ABSTRACT

An electrical fuel control system for internal combustion engines, wherein various data representing the operating conditions of an internal combustion engine are converted into digital signals which are operated on to generate such fuel controlling signals that suit the required characteristics of the engine, whereby the quantity of fuel injected as well as the spark timing are controlled to ensure the optimum amount of fuel injected and the optimum spark timing.

7 Claims, 88 Drawing Figures

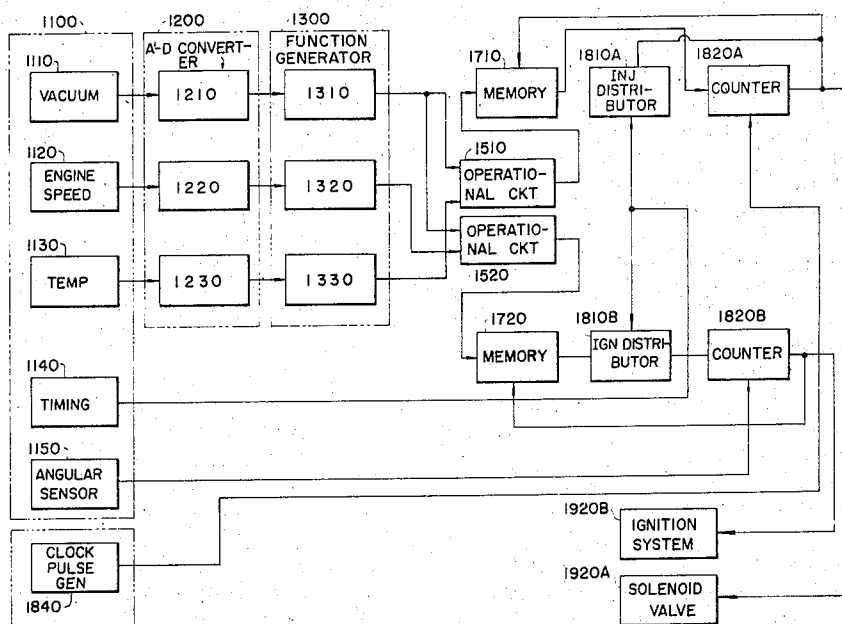
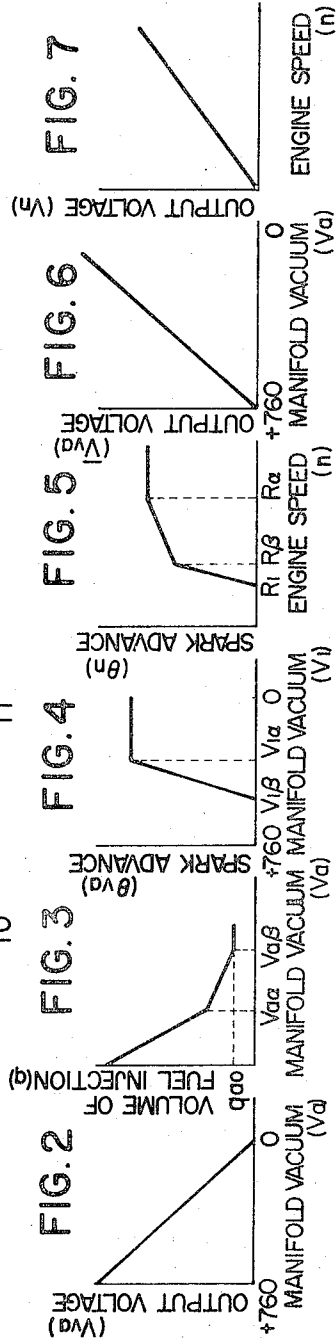
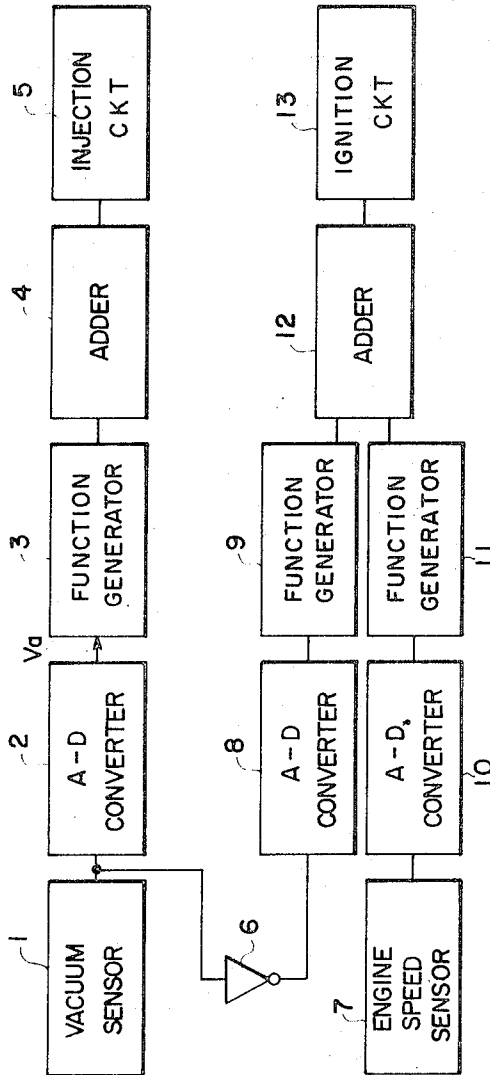


FIG. 1

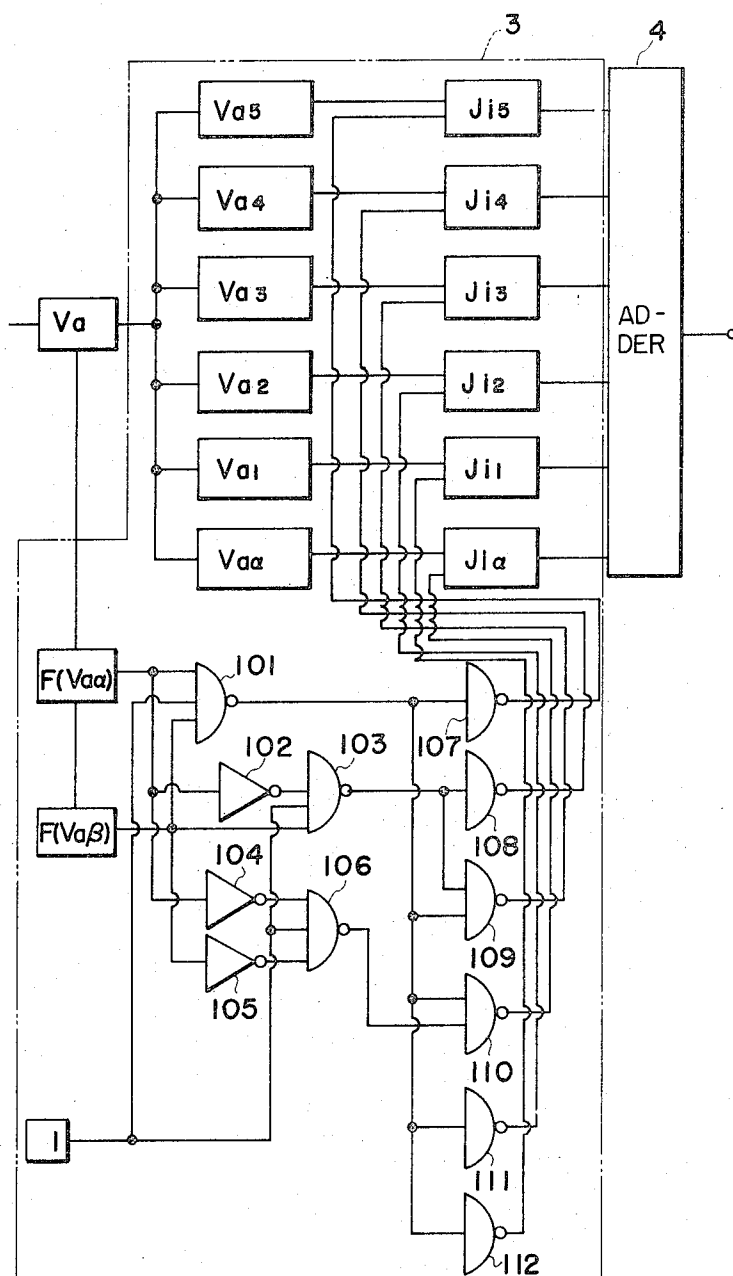


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FIG. 8

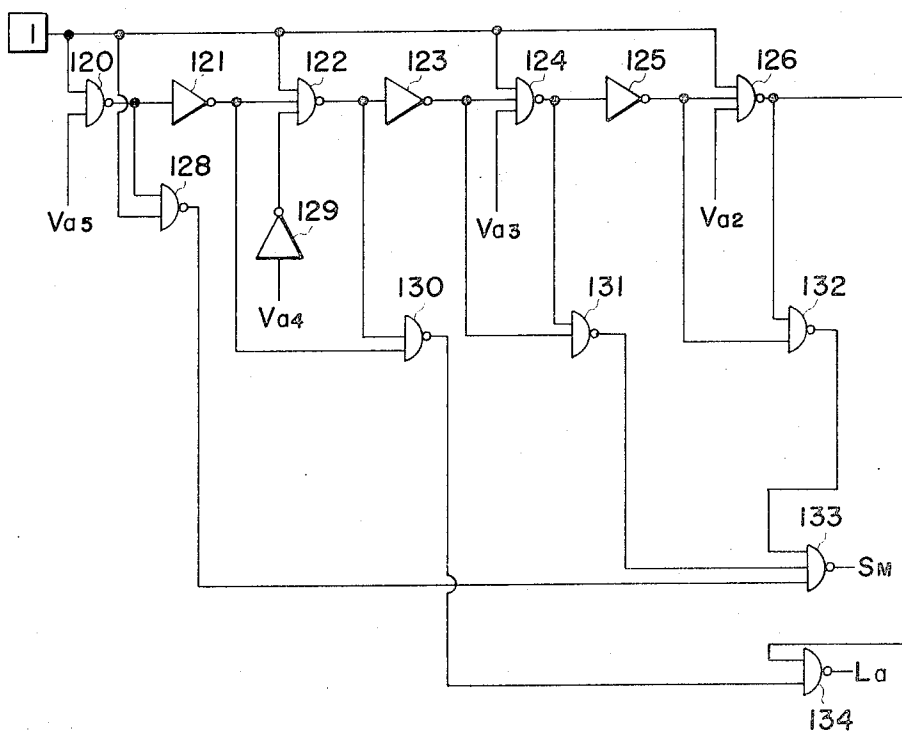


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FIG. 9

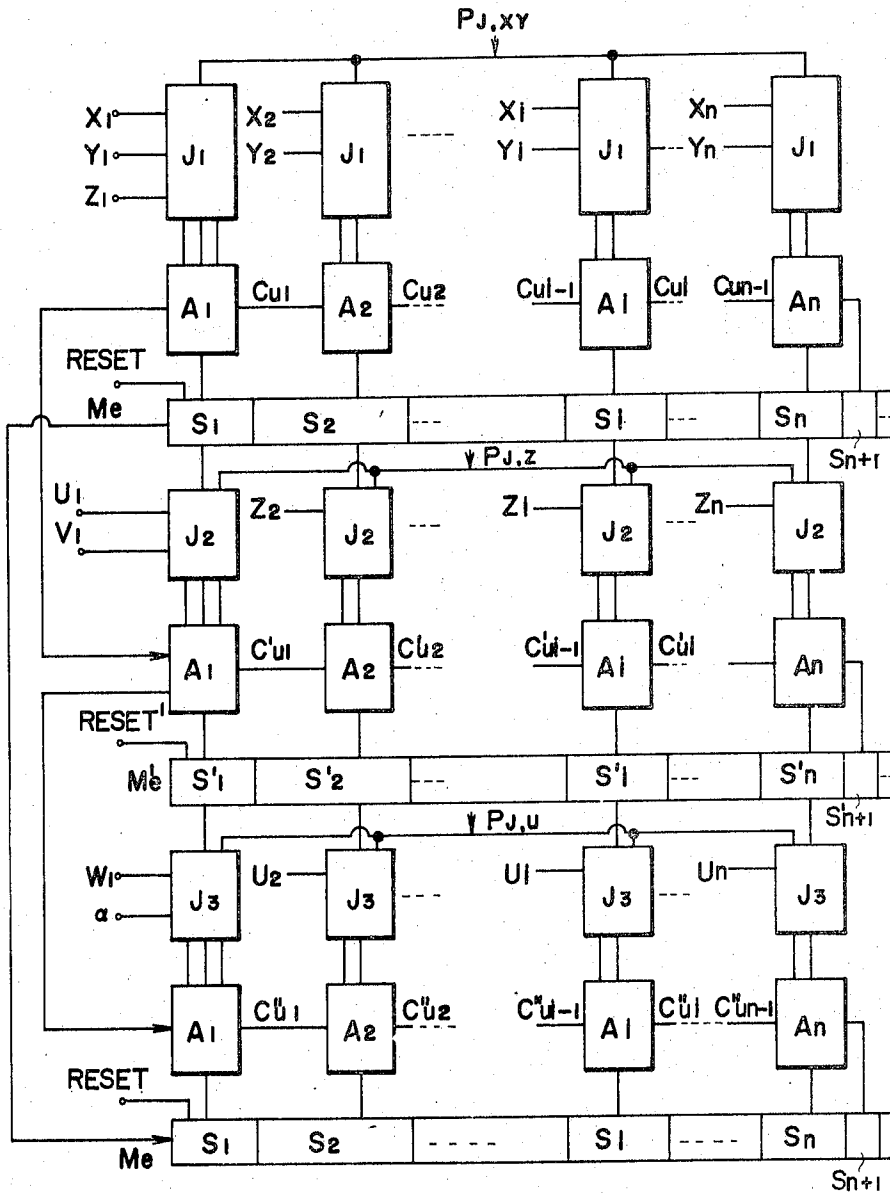


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FIG. 10



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FIG. 11

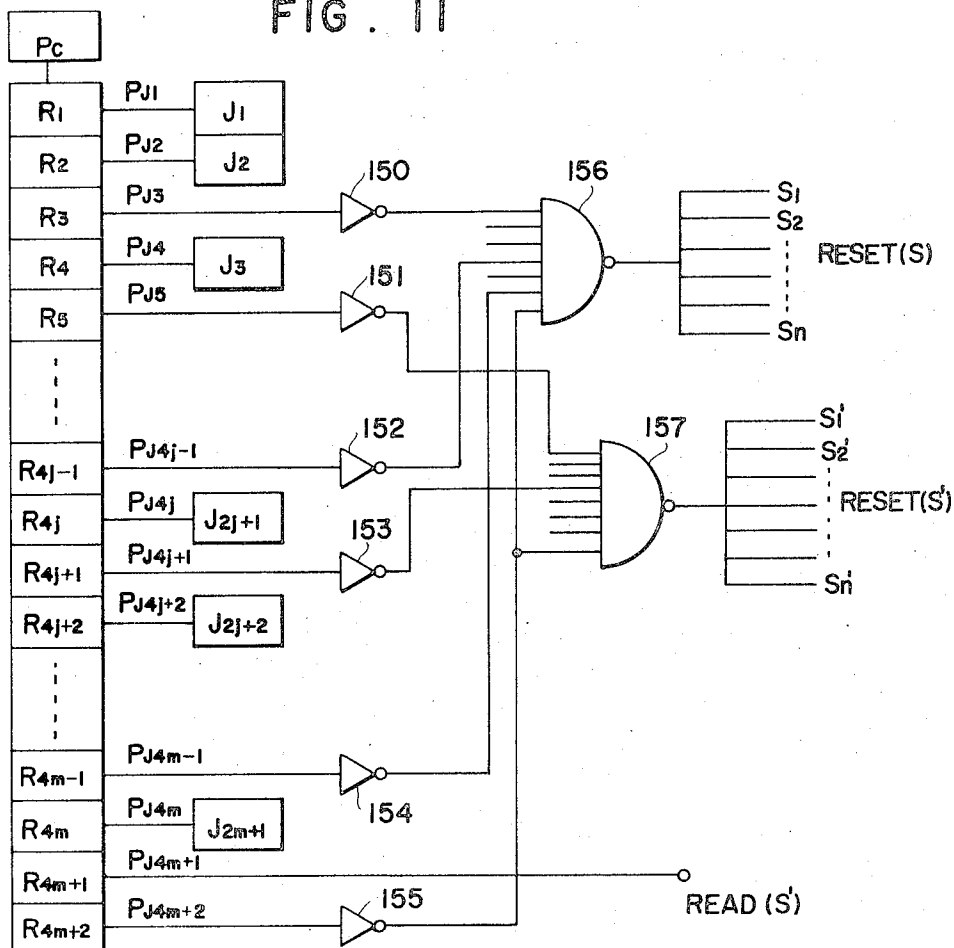
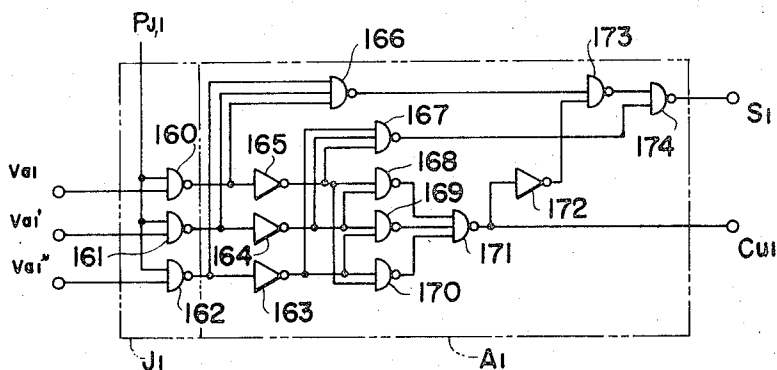


FIG. 12

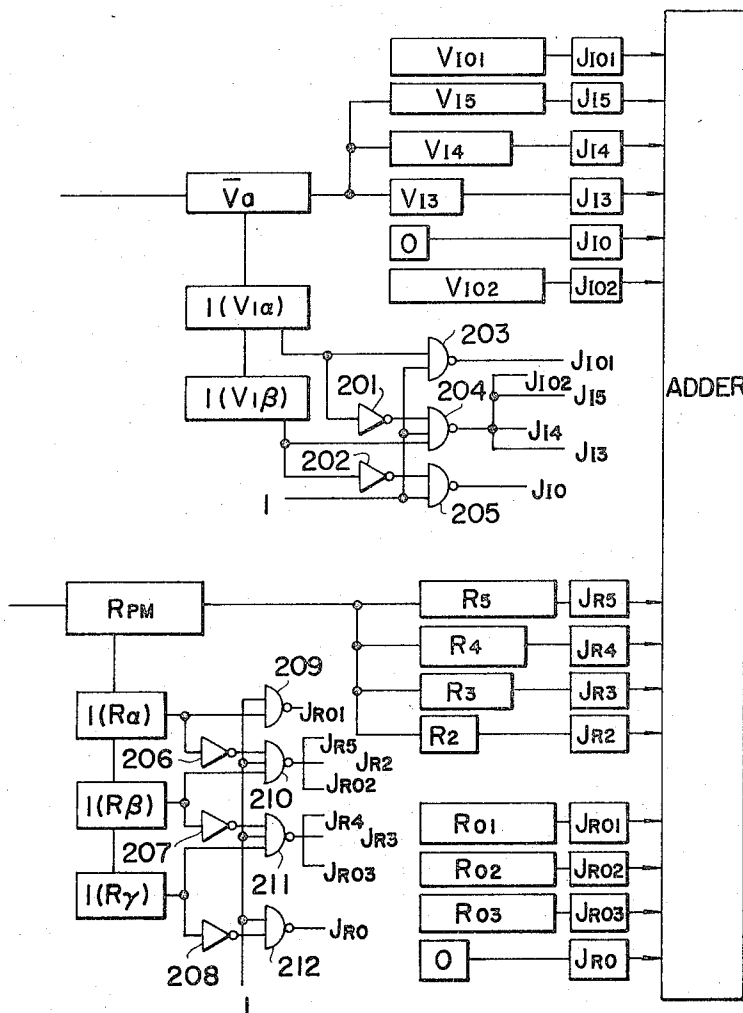


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FIG. 13

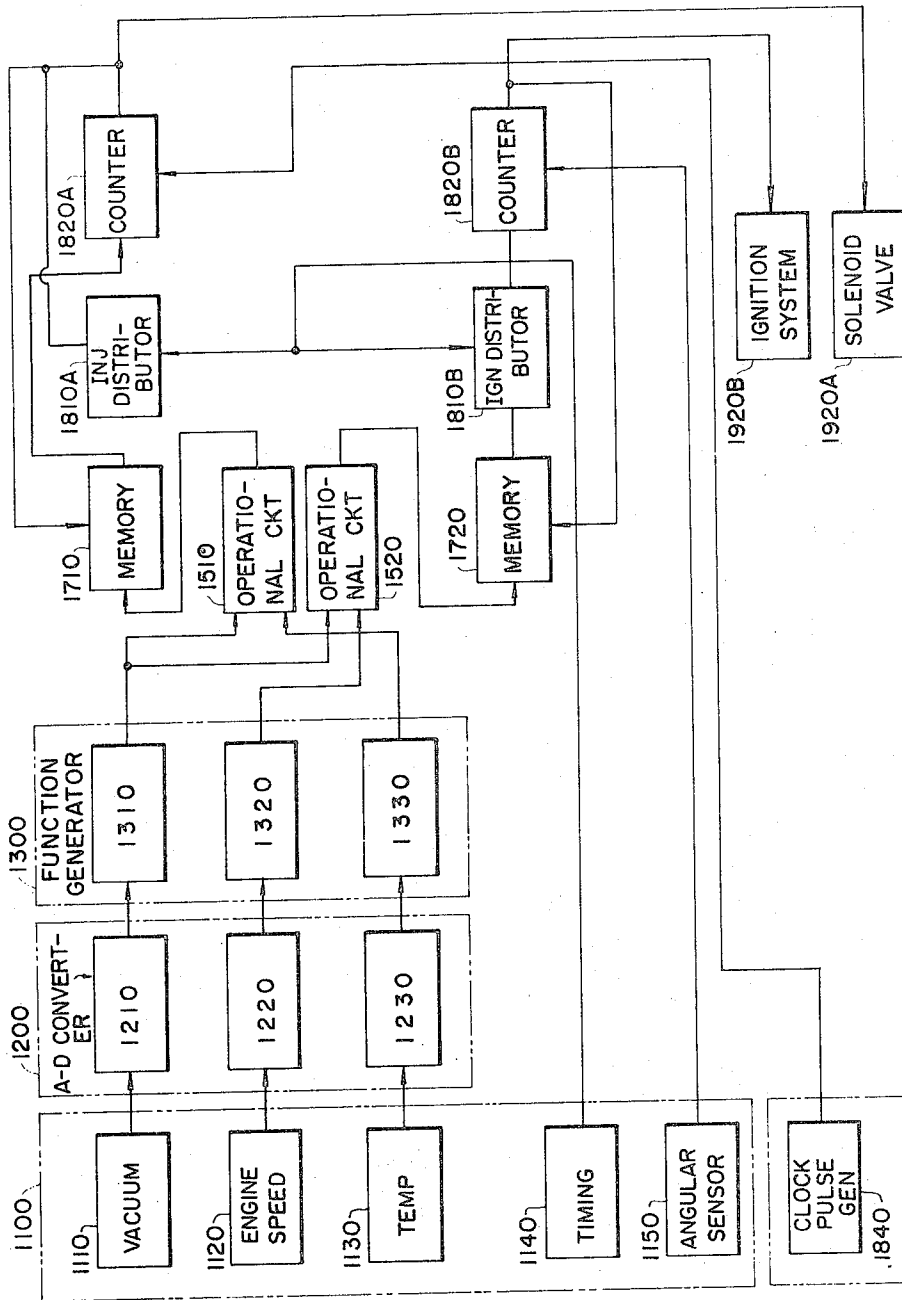


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FIG. 14

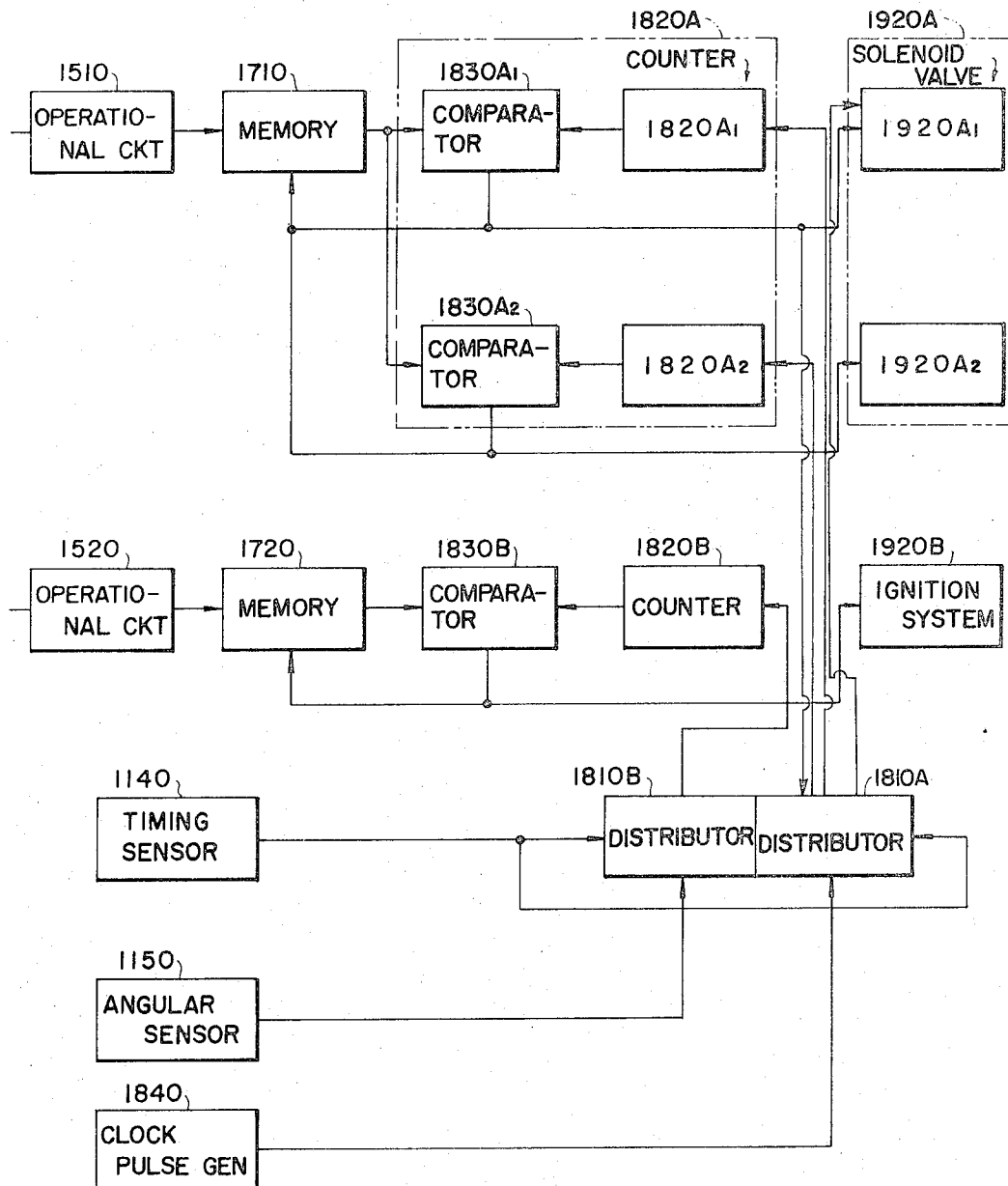


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FIG. 15

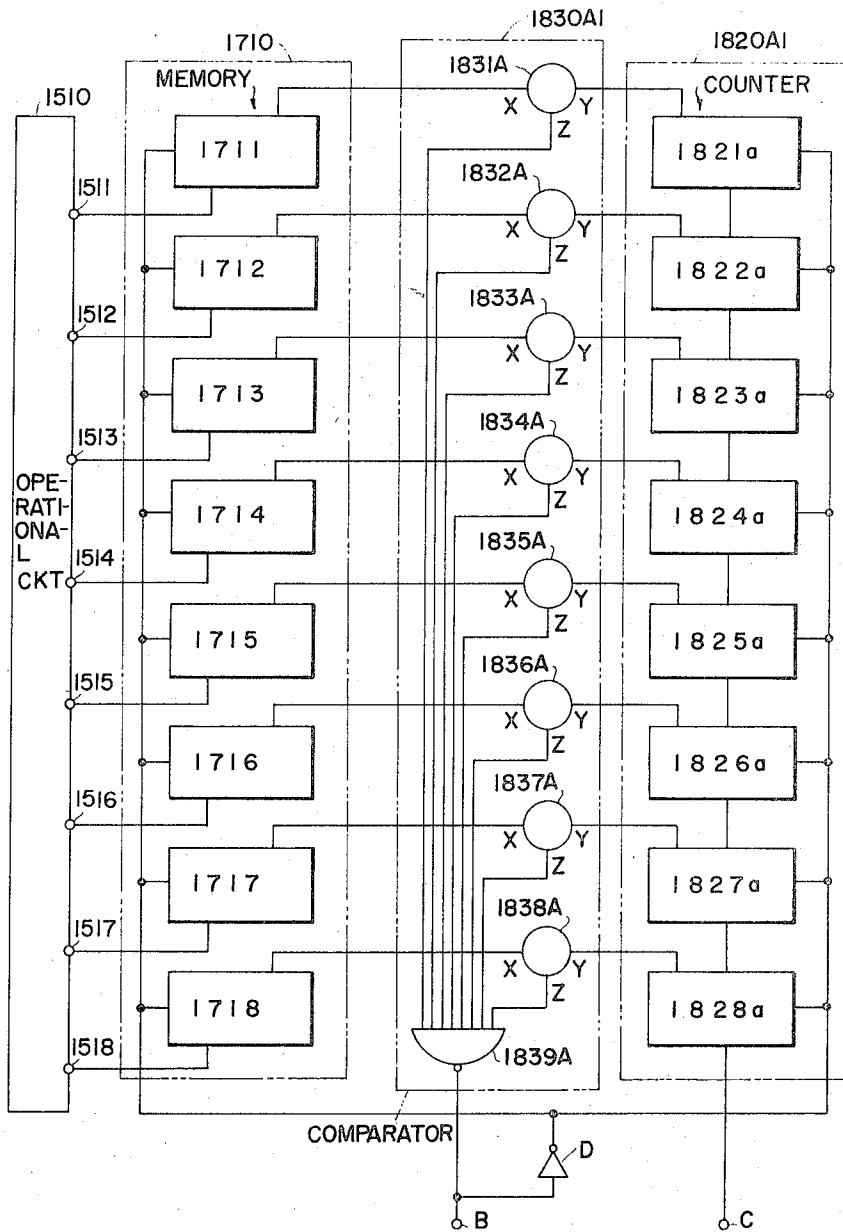


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FIG. 16



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FIG. 17

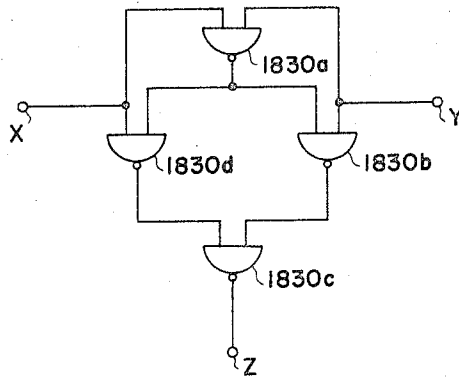


FIG. 18

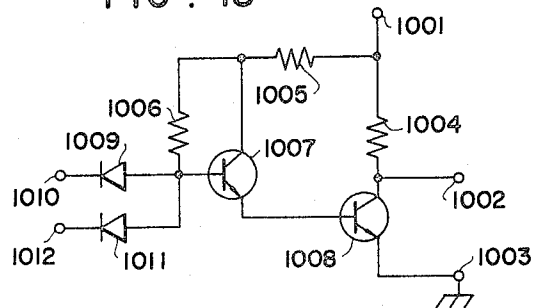
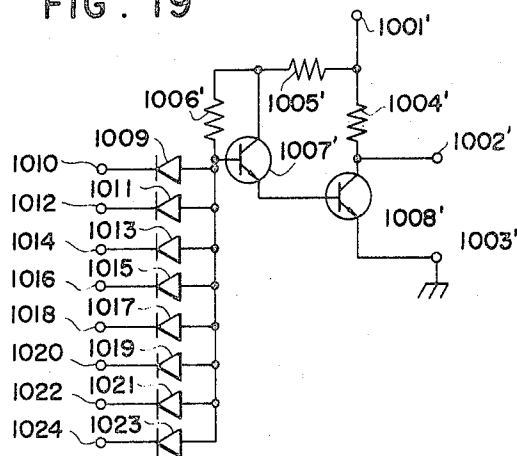


FIG. 19



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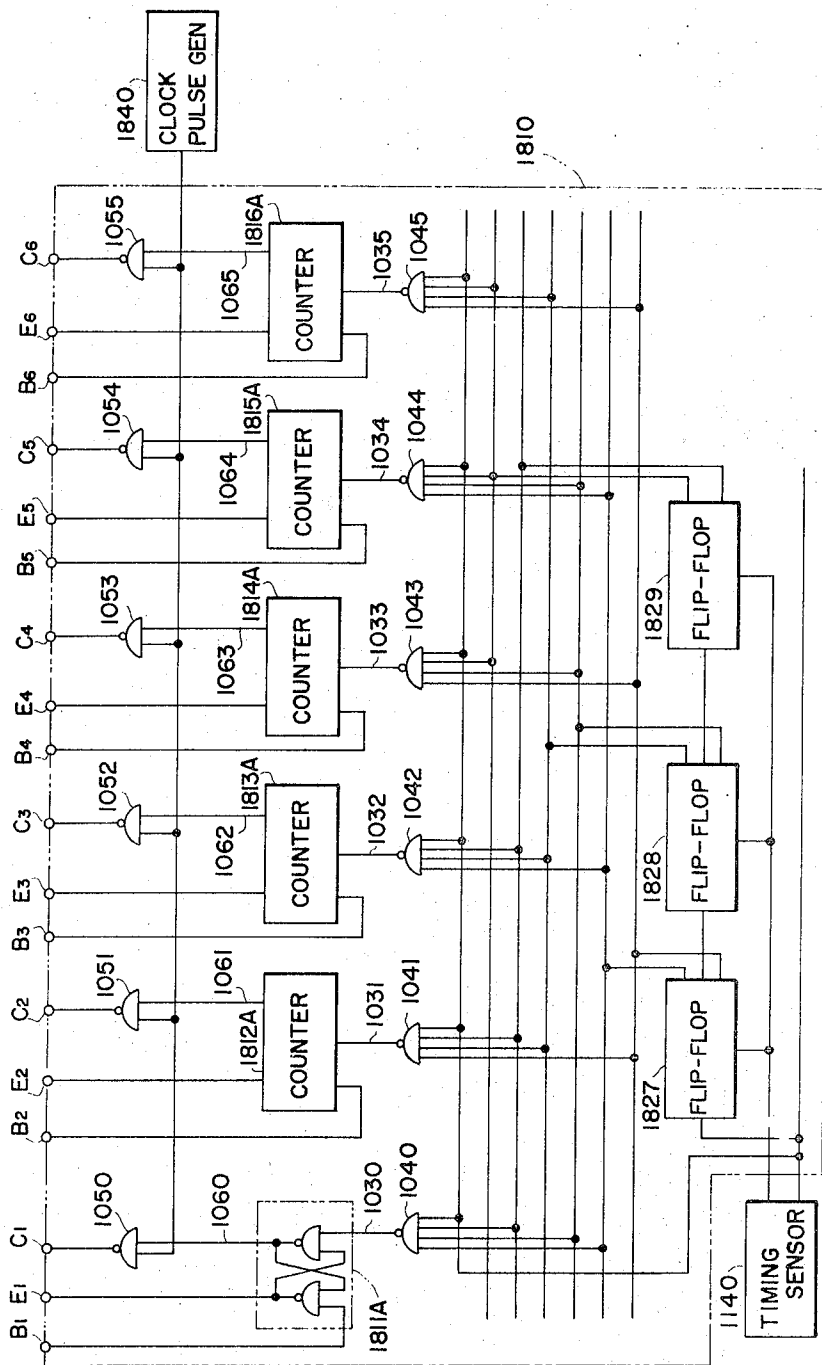
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FIG. 20



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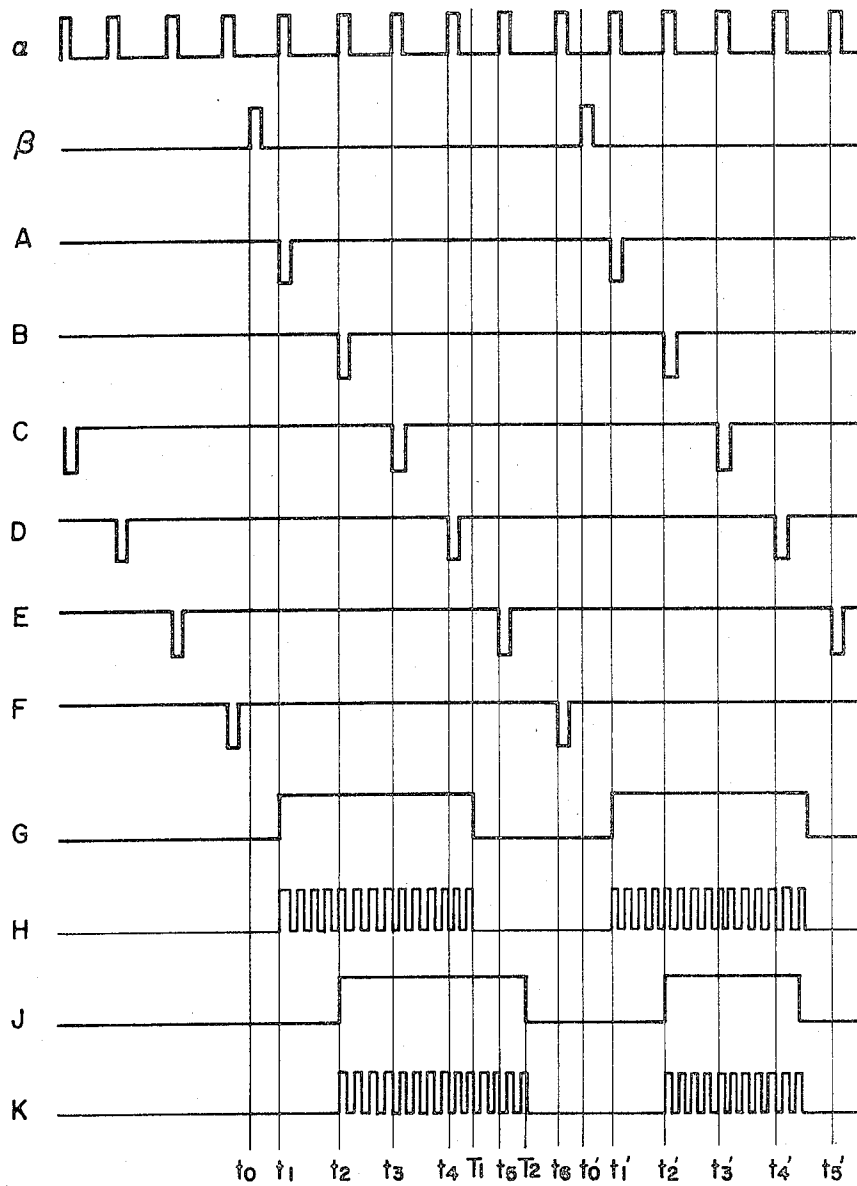
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FIG. 21

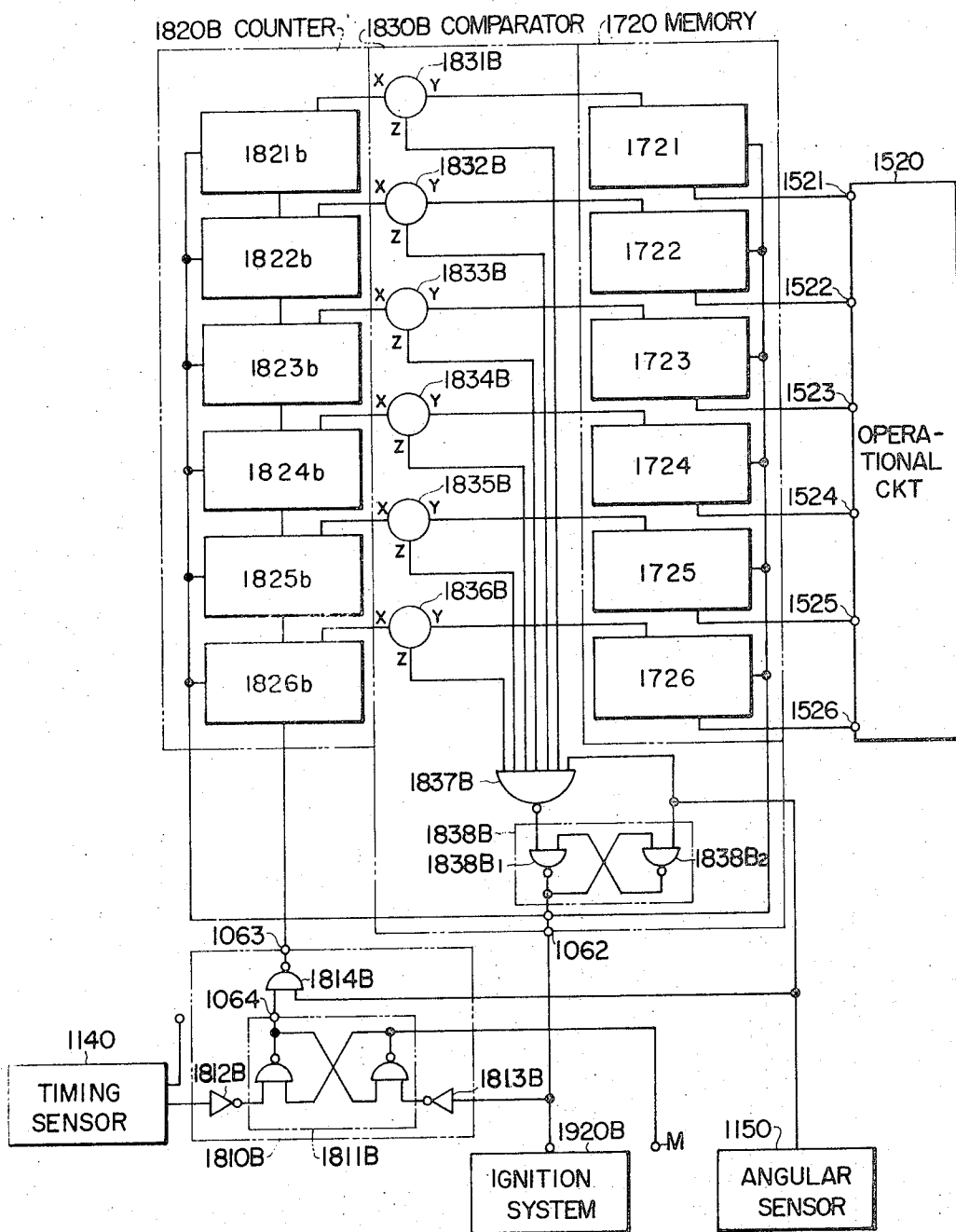


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FIG. 22

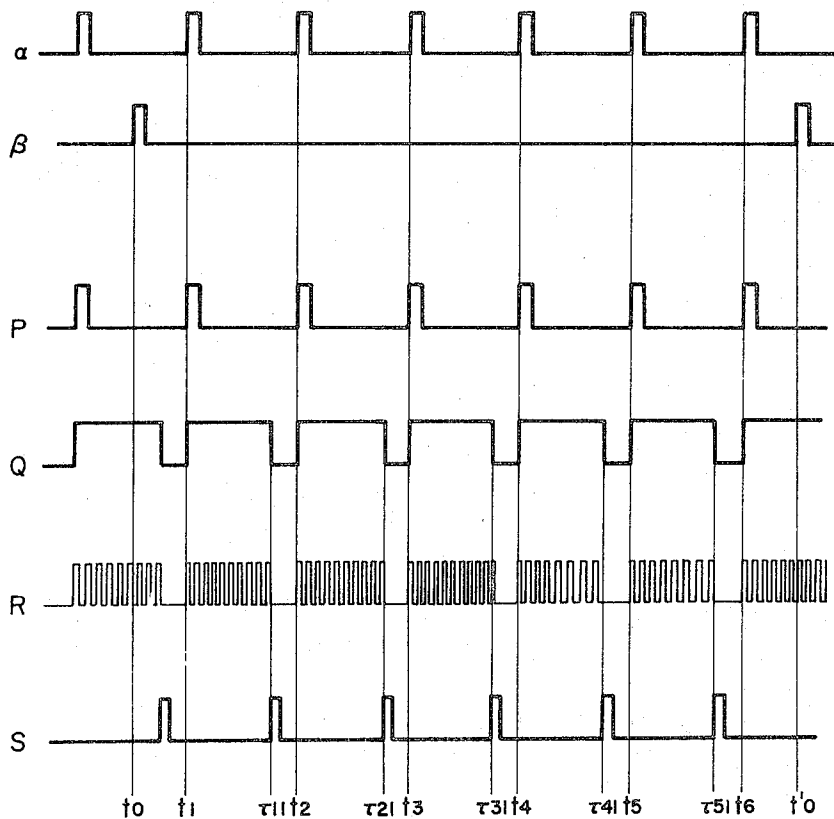


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FIG. 23

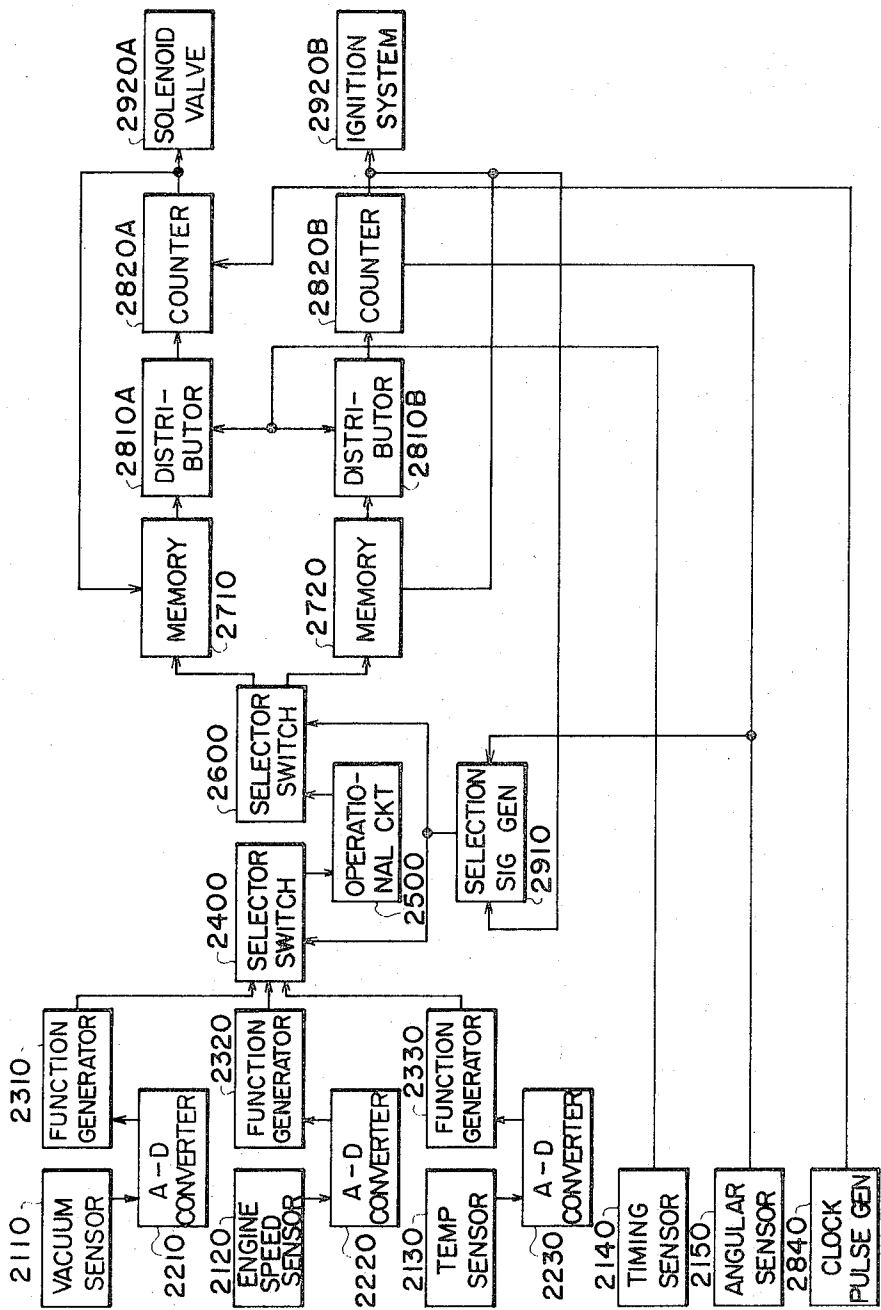


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FIG. 24

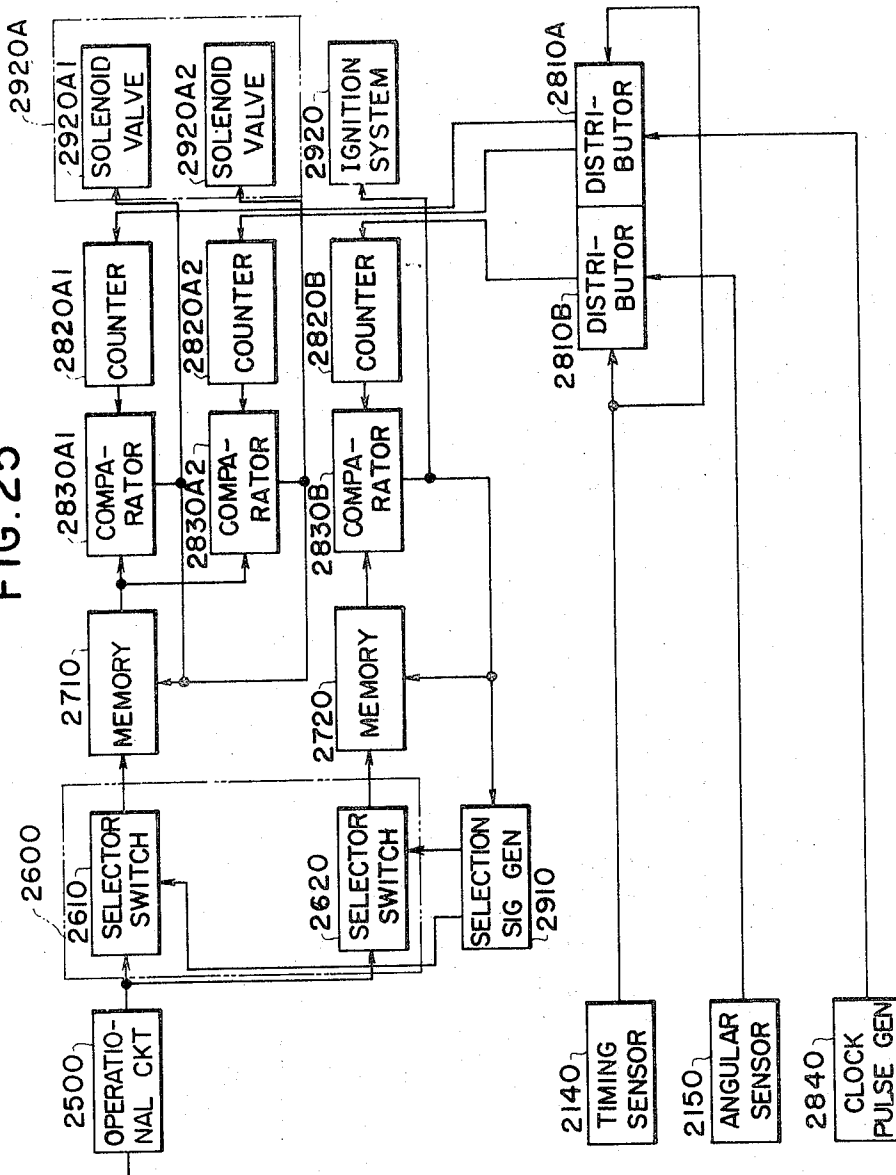


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FIG. 25



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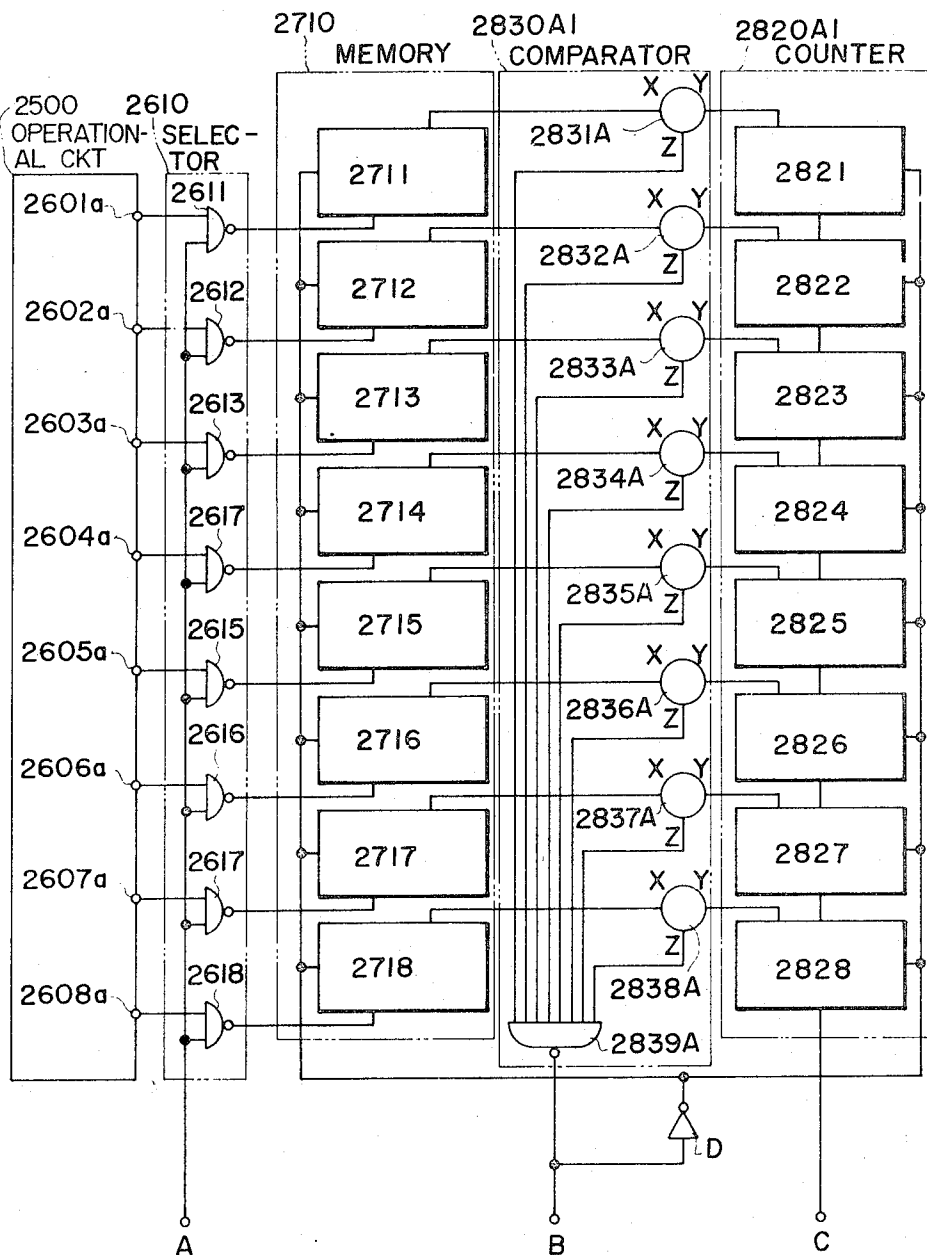
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Kazuo Ishii

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FIG. 26

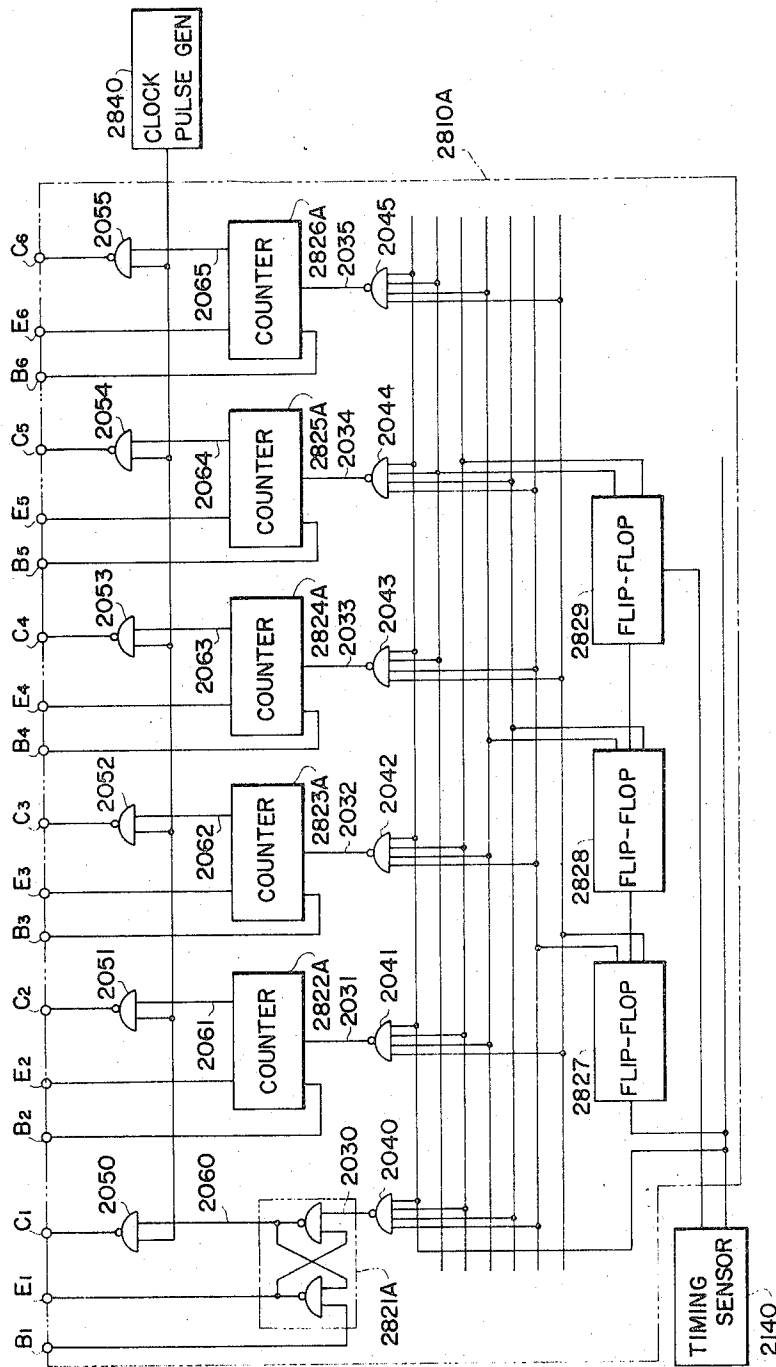


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FIG. 27

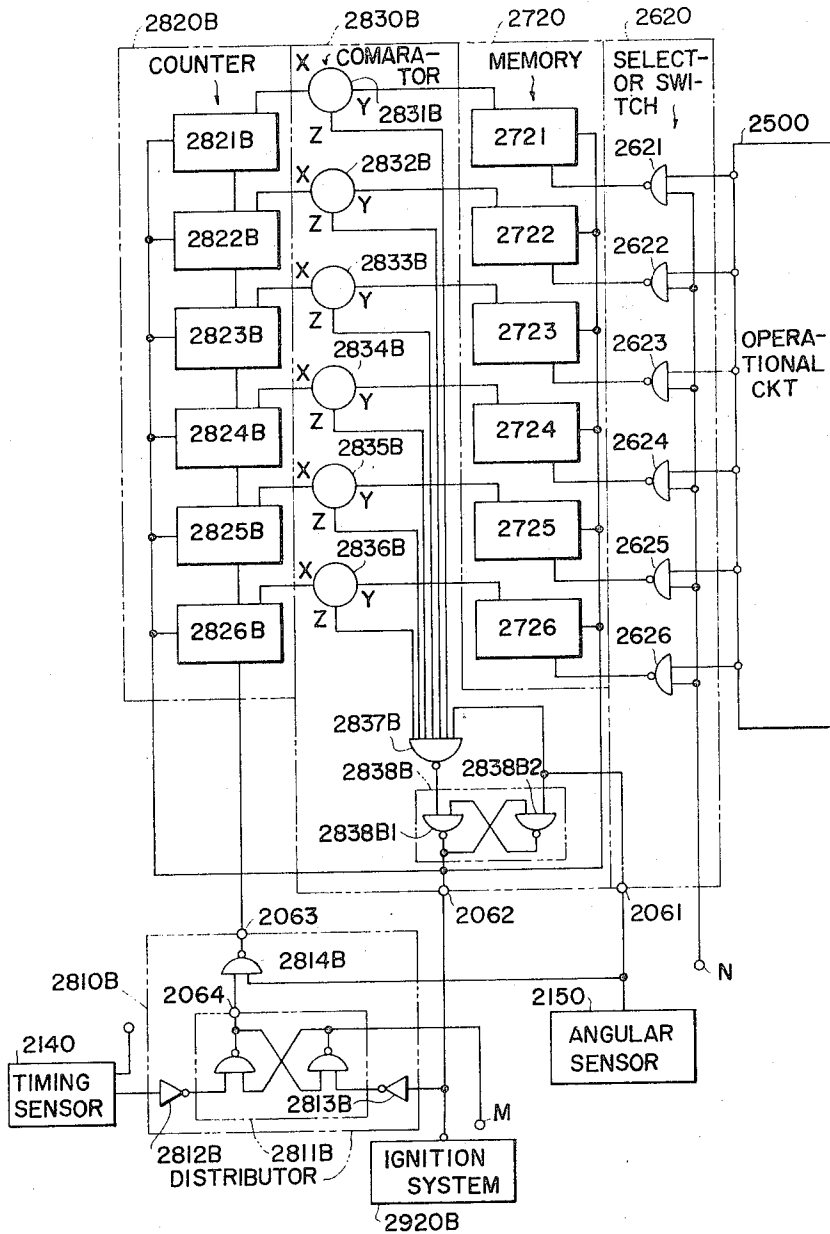


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FIG. 28



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FIG. 29

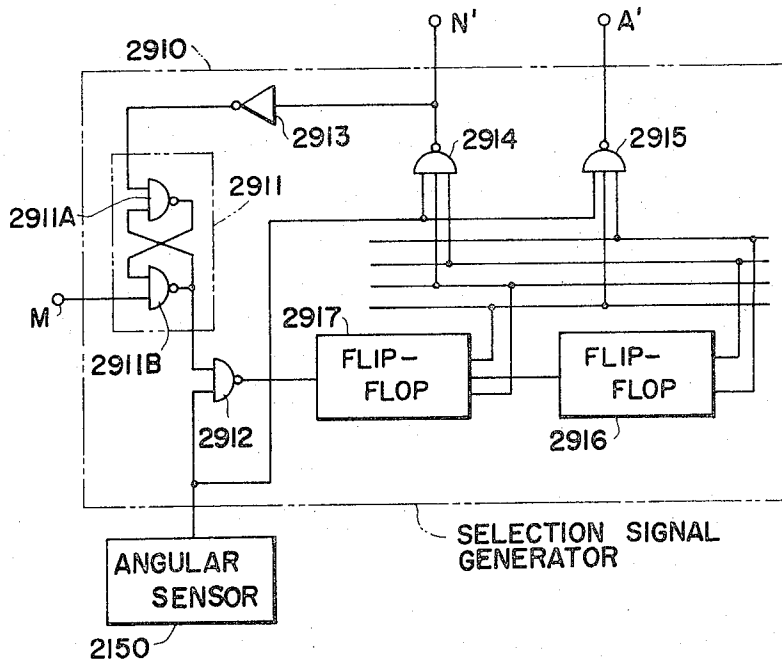
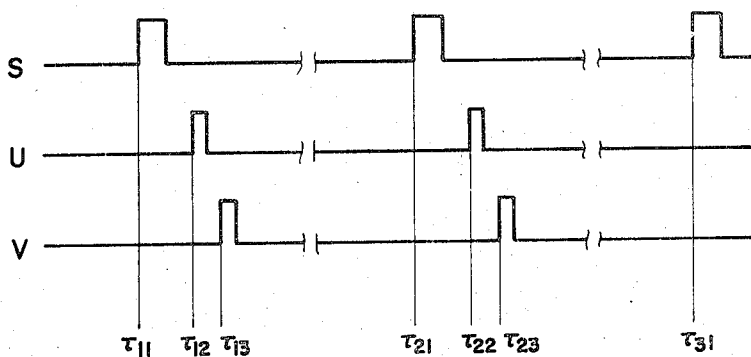


FIG. 31



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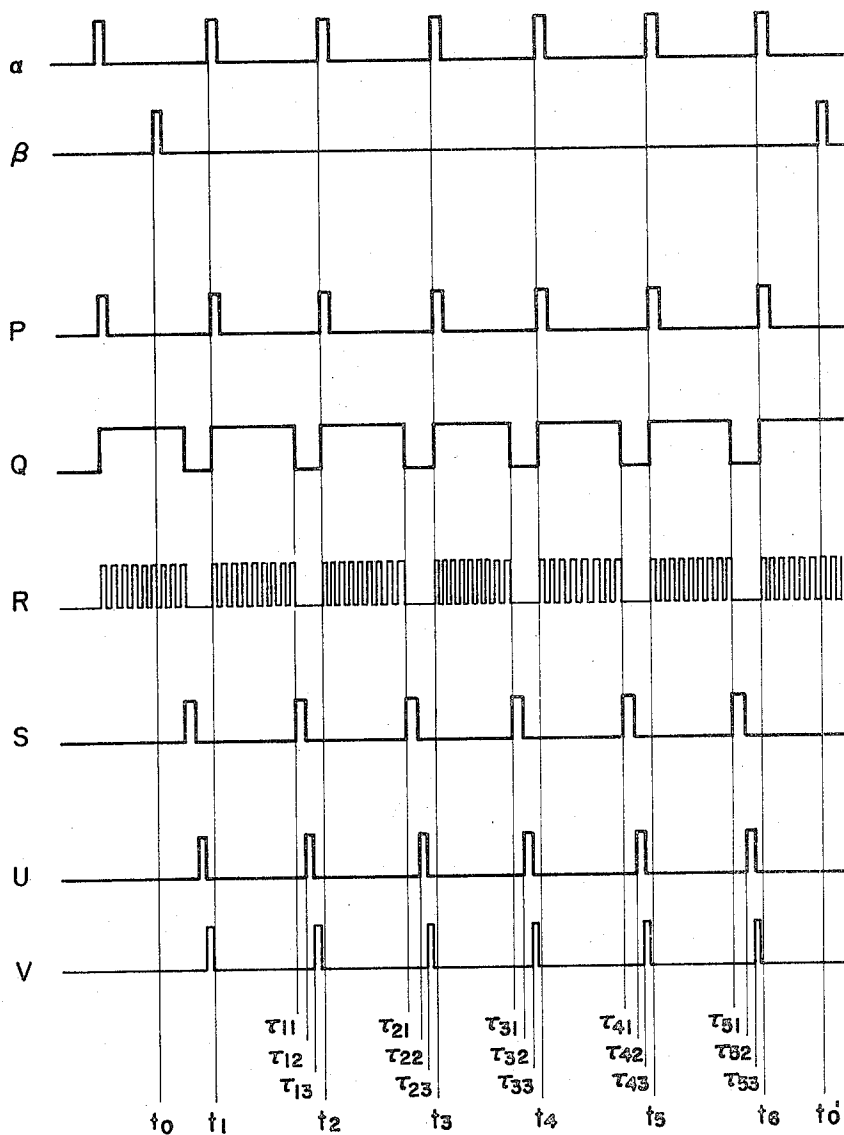
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FIG. 30

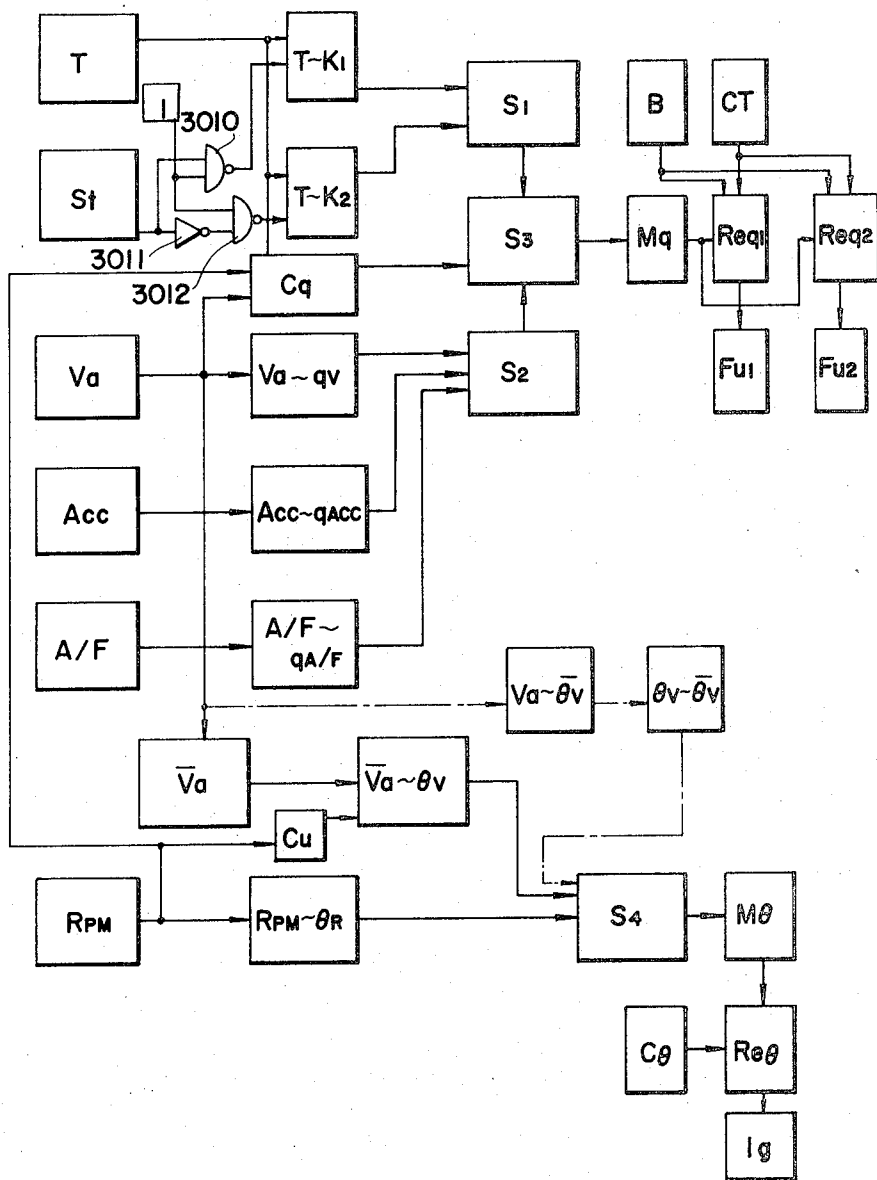


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FIG. 32



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FIG. 33

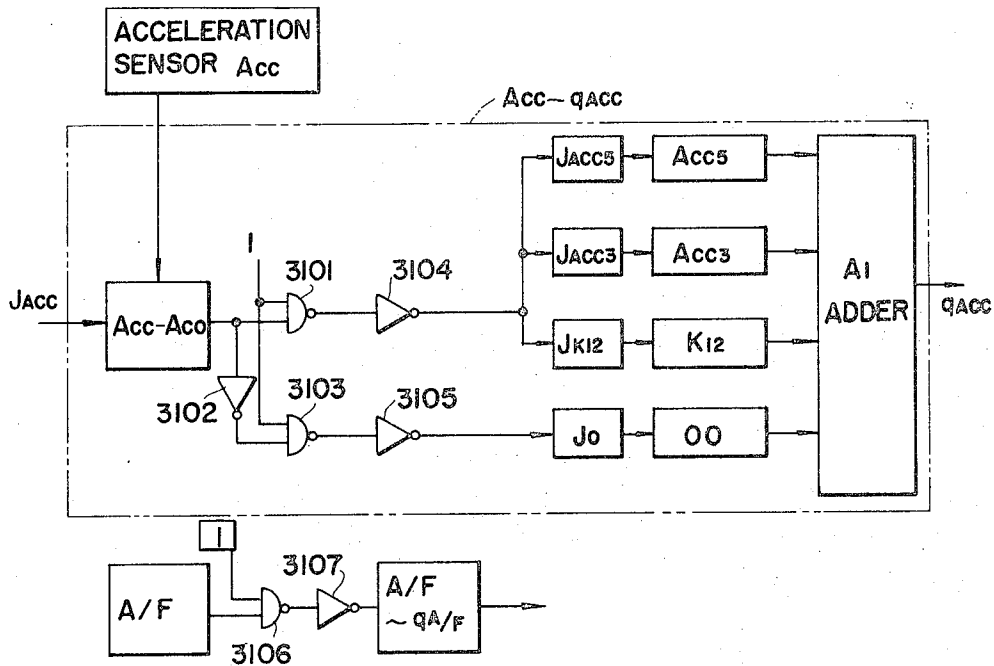


FIG. 34

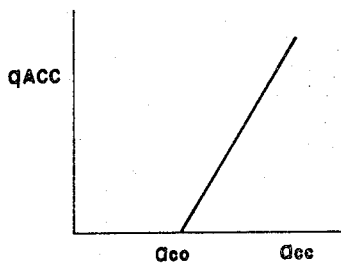
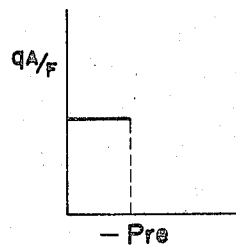


FIG. 35

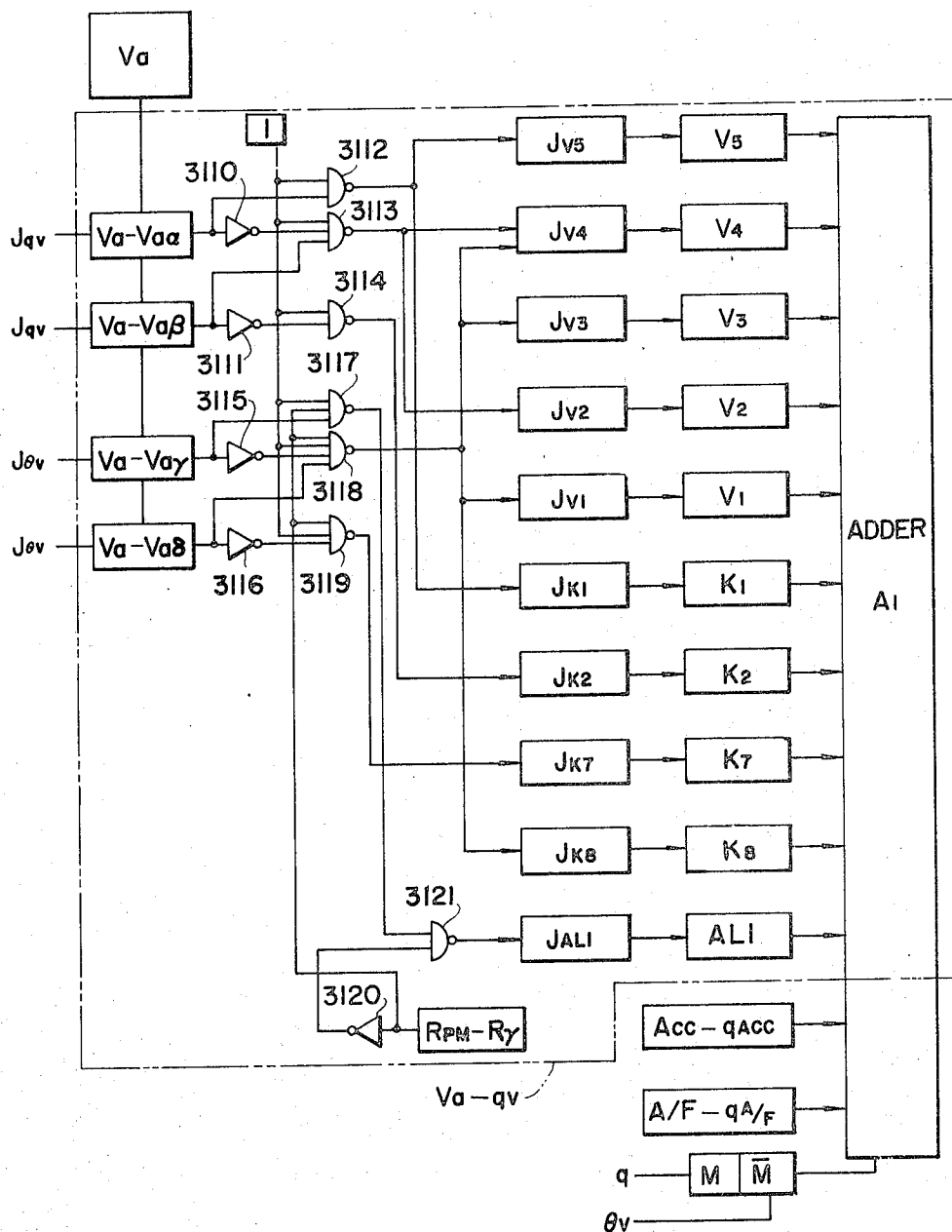


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FIG. 36



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FIG. 37

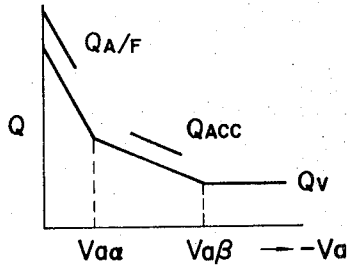


FIG. 38

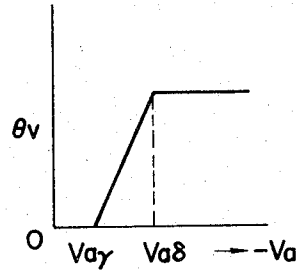
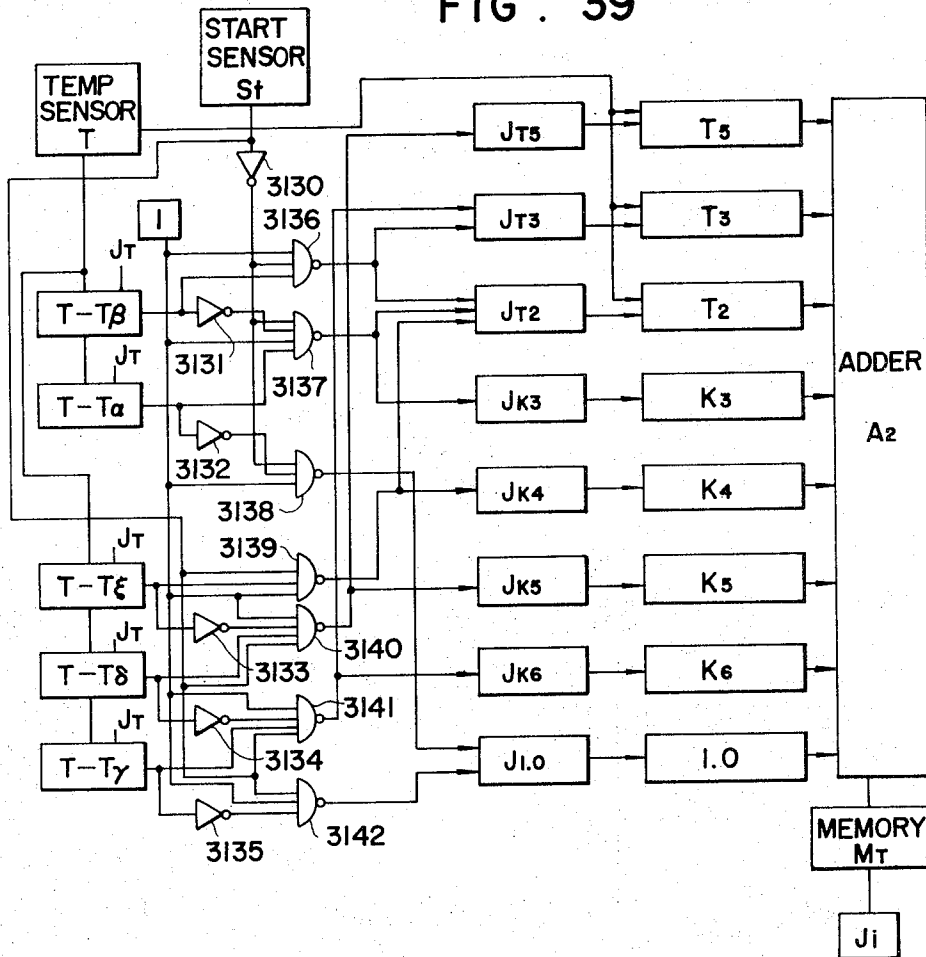


FIG. 39



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FIG. 40

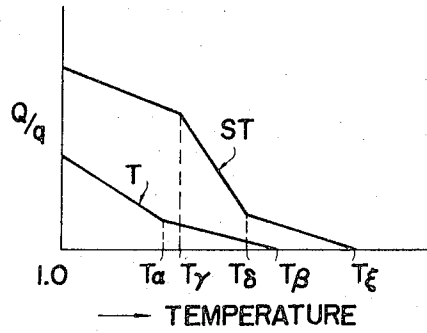
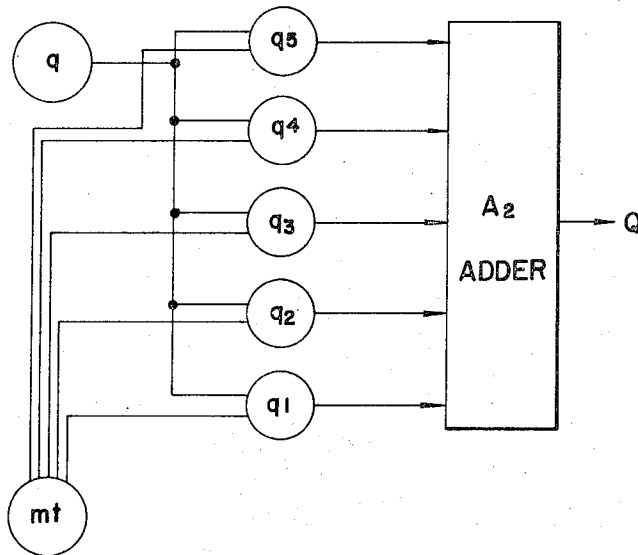


FIG. 41



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FIG. 42

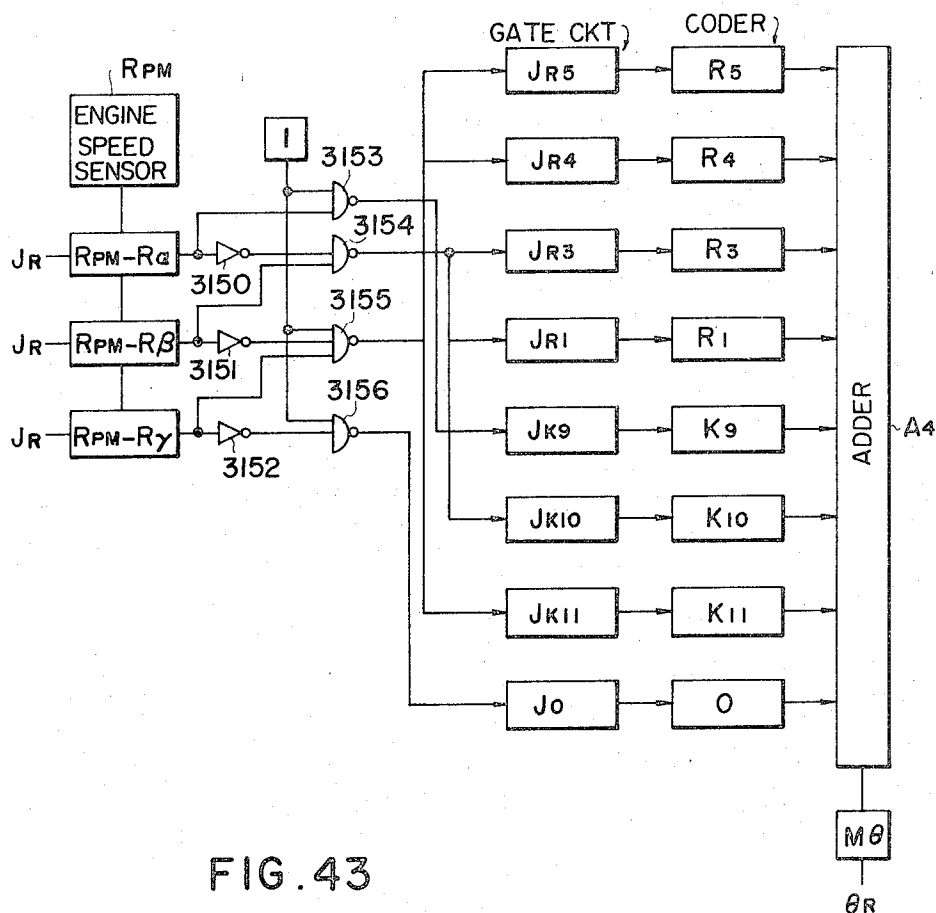


FIG. 43

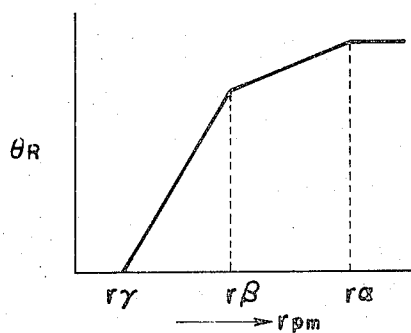
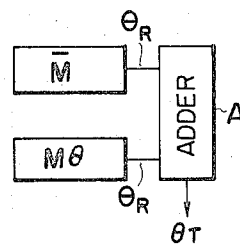


FIG. 44



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FIG. 45

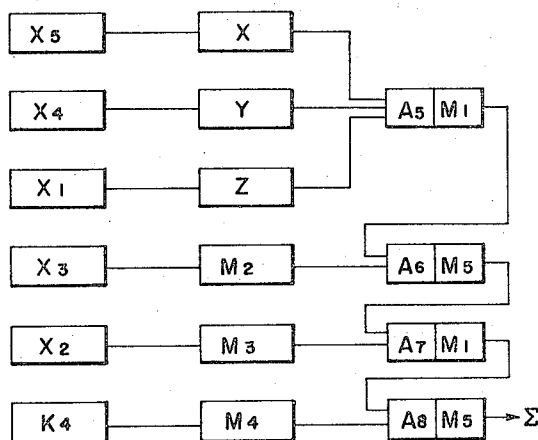
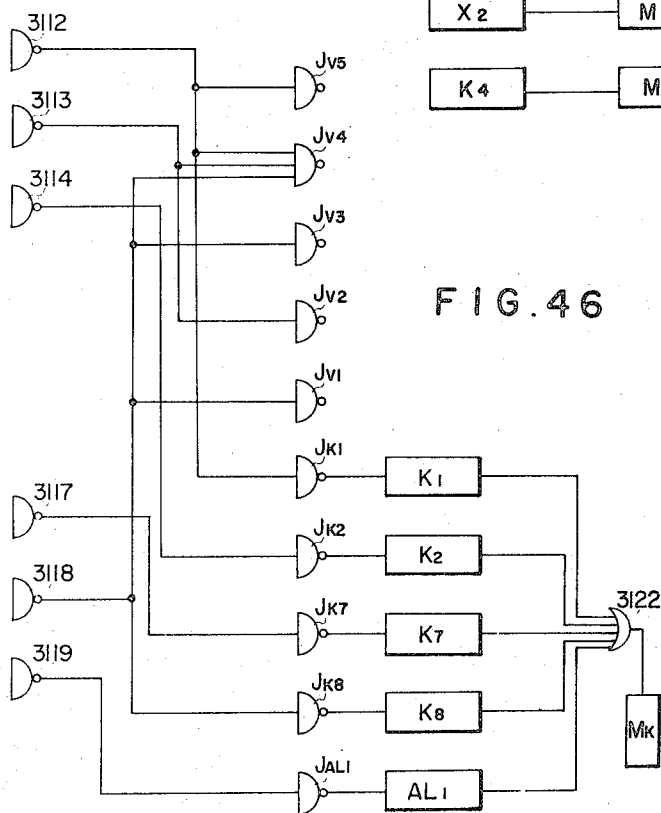


FIG. 46



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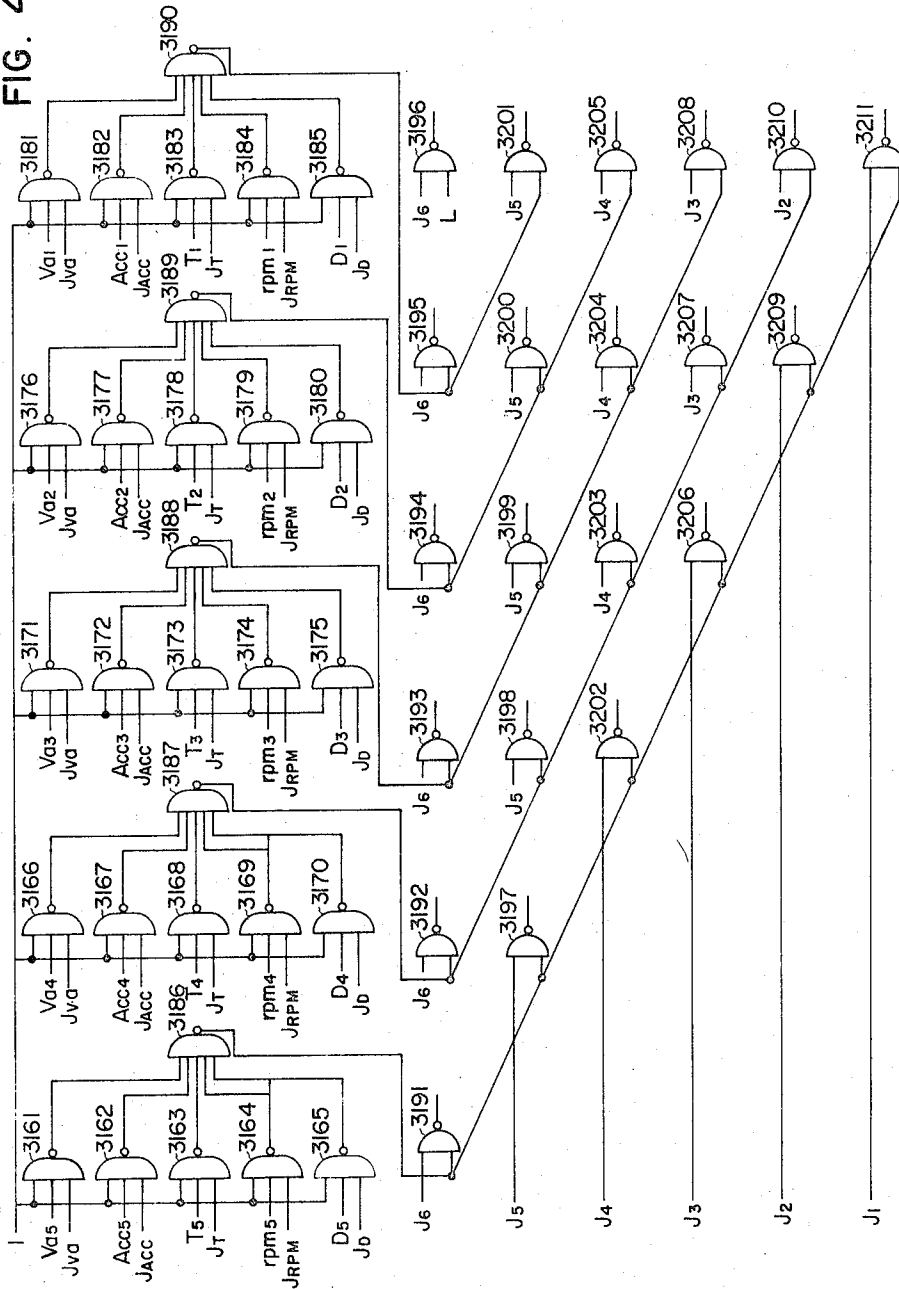
Hiroshi Yoshida

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FIG. 47

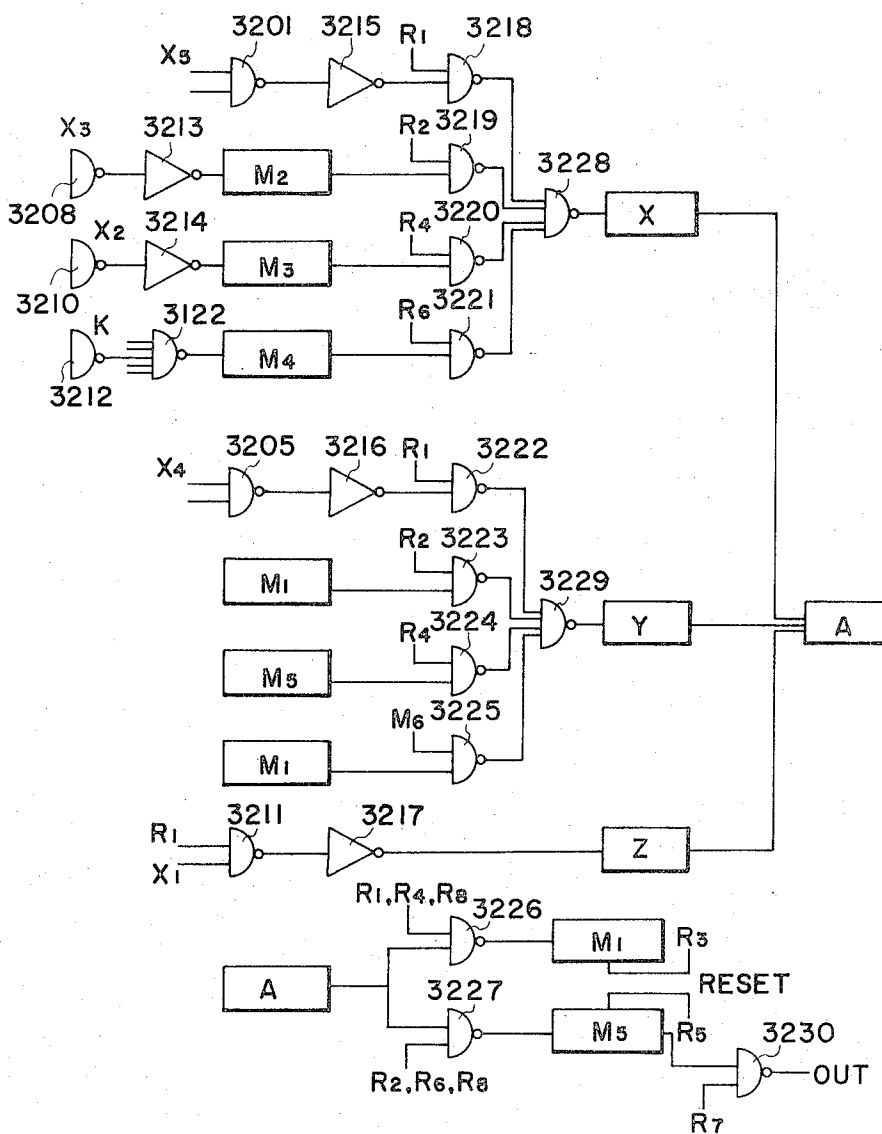


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FIG. 48



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FIG. 49

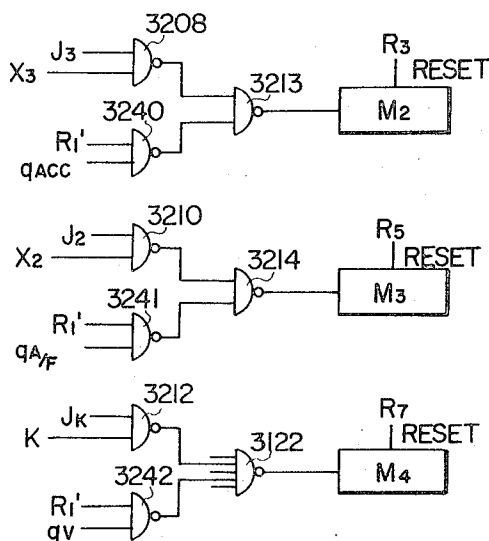
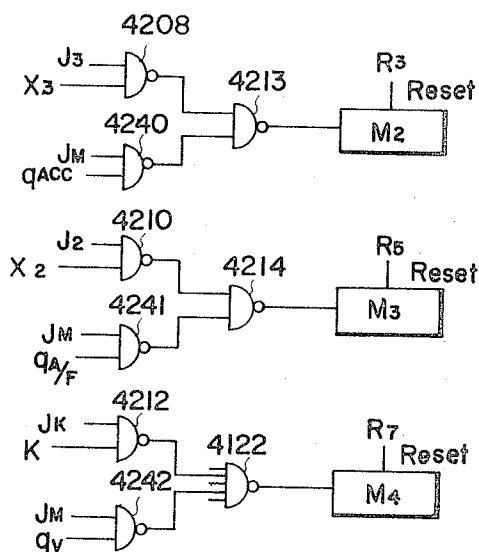


FIG. 56

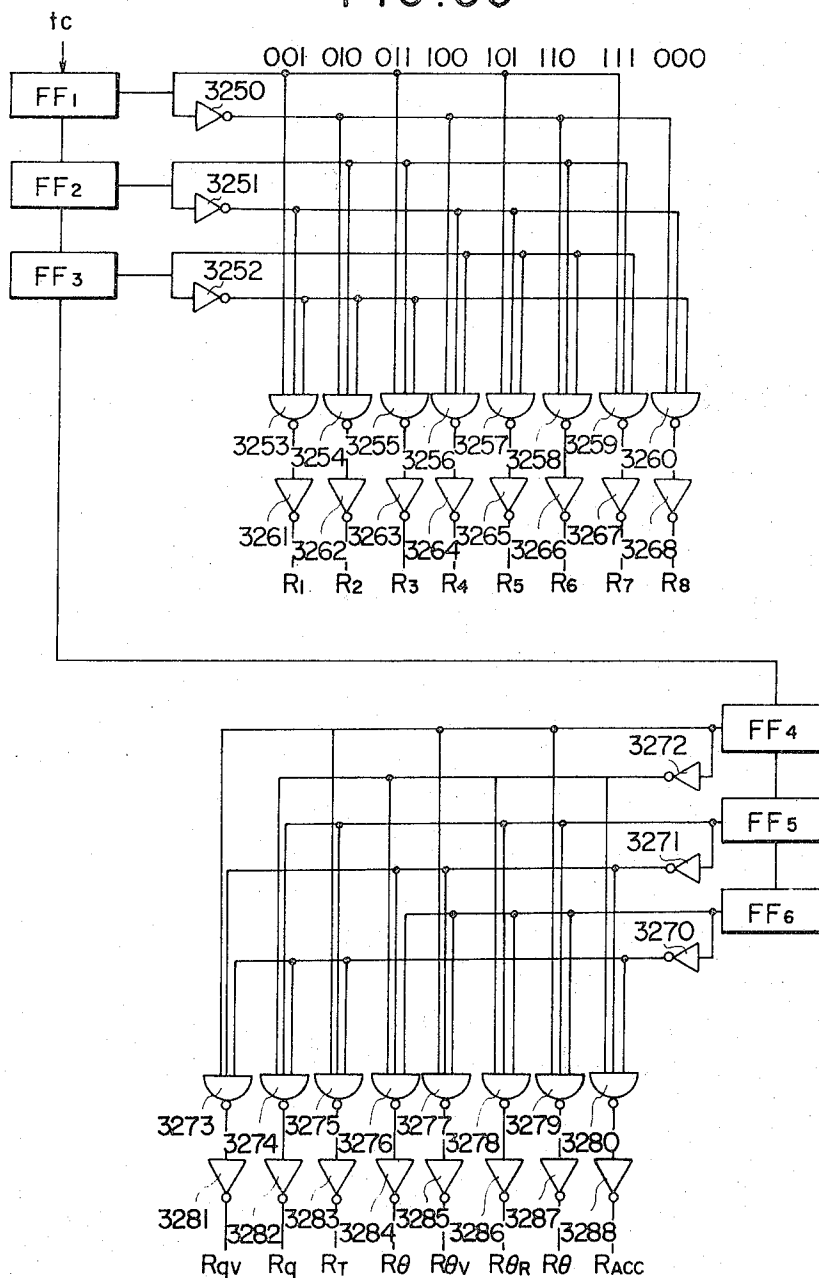


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FIG. 50



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FIG. 51

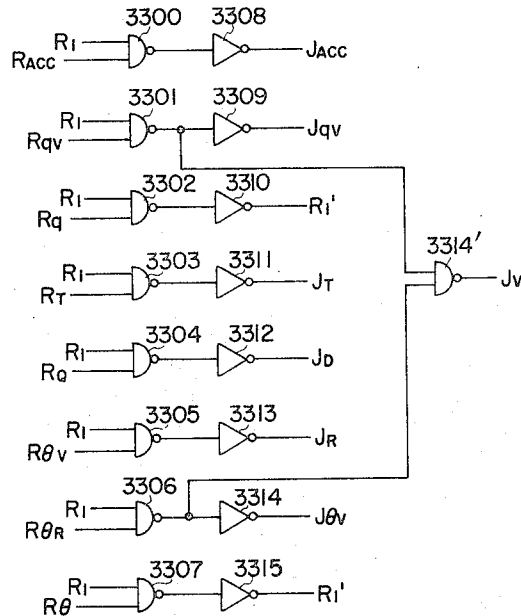
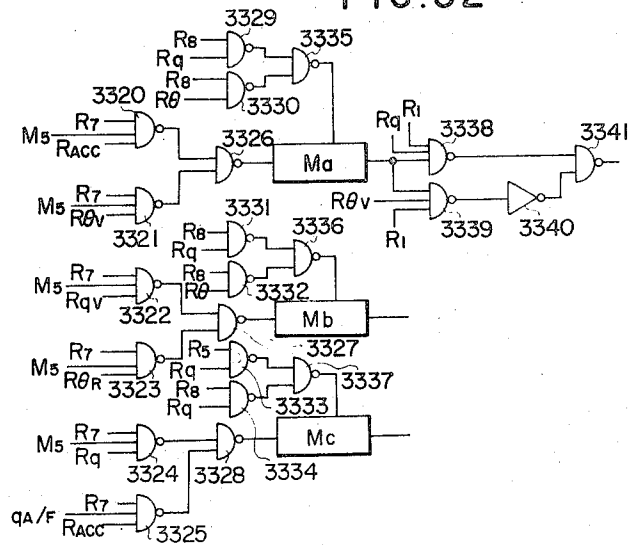


FIG. 52



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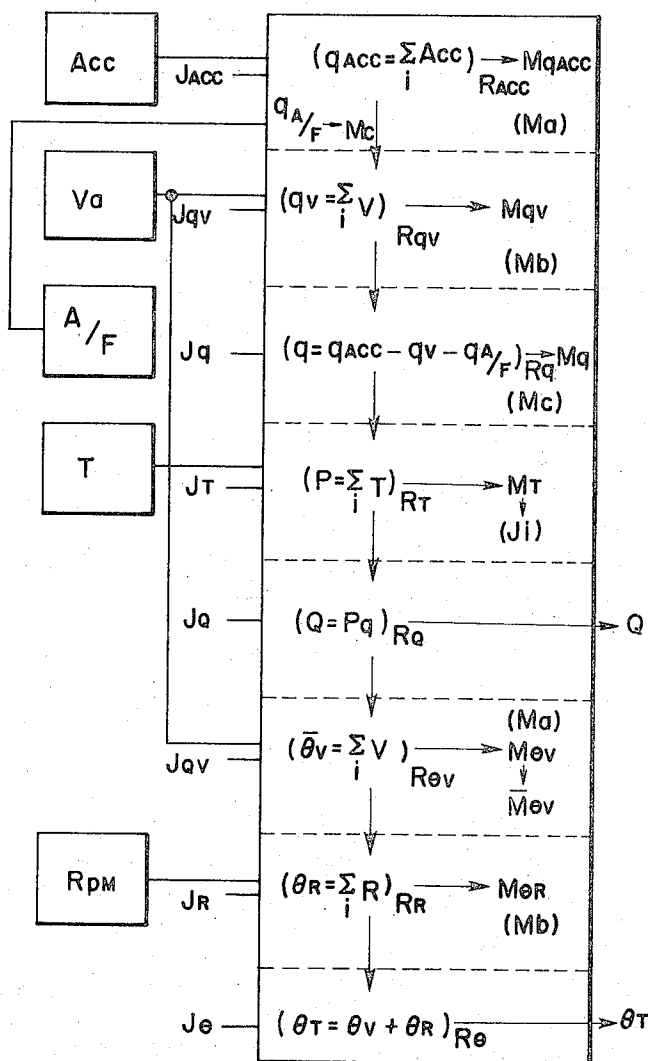
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FIG. 53

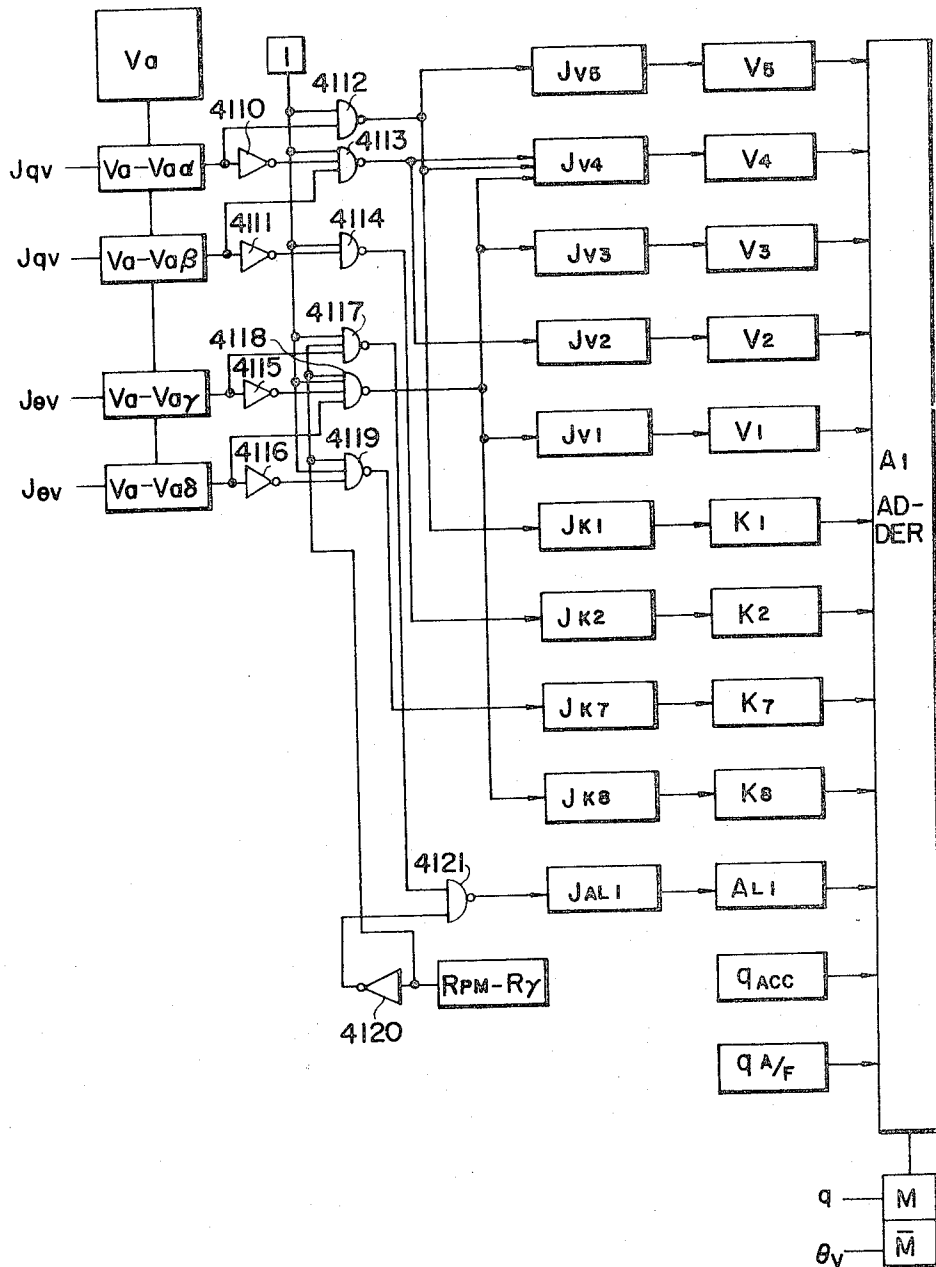


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FIG. 54



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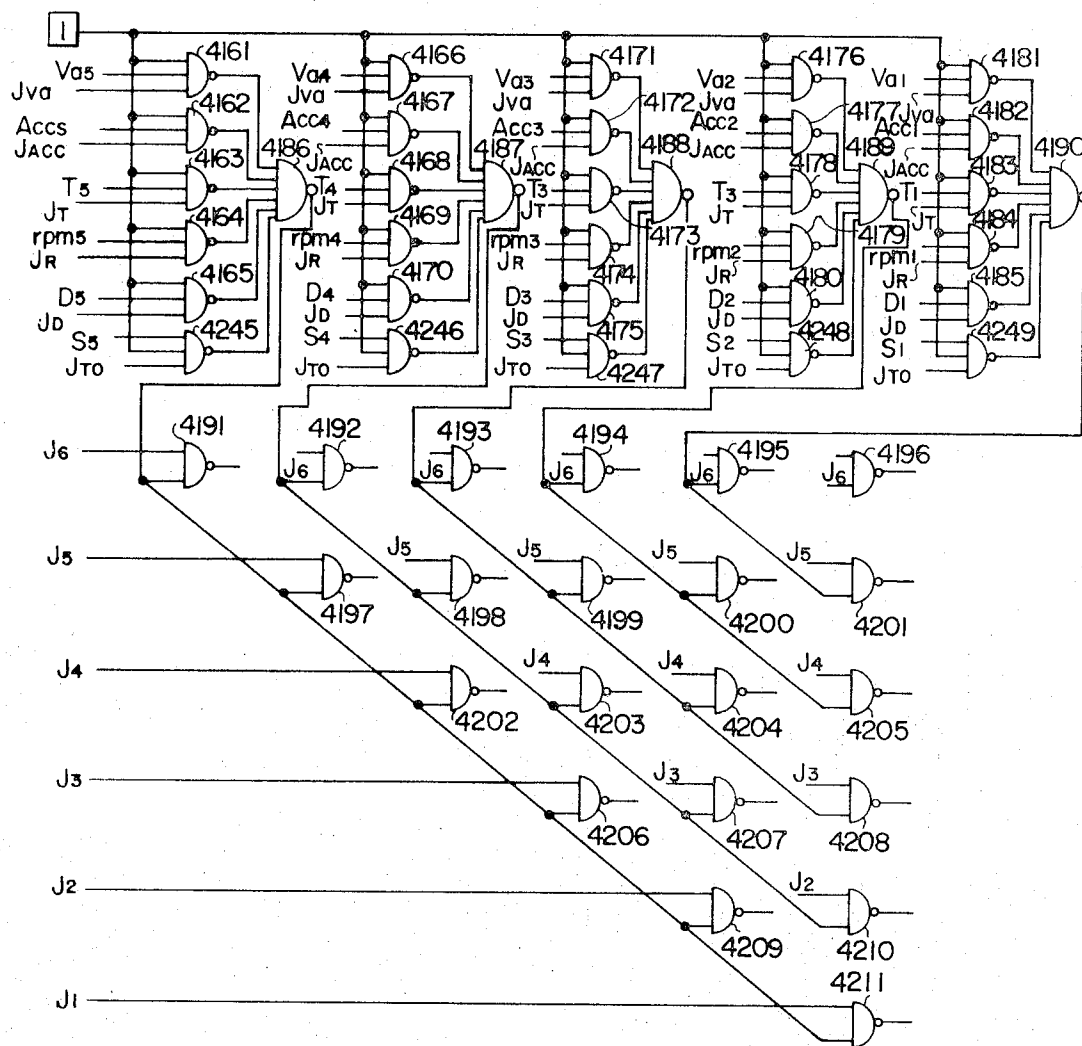
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FIG. 55



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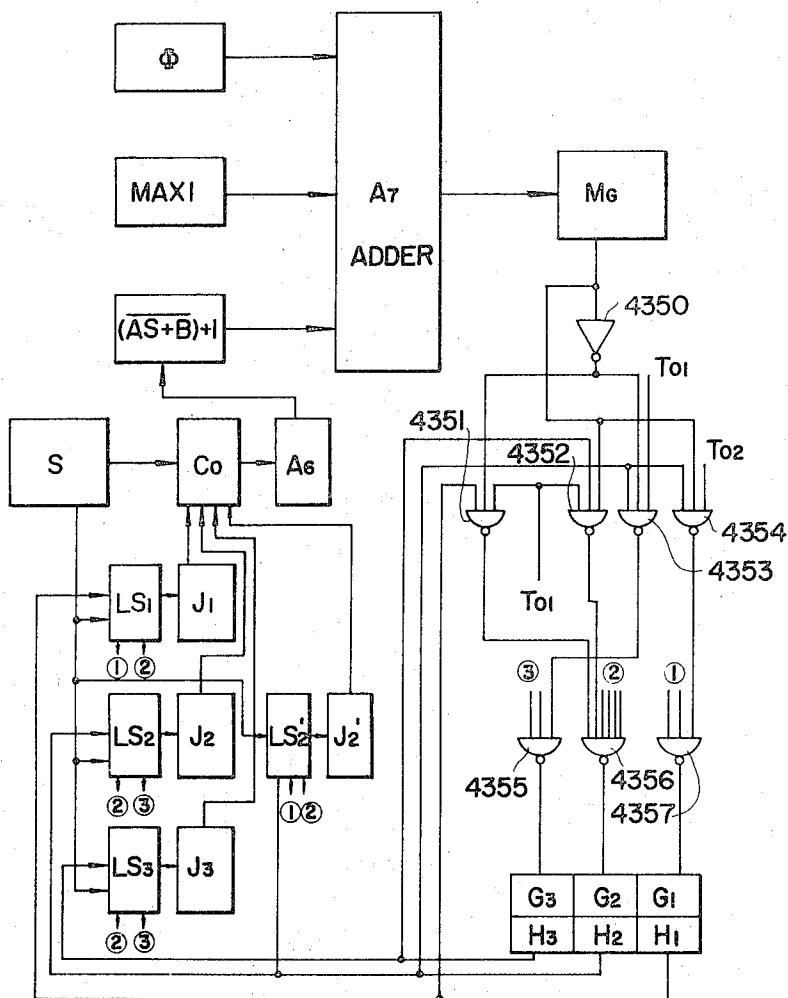
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FIG. 57



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FIG. 58

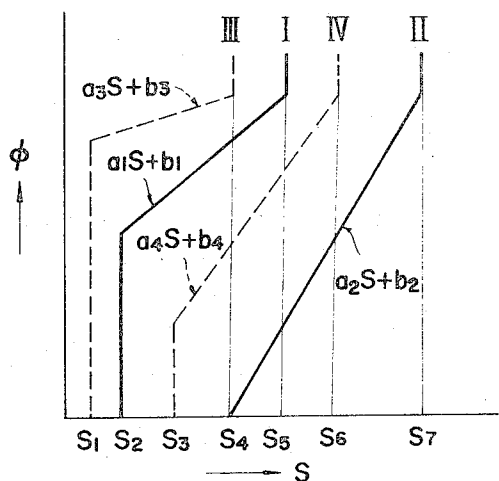


FIG. 61

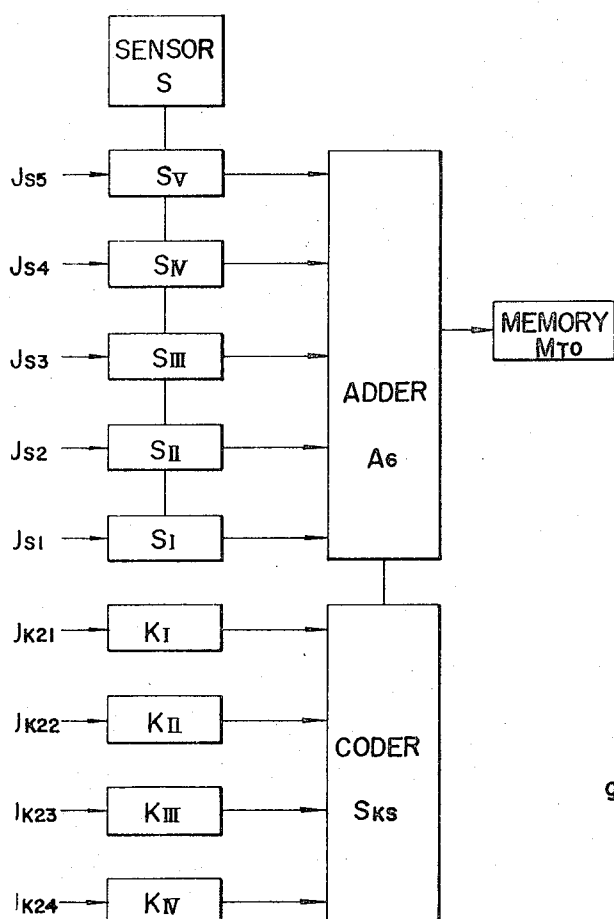
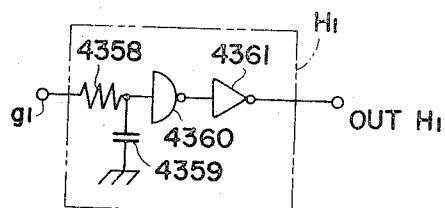


FIG. 59

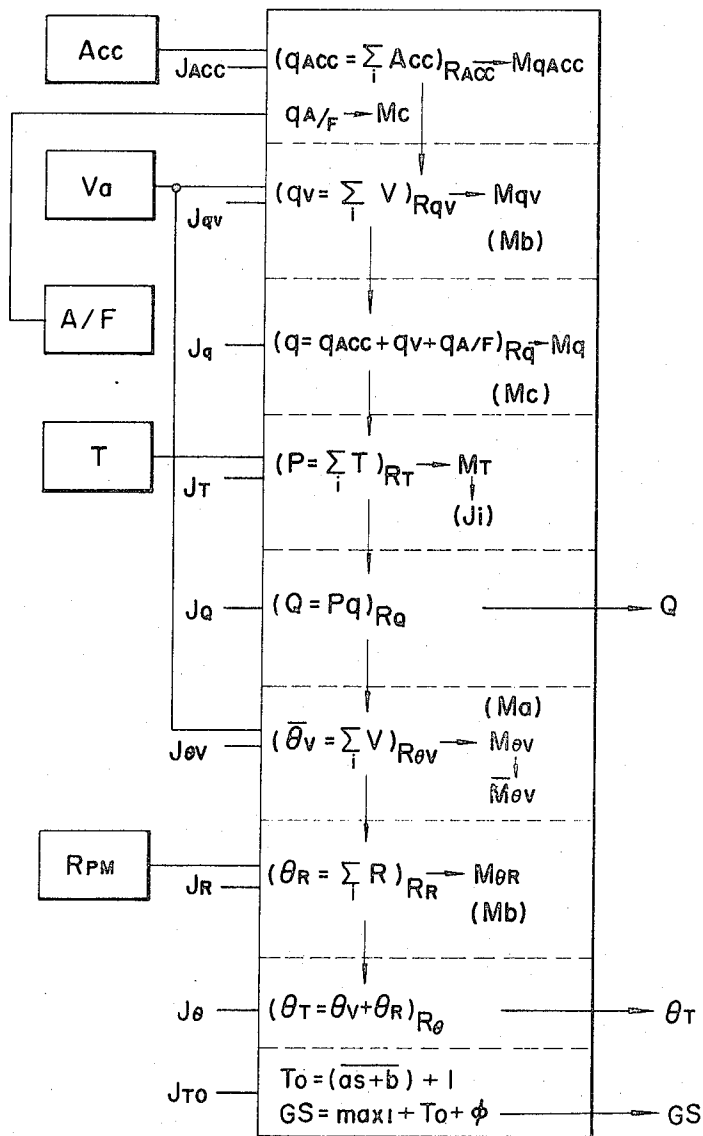


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FIG. 60



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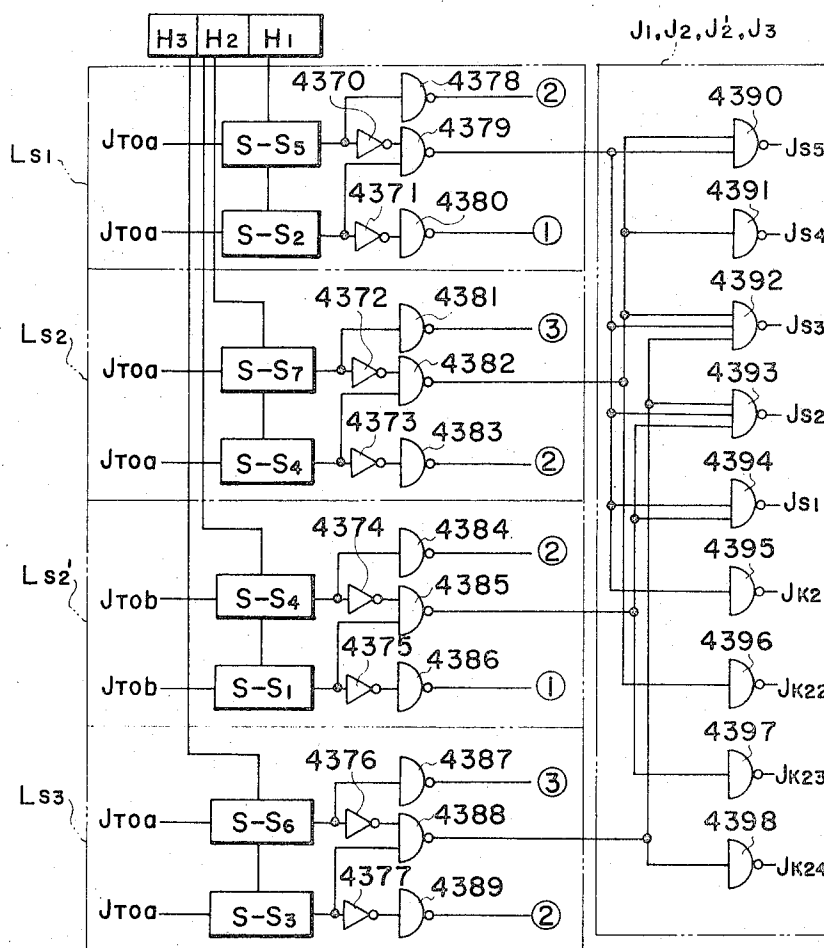
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FIG. 62



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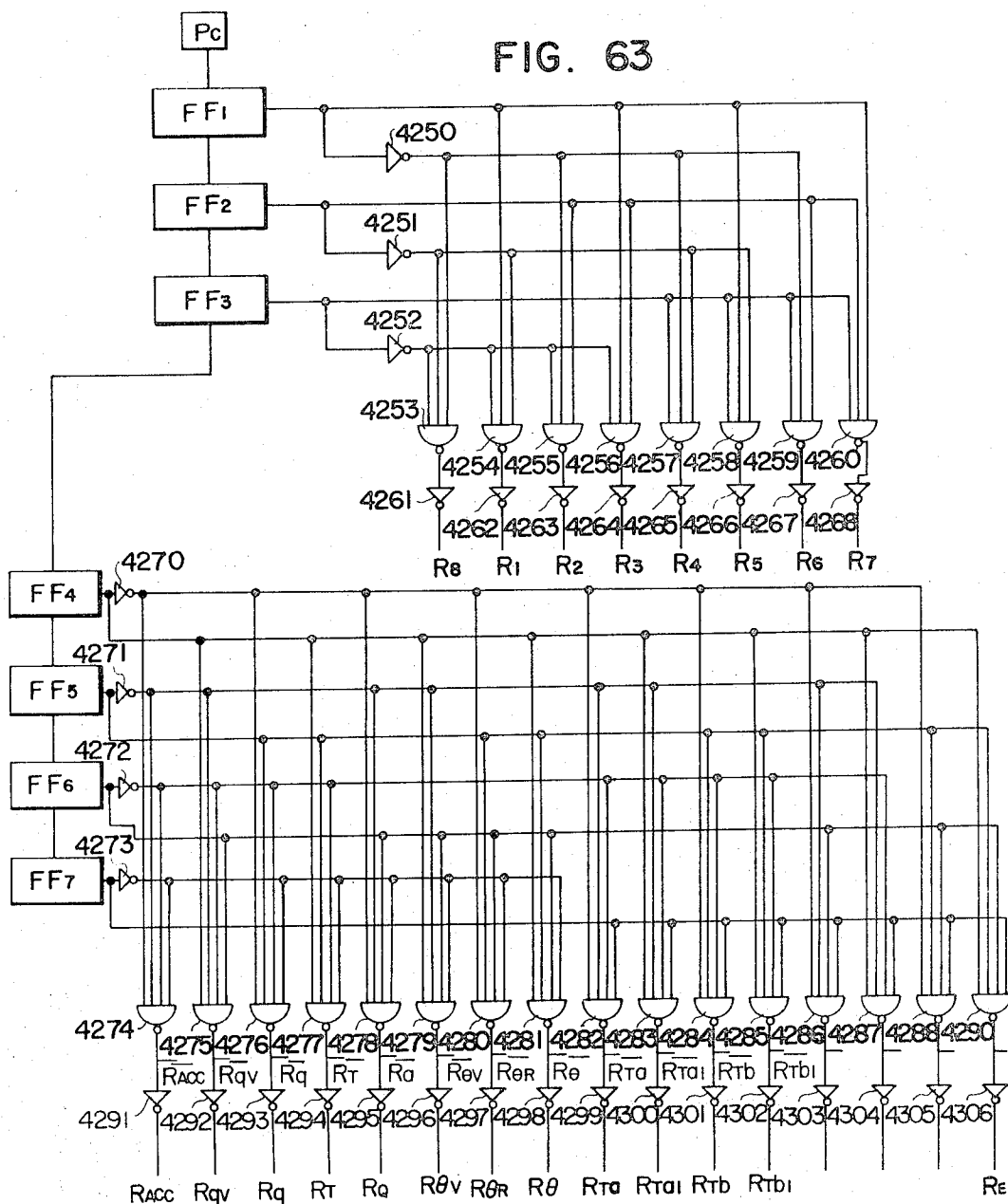
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FIG. 63



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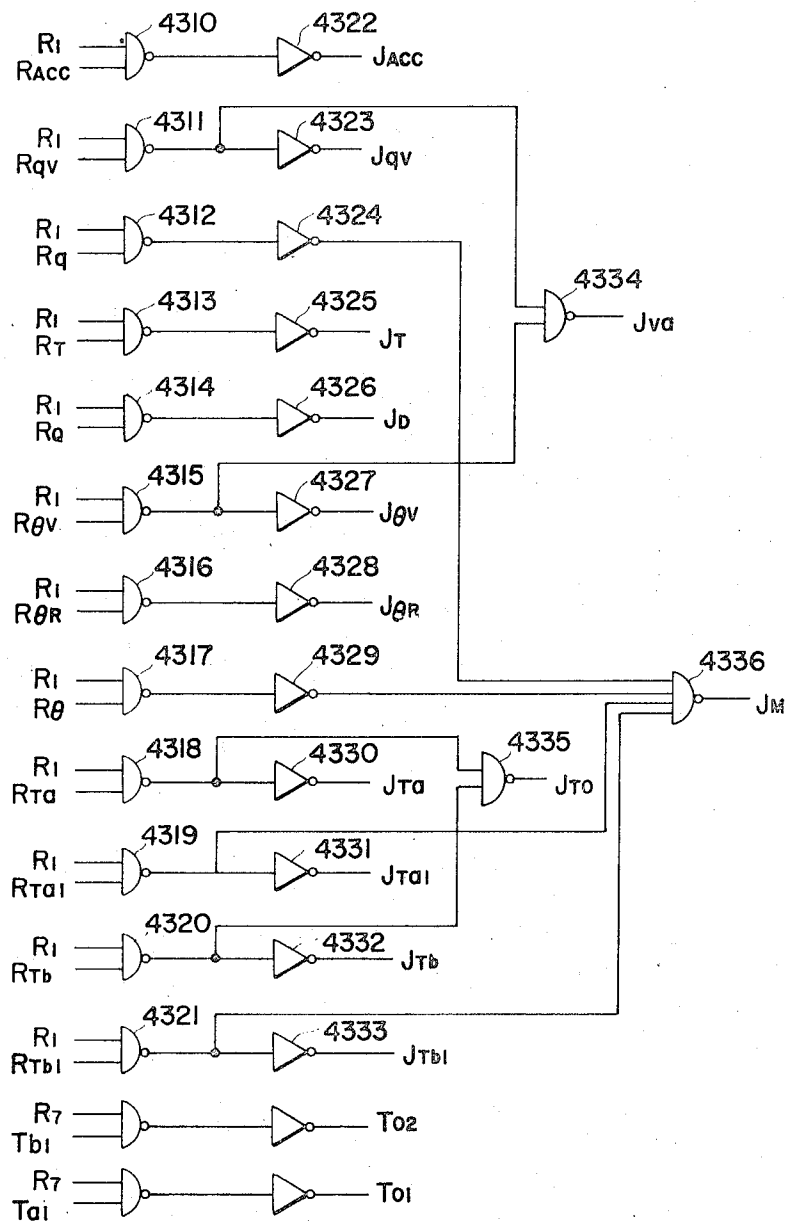
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FIG. 64

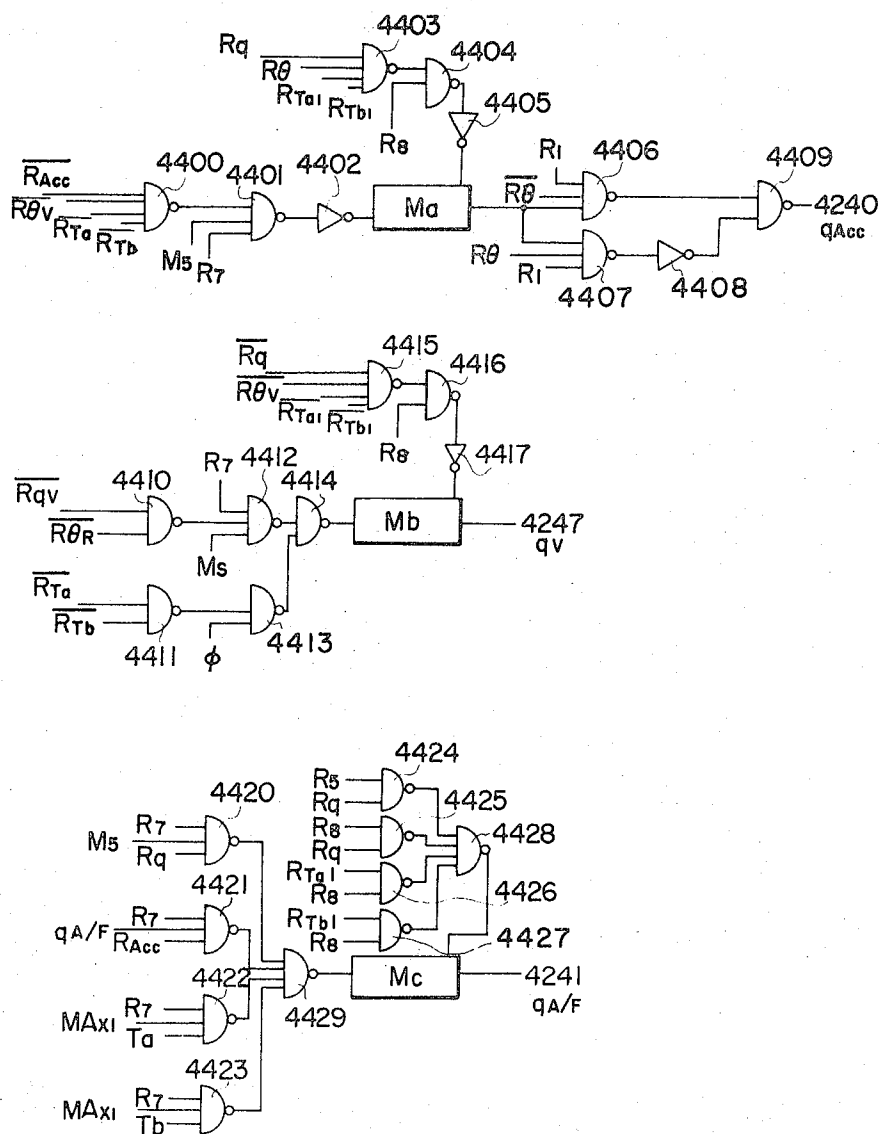


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FIG. 65



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FIG. 66

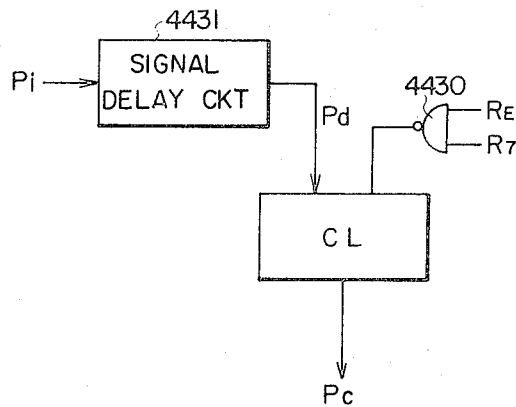


FIG. 67

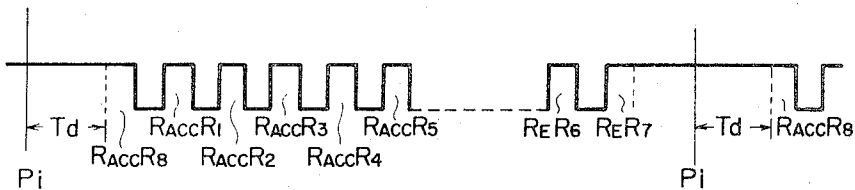
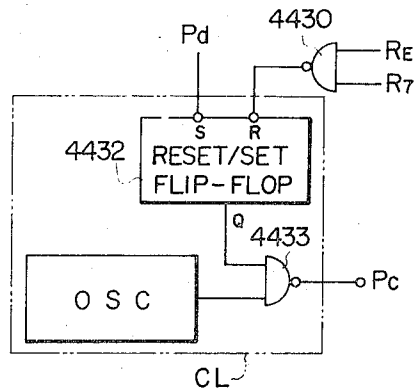


FIG. 68



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FIG. 69

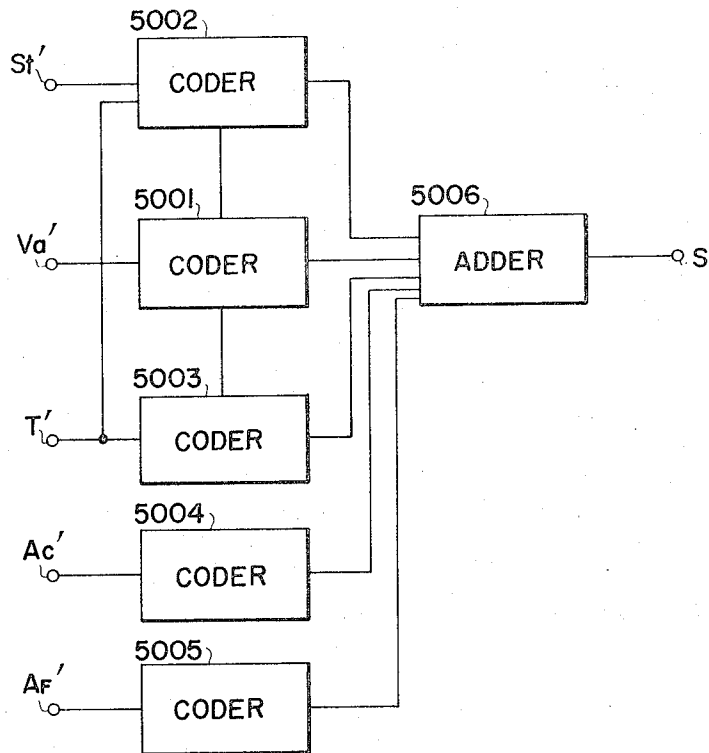
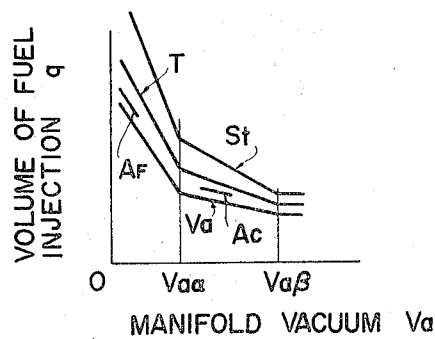


FIG. 70



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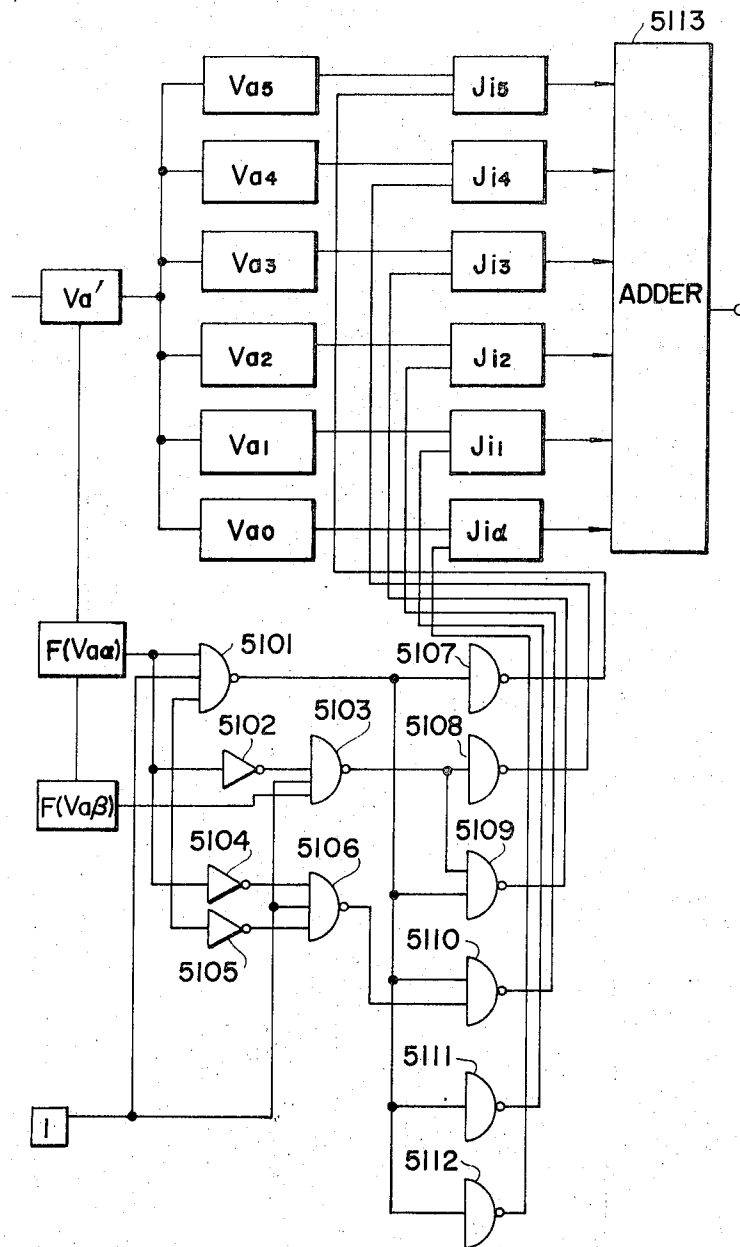
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FIG. 71

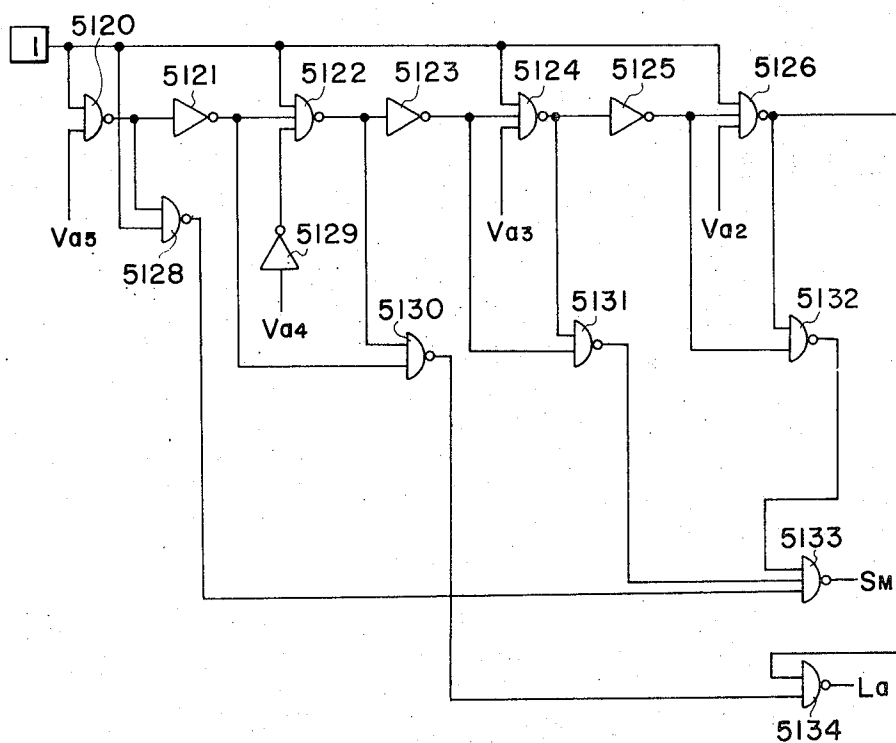


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FIG. 72

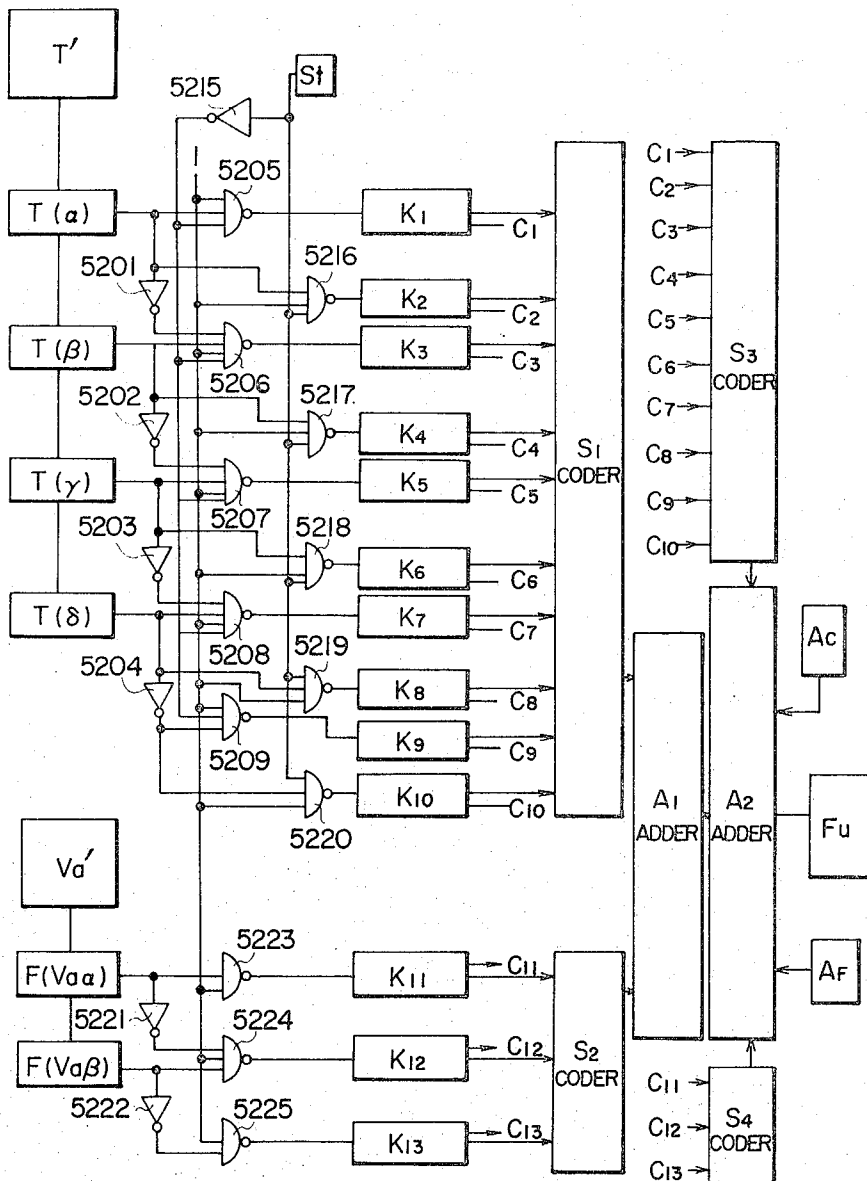


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FIG. 73



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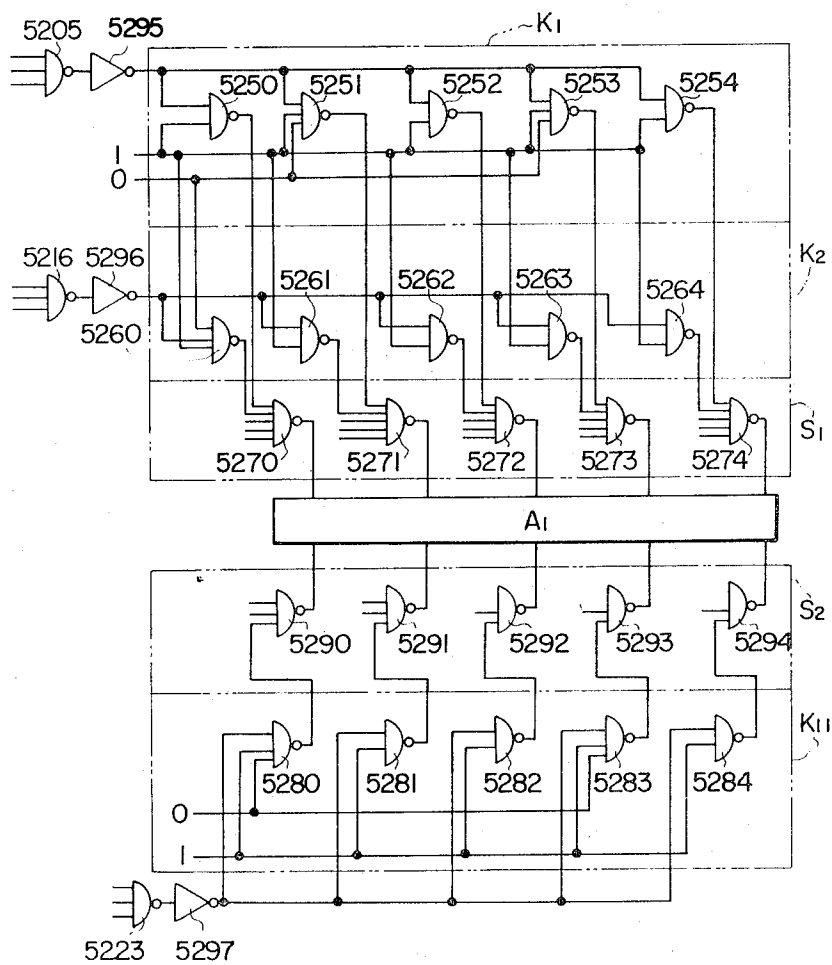
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FIG. 74

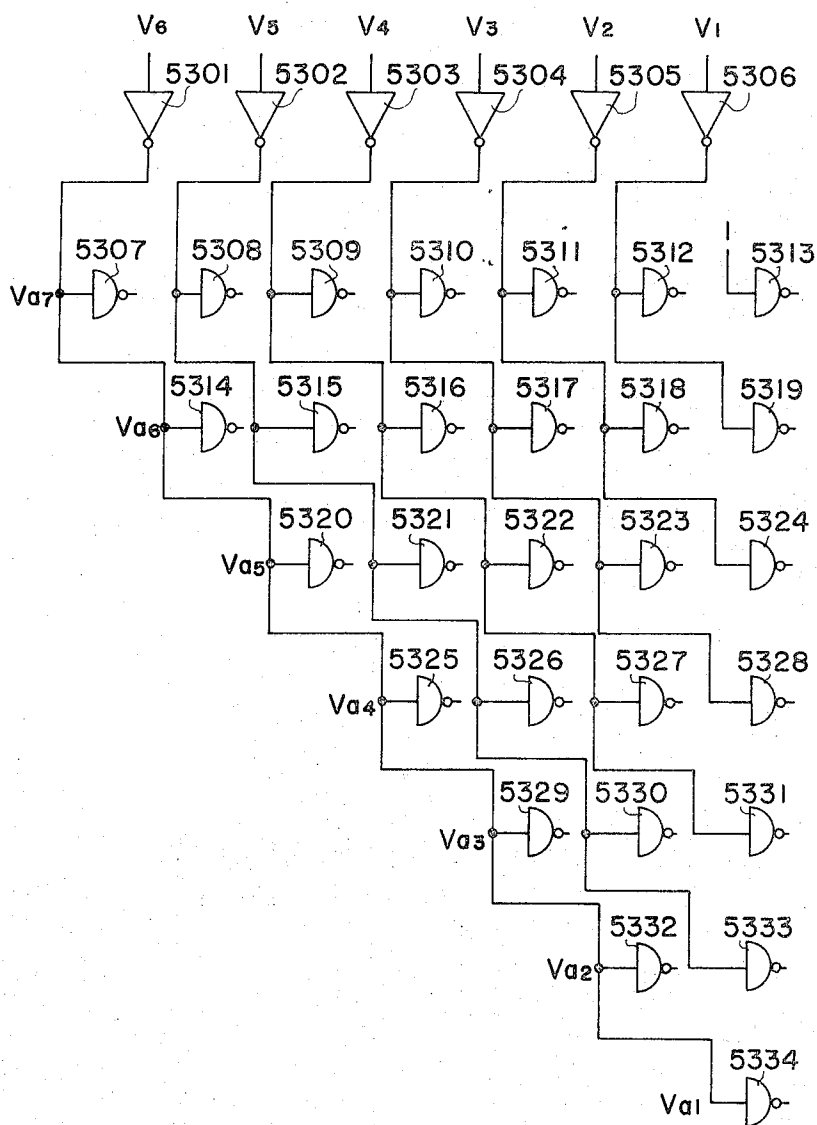


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FIG. 76

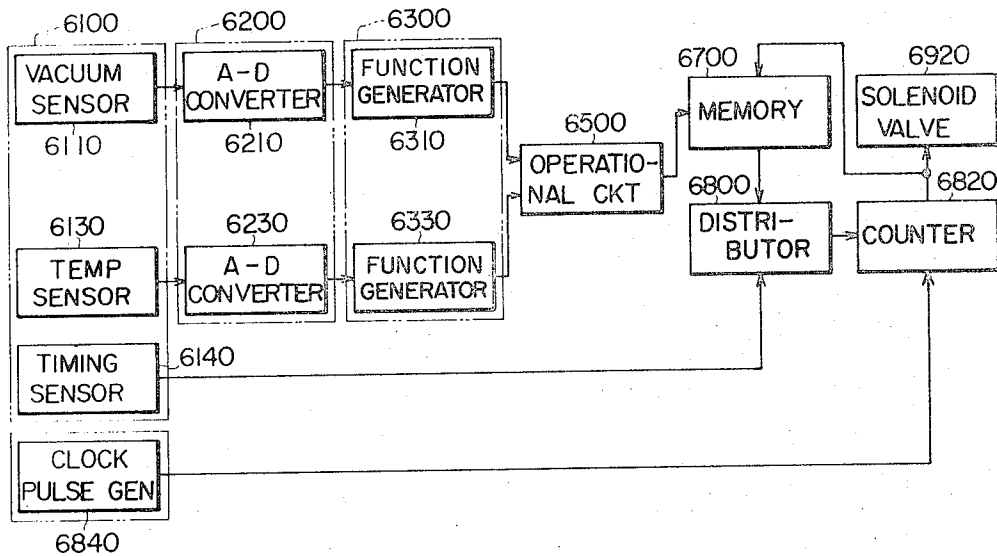
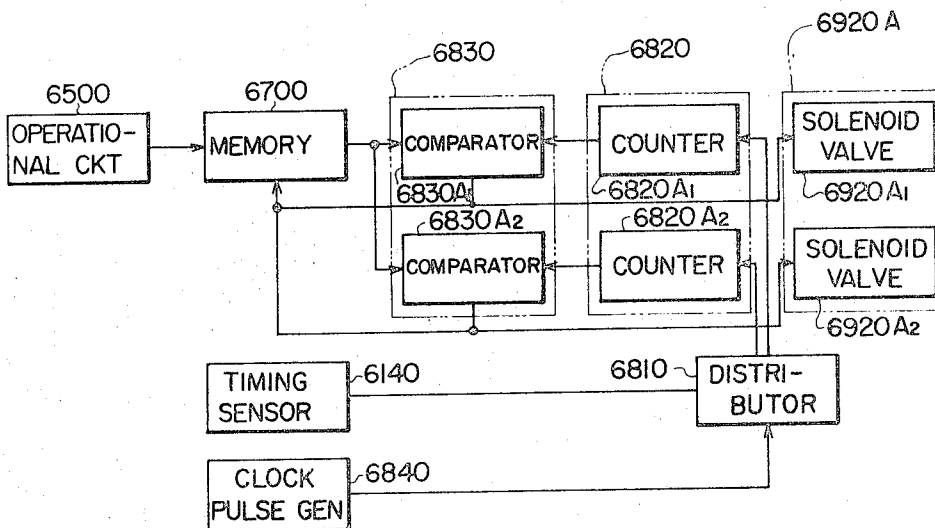


FIG. 77

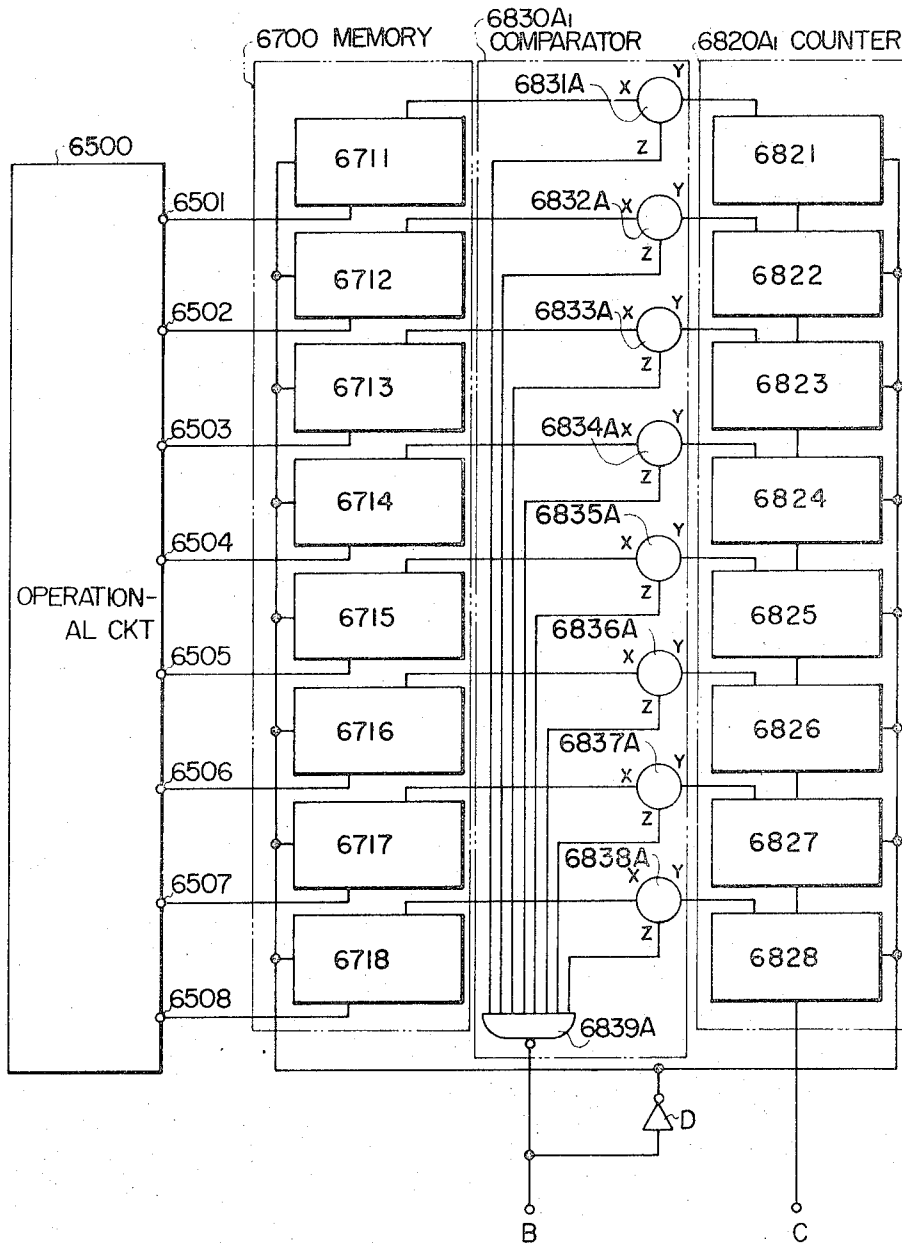


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FIG. 78



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FIG. 79

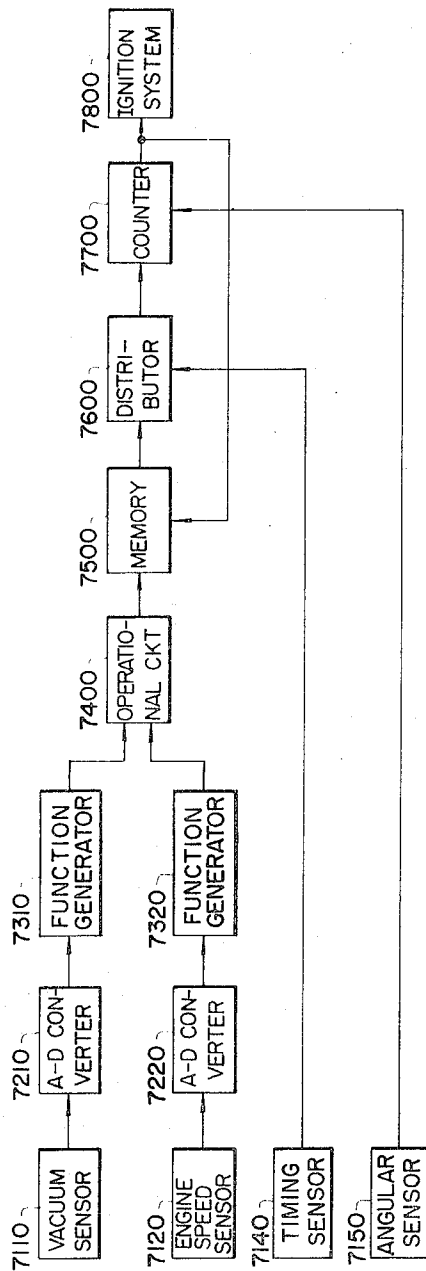
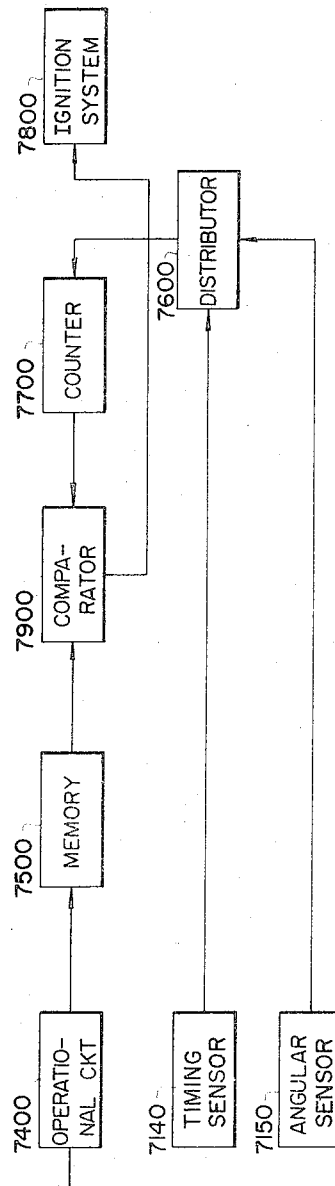


FIG. 80



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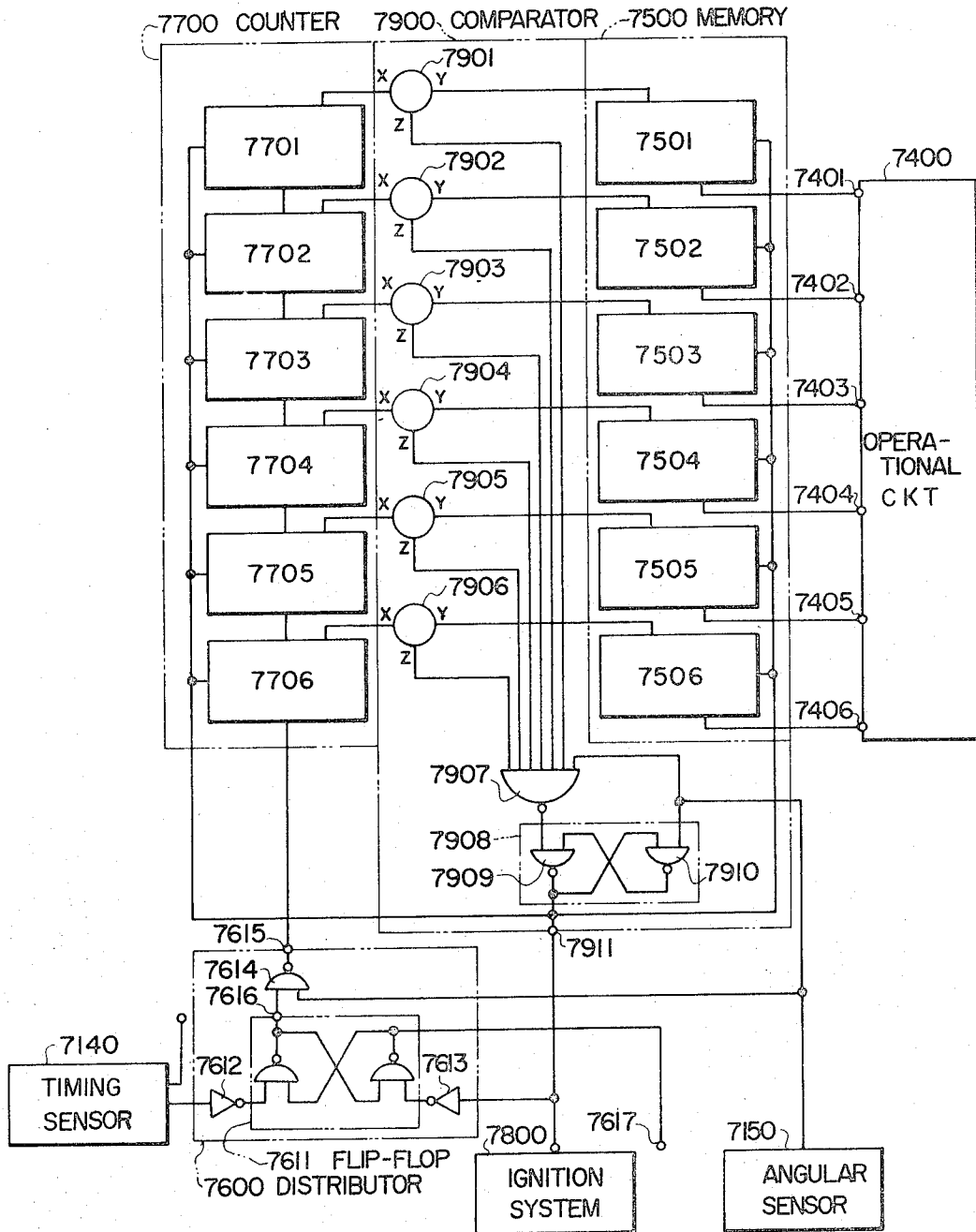
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FIG. 81



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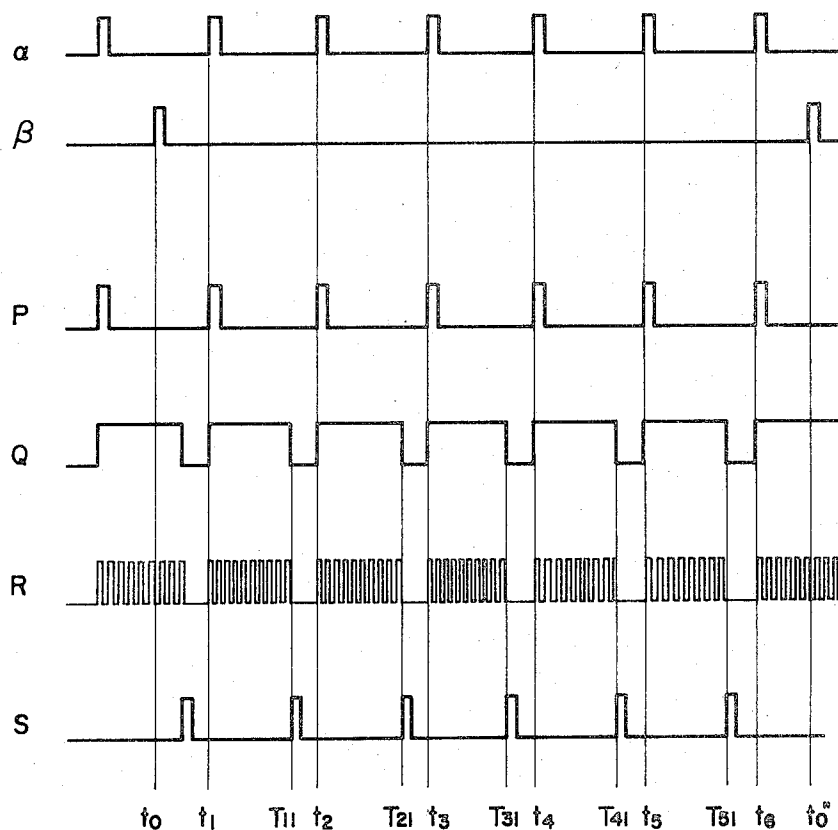
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FIG. 82



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FIG. 83

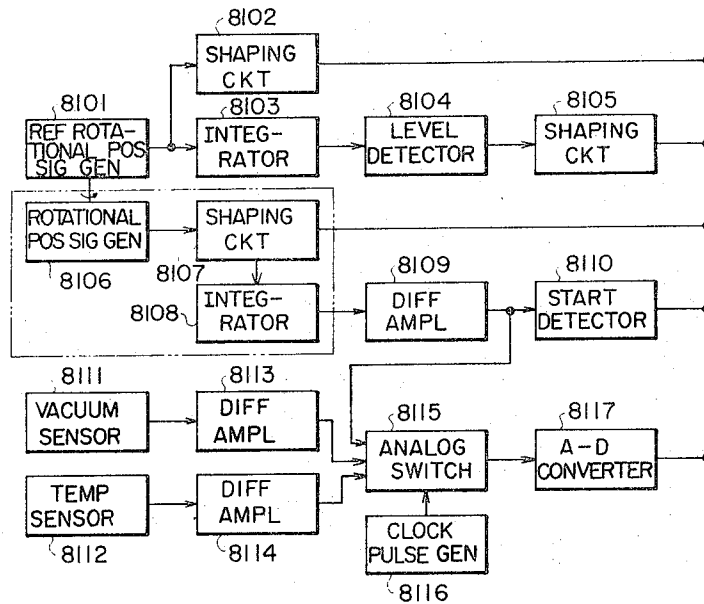


FIG. 84A

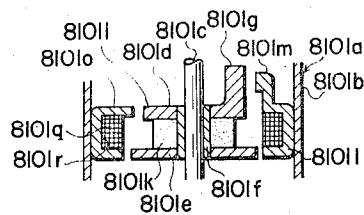
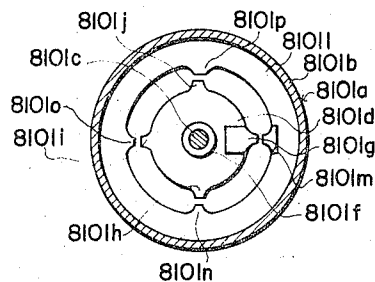


FIG. 84B



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FIG. 85

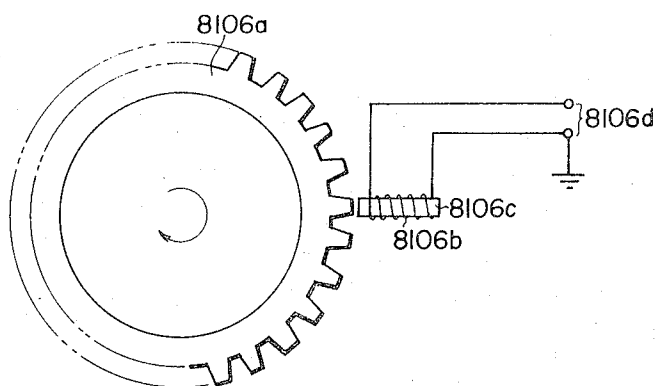
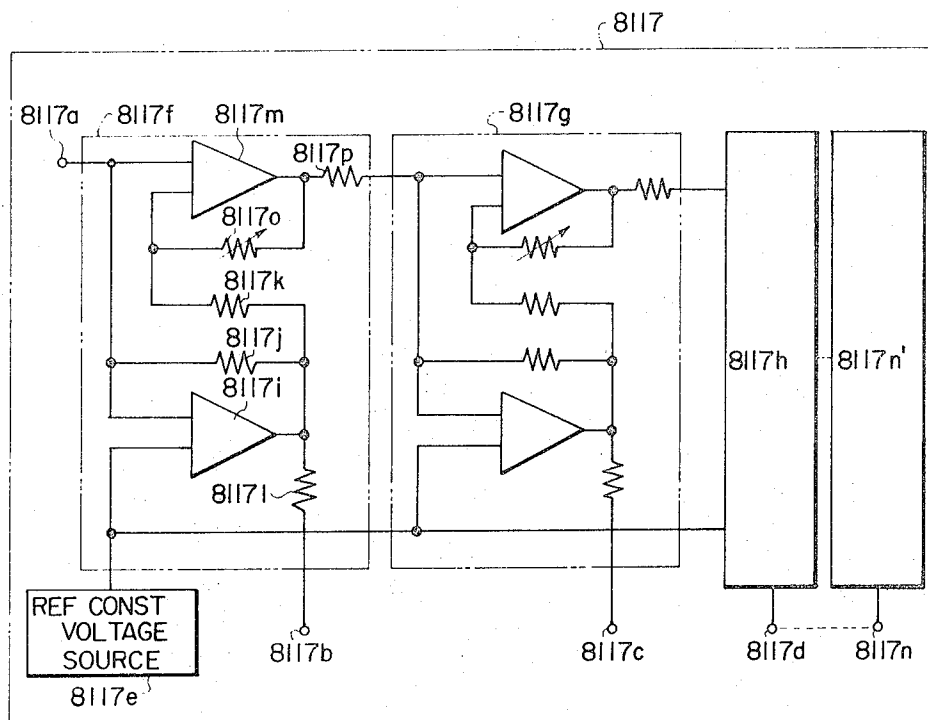


FIG. 86

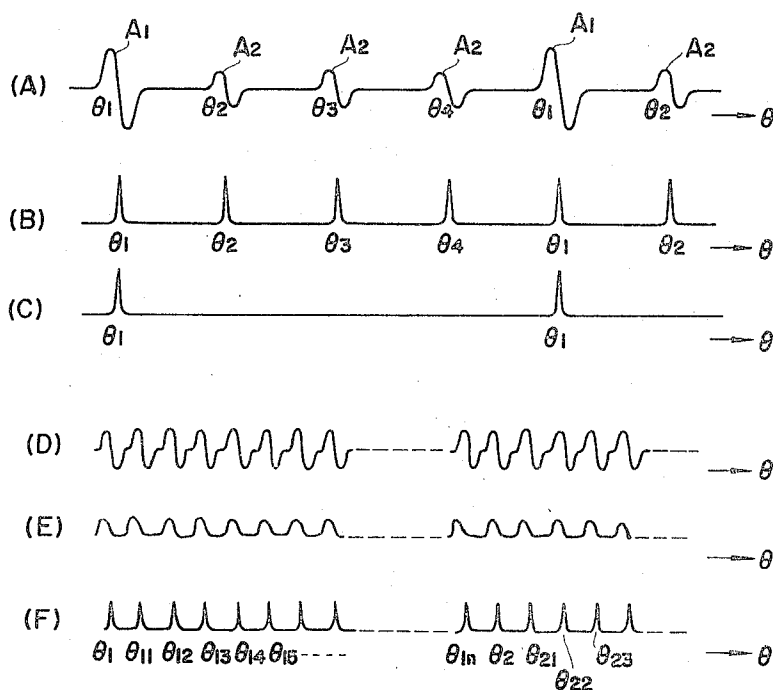


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FIG. 87



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ELECTRICAL FUEL CONTROL SYSTEM FOR INTERNAL COMBUSTION ENGINES

This is a continuation, of application Ser. No. 126,830 filed Mar. 22, 1971, and now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electrical fuel control system for internal combustion engines and more particularly to a fuel control system wherein various data representing the operating conditions of an internal combustion engine are processed in a digital form to control the fuel supply to the engine.

2. Description of the Prior Art

In the conventional electrical fuel control systems for internal combustion engines, when determining the amount of fuel injection, the degree of spark advance and so on for controlling the combustion, the parameters such as the intake manifold vacuum, speed, temperature and the angle of rotation of the engine were detected by means of a vacuum sensor and the like, and the analog signals corresponding to the detected parameters were processed in their analog form to determine the amount of fuel injection, the degree of spark advance and so on.

However, with these conventional systems employing analog quantities to represent such parameters, the circuit required for determining the quantity of fuel to be injected, the correct spark timing etc., could not be uniform or standardized and a large number of linear amplifiers were necessary. Thus, these conventional systems have a drawback in that if it is desired to incorporate integrated circuits, such systems are extremely disadvantageous for this purpose, since strong consideration must be given to the generation of heat in the circuits and the rating of various resistors and transistors used must be precisely determined. There is another drawback in that since the methods of computation used are entirely of an analog nature, not only the amount of fuel injection and the spark timing may be easily caused to change by the variation of the power supply voltage and the variation of the ambient temperature, but also a malfunction may be caused by any disturbing noise. There is a further drawback in that since the conventional systems require a large number of linear amplifiers as previously described and moreover these linear amplifiers are of different characteristics, not only the systems tend to be complicated in construction, but they also tend to be costly.

SUMMARY OF THE INVENTION

The principal object of the present invention is therefore to provide a novel fuel control system for internal combustion engines, wherein in order to solve the previously mentioned deficiencies of the prior art, operations such as addition, multiplication and division are performed with digital techniques on those input signals which correspond to the various parameters of an engine to determine the quantity of fuel to be injected and the spark timing, whereby the standardization of the construction of the digital operational circuits is achieved to provide a fuel control system which is not only simple and economical in construction, but also well adapted for incorporating integrated circuits and at the same time unsusceptible to any malfunctions due

to the variations in the power supply voltage and ambient temperature as well as disturbing noises.

Another object of the present invention is the elimination of those deficiencies which may occur if the digital quantities are processed step-wise in the above-mentioned digital computations. That is, it is the elimination of the drawback in that a complicated wiring circuit must be provided with respect to all the combinations involved in the characteristics of an engine, and that such complicated wiring must be repeated for all the different kinds of engines, particularly when the required characteristics of engines installed in automobiles differ depending on the purposes, capacities, etc. of the engines.

According to the present invention, therefore, the above-mentioned object is achieved by means of a computing method in which the amount of fuel injection and the spark timing are determined by subjecting all the information obtained from various sensors to digital computations including multiplication, division and addition, so that particularly any variation in the required engine characteristic can be met with a simple change of the design, while on the other hand the information from every sensor is utilized as far as possible for various characteristic correcting purposes and moreover, the construction of those converters for calculating the volume of injection and the spark timing is standardized so that the similar procedures may be followed both in the process of computing the volume of injection and in the process of determining the spark timing, while the converters which could be substituted by a single common converter are combined into such a single converter in view of the fact that the above-mentioned computations could be satisfactorily performed at different times, thereby achieving a reduction in the number of circuit component parts and hence an improved reliability and a reduction in cost.

The fuel control system according to the present invention comprises sensors for detecting the parameters of an internal combustion engine and converting these parameters into analogical electric signals, analog to digital converters for converting the output signals of the sensors into digital signals, function generators for performing computations on the digital signals from the analog to digital converters to produce fuel control signals that suit the characteristics of the engine, and means for receiving the fuel control signals to control and supply fuel to the engine.

Those effects which are attributable to the present invention may be set forth as follows:

1. Since all the data handled in the operational circuits are coded as binary codes, computations can be performed in a stabilized manner against variations of the power supply voltage and other external conditions such as the ambient temperature. In other words, computations in these circuits can be performed with absolute accuracy provided that there is no disturbance large enough to interfere with the "on" and "off" signals in the circuits. As a counter measure against such disturbance, a well-known integrated circuit may be employed to design a computing circuit which operates with a considerable degree of accuracy.

2. Since the converters for establishing the characteristics of an internal combustion engine generally include similar circuits, a large number of the same elements may be employed to construct these converters

and this permits a reduction of cost by mass production and a standardization of the fabricating operations.

3. When it is necessary to modify the design characteristics for different uses and types of engines, the characteristics may be modified by varying the patterns of addition.

4. Any characteristics of the fuel injection quantity and the spark advance can be attained, no matter what forms, the characteristic curves may take. Particularly, with those latest engines which require characteristics of complicated forms, the present invention is especially useful. Moreover, discontinuous characteristics can even be attained.

5. The accuracy of characteristics can be improved without making any specific provision in the operational circuits, simply by increasing the number of digits contained in any code. Thus, as far as the accuracy of characteristics is concerned, all energies can be devoted to the manufacture of the system of the present invention, solely bearing in mind the accuracy of the sensors incorporated. This means that the system of the present invention is especially useful when used with engines, particularly automobile engines which are run under considerably varying operating conditions.

6. Since the sensors incorporated are common to the fuel injection system and the spark advance system, the system of the present invention is very advantageous from the aspect of cost, and at the same time it can be made smaller and compact and simpler in construction.

7. Since all the computations can be performed on a time-sharing basis, only a single set of operational circuits is required. This permits a reduction in the number of component parts with a resultant decrease in cost and the failure ratio. This reduced failure ratio lends itself to prevent an engine from stopping its rotation.

8. The inputs to the operational circuits which relate to the operating conditions of an engine, such as, the engine speed, temperature and intake manifold vacuum would change very slowly as compared with the computing speed in the operational circuits, and therefore the required computations can be performed satisfactorily according to the time-sharing system mentioned above. With this time-sharing system, the construction of the system of the invention can be made simpler.

9. Since all the information relating to the operating conditions of an engine are handled in coded form and since, with the use of a simple adapter, it is possible to externally observe the outputs of various sensors relating to the engine parameter, the fuel quantity being delivered to the engine, the degree of engine spark advance as well as the values of correction and characteristics under computation and the digital indication of these data in their numerical values are also possible, and the effectiveness of the present invention regarding engine inspection and the checking of engines under repair and during manufacturing processes is immense.

10. Since a time-sharing system is employed, the converters for establishing various characteristics can be effectively utilized with a minimum number of elements so far as the requirements at the maximum speed of an engine can be satisfied.

Since the amount of fuel injection is controlled by digitally correcting an input code corresponding to the

engine temperature, it is possible to increase the accuracy of the correction even more by reducing the amount of fuel represented by the minimum digit of the input code and correcting the input code by an integer multiple of the minimum digit.

The correction of the input code is performed by producing a plurality of binary codes obtainable by successively shifting the input code to the right one place each shift and ignoring the minimum significant digit of each shifted binary code. Thus, the corrected input code remains as having the same number of places as that of the original binary code and represents approximately a multiple of the number represented by the original binary code without undesirably reducing accuracy of the correction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1 through 13 relate to a first embodiment of the present invention, in which:

FIG. 1 is a block diagram showing schematically the general construction of the first embodiment.

FIG. 2 is a diagram showing the output voltage characteristic of an engine intake manifold vacuum sensor.

FIG. 3 is a diagram showing the required fuel injection quantity characteristic of an engine.

FIG. 4 is a diagram showing the required vacuum advance characteristic of an engine. FIG. 5 is a diagram showing the required centrifugal advance characteristic of an engine.

FIG. 6 is a diagram showing the characteristic of the engine with the output of the intake manifold vacuum sensor being inverted.

FIG. 7 is a diagram showing the output voltage characteristic of an engine speed sensor.

FIG. 8 is a block diagram of a converter for establishing the fuel injection quantity characteristic.

FIG. 9 is an electrical wiring diagram of a discriminator.

FIG. 10 is a block diagram of an adder.

FIG. 11 is a block diagram of the discriminator.

FIG. 12 is an electrical wiring diagram showing a part of the adder and the connecting circuits.

FIG. 13 is a block diagram of a converter for establishing the spark advance characteristic.

FIGS. 14 through 23 relate to a second embodiment of the present invention, in which:

FIG. 14 is a block diagram of the second embodiment.

FIG. 15 is a block diagram showing the fuel injection distribution circuit portion and the ignition distribution circuit portion.

FIG. 16 is a detailed block diagram of the fuel injection distribution circuit portion.

FIG. 17 is an electrical wiring diagram showing the constituent elements of a comparator.

FIG. 18 is an electrical wiring diagram of a two-input NAND circuit.

FIG. 19 is an electrical wiring diagram of an eight-input NAND circuit.

FIG. 20 is an electrical wiring diagram of the distributor.

FIG. 21 is a waveform diagram showing the voltage waveforms which appear at various portions of the distributor shown in FIG. 20.

FIG. 22 is an electrical wiring diagram of the ignition distributor circuit portion.

FIG. 23 is a waveform diagram showing the voltage waveforms which appear at the various portions of the ignition distribution circuit.

FIGS. 24 through 31 relate to a third embodiment of the invention in which:

FIG. 24 is a block diagram of the third embodiment.

FIG. 25 is a block diagram showing the fuel injection distribution circuit portion and the ignition distribution circuit portion.

FIG. 26 is a detailed block diagram of the fuel injection distribution circuit portion.

FIG. 27 is an electrical wiring diagram of the fuel injection distribution circuit.

FIG. 28 is an electrical wiring diagram of the ignition distribution circuit.

FIG. 29 is an electrical wiring diagram of a selection signal generator.

FIGS. 30 and 31 are waveform diagrams showing the voltage waveforms which appear at various portions of the ignition distribution circuit and a selector circuit, respectively.

FIGS. 32 through 53 relate to a fourth embodiment of the invention, in which:

FIG. 32 is a block diagram showing schematically the general construction of the fourth embodiment.

FIG. 33 is a block diagram showing the arrangement for determining the increased fuel quantity for acceleration and the air-fuel ratio setting in accordance with the signal input corresponding to the engine throttle valve opening speed and the engine throttle valve position, respectively.

FIG. 34 is a characteristic diagram showing the additional fuel quantity required for the engine engine for acceleration.

FIG. 35 is a characteristic diagram showing the increased fuel quantity for the air-fuel ratio setting required for the engine.

FIG. 36 is a block diagram showing an arrangement for determining the amount of fuel injection and the degree of vacuum advance according to the engine intake manifold vacuum.

FIG. 37 is a characteristic diagram showing the steady state fuel injection quantity requirement of the engine.

FIG. 38 is a characteristic diagram showing the vacuum advance requirement of the engine.

FIG. 39 is a block diagram showing an arrangement for determining the additional fuel quantity needed for the starting and warming-up operations of the engine, respectively.

FIG. 40 is a characteristic diagram showing the additional fuel quantity requirements of the engine for starting and warming-up operation thereof.

FIG. 41 is a block diagram showing an arrangement for determining the total amount of injection required for the engine.

FIG. 42 is a block diagram showing an arrangement for determining the degree of centrifugal spark advance required for the engine.

FIG. 43 is a characteristic diagram showing the spark advance requirement of the engine.

FIG. 44 is a block diagram showing an arrangement for determining the total engine spark advance.

FIG. 45 is a block diagram of an adder.

FIG. 46 is a block diagram showing an arrangement for setting the patterns which determine the amount of

fuel injection according to the engine intake manifold vacuum.

FIG. 47 is a schematic diagram of a coder for the input codes from the engine.

FIG. 48 is a schematic diagram showing the connections between the codes and the adder.

FIG. 49 is a schematic diagram showing the connections between the codes and memory circuits.

FIG. 50 is a schematic diagram of an operation command signal generator.

FIG. 51 is a schematic diagram of a coding command signal generator operated by the operation command signals.

FIG. 52 is a schematic diagram showing the interconnections between the operational circuits and the memory circuits.

FIG. 53 is a block diagram for explaining the sequence in which the amount of fuel injection and the spark advance required for the engine are to be determined.

FIGS. 54 through 68 relate to a fifth embodiment of the invention, in which:

FIG. 54 is a block diagram showing an arrangement for determining the amount of fuel injection and the degree of spark advance according to the engine intake manifold vacuum.

FIG. 55 is a schematic diagram of a coder for the input codes from the engine.

FIG. 56 is a schematic diagram showing the interconnections between the codes and memory circuits.

FIG. 57 is a block diagram showing an arrangement for generating gear shifting commands for an automatic transmission.

FIG. 58 is a characteristic diagram showing the gear shifting requirement of the automatic transmission.

FIG. 59 is an electrical wiring diagram of a delay circuit.

FIG. 60 is a block diagram for explaining the sequence in which the amount of fuel injection and the degree of spark advance for the engine and the gear shifting of the automatic transmission are determined.

FIG. 61 is a block diagram showing an arrangement for determining the proper or improper movement of the gearshifts in relation to the vehicle speed. FIG. 62 is a schematic diagram of discriminators and coders for determining the proper or improper movement of gear shifts in relation to the vehicle speed.

FIG. 63 is a schematic diagram of an operation command signal generator.

FIG. 64 is a schematic diagram of a coding command signal generator operated by the operation command signals.

FIG. 65 is a diagram of a connecting circuit interconnecting the operational circuit and the memory circuits.

FIG. 66 is a block diagram of a sequencer.

FIG. 67 is a waveform diagram for explaining the operation of the sequencer.

FIG. 68 is a schematic diagram of the clock pulse generator portion.

FIGS. 69 through 75 relate to a sixth embodiment of the invention, in which:

FIG. 69 is a block diagram showing the general construction of the sixth embodiment.

FIG. 70 is a characteristic diagram showing the fuel injection quantity requirement of an engine in relation to the engine intake manifold vacuum.

FIG. 71 is a block diagram of an arrangement for determining the amount of fuel injection in accordance with the engine intake manifold vacuum alone.

FIG. 72 is an electrical wiring diagram of the first and second discriminators.

FIG. 73 is a block diagram of an arrangement for determining the amount of fuel injection with the engine intake manifold vacuum, engine temperature and engine start signals.

FIG. 74 is an electrical wiring diagram of coders for determining the addition patterns.

FIG. 75 is an electrical wiring diagram of a coder for determining the engine intake manifold vacuum.

FIGS. 76 through 78 relate to a seventh embodiment of the invention, in which:

FIG. 76 is a block diagram of a fuel injection system.

FIG. 77 is a block diagram of a fuel injection distribution circuit portion.

FIG. 78 is a detailed block diagram of the fuel injection distribution circuit portion.

FIGS. 79 through 82 relate to an eighth embodiment of the invention, in which:

FIG. 79 is a block diagram showing the general construction of the eighth embodiment,

FIG. 80 is a detailed block diagram showing the principal part of the embodiment of FIG. 79.

FIG. 81 is a detailed electrical wiring diagram of the principal part shown in FIG. 80.

FIG. 82 is a waveform diagram showing the voltage waveforms for explaining the operation of the present embodiment.

FIGS. 83 through 87 relate to a ninth embodiment of the invention, in which:

FIG. 83 is a block diagram showing the general construction of the ninth embodiment.

FIGS. 84a and 84b are a longitudinal sectional view and a plan view of a reference rotational position signal generator.

FIG. 85 is a plan view of a rotational position signal generator.

FIG. 86 is an electrical wiring diagram of a binary code analog to digital converter.

FIG. 87 is a waveform diagram showing the voltage waveforms which appear at various portions of the converter of FIG. 86.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1:

In FIG. 1 illustrating a block diagram of the system according to a first embodiment of the present invention, numeral 1 designates a sensor (hereinafter referred to as a vacuum sensor) which is mounted on the engine to convert the engine intake manifold vacuum into a voltage. Numeral 2 designates an A - D converter for converting the output voltage of the vacuum sensor 1 into a binary code. Numeral 3 designates a function generator which receives the output of the A - D converter 2 to compute the amount of fuel injection in terms of binary codes; 4 an adder for adding the computational results. Numeral 5 designates an injection circuit which injects a fuel into the engine in response to the output signal of the adder 4. Numeral 6

designates an inverter which inverts the output of the vacuum sensor 1; 7 a sensor (hereinafter referred to as an engine speed sensor) which produces a voltage proportional to the engine rpm. Numeral 8 designates an analog to digital (A - D) converter for converting the output of the inverter 6 into a binary code, 9 a converter for converting the output value of the A - D converter 8 into a spark advance. Numeral 10 designates an A - D converter which converts the output voltage of the engine speed sensor 7 which is proportional to the engine rpm into a binary code; 11 a function generator which converts the output value of the A - D converter 10 into a spark advance. Numeral 12 designates an adder which forms the sum of the spark advance signal from the converter 9 representing the vacuum advance and the spark advance signal from the function generator 11 representing the rotational spark advance; 13 an ignition circuit which ignites according to the total spark advance determined by the adder 12.

The vacuum sensor 1 detects the vacuum developed in the engine intake manifold as the engine rotates and it then converts the detected vacuum into an output voltage. The values of this output voltage will be as shown in FIG. 2, for example. In FIG. 2, the abscissa represents the intake manifold vacuum V_a whose value is +760 mHg, i.e., the atmospheric pressure at the origin of the coordinate and the pressure at that point on the horizontal axis which is designated as O, representing a vacuum. The ordinate represents the output voltage V_a of the vacuum sensor 1 whose value is 0 volt at the coordinate origin and it increases in potential as the ordinate lengthens upward. This voltage is converted into a binary code in the A - D converter 2 and the signal in this binary form is then applied to the function generator 3 which performs a computation to obtain the relationship between the intake manifold vacuum V_a and the amount of fuel injection as shown in FIG. 3. In the characteristic shown in FIG. 3, the curve is broken at two points $V_{a\alpha}$ and $V_{a\beta}$ of the intake manifold vacuum V_a . A method by which this characteristic is obtained will be explained later. Then, the output signals produced by the computation in the function generator 3 are added and converted into a code corresponding to the fuel injection quantity q , whereupon a fuel whose amount of injection is determined according to this code is injected into the engine cylinders by means of the injection circuit 5.

On the other hand, the spark advance according to the engine intake manifold vacuum will vary as shown in FIG. 4. In this figure, the abscissa represents the intake manifold vacuum V_i and the ordinate represents the vacuum advance θ_{va} . This required engine spark advance characteristic has a tendency inversely corresponding to that of the required fuel injection quantity characteristic mentioned above. Thus, the inverter 6 is provided to reverse the output characteristic of the vacuum sensor 1, the inverter 6 produces an output as shown in FIG. 6. In FIG. 6, the abscissa represents the intake manifold vacuum V_a and the ordinate represents the output voltage $\bar{V}_{va}$ of the inverter 6. In this connection, the inversion of the output characteristic of the vacuum sensor 1 may be effected in an alternative manner in which the output signal of the vacuum sensor 1 is first converted into a binary code and then the complement of this binary code is formed. The output of the inverter 6 is converted by the A - D converter 8 into a binary code which is in turn converted into an

other binary code representing the amount of spark advance corresponding to the required spark advance characteristic of the engine. On the other hand, the output characteristic of the engine speed sensor 7 for detecting the speed of the engine is shown in FIG. 7 and the output of the sensor 7 is converted into a definite amount of spark advance corresponding to the required spark advance characteristic of the engine. This rotational spark advance characteristic required for the engine is shown in FIG. 5. In FIG. 5, the abscissa represents the engine speed n and the ordinate represents the rotational spark advance θ_n . The binary codes thus obtained are first converted into the corresponding amounts of vacuum advance and rotational advance, respectively, and the sum of the two spark advances is then formed in the adder 12. The total amount of spark advance thus obtained is applied to the ignition circuit 13 which in turn effects the required ignition according to the degree of spark advance as determined by this total amount of spark advance. A readout circuit is included in the injection circuit 5 and the ignition circuit 13, respectively, and in the injection circuit 5 the fuel quantity q delivered is read out by a clock pulse of a definite time duration, since the fuel quantity q is determined by the duration of the injection. On the other hand, with the ignition circuit 13 the read operation is effected by the clock pulses having a time duration corresponding to the unit angle of the engine.

The manner in which the above described characteristics are computed will now be explained. To start with, a block diagram of an arrangement for computing the amount of fuel injection according to the intake manifold vacuum is illustrated in FIG. 8. In this figure, V_a denotes an input representing the engine intake manifold vacuum converted into a signal in the binary code and a block labelled V_a indicates a circuit for producing the signal V_a , i.e., the A-D converter. Other blocks shown in this and other figures, as described hereinafter, indicate respective circuits in the same manner; $F(V_{a\alpha})$ a first discriminator for determining whether the input V_a is greater or smaller than the value of the intake manifold vacuum at the point $V_{a\alpha}$ in FIG. 3; $F(V_{a\beta})$ a second discriminator for similarly determining whether the input V_a is greater or smaller than the intake manifold vacuum at the point $V_{a\beta}$ in FIG. 3. Numeral 101 designates a logical element for producing a "L" signal when V_a is greater than both $V_{a\alpha}$ and $V_{a\beta}$; 102 an inverter; 103 a logical element for producing a "L" signal when it finds that $V_{a\beta} < V_a < V_{a\alpha}$; 104 and 105 inverters; 106 a logical element for producing a "L" signal when it is found that $V_a < V_{a\beta}$. Designated as V_{a5} is a five-place binary code input which represents the value of V_a as it is. V_{a4} designates the value of V_a which is shifted one place to the right so that the least significant digit is lost, thus changing the five-place binary number to a four-place binary number; V_{a3} the value of V_{a4} shifted one place to the right to produce a three-place binary number; V_{a2} the value of V_{a3} shifted one place to the right to produce a two-place binary number; V_{a1} the value of V_{a2} shifted one place to the right to produce a single-place binary number. V_{a0} designates a preset definite numerical value. Designated as J_{15} is a connecting circuit for coupling the five-place V_{a5} to the adder 4, and J_{14} , J_{13} , J_{12} , J_{11} and J_{10} designate circuits for respectively coupling the values of the four-place V_{a4} , the three-place V_{a3} , the two-place V_{a2} , the single-place V_{a1}

and V_{a0} to the adder. Numeral 107 designates a logical element which indicates that J_{15} is to be coupled to the adder 4. Similarly, numerals 108, 109, 111, 112 and 110 designate logical elements for respectively indicating that J_{14} , J_{13} , J_{11} , J_{10} and J_{12} are to be coupled to the adder 4.

With the arrangement described above, the operation will now be explained. To begin with, as the binary code input V_a is introduced, all of V_{a5} , V_{a4} , V_{a3} , V_{a2} , V_{a1} and V_{a0} are set up. Simultaneously, the value of V_a is compared with that of $V_{a\alpha}$ in the discriminator $F(V_{a\alpha})$ to determine whether the former is greater or smaller than the latter. Now, if the value of V_a is smaller than that of $V_{a\alpha}$, it is further compared with $V_{a\beta}$ in the second discriminator $F(V_{a\beta})$. If the result of the comparison indicates that the value of V_a is $V_a > V_{a\alpha}$, then the conditions $V_a > V_{a\alpha}$ and $V_a > V_{a\beta}$ exist and hence $F(V_a) = F(V_{a\beta}) = 1$, so that the logical element 101 produces a "L" signal. When this happens, each of the logical elements 107, 109, 110, 111 and 112 connected to the output of the logical element 101 produces an "H" output, so that V_{a5} , V_{a3} , V_{a2} , V_{a1} and V_{a0} are now ready for connection to the adder 4. In other words, J_{15} , J_{13} , J_{12} , J_{11} and J_{10} are now placed in condition for connection to the adder 4. Commands for coupling the J_{15} , J_{13} , J_{12} , J_{11} and J_{10} to the adder 4 are issued by way of a separate circuit. Consequently, when the condition $V_a > V_{a\alpha}$ is met, the fuel quantity delivered is given as $q = V_{a5} + V_{a3} + V_{a2} + V_{a1} + V_{a0}$ and this value is applied to the injection circuit 5. Similarly, when there is the condition $V_{a\beta} < V_a < V_{a\alpha}$, the fuel quantity delivered is given as $q = V_{a4} + V_{a3}$, and when $V_a < V_{a\beta}$, $q = V_{a0}$. Since V_a is the five-place binary number, there exists the relation $V_{a5} \approx 2V_{a4} \approx 4V_{a3}$. Thus, the value of q , the fuel quantity delivered, is determined from a combination of selected ones of the values of V_{a5} , V_{a4} , V_{a3} , V_{a2} , and V_{a1} . For example, if selected only V_{a5} or V_{a4} or V_{a3} , the value of q becomes roughly 1.0 V_a , 0.5 V_a or 0.25 V_a , respectively. If selected a combination of V_{a5} and V_{a3} or V_{a5} , V_{a4} and V_{a3} , or V_{a4} and V_{a3} , the value of q becomes 1.25 V_a , 1.75 V_a or 0.75 V_a , respectively. Other various values of q may be obtained by changing the combination. The value of V_{a0} may also be added to each of these values to obtain the value of q .

The operation described above will now be explained in detail with reference to an actual circuit. The circuit construction of the first and second discriminators $F(V_{a\alpha})$ and $F(V_{a\beta})$ will be as shown in FIG. 9. In this figure, numerals 120, 122, 124 and 126 designate NAND elements which decide whether the signal in each of the positions 2^4 through 2^1 is "H" or "L." Numerals 121, 123 and 135 designate inverters which invert the signal from "L" to "H" and vice versa; 128, 130, 131 and 132 logical elements which perform the operation of comparison on the respective digits to give an indication of agreement or disagreement; 129 an inverter; 133 and 134 NAND elements, where all the logical elements employed are composed of NAND elements. With this construction, the operation of the discriminators will be explained with reference to the first discriminator $F(V_{a\alpha})$. The preset value of $V_{a\alpha}$ in this circuit is represented in the binary code as 10110 and the comparison operation is performed in the following manner to find whether V_a is greater than this preset value. Now, a "H" signal is applied to one of the input terminals of the NAND elements 120, 122, 124

and 126, respectively, and the five-place signal V_{a5} at the top is applied to the other input terminal of the NAND element 120. Then, if V_{a5} is "H," the NAND element 120 produces a "L" output signal and this is applied to the NAND element 128 which in turn produces an "H" signal at its output. On the other hand, the output of the NAND element 120 is inverted by way of the inverter 121, so that if V_{a5} is "H," the output of the inverter 121 is "H." Next, if V_{a4} is "H," the output of the inverter 129 is "L" and hence the output of the NAND element 122 is "H." In this case, the output of the NAND element 130 is "L" and it is thus established that the value of V_a is greater than that of $V_{a\alpha}$, that is, the comparison $V_a > V_{a\alpha}$ exists. This output of the NAND element 130 is then applied to one of the input terminals of the NAND element 134 so that an "H" signal is produced at its output terminal L_a . In other words, the comparison $V_a > V_{a\alpha}$ is established. Similarly, the operation of comparison is performed on the three-place number and the two-place number, respectively, so that if $V_a > V_{a\alpha}$, an "L" signal is introduced at either one of the input terminals of the NAND element 134 which in turn produces an "H" signal at its output terminal L_a . On the other hand, if $V_a < V_{a\alpha}$, an "L" signal is introduced at either one of the input terminals of the NAND element 133 so that an "H" signal is produced at its output terminal S_M . The signal produced at the terminal L_a is applied to the NAND element 101, while the signal produced at the terminal S_M may be applied directly to the NAND element 103 in place of the signal from the inverter 102. As to the single-place code, there is the condition $V_a > V_{a\alpha}$ if $V_{a1} = 1$ and $V_a = V_{a\alpha}$ if $V_{a1} = 0$ and thus the discriminator may be dispensed with for V_{a1} if the value at the break point in FIG. 3 is chosen so that $V_a > V_{a\alpha}$. Therefore, the circuit is prearranged so that if the value of V_a agrees with respect to the four most significant bits 1011 of the preset binary number 10110 in the first discriminator $F(V_{a\alpha})$, then the condition $V_a > V_{a\alpha}$ is present. It is also prearranged so that the comparison on the most significant bit is performed by comparing the output of the NAND element 120 with an "H" to make a discrimination between "H" and "L," while the comparison operation on the lower order bits is performed only when there is found no agreement thereabout, since the existence of agreement on any higher order bit is indicated by the "H" output of the corresponding inverter. The identical circuit as used with the first discriminator $F(V_{a\alpha})$ may be constructed for the second discriminator $F(V_{a\beta})$. In other words, what is needed is simply to construct a circuit identical with that of the first discriminator excepting that it employs a different binary number in place of the preset number 10110 of the first discriminator $F(V_{a\alpha})$. In the second discriminator $F(V_{a\beta})$, it is also possible to eliminate the comparison operation on the least significant bit, if it is prearranged in the manner described above that the condition $V_a \leq V_{a\alpha, \beta}$ is met when the comparison of the least significant bit produces an "H."

Next, the manner in which the sum of any given numbers is formed in the adder 4 of FIG. 8 will be explained with reference to FIG. 10. For purposes of simplicity, the digits to be added are designated as X, Y, Z, U, V, W and α . The added suffixes 1, 2, ..., i, ..., n indicate the number of places from the least significant position. Designated as A are adders; J discriminators; S and S'

memories for storing the sum of numbers, which are generally designated as memory groups Me and M'e, respectively. Designated as Reset and Reset' are reset terminals which clear the memory groups Me and M'e. In these adders, three digits can be added simultaneously and so three addition signals X_1 , Y_1 and Z_1 will be coupled to the input terminals of the discriminator J_1 . In the adder A_1 , it is possible that an addition performed produces a carry so that the adder for the next lowest order bit adds three digits comprising two variables X_i and Y_i and a carry C_{i-1} . Similarly, the operation of addition is performed on all of the n binary digits. This addition is performed simultaneously from the lowest order bit to the highest order bit by means of a pulse signal $P_{J, XY}$. The sum for each digital position is stored in the corresponding memory in the memory group Me. The application of the next signal $P_{J, Z}$ causes the addition of the sum of the lowest digits U_1 and V_1 and the partial sum stored in the S_1 , Z_1 and the partial sum stored in the memory S_i , so that the result obtained is stored in the memory S'_i . Then, a reset pulse is applied to the reset terminal to clear the memories in the memory group Me. Whereupon, another pulse $P_{J, U}$ is applied so that the sum of the lowest order digits W_1 and α which are corresponding to V_{a5} , V_{a4} , V_{a3} , V_{a2} , ... and V_{a0} , respectively, the partial sum stored in the memory S'_1 , U_1 and the partial sum stored in the memory S'_i is formed. The result of this operation is stored in the memory S_i . Similarly, the addition is repeated with the resulting partial sum being stored alternately in the memory groups Me and M'e, respectively. During the addition of the least significant digits, a greater number of variables can be handled than in the addition of higher order digits. Consequently, in the addition of V_{a5} , V_{a4} , ..., V_{a1} representing the value of the intake manifold vacuum V_a and the same value shifted one or more places to the right, for example, the correct sum can be obtained with a smaller number of addition. Furthermore, once the addition for the least significant digit position is completed, it is possible to perform more addition for the next least significant digit position than for other higher order positions, thus providing that the method of addition described above is extremely convenient. Then, the result finally remaining in the memories S or the memories S' represents the sum total whose value constitutes the very value that indicates the duration of injection.

Referring now to FIG. 11, there is shown the construction of the discriminator J. In FIG. 11, reference character P_C designates a clock pulse generator for producing clock pulses comprising a continuous train of short duration pulses; R_1 , R_2 , ..., R_{4m+2} ring counters; P_{J1} , P_{J2} , ..., P_{J4m+2} output pulses of the ring counters R_1 , R_2 , ..., R_{4m+2} ; J_1 , J_2 , ..., J_{2m+1} connecting circuits for coupling to adders those circuits in each of which the vacuum output V_a is substituted by V_{a5} , V_{a4} , ..., V_{a0} ; 156 a NAND element for resetting the memory group Me; 157 a NAND element for resetting the memory group M'e. S_1 , S_2 , ..., S_n designate reset terminals adapted to be connected to the memory blocks of the memory group Me corresponding to the respective digit positions. In the first place, upon the completion of a first addition the sum in the adder A is entered into the memories S and the result of a second addition is entered into the memories S', and thus it is necessary to reset the memories S in the memory group Me before the operation of a third addition is performed.

Thereafter, for every subsequent addition either the memories S in the memory group Me or the memories S' in the memory group M'e must be alternately reset. It is also necessary that ultimately the final result of the addition is read out and both the memory groups Me and M'e are reset to prepare for the next series of computations. The sequence of this process will now be explained. In the first place, clock pulses P_c having a period of a definite time are applied to the ring counters $R_1, R_2, \dots, R_{4m+2}$. Upon the application of the first clock pulse, the ring counter R_1 is set and it produces an output pulse P_{J1} at its output terminal so that the discriminator J_1 is coupled to the adder. Actually, one connecting circuit is provided for each digit position of $V_{a5}, V_{a4}, \dots, V_{a0}$. Accordingly, if

$$\sum_{i=0}^5 V_{ai},$$

at the time that the ring counter R_1 produces its output signal P_{J1} upon application of the first clock pulse, the discriminator J connected respectively to the digit positions $va1$ to $va5$ of V_{a5} , the digit positions $va1$ to $va4$ of V_{a4} and the least significant digit position of V_{a3} , is coupled to the adder A. This represents the connecting circuit J_1 shown in FIG. 11. When another one of the clock pulses P_c is applied, the ring counter R_1 is restored to its original state and the ring counter R_2 produces an output signal P_{J2} at its output terminal, thereby coupling the connecting circuit J_2 to the adder. In this state, similarly the respective memories S in the memory group Me, the two most significant digit positions of V_{a3} and the least significant digit position of V_{a0} are coupled to the adder. This represents the connecting circuit J_2 . As a further one of the clock pulses is applied, the ring counter R_2 is returned to its initial state and the ring counter R_3 produces an output signal P_{J3} at its output terminal so that, after being inverted in the inverter 150, this output signal P_{J3} is applied to the input of the NAND element 150 which in turn produces a reset pulse at its output. This reset pulse clears the memories $S_1, S_2, \dots, S_n$ in the memory group Me. Similarly, a subsequent application of the clock pulse causes the ring counter R_4 to produce an output signal P_{J4} at its output so that in like manner an addition is performed and the memory group M'e is eventually reset upon application of a succeeding one of the clock pulses. This process is repeated until the required computations are completed. Then, in the final stage of the addition with the ring counter R_{4m} producing an output signal P_{J4m} at its output, the succeeding clock pulse causes the ring counter R_{4m+1} to produce an output signal P_{J4m+1} at its output so that the final result of the addition contained in the memories which are in this case the memories S_i in the memory group Me and read out. Whereupon, the ring counter R_{4m+2} is caused by another succeeding clock pulse to produce an output signal P_{J4m+2} at its output so that the memories S_i and S'_i in the memory groups Me and M'e are reset to prepare for the next series of computations.

Referring now to FIG. 12, there is shown an embodiment of the adders described above. In this figure, reference character P_{J1} designates a signal for commanding the connection to the adder A, $va1, va1'$ are $va1''$ the least significant digits to be added. Numeral 160, 161 and 162 designate NAND elements for coupling

$va1, va1'$ and $va1''$ to the adder; 163, 164 and 165 inverters; 166, 167, 168, 169, 170, 171, 173 and 174 adding NAND elements; 172 an inverter; S_1 an "L" or "H" signal retained in the least significant digit position, C_{u1} a carry signal. When the signal P_{J1} is applied to the NAND element 160, 161 and 162, $va1, va1'$ and $va1''$ are coupled to the adder. The NAND elements 168, 169 and 170 detect the condition that any two of $va1, va1'$ and $va1''$ are "H" signals. If the output of any one of the NAND elements 168, 169 and 170 is an "L" signal, the NAND element 171 acts as a NOR circuit which produces a carry signal "H" and this carry signal appears at a terminal C_u . NAND element 167 detects that $va1, va1'$ and $va1''$ are all "H" signals and upon detecting this it instructs the memory S_1 for the least significant digit position. The NAND element 166 detects that at least one of $va1, va1'$ and $va1''$ is an "H" signal so that excepting when two of $va1, va1'$ and $va1''$ are "H" signals, the NAND element 173 retains an "H" signal at a terminal S. Further, the NAND element 174 detects the conditions in which at least one of $va1, va1'$ and $va1''$ is an "H" signal and all three are "H" signals, respectively, and it then instructs the memory S_1 in the memory group Me to store "H". As for the next least significant digit position, a circuit which operates similarly but has the signal C_{u1} in place of $va1''$ is constructed according to FIG. 10. In like manner, the adder A may be constructed for each of the higher order digit positions including the highest order digit position.

While the arrangement for computing the volume of fuel injection according to the engine intake manifold vacuum has been described, the spark timing can also be computed in exactly like manner. FIG. 13 illustrates a block diagram of an arrangement required for this purpose. In FIG. 13, letter $\bar{V}_a$ designates a binary code representing the inverted intake manifold vacuum; $I(V_{1\alpha})$ and $I(V_{1\beta})$ discriminators for determining whether the value of V_a is greater or smaller than the values at the points $V_{1\alpha}$ and $V_{1\beta}$, respectively; V_{101} and V_{102} constant setting elements; V_{15} ; V_{14} and V_{13} code signals representing the value of $\bar{V}_a$ shifted to the right to produce five-place, four-place and three-place numbers, respectively; 0 a zero setting; $J_{101}, J_{15}, J_{14}, J_{13}, J_{10}$ and J_{102} circuits for coupling $V_{101}, V_{15}, V_{14}, V_{13}, V_{10}$ and V_{102} to an adder; 201 and 202 inverters; 203, 204 and 205 NAND elements for determining the region in which the intake manifold vacuum code lies. Letters $J_{101}, J_{102}, J_{15}, J_{14}, J_{13}$ and J_{10} which are added at the output terminals of the NAND elements 203, 204 and 205 indicate that these NAND elements are connected to respective ends of the connecting circuits $J_{101}, J_{102}, \dots, J_{10}$. Designated as RPM is a binary code representing the engine speed; $I(R_\alpha), I(R_\beta)$ and $I(R_\gamma)$ discriminators for determining whether the value of RPM is greater or smaller than the values of engine speed at the break points; 206, 207 and 208 are inverters; 208, 209, 210, 211 and 212 NAND elements which receive the output of the discriminators to determine the region in which the input RPM lies; R_5, R_4, R_3 and R_2 set values obtained by shifting to the right of the input RPM; R_{01}, R_{02} and R_{03} constants set independent of the input RPM; 0 a zero setting. Designated as $J_{R5}, J_{R4}, \dots, J_{R0}$ are connecting circuits and letters $J_{R01}, \dots, J_{R0}$ added at the outputs of the NAND elements 209, 210, 211 and 212 represent respective ends of the inputs of the like referenced connecting circuits.

With the arrangement described above, the operation will now be explained. In the vacuum advance characteristic diagram of FIG. 4, the curve of the input $\bar{V}_a$ are broken at the points $V_{I\alpha}$ and $V_{I\beta}$. Then, the discriminators $I(V_{I\alpha})$ and $I(V_{I\beta})$ determine whether the value of $\bar{V}_a$ is greater or smaller than the values at the points $V_{I\alpha}$ and $V_{I\beta}$. Further, the NAND elements 203, 204 and 205 detect whether the value of $\bar{V}_a$ lies in the region $\bar{V}_a < V_{I\beta}$, $\bar{V}_{I\beta} < \bar{V}_a < V_{I\alpha}$ or $\bar{V}_a > V_{I\alpha}$.

The amount of vacuum advance is determined according to these three regions on the graph, as follows:

If $\bar{V}_a < V_{I\beta}$, then the amount of vacuum advance $\theta_v = 0$.

If $V_{I\beta} < \bar{V}_a < V_{I\alpha}$, then $\theta_v = V_{I5} + V_{I4} + V_{I3} + V_{I02}$.

If $\bar{V}_a > V_{I\alpha}$, then $\theta_v = V_{I10}$.

These are the connections provided by the connecting circuits so that the results of the addition performed in the adder A produce the curve as shown in FIG. 4. Similarly, the region in which the input RPM lies with respect to the break points R_α , R_β and R_γ of the engine speed spark advance curve is determined by the discriminators $I(R_\alpha)$, $I(R_\beta)$ and $I(R_\gamma)$ as well as the inverters 206, 207 and 208 and the NAND elements 209, 210, 211 and 212, as follows:

If $RPM < R_\gamma$, then the amount of rotational advance $\theta_R = 0$.

If $R_\gamma < RPM < R_\beta$, then $\theta_R = R_4 + R_3 + R_{03}$.

If $R_\beta < RPM < R_\alpha$, then $\theta_R = R_5 + R_2 + R_{02}$.

If $R_\alpha < RPM$, then $\theta_R = R_{01}$. From the foregoing, the characteristic curve shown in FIG. 5 results. Then, an addition $\theta_v + \theta_R$ is performed to ultimately determine the amount θ of the total spark advance.

While in the embodiment described above the engine intake manifold vacuum and speed are detected as engine parameters, it is apparent that other parameters of the engine, such as, the starting conditions and temperature of the engine, the opening speed and position of the throttle valve and so on may be detected. Furthermore, it is evident that the application of the fuel control system of the present invention is not limited to the ignition system and the fuel injection system as in the case of the above described embodiment, but it can be equally applied to the automatic driving system for engines and so on.

Embodiment 2

Referring to FIG. 14 illustrating a second embodiment of the present invention incorporating both the fuel injection system and the ignition system of an engine, numeral 1100 designates a sensor circuit; 1110 a vacuum sensor for producing a DC output voltage proportional to the amount of vacuum in the intake manifold of an internal combustion engine which is not shown; 1120 an engine speed sensor for producing a DC output voltage proportional to the number of revolutions of the rotating shaft of the engine; 1130 a temperature sensor which detects the temperature of the engine to produce a DC output voltage proportional to the detected engine temperature. Numeral 1140 designates a timing sensor for producing a pulse signal voltage according to the rotational speed of a shaft correlated to the rotating shaft of the engine; 1150 an angular sensor for producing 180 pulse signals for every rotation of the shaft correlated to the rotating shaft of the engine, that is, this sensor produces one pulse signal for every two degrees of rotation of the engine shaft. Nu-

meral 1200 designates A - D converters for converting the DC output voltages of the vacuum sensor 1110, engine speed sensor 1120 and temperature sensor 1130 into corresponding digital signals in the binary code, and 1210 designates an A - D converter for converting the DC output voltage of the vacuum sensor 1110 into a digital signal in binary form, 1220 an A - D converter for converting the DC output voltage of the engine speed sensor 1120 into a digital signal in binary form, 1230 an A - D converter for converting the DC output voltage of the temperature sensor 1130 into a digital signal in binary form. Numeral 1300 designates function generators 1310 a function generators for converting the output binary code signal of the A - D converter 1120 into another binary digital signal to suit the fuel quantity requirement of the engine and for obtaining still another binary code signal that suits the spark timing requirement, i.e., the spark advance characteristic of the internal combustion engine, 1320 a function generators for converting the output binary code signal of the A - D converter 1220 into another binary code signal to suit the spark timing characteristic, i.e., the rotational advance characteristic required for the engine, 1330 a function generators for converting the output signal of the A - D converter 1230 into another binary code signal to increase or decrease the volume of fuel injection by a proper amount in accordance with the degree of temperature within the engine. Numeral 1510 designates a first operational circuit for performing an addition on the output binary code signals of the function generators 1310 and 1330 to produce an injection binary code signal corresponding to the fuel injection duration; 1520 a second operational circuit for performing an addition or subtraction on the output binary code signals of the function generators 1310 and 1320 to produce an output binary code signal corresponding to the spark timing, i.e., the spark advance characteristic. Numeral 1710 designates a first memory circuit (hereinafter referred to as an injection memory) for storing the output binary code signal of the first operation circuit 1510 corresponding to the fuel injection duration. Numeral 1720 designates a second memory circuit (hereinafter referred to as an ignition memory) for storing the output binary code signal of the second operational circuit 1520 corresponding to the ignition timing of the engine. Numeral 1810A designates an injection distributor for distributing the content, i.e., the digital signal stored in the injection memory 1710 in accordance with the output signals of the timing sensor 1140 so that the digital signal is distributed to the solenoid valves for the respective engine cylinders in accordance with the order of fuel injection; 1810B an ignition distributor for distributing the digital signal stored in the ignition memory 1720 by virtue of the output signals of the timing sensor 1140 in accordance with the firing order of the respective engine cylinders. Numeral 1820A designates a first counter (hereinafter referred to as an injection counter) which counts the output pulse signals of the clock pulse generator 1840 and it stops its counting operation and erases the content of the injection memory 1710 when the count reaches or equals the content of the injection memory 1710; 1820B a second counter (hereinafter referred to as an ignition counter) which counts the output pulse signals of the angular sensor 1150 so that it stops its counting operation and erases the content of the ignition memory 1720 when the count attains or

equals the content of the ignition memory 1720. Numeral 1840 designates a clock pulse oscillator which generates pulse signals of a predetermined frequency when the injection counter 1820A initiates its operation so that the counter 1820A may count the duration of the fuel injection. Numeral 1920A designates a solenoid valve mounted in the engine intake manifold (not shown) adapted to initiate the injection of fuel by the output signal of the injection counter 1820A, that is, when it starts counting the clock pulses from the clock pulse oscillator 1840 and to stop the injection of fuel when the counter 1820A completes and stops its counting operation. Numeral 1920B designates an ignition system to have an ignition spark produced by one of the spark plugs mounted at the respective engine cylinders by way of the distributor rotor rotatable in correlation with the rotating shaft of the engine which is not shown, after the the ignition counter 1820B initiates the counting of the output pulses of the angular sensor 1150 and then completes the counting.

With the arrangement described above, the operation of the fuel injection system and the ignition system in the present embodiment will now be explained. In the first place, the ignition memory 1720 stores the output digital signal of the second operational circuit 1520 which corresponds to the spark timing and which is derived from the operation on the output digital signals from the function generator 1320 for the engine speed sensor 1120 and the function generator 1310 for the vacuum sensor 1110. On the other hand, the injection memory 1710 stores the output digital signal of the first operational circuit 1510 which corresponds to the duration of the fuel injection and which is derived from the operation on the output digital signal of the function generator 1310 for the vacuum sensor 1110 and the output digital signal of the function generator 1330 for the temperature sensor 1130. In this way, the binary code digital signals are first stored in the ignition memory 1720 and the injection memory 1710, respectively, and then the injection distributor 1810A and the ignition distributor 1810B are brought into action by the timing signals produced by the timing sensor 1140 and the injection counter 1820A starts to count the clock pulses produced by the clock pulse oscillator 1840. Simultaneously, the solenoid valve 1920A is energized so that the solenoid valve 1920A initiates the injection of fuel. Thereafter, as the binary code digital signal counted by the injection counter 1820A becomes equal to the binary code digital information stored in the injection memory 1710, the injection counter 1820A stops counting and at the same time it erases the content of the injection memory 1710 and de-energizes the solenoid valve 1920A so that the solenoid valve 1920A stops the fuel injection. On the other hand, at the same time that the injection counter 1820A starts counting with the output pulse from the timing sensor 1140, the ignition counter 1820B is actuated so that the ignition counter 1820B starts to count the output pulses of the angular sensor 1150. Then, when it is found that the value of the binary code signal stored in the ignition memory 1720 is equal to that of the binary code signal counted by the ignition counter 1720, the ignition system 1920B is energized to deliver an electrical spark to the correct spark plug and at the same time the content of the ignition memory 1720 is erased. Thereafter, a similar process is repeated each time the output signal pulse of the timing sensor 1140 is generated, so that the

solenoid valve 1920A injects a quantity of fuel corresponding to the output digital signals of the vacuum sensor 1110 and the temperature sensor 1130, while the ignition system 1920B produces an ignition spark at the ignition time corresponding to the output digital signals of the vacuum sensor 1110 and the engine speed sensor 1120.

Next, the construction of the fuel injection and the ignition distribution circuits will be explained with reference to FIG. 15. In this figure, numeral 1510 designates the above-mentioned first operational circuit; 1520 the second operational circuit; 1710 the injection memory; 1720 the injection memory. Numerals 1830A₁ and 1830A₂ designate comparators which de-energize the solenoid valve 1920A and erase the content stored in the injection memory 1710 when the duration of fuel injection attains or equals the stored content of the injection memory 1710. Numeral 1820A designates the injection counter representing in FIG. 15 counters 1820A₁ and 1820A₂ provided for the first and second cylinders, for example; 1810A and 1810B the injection distributor and the ignition distributor, respectively. Numeral 1840 designates the clock pulse oscillator; 1920A the solenoid valve representing in FIG. 15 solenoid valves 1920A₁ and 1920A₂ provided for the first and second cylinders, for example; 1920B the ignition system, 1140 the timing sensor, 1150 the angular sensor.

The construction of the fuel injection distribution circuit will now be explained in further detail with reference to FIG. 16. In this figure, numeral 1510 designates the first operational circuit; 1511 to 1518 output terminals for the output binary code signals of the first operational circuit 1510. Numeral 1710 designates the injection memory; 1711 to 1718 flip-flops adapted to be set by the corresponding output binary code signals produced at the output terminals 1511 through 1518. Numeral 1830A₁ designates the comparator which comprises component elements 1831A through 1838A, so that when the signal inputs introduced at the two input terminals X and Y of the respective elements 1831A through 1838A are all at a high (H) or low (L) level simultaneously, each of the component elements 1831A through 1838A produces a signal voltage of low level L at the output terminal Z, while a NAND element 1839A produces a signal voltage of L level at an output terminal B when a H level signal voltage appears at all the output terminals Z of the component elements 1831A through 1838A. Numeral 1820A₁ designates the injection counter for counting the number of clock pulses applied to its input terminal C; 1821a through 1828a flip-flops constituting the counter 1820A₁. Designated as D in an inverter which inverts the output signal of the comparator 1830A₁ so that the content of the injection memory 1710 and the count of the injection counter 1820A₁ are erased when the signal level at the output terminal of the comparator 1830A₁ is low (L).

Referring to FIG. 17, there is shown the construction of one of the elements constituting the comparator 1830A₁. In this figure, numerals 1830a, 1830b, 1830c and 1830d designate NAND elements each thereof having two input terminals, X and Y input terminals; Z an output terminal. With this construction, the truth table of this element is given as follows:

X	Y	Z
L	L	L

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L	H	H
H	L	H
H	H	L

where X = X terminal, Y = Y terminal, Z = Z terminal, H = H level, L = L level.

Next, the construction and operation of one of the NAND element 1830a will be explained in reference to FIG. 18. In this figure, numeral 1001 designates an input terminal for the power supply voltage, 1002 an output terminal; 1003 a grounding terminal, 1004 a collector resistor; 1005 a resistor; 1006 a base resistor; 1007 a common-collector transistor; 1008 a common-emitter transistor; 1009 and 1011 diodes for an input AND circuit; 1010 and 1012 input terminals. With this construction, if the level at the input terminals 1010 and 1012 is a H level, the output terminal 1002 is at L, whereas if any one of the input terminals 1010 and 1012 is at L, the output terminal 1002 is at H. On the other hand, if both of the input terminals 1010 and 1012 are simultaneously at L, the output terminal 1002 is also at H. The other NAND elements 1830b, 1830c and 1830d are identical in construction and operation with the NAND element 1830a.

Next, the NAND element 1839A will be explained with reference to FIG. 19. In this figure, numeral 1001' designates an input terminal for the power supply voltage; 1002' an output terminal; 1003' a grounding terminal; 1004' a collector resistor; 1005' a resistor; 1006' a base resistor; 1007' a common-collector transistor; 1008' a common-emitter transistor; 1009, 1011, 1013, 1015, 1017, 1019, 1021 and 1023 diodes for the input AND circuits; 1010, 1012, 1014, 1016, 1018, 1020, 1022 and 1024 input terminals. Now, if all the input terminals 1010 through 1024 at a signal level H, the output terminal 1002' is at L, whereas if any one of the input terminals 1010 through 1024 is at L, the output level of the output terminal 1002' is at H.

The operation of the fuel injection distribution circuit as described with reference to FIGS. 15 to 19 will now be explained. In the first place, the binary code signals produced at the output terminals 1511 through 1518 of the first operational circuit 1320 are stored in the flip-flops 1711 through 1718 which are constituent elements of the injection memory 1710. Then the clock pulse oscillator 1840 applies clock pulses to the input terminal C of the injection counter 1820A, the flip-flops 1821a through 1828a of the counter 1820A, are set in succession to count the input clock pulses in binary number. Then, when the binary code signal at the single output terminals Y of the flip-flops 1821a through 1828a in the injection counter 1820A, differs altogether from the binary code signal at the single output terminals X of the flip-flops 1711 through 1718 in the injection memory 1710, the output terminal B of the comparator 1830A₁ is at a low level (L), whereby with the high level (H) signal pulse inverted by the inverter D, the flip-flops 1821a through 1828a in the injection counter 1820A, and the flip-flops 1711 through 1718 in the injection memory 1710 are reset to clear the contents stored therein and at the same time the injection distributor 1810A is rendered inactive with the output pulse signal from the output terminal B and the clock pulses are no longer applied to the input terminal C.

While only the one injection counter 1820A₁ has been described, the other injection counter 1820A₂ for the second cylinder and the remaining injection count-

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ers (not shown) are identical in operation with the injection counter 1820A₁, that is, the time that these counter are triggered to start action is determined by the injection distributor 1810A and the counter are caused to stop counting by means of an injection comparator provided for each counter, when the count of the respective counters attains the content stored in any corresponding memory.

Next, the construction and operation of the injection distributor 1810A mentioned above will be explained with reference to FIGS. 20 and 21. In FIG. 20, numeral 1140 designates the timing sensor having two output terminals one of which produces as many pulse signals as there are cylinders in the engine, for example, six pulse signals if the engine has six cylinders and the other output terminal produces one pulse signal for every six pulse signals produced from said one output terminal. Numeral 1840 designates the clock pulse oscillator for producing pulse signals having a predetermined frequency. Numerals 1811A, 1812A, 1813A, 1814A, 1815A and 1816A designate set/reset flip-flops (hereinafter simply referred to as S.R.F.F) each of which changes from one state to the other upon application of a first signal voltage to one input terminal and which is brought back to the state that existed just before the application of the first signal upon the application of a second signal voltage to the other input terminal; 1040, 1041, 1042, 1043, 1044 and 1045 NAND elements each thereof having four input terminals so that the signal level at the output terminal is L only when the signal levels at the four input terminals are all H. Numerals 1030, 1031, 1032, 1033, 1034 and 1035 designate the output terminals of the NAND elements 1040 through 1045, respectively. Numerals 1827, 1828 and 1829 designate flip-flops which are set with the pulse signals from the one output terminal of the timing sensor 1140 and which are reset with the pulse signal from the other output terminal of the timing sensor 1140. Designated as B₁, B₂, B₃, B₄, B₅ and B₆ are input terminals for resetting the S.R.F.F 1811A to 1816A respectively when the output signals of the six injection comparators which are not shown (though the comparators 1830A₁ and 1830A₂ are shown in FIG. 15) are at a low level (L). Numerals 1050, 1051, 1052, 1053, 1054 and 1055 designate NAND elements each thereof having two input terminals so that clock pulses are applied to the one input terminals and the signals produced at the single output terminals of the S.R.F.F 1811A to 1816A respectively are applied to the other input terminals, whereby clock pulses are generated at the output terminals at the predetermined times as determined by the timing signals from the timing sensor 1140 for the predetermined duration. Designated as C₁, C₂, C₃, C₄, C₅ and C₆ are coupling terminals for connecting to the input terminals of the six injection counters which are not shown (though the counter 1820A₁ and 1820A₂ are shown in FIG. 15), E₁, E₂, E₃, E₄, E₅ and E₆ coupling terminals for connecting to the six solenoid valves which are not shown (though the solenoid valves 1920A₁ and 1920A₂ are shown in FIG. 15). Numerals 1060, 1061, 1062, 1063, 1064 and 1065 designate the output terminals of the S.R.F.F 1811A, 1812A, 1813A, 1814A, 1815A and 1816A, respectively.

With the construction described above, the operation of the injection distributor 1810A will now be explained with reference to FIG. 21. In this figure, letter

α is the pulse voltage waveform produced at the one output terminal of the timing sensor 1140, β is the pulse voltage waveform produced at the other output terminal of the timing sensor 1140. Designated as A is the voltage waveform at the output terminal 1030 of the four-input NAND element 1040; B the voltage waveform at the output terminal 1031; C the voltage waveform at the output terminal 1032; D the voltage waveform at the output terminal 1033; E the voltage waveform at the output terminal 1034; F the voltage waveform at 1035. G is the voltage waveform produced at the single output terminal 1060 of the S.R.F.F 1811A when this flip-flop is set by the signal voltage waveform produced at the output terminal 1030 of the four-input NAND element 1040; H the signal voltage waveform generated at the output terminal C₁ by the application of the signal voltage produced at the output terminal 1060 and the clock pulse signal of the clock pulse oscillator 1840 to the NAND element 1050. J is the voltage waveform produced at the single output terminal 1061 of the S.R.F.F 1812A when this flip-flop is set by the signal voltage which is produced at the output terminal 1031 of the four-input NAND element 1041 by virtue of the output signal pulse from the timing sensor 1140; K the voltage waveform produced at the output terminal C₂ of the NAND element 1051 by the application of the signal voltage produced at the output terminal 1061 and the clock pulse signal of the clock pulse oscillator 1840 to the NAND element 1051. In like manner, the waveforms (not shown) which are similar with the signal voltage waveforms G and H are produced at the single output terminals 1062, 1063, 1064 and 1065 of the S.R.F.F 1813A, 1814A, 1815A and 1816A, respectively. The clock pulse signal voltages (not shown) similar to the waveforms H and K are also produced at the output terminals C₃, C₄, C₅ and C₆. In operation, the signal voltage β is first produced at time t_0 at the one output terminal of the timing sensor 1140, so that the flip-flops 1827, 1828 and 1829 are reset. Then, at time t_1 the signal voltage α is produced at the other output terminal of the timing sensor 1140 and this signal voltage α sets the flip-flop 1827. This results in the voltage waveform at the output terminal 1030 of the four-input NAND element 1040 which is shown as A in FIG. 21. Then, at time t_2 the voltage waveform at the output terminal 1031 of the four-input NAND element 1041 falls as shown in FIG. 21-B. At time t_3 , the voltage waveform at the output terminal 1032 of the four-input terminal NAND element 1042 also falls as shown in FIG. 21-C, and similarly the voltage waveforms at the output terminals 1033, 1034 and 1035 vary at times t_4 , t_5 and t_6 as shown in FIGS. 21-D, 21-E and 21-F, respectively. At time t'_0 , the flip-flops 1827, 1828 and 1829 which have been set from time t_1 to time t_6 are reset. Thereafter, at times t'_1 , t'_2 , t'_3 , t'_4 and t'_5 , the output voltages at the output terminals 1030 to 1035 vary as shown in FIGS. 21-A, 21-B, 21-C, 21-D, 21-E and 21-F. As with the output terminals C₁ and C₂, clock pulses equivalent to those shown in FIGS. 21-H and 21-K appear at the output terminals C₃ through C₆, that is, for the output terminal C₃ at time t_2 , C₄ at time t_4 , C₅ at time t_5 and C₆ at time t_6 . Then, when the clock pulses as shown in FIG. 21-H appear at the output terminal C₁, the counter counts these clock pulses so that when its count in binary number attains the binary number stored in the memory (which is not shown), that is, at

time T_1 , the output signal level of the comparator changes to L. This low level signal is in turn applied to the input terminal B₁ of the S.R.F.F 1811A, whereupon the S.R.F.F 1811A is reset and the signal voltage at the output terminal 1060 extinguishes at time T_1 and hence the clock pulse signal at the output terminal C₁ also extinguishes at time T_1 . In this case, the voltage at the output terminal E₁ disappears at time t_1 and it then reappears at time T_1 . Thus, if the output voltage at the output terminal E₁ is inverted, that is, if it is applied to a solenoid valve by way of an inverter circuit, the time interval between time t_1 and time T_1 will be the time during which the solenoid valve for the cylinder I is energized. In other words, the volume of fuel injection is determined by the binary digital signal code stored in the injection memory. Then, at time t_2 the counter for the cylinder II starts to count the clock pulses in the like manner as described above and the counter continues to count until the count becomes equal to the content of the corresponding memory, that is, up to time T_2 at which the counter stops its counting operation. Thus, the solenoid valve mounted on the cylinder II injects fuel from time t_2 to time T_2 . In like manner, the injection counters for the cylinders III, IV, V and VI start to count the clock pulses at times t_3 , t_4 , t_5 and t_6 respectively and at the same time the corresponding solenoid valves are energized to start fuel injection. Then, when the binary counts of these injection counters attain the values stored in the corresponding injection memories, the fuel injection stops. This process is repeated for the cylinders I through VI in sequence and the respective injection memories are cleared whenever the fuel injection stops, that is, the levels at the output terminals of the corresponding comparators change to L. However, as will be explained later, each time an ignition signal for producing an ignition spark to any cylinder is generated, the corresponding ignition memory is caused to restore and then a restore operation is also performed on the corresponding injection memory. Thus, no inconvenience can arise.

Next, the construction and operation of the ignition distribution circuit will be explained. Referring to FIG. 22, numeral 1520 designates the second operational circuit for producing an output binary code signal corresponding to the amount of spark advance; 1820B the ignition counter for counting the pulse signals from the angular sensor 1150; 1821b through 1826b flip-flops constituting the ignition counter 1820B. Numeral 1720 designates the ignition memory for storing the output binary code signal produced at the output terminals 1521 through 1526 of the second operational circuit 1520; 1721 through 1726 flip-flops constituting the memory 1720. Numeral 1830B designates the comparator designed so that as the count of the ignition counter 1820B is found to be equal to the stored content of the ignition memory 1720, it produces an output signal to stop the counting operation of the ignition counter 1820B and at the same time it resets the counter 1820B and clears the stored content of the ignition memory 1720; 1831B through 1836B elements constituting the comparator 1830B and arranged to give their output signals when both the flip-flops 1721 through 1726 of the ignition memory 1720 and the flip-flops 1821b through 1826b of the ignition counter 1820B are at the same level. Numeral 1837B designates a seven-input NAND element adapted to produce an output signal only when all the constituent elements

1831B through 1836B of the comparator 1830B produce output signals and the signal level of the angular sensor 1150 changes to H. Numeral 1838B designates a S.R.F.F so designed that it is set to produce an output signal at its single output terminal when the output signal of the seven-input NAND element 1837B is applied to one of the two input terminals and thereafter it is reset to reset the output voltage at the said single output terminal only when the signal pulse from the angular sensor 1150 is applied to the other input terminal of the S.R.F.F 1838B; 1838B₁ and 1838B₂ two-input NAND elements constituting the S.R.F.F 1838B. Numeral 1150 designates the angular sensor which produces angular signals correlated with the rotational speed of the rotating shaft of an engine, that is, it produces a preset number of pulses for every rotation of the rotating shaft. Numeral 1140 designates the timing sensor for producing pulse signals correlated with the rotation of the engine shaft; 1810B the ignition distributor so designed that it is actuated as the output signal of the timing sensor 1140 is applied to one of its input terminals, it supplies to the ignition counter 1820B the signal pulses applied to the other input terminal from the angular sensor 1150, and then it is rendered inactive by the output signal of the comparator 1830B to stop the application of the angular signal pulses to the ignition counter 1820B; 1811B a S.R.F.F constituting the ignition distributor 1810B; 1812B and 1813B inverters for inverting the signal level at the output terminal with respect to that at the input terminal; 1814B a two-input NAND element which conducts when the signal level at the single output terminal of the S.R.F.F changes to H, thereby applying the angular signal pulses to the counter 1820B. Numeral 1920B designates the ignition system for having an ignition spark produced by a spark plug (not shown) when the comparator 1830B produces an output signal; 1062 an output terminal of the comparator 1830B; 1063 an output terminal of the distributor 1810B; 1064 an output terminal of the S.R.F.F 1811B. Designated as M is an output terminal of the distributor 1810B which inverts a low level (L) output signal voltage produced at the output terminal 1062 of the comparator 1830 to a high level (H).

Next, the operation of the ignition distribution circuit illustrated in FIG. 22 will be explained with reference to FIG. 23. In this figure, designated as α and β are the output voltage waveforms at the two input terminals of the timing sensor 1140; P the input voltage waveform at the input terminal of the inverter 1812B by which the S.R.F.F 1811B is set to produce at its output terminal 1064 the signal voltage which is designated as Q. Letter R designates the output signal voltage waveform at the output terminal 1063 of the distributor 1810B; S the signal voltage waveform at the output terminal 1062 of the comparator 1830B. At time t_1 , the output signal α of the timing sensor 1140 sets the S.R.F.F to produce the signal voltage Q at its output terminal 1064. This produces the angular signal pulse voltage such as the waveform R at the output terminal of the two-input NAND element 1814B, i.e., the output terminal 1063 of the distributor 1810B. When this happens, the ignition counter 1820B counts the angular signals so that when the count of the ignition counter 1820B attains the same value as the stored content of the ignition memory 1720 at a later time τ_{11} , the signal voltage S is produced at the output terminal 1062 of

the comparator 1830B. Thus, at time τ_{11} the ignition system 1920B is actuated to have ignition sparks produced by the spark plugs. At the same time, the signal voltage at the output terminal 1062 resets both the flip-flops 1721 through 1726 of the ignition memory 1720 and the flip-flops 1821b through 1826b of the ignition counter 1820B, while this signal voltage S is applied, after being inverted by the inverter 1813B, to the S.R.F.F 1811B so that this S.R.F.F 1811B is simultaneously reset to terminate the signal voltage at the output terminal 1064 as shown by the waveform Q. This terminates the angular signal pulses at the output terminal 1063. This process of operation is repeated at later times $t_2, t_3, \dots, t_6$ to keep the engine operating. While the ignition sparks occur at the time τ_{11} which is delayed by the time from t_1 to τ_{11} with respect to the time t_1 , this time τ_{11} is an earlier time than the time t_2 . In other words, the "retard" with respect to the time t_1 for the output signal pulse from the timing sensor 1140 is an "advance" with respect to the time t_2 . Thus, in distributing the high voltage surge produced by the ignition system 1920B to the spark plugs, it can be arranged to have the spark occur with a "positive" spark advance so that by arranging to compute the delay time (spark retard) of the time from t_1 to τ_{11} , it is possible to compute the lead time (spark advance) of the time from t_2 to τ_{11} .

In the operation described above, the injection memory 1710 is cleared each time the injection is completed, that is, at times $T_1, T_2, \dots$. Therefore, while the content of the injection memory 1710 is zero thereafter, the injection counter 1820A is already counting at times $t_1, t_2, \dots, t_6$, so that the content of the injection memory 1710 and the count of the injection counter 1820A are not equal to each other. Thus, even if the stored content of the injection memory 1710 is erased while the injection counter 1820A is counting, there is no danger that the clearing of the memory 1710 immediately causes the injection counter 1820A to stop its counting operation, thereby stopping the injection of fuel.

It is now evident from the foregoing that the system of the present embodiment is extremely advantageous economically, since the fuel injection system and the ignition system are combined in a very rational way so that, for example, a single common vacuum sensor can be employed for the fuel injection and the ignition systems. Embodiment 3:

The construction of a third embodiment of the present invention will now be explained with reference to FIG. 24. In this figure, numeral 2110 designates a vacuum sensor for producing a DC output voltage corresponding to the amount of vacuum in the intake manifold of an internal combustion engine which is not shown; 2120 an engine speed sensor for producing an output DC voltage corresponding to the number of revolutions of the rotating shaft of the engine; 2130 a temperature sensor for detecting the temperature of the engine to produce an output DC voltage corresponding to the detected temperature; 2140 a timing sensor mounted on a shaft correlated to the rotating shaft of the engine to produce a pulse signal voltage (hereinafter referred to as a timing pulse signal) corresponding to the speed of the engine; 2150 an angular sensor mounted on a shaft correlated to the rotating shaft of the engine to produce 180 pulse signals for every rotation of the engine shaft, that is, one pulse signal (here-

inafter referred to as an angular pulse signal) is produced for every two degrees of the engine shaft rotation. Numeral 2210 designates an A - D converter for converting the output DC voltage of the vacuum sensor 2110 into a digital signal in binary form; 2220 an A - D converter for converting the output DC voltage of the engine speed sensor 2120 into a binary digital signal; 2230 an A - D converter for converting the output DC voltage of the temperature sensor 2130 into a binary digital signal. Numeral 2310 designates a function generator for the vacuum sensor 2110 which converts the binary coded output signal of the A - D converter 2210 into another binary coded signal to suit the fuel quantity requirement of the engine and which obtains still another binary coded signal that suits the spark timing, i.e., the vacuum advance characteristic required for the engine; 2320 a function generator for the engine speed sensor 2120 which converts the binary coded output signal of the A - D converter 2220 into another binary coded signal to suit the spark timing characteristic, i.e., the rotational advance characteristic required for the engine; 2330 a function generator for the temperature sensor 2130 which converts the binary coded output signal of the A - D function generator 2230 into another binary coded signal to increase or decrease the volume of fuel injection by a proper amount according to the degree of temperature within the engine. Numeral 2400 designates a selector switch for selectively coupling the binary coded output signals of the function generators 2310, 2320 and 2330 to an operational circuit which will be explained later. Numeral 2500 designates the aforesaid operational circuit which performs an addition or subtraction on the binary coded output signals of the function generators 2310, 2320 and 2330 so that a binary coded digital signal corresponding to the duration of fuel injection is derived from the binary coded output signal of the function generator 2310 for the vacuum sensor 2110 and the binary coded output signal of the function generator 2330 for the temperature sensor 2130, or alternately a binary coded output digital signal corresponding to the spark timing, i.e., the spark advance characteristic is derived through the action of the selector switch 2400 from another binary coded output signal of the function generator 2310 for the vacuum sensor 2110 and the binary coded output signal of the function generator 2330 for the engine speed sensor 2130. Numeral 2600 designates a selector switch adapted to be actuated in synchronism with the selecting action of the selector switch 2400 to transmit the binary coded output digital signal of the operational circuit 2500 to memory circuits which will be explained later. Numeral 2710 designates a first memory circuit (hereinafter referred to as an injection memory) adapted so that when the operational circuit 2500 produces its binary coded output signal corresponding to the fuel injection quantity (duration) through the action of the selector switch 2400, this binary coded output signal is stored in the injection memory by the action of the selector switch 2600. Numeral 2720 designates a second memory circuit (hereinafter referred to as an ignition memory) adapted to store through the action of the selector switch 2600 the binary coded output signal corresponding to the spark timing of the engine when this output signal is produced by the operational circuit 2500 through the action of the selector switch 2400. Numeral 2810A designates an injection distribution

circuit for distributing the stored content of the injection memory 2710, i.e., the digital signals stored therein to the engine cylinders according to the output signals of the timing sensor 2140; 2810B an ignition distribution circuit for distributing the digital signals stored in the ignition memory 2720 to the spark plugs of the engine in their ignition order according to the output signal of the timing sensor 2140. Numeral 2820A designates a first counter (hereinafter referred to as an injection counter) which counts the duration of the fuel injection and stops its counting operation when its count is found to be equal to the stored content of the injection memory 2710 and at the same time it erases the content of the injection memory 2710; 2820B a second counter (hereinafter referred to as an ignition counter) which counts the angular pulse signals from the angular sensor 2150 and stops its counting operation when it is found to be equal to the stored content of the ignition memory 2720 and at the same time it erases the content of the ignition memory 2720. Numeral 2840 designates a clock pulse oscillator which, upon actuation of the injection counter 2820A, produces pulse signals (hereinafter referred to as clock pulse signals) having a predetermined frequency so that the counter 2820A counts the clock pulse signals to compute the duration of the fuel injection. Numeral 2910 designates a selection signal generator which is actuated with the output signal of the ignition counter 2820B and the angular pulse signal from the angular sensor 2150 so as to supply selection signals to the selector switches 2400 and 2600 with the two pulses of the angular pulse signals produced by the angular sensor 2150 after the generation of the output signal of the ignition counter 2820B. The selection signal generator 2910 and the selector switches 2400 and 2600 constitute a selection circuit. Numeral 2920A designates the solenoid valve mounted in the engine intake manifold which initiates the injection of fuel with the output signal of the injection counter 2820A, that is, when the counter 2820A starts counting and stops the fuel injection as the counter 2820A completes and stops its counting operation. Numeral 2920B designates an ignition system so designed that when the ignition counter 2820B initiates its counting operation and then stops the operation upon completion of the counting, an ignition spark is produced by one of the spark plugs mounted in the engine cylinders by way of the distributor rotor which rotates in a correlated manner with the rotating shaft of the engine (not shown).

With the construction described above, the operation of the system of the present embodiment will now be briefly explained. To start with, when the ignition counter 2820B stops its operation upon completion of the counting, the ignition system 2920B is actuated as previously explained so that an ignition spark is produced by the spark plug of the engine. At the same time, the selection signal generator 2910 is also actuated. Then, the selector switch 2400 is actuated with a first single angular signal pulse produced by the angular sensor 2150 so that in the first place the function generator 2320 for the engine speed sensor 2120 and the function generator 2310 for the vacuum sensor 2110 are connected to the operational circuit 2500 and simultaneously the selector switch 2600 is actuated to connect the operational circuit 2500 to the ignition memory 2720. This causes the ignition memory 2720 to store the binary coded signal corresponding to the

binary coded output signal of the function generator 2310 and the binary coded output signal of the function generator 2320, that is, the spark advance characteristic of the engine. Then, a second angular output pulse signal of the angular sensor 2150 is applied to the selector switches 2400 and 2600 so that the operational circuit 2500 is now connected with the function generator 2310 for the vacuum sensor 2110 and the function generator 2330 for the temperature sensor 2130 and simultaneously the operational circuit 2500 is connected to the injection memory 2710. This causes the injection memory 2710 to store a binary coded signal corresponding to the binary coded output signal of the vacuum sensor 2110 and the binary coded output signal of the temperature sensor 2130, that is, the binary coded signal corresponding to the quantity (duration) of the fuel injection. Once the corresponding binary coded signals are stored in this way in the ignition memory 2720 and the injection memory 2710, the selector switches 2400 and 2600 remain inoperative until the ignition counter 2820B stops its operation upon completion of the counting and hence the ignition system 2920 is actuated, and thus during this time the connections between the injection memory 2710 and the ignition memory 2720 and the function generators 2310, 2320 and 2330 are entirely cut off. Thereafter, the injection distributor 2810A and the ignition distributor 2810B are set into action with the timing pulse signals from the timing sensor 2140, and the injection counter 2820A starts to count the clock pulse signals from the clock pulse oscillator 2840. Simultaneously, the solenoid valve 2920A is energized to start the fuel injection. Then, as the binary coded output signal of the injection counter 2820A is found to be equal to the content of the injection memory 2710, the injection counter 2820A stops its operation and at the same time it erases the stored contents of the injection memory 2710 and de-energizes the solenoid valve 2920A so that the solenoid valve 2920A stops the fuel injection. On the other hand, at the same time that the injection counter 2820A is actuated with the output timing pulse signal of the timing sensor 2140, the ignition counter 2820B is also set in action to count the output angular pulse signals of the angular sensor 2150. Then, when the contents of the ignition memory 2720 and the binary coded output signal of the ignition counter 2820B are found to be equal in value, a current is supplied to the ignition system 2920B to have an electric spark produced by the spark plug and at the same time the content of the ignition memory 2720 is erased and an actuating signal is applied to the selection signal generator. A similar procedure is thereafter repeated each time the timing sensor 2140 produces an output timing pulse, so that the solenoid valve 2920 injects the amount of fuel corresponding to the output signals of the vacuum sensor 2110 and the temperature sensor 2130 and the ignition system 2930 delivers an ignition spark according to the spark timing corresponding to the output signals of the vacuum sensor 2110 and the engine speed sensor 2120.

Referring to FIG. 25, there is shown the construction of the fuel injection distribution circuit and the ignition distribution circuit. In FIG. 25 where those parts which bear the like reference numerals as used in FIG. 24 designate like component parts, numerals 2610 and 2620 designate selector switches, 2830A₁ and 2830A₂ comparators which stop the solenoid valve 2920A and

erase the injection memory 2710 when the duration of the fuel injection is found to be equal to the contents of the injection memory 2710.

Next, the construction of the fuel injection distribution circuit will be explained in more detail with reference to FIG. 26. In FIG. 26 wherein the like reference numerals as used in FIG. 25 designate the like component parts, letter A designates an input terminal for receiving the selection signal from the selector switch 2610, 2611 through 2618 NAND elements constituting the selector switch 2610; 2601a through 2608a input terminals for receiving the binary coded output signal of the operational circuit 2500. Numerals 2711 through 2718 designate flip-flops constituting the injection memory 2710 which are set or reset with the binary coded output signals of the selector switch 2600. Numerals 2831A through 2838A designate comparator elements constituting the comparator 2830A₁, each of which is provided with two input terminals X and Y so that if the signal input levels are concurrently high (H) or low (L) at the two input terminals X and Y, then a signal voltage of low level L is produced at the output terminals Z of the respective comparator elements 2831A through 2838A, while a NAND element 2839A produces a signal voltage of low level L at its output terminal when the signal voltage level is high (H) at all the output terminals of the comparator elements 2831A through 2838A. Designated as B is the output terminal of the comparator 2830A₁; 2821 through 2828 flip-flops constituting the injection counter 2820A₁. Letter D designates an inverter which inverts the output signal of the comparator 2830A₁ so that when the signal level at the output terminal B of the comparator 2830A₁ is L, the stored contents of the flip-flops 2711 through 2718 of the injection memory 2710 and the counts of the flip-flops 2711 through 2718 of the injection counter 2820A₁ are erased.

The construction and operation of the comparator 2830A₁ and the comparator elements 2831A through 2838A are identical with those of the corresponding comparator and comparator elements of the second embodiment as explained with reference to FIGS. 17 and 18. The NAND element 2839A is also as that of the second embodiment which is explained with reference to FIG. 19.

The operation of the injection counter 2820A₁, comparator 2830A₁, memory 2710 and selector switch 2610 as employed in the injection distribution circuit shown in FIGS. 25 and 26 will now be explained. In the first place, when a signal pulse voltage for initiating a writing operation is applied from the selection signal generator 2910 to the input terminal A of the selector switch 2610, this operates the selector switch 2610 so that the binary coded signal produced by the operational circuit 2500 is written by way of the NAND elements 2611 through 2618 of the selector switch 2610 into the corresponding flip-flops 2711 through 2718 which are the constituting elements of the injection memory 2710. Whereupon, the signal pulse voltage applied to the input terminal A of the selector switch 2610 is turned off so that the connection between the operational circuit 2500 and the injection memory 2710 is interrupted. Then, as the clock pulses are applied at the input terminal C of the injection counter 2820A₁ from the clock pulse oscillator 2840, the flip-flops 2821 through 2828 of the counter 2820A₁ are set in succession thereby counting the applied clock pulses

in a binary number system. In this situation, when the binary coded signal appearing at the single output terminals of the respective flip-flops 2821 through 2818 of the injection counter 2820A₁, differ altogether from the binary coded signal appearing at the single output terminals of the flip-flops 2710 through 2718 constituting the injection memory 2710, the output signal at the output terminal B of the comparator 2830A₁ changes to L so that the injection counter 2820A₁ and the injection memory 2710 are reset with the signal pulse inverted by the inverter D, thereby erasing the count of the counter and the content of the memory, respectively. Concurrently, the distributor 2810A stops the operation so that the clock pulse signals are no longer applied at the input terminal C of the injection counter 2820A₁. While the injection counter 2820A₁ has been described by way of an example, the operation of the injection counter 2820A₂ and other counters (not shown) for other engine cylinders is identical with the above described operation of the injection counter 2820A₁, that is, the time of operation is set by the distributor 2810A, and when a comparator provided for each counter finds the count of the counter to be equal to the content of the corresponding injection memory, the counter stops its operation.

Next, the construction and operation of the injection distributor 2810A will be explained with reference to FIGS. 27 and 21 (second embodiment). In FIG. 27, the timing sensor 2140 produces as many pulse signals as there are cylinders in an engine and thus if the engine has six cylinders, it produces six such pulse signals plus one pulse signal for every six pulse signals. Numerals 2821A through 2826A designate set/ reset flip-flops (hereinafter simply referred to as S.R.F.F.) each thereof being adapted so that it is set when a signal voltage is applied at one of its input terminals and it is reset when another signal voltage is applied at the other input terminal. Numerals 2040 through 2045 designate NAND elements each thereof having four input terminals so that the signal level at the output terminal is L if and only if all the signal levels at the four input terminals are "Hs." Numerals 2030 through 2035 designate the output terminals of the NAND elements 2040 through 2045; 2827 through 2829 flip-flops each thereof being adapted so that it is set to count with a timing pulse signal from the one output terminal of the timing sensor 2140 and it is reset with another timing pulse signal from the other output terminal. Designated as B₁ through B₆ are the respective input terminals of the S.R.F.F. 2821A through 2826A so that the S.R.F.F. 2821A through 2826A are reset when the signal level at the output of the comparator which is not shown is L. Numerals 2050 through 2055 designate NAND elements each thereof having two input terminals so that when the clock pulse is applied at one of the two input terminals and the signal produced at the output terminal of the corresponding one of the S.R.F.F. 2821A through 2826A is applied at the other input terminal, it produces at the output terminal those clock pulses which are produced at predetermined times and for a predetermined period of time as determined by the output timing pulse signals of the timing sensor 2140. Letters C₁ through C₆ designate coupling terminals for providing connections to the input terminals of the injection counters (in FIG. 26), the input terminal C of the memory 2820A₁, E₁ through E₆ coupling terminals for providing connections to the solenoid valves mounted

on the engine cylinders. Numerals 2060 through 2065 designate the output terminals of the S.R.F.F. 2821A through 2826A.

The operation of the injection distributor 2810A constructed as described above is identical with that of its counterpart in the second embodiment as explained with reference to FIG. 21.

Next, the construction of the injection distribution circuit will be explained with reference to FIG. 28. In this figure, like reference numerals as used in FIG. 25 designate the like component parts. The selector switch 2620 is adapted so that when there is a high level (H) at one its input terminals, it conducts with the resultant conduction among the remaining plurality of input terminals and its plurality of output terminals, and numerals 2621 through 2626 designate two-input NAND elements. The ignition memory 2720 comprises flip-flops 2721 through 2726. The ignition counter 2820B comprises flip-flops 2821B through 2826B. Comparator elements 2831B through 2836B of the comparator 2830B are adapted to produce their output signals when the contents of the flip-flops 2721 through 2726 of the ignition memory 2720 attain the same levels as the counts of the flip-flops 2821B through 2826B of the ignition counter 2820B. Numeral 2837B designates a seven-input NAND element which produces its output signal only when all the comparator elements 2831B through 2836B produce their output signals and the angular pulse signal attains a high level (H). Designated as 2838B is a S.R.F.F. which is set to produce an output signal at its single output terminal when the output signal of the seven-input NAND element 2837B is applied to one of its input terminals and which is reset to reset the output voltage at its single output terminal when the angular pulse signal is applied later at the other input terminal; 2838B₁ and 2838B₂ two-input NAND elements constituting the S.R.F.F. 2838B. The ignition distributor 2810B is designated so that it is set in operation with the timing pulse signal applied to one of its input terminals from the timing sensor 2140 and it supplies the angular pulse signals applied to the other input terminal to the ignition counter 2820B, thereafter it stops the operation with the output signal of the comparator 2830B and interrupts the supply of the angular pulse signals to the ignition counter 2820B. Numeral 2811B designates a S.R.F.F.; 2812B and 2813B inverters to invert the signal levels at the output terminals with respect to the input terminals; 2814B a two-input NAND element which conducts to supply the angular pulse signals to the ignition counter 2820B when the signal level at the single output terminal of the S.R.F.F. 2811B is H. Numeral 2061 designates an input terminal of the selector switch 2620; 2062 the output terminal of the comparator 2830B; 2063 the output terminal of the ignition distributor 2810B; 2064 the output terminal of the S.R.F.F. 2811B. Designated as M is an output terminal of the distributor 2810B which is inverted to H when the output signal voltage appears at the output terminal 2062 of the comparator 2830B; N an input terminal of the selector switch 2620.

Next, the construction of the selection signal generator 2910 will be explained with reference to FIG. 29. In this figure, numeral 2911 designates a S.R.F.F. which is set to produce a signal voltage when a signal voltage is applied at one input terminal and which is reset to produce a signal voltage at the other output terminal when another signal voltage is applied later at the other

input terminal; 2911A and 2911B two-input NAND elements constituting the S.R.F.F 2911. Numeral 2912 designates a NAND element; 2913 an inverter; 2914 and 2915 three-input NAND elements for distributing the angular pulse signals; 2916 and 2917 flip-flops for counting the angular pulse signals. Designated as N' is an output terminal for supplying a selection signal to the input terminal N of the selector switch 2620; A' an output terminal for supplying a selection signal to the input terminal A (FIG. 26) of the selector switch 2400; M an input terminal of the S.R.F.F 2911 to which is applied the signal voltage which the ignition distributor 2810B produces concurrent with the occurrence of an ignition spark upon the application of the signal voltage to the ignition system by the comparator 2830B.

Next, the operation of the ignition memory 2720, comparator 2830B, ignition distributor 2810, ignition counter 2820B and selection signal generator 2910 which are constructed as described above will be explained with reference to FIGS. 30 and 31. In FIG. 30, designated as α and β are the timing pulse voltage waveforms produced at the two output terminals of the timing sensor 2410; P the input voltage waveform at the input terminal of the inverter 2812B which sets the S.R.F.F 2811B to produce at its output terminal 2064 the signal voltage designated as Q; R the output signal voltage waveform at the output terminal 2063 of the distributor 2810B; S the signal voltage waveform at the output terminal 2062 of the comparator 2830B; U the selection signal voltage waveform produced at the output terminal N' of the selection signal generator 2910; V the selection signal voltage waveform appearing at the output terminal A' of the selection signal generator 2910. In FIG. 31, the waveforms S, U and V are shown in enlarged form in time. Now at time t_1 , the output signal α of the timing sensor 2140 sets the S.R.F.F to produce the signal voltage Q at its output terminal 2064'. This causes the angular pulse signal voltage as shown in FIG. 30-R to appear at the output terminal of the two-input NAND element 2814B, that is, at the output terminal of the ignition distributor 2810B. Whereupon, the flip-flops 2821B through 2826B of the ignition counter 2820B count the angular pulse signals, so that when the count of the ignition counter 2820B attains the value of the content of the ignition memory 2720 at a later time τ_{11} , the signal voltage S appears at the output terminal 2062 of the comparator 2830. Consequently, at time τ_{11} , the ignition system 2920B is actuated to cause the spark plug to produce an ignition spark. Concurrently, the signal voltage S at the output terminal 2062 resets the flip-flops 2721 through 2726 of the ignition memory 2720 and the flip-flops 2821B through 2826B of the ignition counter 2820B so as to erase the content of the memory 2720 and the count of the counter 2820B, and at the same time the signal voltage S is inverted by the inverter 2813B which is then applied to the S.R.F.F. 2811B so that this S.R.F.F. 2811B is reset to terminate the signal voltage at the output terminal 2064 as shown by the waveform Q, thereby terminating the angular pulse signal at the output terminal 2063. Concurrently, the signal voltage S sets the S.R.F.F 2911 of the selection signal generator 2911 to initiate the counting of the angular pulse signals by the flip-flops 2916 and 2917, whereby at time τ_{12} the selection signal U appears at the output terminal N' and then at time τ_{13} the selection signal V appears at the output terminal A'. Here, the signal voltage U is

applied at the input terminal N of the selector switch 2620 and the signal voltage V is applied at the input terminal A of the selector switch 2400 and thus, while the contents of the ignition memory 2720 and the injection memory 2710 are respectively erased at time τ_{11} and at time T_1 at which the fuel injection stops, at time τ_{12} the injection memory 2720 newly stores a further binary coded signal and at time τ_{13} the injection memory 2710 newly stores a further binary coded signal. This process is repeated thereafter at times $t_2, t_3, \dots, t_6$, thereby maintaining the continued operation of the engine. In this connection, while the ignition spark occurs at time τ_{11} which is delayed by the time from τ_{11} to t_1 with respect to the time t_1 , this time τ_{11} is earlier than the time t_2 . In other words, the "retard" with respect to the time t_1 of the output timing pulse signal of the timing sensor 2140 is the "advance" with respect to the time t_2 . Thus, in distributing the high voltage surge produced by the ignition system 2920B to the spark plug, it can be arranged to have the spark occur with a "positive" spark advance so that by computing the delay time (spark retard) of from τ_{11} to t_1 , it is possible to compute the lead time (spark advance) of from t_2 to τ_{11} .

In the operation described hereinbefore, the injection memory 2710 is erased each time the injection is completed, that is, at times $T_1, T_2, \dots, T_6$. Thus, as previously explained, the content of the injection memory 2710 remains at zero until such times as $\tau_{13}, \tau_{23}, \dots$. However, the injection counters 2820A₁ and 2820A₂ are already set to count at the times t_1 and t_2 and therefore the content of the injection memory 2710 and the counts of the injection counters 2820A₁ and 2820A₂ are unequal. It should be apparent that even if the injection memory 2710 is erased while the injection counters 2820A₁ and 2820A₂ are operating, this clearing of the memory 2710 would not cause the injection counters 2820A₁ and 2820A₂ to stop their counting operation to stop the fuel injection.

It is now evident from the foregoing that the system of the present embodiment is advantageous over the system of the second embodiment in that since it incorporates a selection circuit for selectively coupling the first and second output digital signals of an operational circuit to the succeeding stage and the circuit for supplying selection command signals to the selection circuit, both the fuel injection system and the ignition system can be combined in a very rational manner by virtue of the so-called time sharing system realized by these operational and selection circuits.

Furthermore, since a distribution circuit is incorporated for a plurality of first counters which count a first reference digital signal, this first reference digital signal is applied sequentially to the plurality of counters by this distribution circuit in accordance with the fuel injection timing, and thus the amount of fuel that suits the requirements of the respective cylinders can be positively injected without any fluctuation not only throughout the range of low engine speeds, but also at higher engine speeds and for acceleration, thereby ensuring the efficient operation of the engine at all engine speeds.

Embodiment 4:

The general construction and operation of the system of a fourth embodiment of the invention will be explained with reference to FIG. 32. In this figure, designated as T is a temperature sensor for detecting the

temperature of an engine, which comprises a thermistor for measuring the temperature of the engine oil, cooling water or the like, a constant voltage source which supplies a constant voltage to the thermistor and an A - D converter for detecting and converting the voltage across the thermistor into a digital signal. Letter St designates a start sensor for detecting the start of the engine to produce an "H" or "L" signal, that is, a sensor which detects, for example, the voltage across the starting terminal of the engine starting motor switch, i.e., the key switch, or an engine speed lower than a predetermined value to thereby produce an "H" or "L" signal. In response to the output of the start sensor St, NAND elements 3010 and 3012 and an inverter 3011 come into operation to make a final detection of the starting of the engine. The NAND elements 3010 and 3012 function only when all the NAND inputs are "Hs." Letter Va designates a vacuum sensor for detecting the engine intake manifold vacuum which comprises, for example, a transducer for converting the engine intake manifold vacuum into a DC voltage and an A - D converter for converting the output voltage of the transducer into a digital quantity. The transducer for converting the engine intake manifold into a DC voltage may comprise, for example, a circuit combining a core movable by the vacuum in the intake manifold, an oscillator for converting the movement of the core into a voltage and a differential transformer, whereby the output of the oscillator is applied to the input winding of the differential transformer and the output winding of the differential transformer is coupled to a rectifier smoothing circuit so that the DC output voltage of the rectifier smoothing circuit assumes a value which varies with the movement of the core. Designated as Acc is an acceleration sensor for producing an output proportional to the opening speed of the engine throttle valve; the acceleration sensor may comprise a generator which produces a voltage proportional to the opening speed of the engine throttle valve, a time constant circuit operable in response to the output voltage of the generator and an A - D converter, wherein the output voltage of the generator is applied to the time constant circuit where the voltage proportional to the output voltage of the generator is converted into a damped waveform decreasing with a predetermined time constant and the A - D conversion is performed according to this waveform to obtain a digital output corresponding to the opening speed of the throttle.

Letter A/F designates a switch which varies the air-fuel ratio so that in order to obtain the maximum amount of power from the engine, the mixture is richer when the engine throttle valve is almost fully opened than when the throttle openings are other than full-throttle. The switch may comprise two chambers one of which is opened to the atmosphere and the other communicates with the intake manifold to admit the intake manifold thereto, a diaphragm displaceable by the difference in pressure between the two chambers and a switch which operates in response to the movement of the diaphragm, whereby the switch may be closed or opened to produce an "H" or "L" signal. Letter RPM designates an engine speed sensor for detecting the engine speed in terms of a digital quantity, which may comprise a generator that rotates in synchronism with the engine, a detector which detects the maximum value of the output voltage of the generator and an A - D converter for converting the detected

maximum voltage into a digital quantity. Alternately, the engine speed sensor may comprise an integrating circuit which integrates a voltage waveform synchronized with the rotation of the engine and having a constant magnitude and a constant pulse width so as to produce a DC voltage proportional to the number of pulses per unit time, and a circuit which effects the A - D conversion of this DC voltage.

These are the sensors for obtaining those numerical values which are necessary to control the fuel injection and the ignition timing of an engine. In addition, some other sensors are required for the computation of the fuel injection and the ignition timing requirements of the engine. Such sensors include an injection start sensor for initiating the fuel injection, a rotational angle sensor C_θ which detects the angle of rotation of the engine crankshaft to determine the ignition timing, and a clock pulse generator CT for generating clock pulses on the basis of the minimum duration of the injection.

Next, explanation will be made of those converters which are incorporated in the system of the present embodiment. Designated as $T - K_1$ and $T - K_2$ are function generators which respectively receive the output signals of the temperature sensor T and the start sensor St to determine a pattern in a manner that will be explained later, so that how much quantity of fuel as determined according to the intake manifold vacuum and other conditions may be increased to suit the temperature of the engine at the start thereof will be calculated according to this pattern. Letter C_q designates a fuel cutoff signal generator, $V_a - qv$ a function generator which receives the output signal of the vacuum sensor V_a to convert the amount of the engine intake manifold into the rate of fuel flow required for the engine; $A_{cc} - qA_{cc}$ a converter which receives the output signal of the acceleration sensor A_{cc} to increase the volume of injection; $A/F - qA/F$ a function generator for determining the amount of fuel to be increased to change the air-fuel ratio according to the output signal of the switch A/F, and whether the volume of fuel injection should be increased by a predetermined amount is determined by this converter. Letter S_1 designates a coder into which the numerical value contained in either the converter $T - K_1$ or $T - K_2$ is transferred; S_2 an adder for forming the sum of the output signals of the function generators $V_a - qv$, $A_{cc} - qA_{cc}$ and $A/F - qA/F$; S_3 an adder which adds the output signal of the adder S_2 according to the output signal pattern of the coder S_1 , and the output value of the adder S_3 ultimately determines the volume of injection. Letter M_q designates a memory circuit into which the output signal value of the adder S_3 is transferred for storage; Req_1 and Req_2 read circuits for reading out the content of the memory circuit M_q according to the output signals of the injection start sensor B and the clock pulse oscillator CT; F_{u1} and F_{u2} injection circuits each having an electromagnetically operated injection valve mounted on the engine, so that the volume of each injection is determined by the time during which the solenoid coil of the injection valve is energized, that is, the time that the injection valve remains open.

It is to be noted here that the system of the present embodiment is applied to a six-cylinder engine and that the injection circuits F_{u1} and F_{u2} and their read circuits Req_1 and Req_2 are provided for two of the six cylinders, and thus the corresponding injection circuits and their

read circuits (not shown) are similarly provided for the remaining four cylinders. In the case of a multiple-cylinder engine wherein the injection of fuel into the respective cylinders is performed at different times, it is possible to arrange so that only the injection circuits are provided in like number and each of the read circuits of a smaller number serves on a plurality of the injection circuits to effect the required injection. Designated as $\bar{V}_a$ is an inverter circuit which receives and inverts the digital output of the vacuum sensor V_a to produce an inverted signal and this can be readily carried out by inverting the output of the vacuum sensor V_a through an inverter; $\bar{V}_a - \theta_v$ a function generator which converts the output signal of the inverter circuit $\bar{V}_a$ into the required amount of spark advance corresponding to the engine intake manifold vacuum; $V_a - \theta_v$ a function generator which is employed in an alternative form, that is, a converter which converts the output of the vacuum sensor V_a into θ_v which is in turn converted by way of an inverter circuit into the spark advance θ_v corresponding to the engine intake manifold vacuum; C_u a spark advance cutout signal generator which prevents the occurrence of any spark advance by the engine intake manifold vacuum when the engine speed is lower than a predetermined engine rpm; $RPM - \theta_R$ a function generator for converting the output signal of the engine speed sensor RPM into the amount of spark advance required; S_4 an adder for forming the sum of the amount of vacuum advance impressed from the function generator $\bar{V}_a - \theta_v$ and the amount of rotational advance impressed from the function generator $RPM - \theta_R$, the output of the adder S_4 representing the total amount of spark advance required; M_θ a memory circuit into which the output of the adder S_4 representing the total advance required is introduced for storage; $Re\theta$ a read circuit for reading out the content of the memory circuit M_θ in accordance with the output signal of the rotational angle sensor C_θ which detects the angle of rotation of the engine; Ig an ignition system which effects the ignition of the engine upon completion of a read operation by the read circuit $Re\theta$.

With the arrangement described above, the output signal of the acceleration sensor A_{cc} is first converted in the function generator $A_{cc} - qA_{cc}$ into a signal representing the amount of fuel to be increased for acceleration and simultaneously whether the fuel quantity should be increased to change the air-fuel ratio is determined in the function generator $A/F - qA/F$ according to the output signal of the switch A/F . The acceleration increment signal qA_{cc} produced in the function generator $A_{cc} - qA_{cc}$ is temporarily stored. Then, upon receipt of the output signal from the vacuum sensor V_a , the function generator $V_a - qv$ produces the fuel injection signal qv corresponding to the intake manifold vacuum, so that this signal is added to the previously produced acceleration increment signal qA_{cc} and the air-fuel ratio change signal qA/F from the function generator $A/F - qA/F$ in the adder S_2 to compute the steady state fuel injection quantity q . That is, the steady state fuel injection quantity $q = qv + qA_{cc} + qA/F$ is stored. Whereupon, depending on whether the engine is at start and whether the engine is warming up; either one of the function generators $T - K_1$ and $T - K_2$ is brought into action, thus transferring its pattern K into the coder S_1 . When this happens, the preliminary stored value of the fuel injection quantity q is added to the value of the pattern K in the adder S_3 to determine the

ultimate total fuel injection quantity Q which is in turn stored in the memory circuit M_q . Then, the output signal of the vacuum sensor V_a is inverted by way of the inverter circuit $\bar{V}_a$ and it is then applied to the function generator $\bar{V}_a - \theta_v$ so that the function generator $\bar{V}_a - \theta_v$ computes and stores the spark advance θ_v corresponding to the intake manifold vacuum. On the other hand, upon receipt of the output signal of the engine speed sensor RPM, the function generator $RPM - \theta_R$ computes and stores the spark advance θ_R corresponding to the engine speed, so that this spark advance θ_R is added to the spark advance θ_v in the adder S_4 to produce the final total spark advance $\theta_T = \theta_v + \theta_R$ which is in turn stored in the memory circuit M_θ .

In the foregoing explanation, all the computations are performed in binary codes. The method of computation employed in this embodiment will now be explained with reference to FIGS. 33 et seq. FIG. 33 illustrates a block diagram of an arrangement for producing the acceleration increment signal qA_{cc} and the air-fuel ratio change signal qA/F ; FIG. 34 a diagram showing the required acceleration increment qA_{cc} of the engine corresponding to the output signal a_{cc} of the acceleration sensor A_{cc} ; FIG. 35 a diagram showing the required air-fuel ratio change increment qA/F of the engine corresponding to the relative vacuum, i.e., the ratio of the intake manifold vacuum to the atmospheric pressure. In FIG. 33, letter A_{cc} designates the acceleration sensor whose output signal is the output of the time constant circuit whose input is a voltage signal proportional to the opening speed of the engine throttle valve; J_{acc} a signal input for computing the acceleration increment, which will be explained later; $A_{cc} - A_{co}$ a discriminator which determines whether the output signal a_{cc} of the acceleration sensor A_{cc} is greater or smaller than the value at point a_{co} on the graph of FIG. 34. Numerals 3101 and 3103 designate NAND elements for determining whether the output signal a_{cc} of the acceleration sensor A_{cc} is greater or smaller than the value of a_{co} ; 3102, 3104 and 3105 inverters; A_{cc5} a coder for producing a five-place code in which the most significant position contains the most significant digit of the input code applied to this coder by way of the inverter 3104; A_{cc3} a coder for producing a three-place code; K_{12} a coder for producing a code which represents a constant, 00 a coder for producing a code which represents zero; J_{acc5} , J_{acc3} , J_{K12} and J_0 circuits which supply inputs to the coders A_{cc5} , A_{cc3} , K_{12} and 00; A/F the switch which detects the throttle opening to vary the air-fuel ratio; 3106 a NAND element which detects whether the output signal qA/F of the switch A/F is "H" or "L"; 3107 an inverter; $A/F - qA/F$ a function generator which determines, whether if any, increase in the fuel quantity is necessary.

With the arrangement described above, when the command signal input J_{acc} for initiating the computation of an increased fuel quantity for acceleration changes from "L" to "H," the discriminator $A_{cc} - A_{co}$ receives the acceleration increment signal a_{cc} from the acceleration sensor A_{cc} to determine whether the acceleration increment signal a_{cc} is greater or smaller than a_{co} . If the result shows that $a_{cc} > a_{co}$, the discriminator $A_{cc} - A_{co}$ produces an "H" signal, whereas it produces an "L" signal if the result is contrary. Whether the signal is "H" or "L" determines which of the coders are to be connected, that is, the coders A_{cc5} , A_{cc3} and K_{12} are to be connected, or the coder 00 is to be con-

nected to the adder A_1 . This is determined by the circuits J_{acc5} , J_{acc3} , K_{12} and J_0 and the inputs to these circuits are supplied by way of the inverters 3104 and 3105. It is to be noted here that while it is illustrated that the "H" signal is applied to the circuit including the NAND elements 3101 and 3103, this circuit may operate without receiving such an "H" signal and therefore the practical circuit can be simplified. However, for purposes of explanation, it is assumed that the circuit produces an "H" signal upon the application of an "H" input thereto. In like manner, an "H" signal is also added to other figures. The coder 00 is provided to indicate the absence of any input to the adder A_1 and therefore it can be eliminated in a practical circuit. However, this coder is also included for purposes of explanation. On the other hand, if the signal output of the switch A/F is "H," the function generator A/F - qA/F comes into operation, while it does not operate, that is, it produces an "L" output, if the output of the switch A/F is "L." Now returning to the explanation of the manner in which the acceleration increment is computed, in the process of producing the acceleration increment signal qA_{cc} corresponding to the output signal a_{cc} of the acceleration sensor A_{cc} , the coders A_{cc5} , A_{cc3} , A_{cc1} and K_{12} are connected to the adder A_1 , so that in effect the acceleration increment signal qA_{cc} is given in the present embodiment, as follows:

$$qA_{cc} = a_{cc5} + a_{cc3} + K_{12}$$

where a_{cc} , a_{cc3} and K_{12} are the output signals of the coders A_{cc5} , A_{cc3} and K_{12} . While, in this case, it is given that $qA_{cc} = a_{cc5} + a_{cc3} + K_{12}$, many other combinations than this one are possible among the coders A_{cc5} , A_{cc3} and A_{cc1} . Thus, if $a_{cc5} = 1.00$, then $a_{cc1} = 0.0625$, so that with the minimum unit of 0.0625 straight lines at varying angles may be obtained. Thus, a combination can be selected which would ensure an increased fuel quantity characteristic required for an engine, such as the one which is very close to the characteristic shown in FIG. 34. Therefore, when a change in the design is required due to any variation of such a characteristic, and desired characteristic may be obtained by varying the above-mentioned combination and the constant value of the coder K_{12} . This is also true with any other function generators employed in this embodiment. Now, by increasing the amount of fuel for acceleration and changing the air-fuel ratio in the manner as described hereinbefore, various special qualities in the operation of the engine can be ensured as will be explained hereinafter. In the first place, when the engine throttle valve is opened rather quickly to increase the speed of the engine, there results a rapid increase in the amount of air drawn in, and since this quick opening of the throttle valve does not produce a corresponding rapid increase of the engine speed, the pressure in the intake manifold temporarily approaches a level which is close to atmospheric pressure. Under these circumstances, the output value of the vacuum sensor V_a cannot rapidly follow such development, resulting in a lean air-fuel mixture being supplied to the engine. This lean air-fuel mixture is compensated by the aforesaid increased fuel supply for acceleration, so that the leaning out of the air-fuel mixture due to any rapid variation of the throttle valve opening may be preventing, thereby obtaining efficient operation of the engine without any misfiring. On the other hand, when the throttle valve is almost in the fully opened position, it is required that

instead of operating the engine so as to accomplish the minimum rate of fuel consumption, the engine should be operated at its fuel-power to obtain a fully efficient operation of the engine. To meet this requirement, the air-fuel ratio of the engine must be made richer than is needed to attain the minimum rate of fuel consumption and this is attained by the use of the switch A/F and the function generator A/F - qA/F . And this requirement must be satisfied under all the operating conditions of the engine. In other words, when the engine is operated with an almost wide-open throttle on the road where the atmospheric pressure is low, the vacuum sensor V_a produces the absolute pressure output and it is impossible to measure the throttle opening from this output valve, thus making it necessary to increase the supply of fuel according to the output of the switch A/F. FIG. 36 illustrates a block diagram of an arrangement for computing the volume of fuel injection and the amount of spark advance according to the intake manifold vacuum. FIG. 37 illustrates a diagram showing, in relation to the intake manifold vacuum- V_a , the fuel injection quantity Q_v required for the engine and the fuel injection quantity Q representing Q_v plus the acceleration increment Q_{acc} and the air-fuel ratio changing increment QA/F , and in the figure the segments Q_{acc} and QA/F as related to the intake manifold vacuum- V_a show examples where an increased fuel supply is required. FIG. 38 illustrates a characteristic diagram showing the vacuum spark advance θ_v required for the engine in relation to the intake manifold vacuum- V_a .

The construction and operation of the arrangement will be explained with reference to FIG. 36. In this figure, designated as V_a is the vacuum sensor; J_{qv} represents an operational signal for computing the volume of fuel injection according to the intake manifold vacuum; $V_a - V_{a\alpha}$, $V_a - V_{a\beta}$ discriminators for determining whether the intake manifold vacuum- V_a is greater or smaller than $V_{a\alpha}$ and $V_{a\beta}$ shown in FIG. 37; 3110, 3111, 3115 and 3116 inverters; 3112, 3113 and 3114 NAND elements which, depending on the regions of the output signals of the vacuum sensor V_a on the graph shown in FIG. 37, open the gates corresponding to the regions; J_{θ_v} a signal for computing the spark advance according to the intake manifold vacuum; $V_a - V_{a\gamma}$ and $V_a - V_{a\delta}$ discriminators for determining the regions of the intake manifold vacuum- V_a in relation to the break points $V_{a\gamma}$ and $V_{a\delta}$; 3117, 3118 and 3119 NAND elements for opening the relevant gates according to the regions as determined by the last-mentioned discriminators; V_5 a coder for converting the maximum numerical value of the output of the vacuum sensor V_a into a five-place code; V_4 , V_3 , V_2 and V_1 similar coders for producing four-place, three-place, two-place and single-place codes, with the coder V_1 producing an "H" code only when the most significant digit of the vacuum sensor output is an "H." While this coding method will be explained later, it is identical to the method employed in the computation of the acceleration increment explained with reference to FIG. 33. Designated as J_{v5} may be a connecting circuit for coupling to the adder A_1 the coder V_5 which produces the five-place code or a gate circuit which issues commands to the coder V_5 to indicate whether the coding operation is to be initiated. In the current explanation of the present embodiment, J_{v5} is assumed to be the latter gate circuit. When this gate circuit J_{v5} does not

cause the coder V_5 to produce any binary code signal, the coder V_5 contains an "L" in every digit positions so that the result of the addition in the adder A_1 shows the same value as that obtained before the addition. Designated as J_{11}, J_{13}, J_{12} and J_{11} are similar gate circuits for the coders V_4, V_3, V_2 and V_1 ; K_1, K_2, K_7 and K_8 coders for producing the constant codes; AL_1 a coder for producing a code in which all the digit positions are "H"s; M a memory; $\bar{M}$ a memory for storing the stored code of the memory M in the inverted form. While the arrangement of FIG. 33, the output code of the vacuum sensor V_a is first inverted and the computation of the spark advance related to the intake manifold vacuum is performed on the basis of this inverted code, the same result may be obtained by a method in which the output code of the vacuum sensor V_a is utilized in its uninverted form on the assumption that the necessary inversion would eventually take place, and the inversion is carried out after computation. This latter method of computation is shown with one-dot chain lines in the block diagram of FIG. 32. In the discussion to follow, the latter method of the computation is used.

With the arrangement shown in FIG. 36, now assume that the signal J_{qv} for computing the volume of fuel injection is "H," then the output of the vacuum sensor V_a at this time, i.e., the value of the intake manifold vacuum $-V_a$ is located on the graph of FIG. 37 to see in which portion of the broken lines the value lies. In other words, the discriminator $V_a - V_{a\alpha}$ determines whether there is the condition $-V_a > V_{a\alpha}$ or $-V_a < V_{a\alpha}$ and concurrently the discriminator $V_a - V_{a\beta}$ determines whether there is the condition $-V_a \geq V_{a\beta}$, whereupon any one of the NAND elements 3112, 3113 and 3114 produces an "L" signal. For example, if there is the condition $V_a > V_{a\alpha}$, then the output of the NAND element 3112 is "L" and the other NAND elements 3113 and 3114 respectively produces an "H" signal. Consequently, the gate circuits J_{15}, J_{14} and J_{13} are opened such that the coders V_5 and V_4 convert the output value of the vacuum sensor V_a into the corresponding binary codes. The coder K_1 produces its constant code. Since the outputs of the remaining coders are all "L"s, the result of the addition in the adder A_1 indicates the fuel injection quantity $qv = V_5 + V_4 + K_1$, where V_5, V_4 and K_1 are the binary coded output signals of the coders V_5, V_4 and K_1 . In other words, since $V_5 \approx 2V_4$ in this case, the slope of the fuel injection quantity qv in the region $-V_a > V_{a\alpha}$ is equal to 1.5 times the slope for the output code of the vacuum sensor V_a . Then, as the value of the steady state fuel injection quantity q , the value representing this quantity qv plus the quantities of the previously mentioned acceleration increment signal qA_{cc} and the air-fuel ratio change increment signal qA/F , i.e., $q = qv + qA_{cc} + qA/F$ is stored in the memory M . As will be explained latter, the value of the steady state fuel injection quantity q must be compensated according to the engine temperature and thus it is stored in the memory M until such time that this computation takes place. In this manner, the output value of the vacuum sensor V_a is sorted on the basis of its current value and the operation of addition is performed according to the predetermined pattern of the corresponding region. Next, if it is the time that the degree of spark advance according to the intake manifold vacuum must be computed, then $J_{\theta} = 1$. Of course, it also follows that $J_{qv} = 0$. The out-

put code of the vacuum sensor V_a is then compared in the discriminators $V_a - V_{a\gamma}$ and $V_a - V_{a\delta}$ with the two values at the break points $V_{a\gamma}$ and $V_{a\delta}$ on the graph of FIG. 38 showing the required spark advance characteristics of the engine in relation to the intake manifold vacuum, thereby determining whether this output code is greater or smaller than these two values. The outputs of the discriminators $V_a - V_{a\gamma}$ and $V_a - V_{a\delta}$ cause any one of the NAND elements 3117, 3118 and 3119 to produce an "L" output, depending on the output value of the vacuum sensor V_a at this time, and according to the "L" output the gate circuits J_5 to J_1 actuate the coders V_5 to V_1 . Similarly, any one of the gate circuits J_7, J_8 and J_{AL1} is opened by the NAND elements 3117, 3118 or 3119 so that any one of the coders K_7, K_8 and K_{AL1} produces its predetermined code. As previously explained, the slope of the required spark advance characteristic θ_v of the engine according to the intake manifold vacuum has a reciprocal relation to that of the intake manifold vacuum fuel injection quantity Q required for the engine according to the intake manifold vacuum as will be seen from a comparison between FIGS. 37 and 38. Therefore, although it is possible to invert the output code of the vacuum sensor V_a in the manner shown in FIG. 32, in the discussion to follow this inversion will be performed after the completion of the required computation. As will be seen from FIG. 38, in the circuit shown in FIG. 36, if $-V_a < V_{a\gamma}$, then the degree of spark advance is zero; if $V_{a\gamma} < -V_a < V_{a\delta}$, then the spark advance has a certain slope; if $-V_a > V_{a\delta}$, the spark advance has a certain value. Now, if $-V_a < V_{a\gamma}$, then the degree of spark advance is zero, that is, the code must contain "H"s in all the digit positions before the inversion is performed. This is the constant code which is produced by the coder AL_1 . This code is then introduced into the memory $\bar{M}$ so that if the inverse is read out, it directly represents the degree of vacuum advance. On the other hand, when the engine is idling or operating at a speed below the idling speed, the intake manifold vacuum should not be taken into as a parameter. Thus, the discriminator $RPM - R_{\gamma}$ is provided to produce an "H" output when it detects the condition that the output code signal rpm of the engine speed sensor RPM is $rpm < r_{\gamma}$ (see FIG. 43), where r_{γ} is the idle speed or the like. Accordingly, if the output of the inverter 3120 is "H," then $rpm < r_{\gamma}$, so that the gate circuit J_{AL1} is opened to actuate the coder AL_1 , where rpm is the output signal of the engine speed sensor RPM . Numeral 3121 designates a NAND element for the NAND element 3119 and the inverter 3120. Then, at this time all the other gate circuits must be in their closed states and therefore the output of the discriminator is coupled to the NAND elements 3117, 3118 and 3119 as an input thereto. In this way, the degree of vacuum advance is given, as follows:

If $rpm > r_{\gamma}$, then with $-V_a > V_{a\delta}$, $\theta_v = K_7$.

If $rpm > r_{\gamma}$, then with $V_{a\gamma} < -V_a < V_{a\delta}$,

$$\theta_v = \frac{V_4 + V_3 + V_1 + K_8}{V_5 + V_4 + K_1}$$

If $rpm > r_{\gamma}$, then with $-V_a < V_{a\gamma}$, $\theta_v = \bar{AL}_1 = 0$.

If $rpm < r_{\gamma}$, the $\theta_v = 0$ independent of the value of $-V_a$. In this way, the degree of spark advance is obtained which meets the required spark advance characteristic of the engine. The output θ_v is the inverted output read out from the memory $\bar{M}$.

Next, the method of computing the additional amount of fuel injection that must be provided for starting and in consideration of the engine speed, will be explained with reference to the block diagram shown in FIG. 39. In this connection, FIG. 40 illustrates a diagram showing the additional fuel supply requirements of the engine for the starting and engine warming up operation, with the abscissa representing the engine temperature and the ordinate representing the ratio of the totals amount Q of fuel injection to the steady state fuel injection quantity q . In FIG. 40, letter S_t designates the additional amount of fuel injection required for the engine for starting, t the additional amount of fuel required for the engine warming up operation; T_ζ , T_δ and T_γ the break points for the starting fuel increment curve; T_β and T_α the break points for the engine warming up fuel increment curve. In FIG. 39, designated as T is the temperature sensor; $T - T_\beta$ and $T - T_\alpha$ discriminators for the engine warming up operation; $T - T_\zeta$, $T - T_\delta$ and $T - T_\gamma$ discriminators for the start of the engine; JT a temperature increment computation timing signal which will be at "H" when the computation of temperature increment is to be performed; ST the start sensor. Numerals 3131, 3132, 3133, 3134 and 3135 designate inverters; 3136, 3137, 3138, 3139, 3140, 3141 and 3142 NAND element selected one of which will be in the "H" state depending on the engine operating conditions as determined by the temperature of the engine and by the fact that the engine is starting or not; T_5 , T_3 and T_2 coders for converting the temperature input code into the corresponding five-place, three-place and two-place codes; K_3 , K_4 , K_5 , K_6 and 1.0 coders for producing the constant codes; J_{T_5} , J_{T_3} , J_{T_2} , J_{K_3} , J_{K_4} , J_{K_5} , J_{K_6} and $J_{1.0}$ gate circuits connected to the corresponding coders; A_2 an adder; MT a memory which stores the total sum of the addition.

In operation, in the same manner as previously explained, a selected one of the NAND elements 3136 through 3142 is caused to produce an "L" output according to the output of the temperature sensor T and the start sensor ST . This opens certain designated gate circuits to actuate the corresponding coders to produce their output codes. These output codes are then added in the adder A_2 and the sum thus obtained is stored in the memory MT . As will be seen from FIG. 40, all what is needed for the computation of the temperature increment is to determine a percentage by which the value of the steady state fuel injection quantity q must be increased, and thus the value obtained from the addition is the value by which the initial value of the steady state fuel injection quantity q is to be multiplied. The code thus obtained opens the corresponding gate circuits and at the same time the value of the previously computed steady state fuel injection quantity q is supplied as the input code, so that the total sum formed represents the total fuel injection quantity Q . This process is illustrated in FIG. 41. In this figure, designated as q is the five-place binary code signal representing the steady state fuel injection quantity whose value is previously calculated and stored; q_5 , q_4 , q_3 , q_2 and q_1 the binary code signals representing the code of the fuel injection quantity q but shifted to the right by the corresponding number of positions; mt the binary code signal stored in the memory MT of FIG. 39 which determines the temperature increment; A_2 the adder; Q the sum total representing the ultimate total amount of fuel injection. In operation, when the steady state injection

quantity q and the stored code mt of the memory MT are made available, the codes q_5 through q_1 are produced in accordance with the code mt of the memory MT . Now, if, for example, $mt = 10101$, then the codes q_5 , q_3 and q_1 are established as the five-place, three-place and single-place binary code signals representing the steady state injection quantity q but shifted to the right by the corresponding number of positions. Thus, if $q = 11011$, then $q_5 = 11011$, $q_3 = 110$ and $q_1 = 1$. In this case, q_4 and q_2 are "L"s, since mt contains "L"s in the fourth and second places. To obtain the total injection quantity Q , the sum of these codes q_5 through q_1 is formed, so that the sum total of $Q = 1.315_q$ (decimal number) or $Q = 100010$ (binary number) is the ultimately determined total amount of injection.

Referring now to FIG. 43, there is shown a block diagram of an arrangement for computing the degree of rotational spark advance related to the engine rpm. FIG. 43 illustrates the spark advance characteristic required for the engine. In FIG. 43, the binary coded output signal rpm of the engine speed sensor RPM is selected into four portions, i.e., $rpm > r\alpha$, $r\beta < rpm < r\alpha$, $r\gamma < rpm < r\beta$ and $rpm < r\gamma$ by the broken line curve. In FIG. 42, RPM is the engine speed sensor; JR the signal which provides an "H" signal when the rotational advance is to be computed, $RPM - R\alpha$, $RPM - R\beta$, and $RPM - R\gamma$ discriminators for comparing the output code rpm of the engine speed sensor RPM with the values at points $r\alpha$, $r\beta$ and $r\gamma$ on the graph of FIG. 43; 3150, 3151 and 3152 inverters; 3153, 3154, 3155 and 3156 NAND elements which produce an "H" signal depending in which region on the abscissa on the graph of FIG. 43 contains the output code rpm ; R_5 , R_4 , R_3 and R_1 coders for converting the output code rpm into the corresponding codes shifted to the right by appropriate positions; K_9 , K_{10} , K_{11} and 0 coders for establishing the constant codes; J_{R_5} , J_{R_4} , J_{R_3} and J_{R_1} gate circuits for the coders R_5 , R_4 , R_3 and R_1 ; J_{K_9} , $J_{K_{10}}$, $J_{K_{11}}$ and J_0 gate circuits for the corresponding constant coders; A_4 and adder; M_θ a memory for storing the degree of rotational advance; θR the output of the memory M_θ .

With the arrangement described above, the process of computation which takes place when $r\beta < rpm < r\alpha$ will be explained by way of example. In this situation, the discriminator $RPM - R\alpha$ produces "L" output and the discriminator $RPM - R\beta$ an "H" output, so that only the NAND element 3154 produces a "L" output to open the gate circuits J_{R_3} , J_{R_1} and $J_{K_{10}}$. This causes the coders R_3 and R_1 to convert the output binary code of the engine speed sensor RPM into the right-shifted three-place and single-place codes, respectively, and the coder K_{10} establishes its predetermined constant code. Then, the adder A_4 forms the sum of these codes and the sum thus obtained is stored in the memory M_θ . Consequently, the engine speed spark advance θR is obtained. The similar process of computation can take place in exactly the same manner with respect to the remaining regions of the output of the engine speed sensor RPM . If $rpm < r\gamma$, then the amount of rotational advance is zero and hence the 0 code is established by way of the NAND element 3156. However, in a practical circuit it is possible to arrange matters so that the 0 code will not be established.

In the foregoing, the gate circuits are provided for the respective coders. However, the result will be the same, if to the contrary the gate codes are applied to the

NAND elements which are provided in like numbers as the regions of the engine speed sensor output. Then, the sum of the rotational advance θ_R and the output of the memory $\bar{M}$ representing the spark advance according to the engine intake manifold vacuum is formed to obtain the total spark advance θ_T required for the engine in the manner illustrated in FIG. 44.

As will be apparent from the foregoing explanation, each time the addition is performed in the course of computing the acceleration increment qA_{cc} , the fuel injection quantity qv according to the intake manifold vacuum, the steady state injection quantity q , the temperature increment code mt , the vacuum spark advance θ_v , the rotational spark advance θ_R and the total spark advance θ_T , the operation of addition is performed according to the similar patterns. Accordingly, a method of performing these separate additions in a consolidated manner will be explained hereinafter. A form of the consolidated addition pattern is illustrated in FIG. 45. In this figure, designated as X_5, X_4, X_1, X_3, X_2 and K_4 are coders for establishing the five-place, four-place, single-place, three-place and two-place codes and the constant code, respectively; X, Y and Z input terminals of an adder A capable of, as a rule, adding three inputs at a time in the lowest order position and the addition of only the two inputs X and Y in the higher order positions; M_2, M_3, M_4, M_1 and M_5 memories; Σ the sum total of the addition. In operation, assuming that the coders X_1 through X_5 and the coder K_4 are actuated, the output code of the coder X_5 is coupled to the input terminal X and the output code of the coder X_4 to the input terminal, while the output of the coder X_1 is coupled to the input terminal Z since it is a single-place number and one more input in addition to the first mentioned two codes is available for the first addition. The outputs of the remaining coders X_3, X_2 and K_4 are stored in the memories M_2, M_3 and M_4 . As a result of this first connection, the sum of the outputs of the coders X_5, X_4 and X_1 at the input terminals X, Y and Z , i.e., $X'_5 + X'_4 + X'_1$ is stored in the memory M_1 by way of the adder A . Next, by the second addition, the sum m_1 stored in the memory M_1 and the content of the memory M_2 storing the output X'_3 of the coder X_3 are stored in the memory M_5 by way of the adder A . In this case, the least significant digit of the memory M_3 containing the output of the coder X_2 may also be added in the second addition. Then, the output of the memory M_5 and the content of the memory M_3 are added by way of the adder A . In the course of these operations, the memory M_1 is reset. That is, the memory M_1 is reset following the addition $m_1 + m_2 = m_5$ (where m_1, m_2 and m_5 are the outputs of the memories M_1, M_2 and M_5). Therefore, in the process of the operation $m_5 + m_3$, the content of the memory M_1 is zero, so that the memory M_1 now stores $m_3 + m_5 = m_6$. After the sum of $m_3 + m_5$ is stored in the memory M_1 as its new content, the memory M_5 is reset. Then, the content of the memory M_4 which is the output of the coder K_4 is added to the content of the memory M_1 in the adder A , so that the sum obtained is stored in the memory M_5 . At this time, the stored content of the memory M_5 is $m_5 = X'_1 + X'_2 + X'_3 + X'_4 + X'_5 + K'$ (where X'_2, X'_3 and K are the outputs of the coders X_2, X_3 and K). It is now apparent that the adders A_5 to A_8 may be replaced with a single adder by introducing a definite time delay between the succeeding steps of the addition. Furthermore, while it is unavoidable that the inputs change

momentarily depending on the conditions of an engine and hence their least significant digits vary during the addition, no change in the pattern of addition can be admitted since it may exert a serious effect on the volume of fuel injection and the amount of spark advance. In other words, should any other addition pattern be established during the current operation and carried out in addition, it results in a double addition calculating an extremely large amount of fuel injection or an unintended spark timing. This deficiency is solved in the computation performed according to the arrangement shown in FIG. 45. In other words, all codes are stored in the memories during the first step of the addition. Therefore, even if there is a change in the first pattern during the second step et seq. of the addition, it can have no effect on the current addition and thus ultimately a correct value is stored in the memory M_5 .

Referring now to FIG. 46, there is shown the arrangement of the gate circuits and the coders for constant codes by way of example. In this instance, the input is supplied from the vacuum sensor V_a . NAND elements 3112, 3113 and 3114 as well as the NAND elements 3117, 3118 and 3119 are identical with those which are shown in FIG. 36. The gate circuits J_{v5} through J_{v1} and $J_{K1}, J_{K2}, J_{K7}, J_{K8}$ and J_{AL1} are identical with those of FIG. 36 and so are the coders K_1, K_2, K_7, K_8 and AL_1 . Letter M_k designates a memory, 3122' an OR element. As previously explained, depending on the requirements according to the engine temperature and the conditions of the engine when starting, the selected one of the NAND elements 3112, 3113, 3114 and 3117, 3118, 3119 is in the "L" state. Then, since the gate circuits J_{v5} through J_{AL1} consist of NAND elements, the "L" output of the NAND element causes a set of the NAND elements to produce an "H" output, respectively. For example, when the output of the NAND element 3112 is "L", the respective NAND elements of the gate circuits J_{v5}, J_{v4} and J_{K1} produce an "H" output, so that the corresponding coders produce their outputs according to the output of the vacuum sensor V_a and the remaining coders produce no output. By simply employing the NAND elements as the gate circuits, a set of the designated codes can be always produced, as only selected one of the NAND elements 3112, 3113, 3114, 3117, 3118 and 3119 produce an "L" output at a time. Next, regarding the constant coders, there is no possibility that a plurality of constants are set for one NAND element. This is self-evident if one notes that the constant code is determined by a single straight line plus a single slope and a single constant. Thus, the fact that the selected one of the coders K_1, K_2, K_7, K_8 and AL_1 produces an output at a time means that the desired effect can be accomplished by providing an OR circuit for these coders to store their output such that the OR output is applied to the adder of FIG. 45 as the value of the coder K , that is, the NAND output is stored in the memory M_k . This situation is represented by the OR element 3122'. In actual practice, there are as many OR circuits as there are digits in the code and therefore a large number of the OR elements 3122' will be employed.

Referring now to FIG. 47, there is illustrated an arrangement in which a single coder is employed for the above described several input codes from the engine to establish the converted codes corresponding to the input codes, so that the converted codes are successively delivered to the output at different times accord-

ing to the inputs. In this way, the previously described several additions of the similar pattern can be performed entirely in a single adder. In FIG. 47, numeral 3161 designates a NAND element for setting up the most significant digit input of the five-place input from the vacuum sensor V_5 ; 3166, 3171, 3176 and 3181 NAND elements for setting up the lower order fourth-place, third-place, second-place and first-place or the lowest order digits of the same five-place input, respectively. Similarly, numerals 3162, 3167, 3172, 3177 and 3182 designate NAND elements for setting up the most significant digit and the fourth-place, third-place, second-place and first-place digits of the acceleration signal a_{cc} from the acceleration sensor A_{cc} . Numerals 3163, 3168, 3173, 3178 and 3183 designate NAND elements for setting up the similar digit positions of the output signal of the temperature sensor T ; 3164, 3169, 3174, 3179 and 3184 NAND elements for setting up the similar digit positions of the output signal of the engine speed sensor RPM; 3165, 3170, 3175, 3180 and 3185 NAND elements for setting up the similar digit positions of the steady state fuel injection quantity q . Designated as V_{a5} is the fifth-place signal from the vacuum sensor V_a ; V_{a4} , V_{a3} , V_{a2} and V_{a1} the similar codes from the vacuum sensor V_a having the digit positions as indicated by their suffixes; A_{cc5} , A_{cc4} , A_{cc3} , A_{cc2} and A_{cc1} the similar codes of the acceleration signal A_{cc} ; T_5 , T_4 , T_3 , T_2 and T_1 the similar codes from the temperature sensor T ; rpm5, rpm4, rpm3, rpm2 and rpm1 the similar codes of the output signal from the engine speed sensor RPM; D_5 through D_1 the similar codes of the steady state fuel injection quantity. Numeral 3186 designates a NAND element for the most significant digit input codes; 3187, 3188, 3189 and 3190 NAND elements for the fourth-place, third-place, second-place and first-place or the lowest place digits, respectively. Designated as J_{va} is the signal which provides an "H" output at the time that the output code of the vacuum sensor V_a is to be converted; J_{acc} , J_T , J_{RPM} and J_D the similar signals which produce an "H" output when the acceleration signals A_{cc} , the output signals of the temperature sensor T and the engine temperature sensor RPM and the steady state fuel injection quantity q , respectively, are to be converted. Although not shown in the previously described embodiments, according to the arrangement described herein the five-place input can be converted into the codes including from the six-place code down to the single-place code. By following the similar procedures, the seven-place code, the eight-place code and so on can be readily obtained. Numerals 3191 through 3195 designate the sixth-place to second-place NAND elements for setting up the six-place code; 3196 a NAND element for setting up the first-place or the lowest order digit of the six-place code, the output thereof being always "L." Numerals 3197 through 3201 designate NAND elements for setting up the five-place code, 3202 through 3205 NAND elements for setting up the four-place code. Similarly, numerals 3206 through 3208, and 3209 and 3210, respectively, designate NAND elements for setting up the three-place and two-place codes, 3211 a NAND element for setting up the single-place code; J_6 a signal for initiating the setting up of the six-place code; J_5 , J_4 , J_3 , J_2 and J_1 signals for initiating the setting up of the five-place through single-place codes, respectively.

With the arrangement described above, assume that it is the time that the output code of the vacuum sensor

V_a is to be converted and that the NAND element 3112 in FIG. 46 is in its established state. Then, the outputs of the NAND elements J_{v5} , J_{v4} and J_{v1} in FIG. 46 are all "Hs". In this coordinated coder, the NAND elements constituting the gate circuits are no longer used exclusively for any sensors, such as, the vacuum sensor V_a and the engine speed sensor RPM, and therefore in this case the gate circuits J_{v5} , J_{v4} and J_{v1} are simply opened or producing an "H" output, respectively. Particularly, so far as the variable codes are concerned the gate circuits J_{v5} and J_{v4} respectively produce an "H" output. Now, since the codes related to the intake manifold vacuum are to be set up, $J_{va} = 1$ and then the output of the vacuum sensor V_a are now established in the five NAND elements 3186, 3187, 3188, 3189 and 3190. Since all other signals J_{acc} , J_T , J_{RPM} and J_D are "L"s, there is no possibility that any other signal input is established in the NAND elements 3186 through 3190. Then, since the input signals J_5 and J_4 are in the "H" state, the fifth-place signal V_{a5} is introduced at the inputs of the NAND elements 3197 and 3202 thereby producing at the output thereof a code which is the inverse of the fifth-place signal V_{a5} . In like manner, the inverted signal of the fourth-place signal V_{a4} appears at the output of the NAND elements 3198 and 3203, respectively, the inverted signal of the third-place signal V_{a3} at the outputs of the NAND elements 3199 and 3204, the inverted signal of the second-place signal V_{a2} at the outputs of the NAND elements 3200 and 3205, and the inverted signal of the first-place signal V_{a1} at the outputs of the NAND element 3201. The outputs of the remaining NAND elements are all "H" signals thus establishing no outputs. By this inversion of all the codes, the intended codes are obtainable. This may be readily attained by means of inverters connected in series to these NAND elements or by employing a flip-flop as a memory so that the element whose state is inverted with respect to the input may be read out. Now, if the signal J_6 for initiating the setting up of the six-place code is "H," the NAND element 3196 for the lowest order digit position of the six places has no corresponding input and so it is designed such that an "H" signal is always produced at the output of this NAND element. In other words one input terminal of the NAND element is kept always at "L". Then, the code shifted one place to the left is obtained. Now consider the input to the NAND element 3191. If the output code of the vacuum sensor V_a is 10110, then the six-place code obtained is 101100. In other words, the original code is shifted one place to the left. On the other hand, if the input signal $J_4 = 1$, then with the output code 10110 of the vacuum sensor V_a the input to the NAND elements 3202 through 3205 consists of a four-place code of 1011. For purposes of clarity, these six-place code 101100 and the four-place code 1011 are shown as the input codes to the respective NAND elements, although the signals appearing at their outputs are inverted with respect to the inputs. Now, regarding the codes having more digit positions than the input codes, so that some of their lower order digit positions have no corresponding input codes, there can be practically no problem if they contain "L"s in the reinverted outputs of the NAND elements and therefore there is no need to provide any specified circuit for this purpose.

Referring now to FIG. 48, there is illustrated the construction of a circuit for connecting the outputs of the

above-mentioned coders to the adder. In this figure, the operation of the arrangement shown by the block diagram of FIG. 45 is shown as an example of the actual circuit. To avoid any complexity which may arise if the circuits of all the digit positions are explained, the circuit construction will be illustrated for the lowest digit positions only. In FIG. 48, designated as X_5 , X_4 , X_3 , X_2 and X_1 are coders for producing the coders having as many digits as indicated by their suffixes; 3201, 3208, 3210, 3205 and 3211 the same NAND elements as designated by the reference numerals in FIG. 47; 3122 the same OR element as designated by the same reference numeral in FIG. 46; 3213, 3214, 3215, 3216 and 3217 inverters whose inverted outputs represent the desired converted codes; 3218, 3219, 3220, 3221, 3222, 3223, 3224 and 3225 NAND elements which indicate the timing of computations; 3226 and 3227 NAND elements which determine whether the data obtained after the addition should be stored in a memory M_1 or a memory M_5 ; 3228 and 3229 NAND elements for applying the data to input terminals X and Y, respectively; 3230 a NAND element for connecting the final result of the addition to the output circuit; M_2 , M_3 , M_4 , M_1 , M_5 , X, Y, Z and A the identical elements being designated by the same reference numerals in FIG. 45; R_1 through R_8 signals indicating the sequence of computations which are to be performed in the order as indicated by the suffixes. In the first step of the addition where R_1 is the "H" state, the codes from the coders X_5 , X_4 and X_1 are coupled to the input terminals X, Y and Z respectively by way of the inverters 3215, 3216, 3217 and the NAND elements 3218 and 3222, and the sum of these codes is applied to the input of the memory M_1 by way of the adder A. Since the code produced in the coder X_1 is a single-place code, no circuit will be connected to the input terminal Z during the succeeding operations on the next least significant position et seq. Next, with R_2 in the "H" state the memory M_2 storing the output code of the coder X_3 is coupled to the input terminal X and the result of the first addition stored in the memory M_1 is connected to the input terminal Y by way of the NAND elements 3219, 3223 and the NAND elements 3228, 3229, so that the second addition is performed in the adder A and the result of the addition is then stored in the memory M_5 . This situation is shown in the lower part of FIG. 48. In this state, there is no memory available to store the result of the succeeding addition unless one of the previously set memories M_1 and M_5 is reset. Thus, with R_3 in the "H" state, the memory M_1 is reset to erase its content which is utilized in the second addition and is now useless. Then, with R_4 in the "H" state, the two-place code from the coder X_2 is coupled to the input terminal X and the memory M_5 is coupled to the input terminal Y with the memory M_1 being coupled to the output of the adder A, and a further addition now takes place in the adder A. Thereafter, with R_5 in the "H" the memory M_5 is reset, and with R_6 in the "H" state the memory M_4 storing the constant code is coupled to the input terminal X and the memory M_1 is coupled to the input terminal Y, with the memory M_5 being coupled to the output of the adder A. With the end of this step, the whole operation of the addition is finally completed, and now with R_7 in the "H" state the output of the memory M_5 storing the final result of the addition is coupled to the output circuit by way of the NAND element 3230. Then, with R_8 representing the eighth step of the addition now in the

"H" state, the whole procedure is over and the contents of all the memories are reset. In fact, the memories M_2 , M_3 and M_4 may be reset earlier in the addition cycle, since these memories are such that they could be reset upon completion of the operations to which these memories are pertinent.

With the addition system illustrated in FIG. 48, the addition of any arbitrary code independent of the established codes is only possible by way of the memory M_4 which stores the constant code from the coder K. Thus, without any modification in this system, it is difficult to effect the addition of the fuel quantities for acceleration and for changing the air-fuel ratio and the fuel quantity according to the intake manifold vacuum which are necessary for computing the volume of fuel injection, and it is also difficult to effect the addition of the vacuum spark advance and the centrifugal spark advance. This problem is solved by the circuit shown in FIG. 49. In this figure, only those portions which relate to the addition of the most significant digits or the first-place digits of the respective codes are shown. The component parts designated by the identical reference numerals as used in FIG. 48 will not be explained. While numerals 3213 and 3214 designate the inverters in FIG. 48, the same numerals designate NAND elements in this figure, since these inverters can act as NAND elements by simply adding one more input to each of the inverters. Numerals 3240, 3241 and 3242 designate NAND elements for setting up the most significant digits of the codes qA_{cc} , qA/F and qv ; R_1 designates the time that the computation of the steady state fuel injection quantity $q = qA_{cc} + qA/F + qv$ should be initiated. As already mentioned, the memories M_2 , M_3 and M_4 may be reset as soon as the computations to which they are related are over and thus these memories are reset at R_3 , R_5 and R_7 , respectively, in this figure. At the time that the steady state fuel injection quantity q is to be computed, it is only necessary to store the values of qA_{cc} , qA/F and qv in the memories M_2 , M_3 and M_4 in place of the outputs of the coders X_3 , X_2 and K. Accordingly, when the timing signal R'_1 is in the "H" state, the values of qA_{cc} , qA/F and qv are stored in the memories M_2 , M_3 and M_4 by way of the NAND elements 3122, 3214 and 3213 and the addition is performed according to the same procedure as shown in FIG. 48 to thereby attain the desired result. Of course, at this time the signals J_3 , J_2 and J_K are all "L"s.

While the addition on the least significant digits has been described, the operations on the higher order digits can be performed in like manner. In the foregoing explanation of the addition, no mention has been made of the subtraction operation. However, while in the process of computing the various characteristics the slopes can be made almost consistent according to the procedures described hereinbefore, it is believed that the operation of subtraction is needed for the constant codes. In the discussion to follow, the situations where such subtractions are needed will be explained. Now, assume that the adder A has five digit positions. Then, consider the situation where the code to be obtained is $X'_5 + X'_4 - 1$. In this case, the subtraction by the addition of the complement is well known, in which the adder A will be considered as having six digit positions so that the digits in the five least significant positions represent $X'_5 + X'_4 - 1$, that is, an "H" is added to the inverted code of the 1 which here results in 11111 and

this code is added to effect the subtraction. In this way, the subtractions can also be performed to give characteristics which are represented by any given straight lines.

Next, referring to FIG. 50 there is shown a circuit for indicating the timing and sequence of computations to be performed. In this figure, designated as FF₁, FF₂ and FF₃ are flip-flop circuits which are set upon receipt of clock pulses t_c ; FF₄, FF₅ and FF₆ flip-flop circuits connected in series with the flip-flops FF₁, FF₂ and FF₃; 3250, 3251 and 3252 inverters; 3253 through 3260 NAND elements which sequentially produce outputs according to the outputs of the flip-flop circuits FF₁, FF₂ and FF₃; 3261 through 3268 inverters; 3270, 3271 and 3272 inverters; 3273 through 3280 NAND elements; 3281 through 3288 inverters; R₁ through R₈ signals adapted to successively assume the "H" output state in accordance with the output codes of the flip-flops FF₁, FF₂ and FF₃, with the inverters 3281 through 3288 similarly successively assuming the "H" output state so that R_{Acc}, R_{qv}, R_q, R_T, R_θ, R_{θv}, R_{θR} and R_θ successively assume the "H" state. In the first-place, if the flip-flops FF₁ through FF₆ are all in the "L" state, then the memories are reset altogether. Then, upon arrival of the first clock pulses, since R_{Acc} is in the "H" state, with R₁ now assuming the "H" state the output code of the acceleration sensor A_{cc} is converted through the circuit of FIG. 47 so that as shown in FIG. 48 the result of the addition of the five-place, four-place and single-place codes is stored in the memory M₁ by way of the adder A and the other codes are stored in the memories M₂, M₃ and M₄; thereafter the addition procedures are followed as previously described in accordance with the signals R₂, R₃, ..., R₈. At R₂ through R₈, these signals have nothing to do with the input codes and thus these signals are simply employed for the purposes of computation. When the flip-flops FF₁ through FF₆ all contain "L"s, upon completion of the above-mentioned process, the flip-flops are reset to "L" altogether and as also shown in FIG. 49, all the memories are cleared to "L" so that they are available for new inputs.

Referring to FIG. 51, there is illustrated a diagram showing the relations and connections of the various gate signals with the above-described circuit of FIG. 50 for directing the sequence of computations. In FIG. 51, numerals 3300 through 3307 designate NAND elements for generating gate signals; 3308 through 3315 inverters; 3314 a NAND element for establishing the engine intake manifold vacuum. Assuming that now is the time to compute the additional amount of fuel supply for acceleration, then the acceleration increment signal a_{cc} must be introduced at the input of the corresponding coders. Thus, in FIG. 47 it is necessary that J_{Acc} = 1. To attain this, it is designed such that J_{Acc} assumes the "H" state when each of the outputs R₁ and R_{Acc} change from the "L" to "H" signal simultaneously, and, at the same time, all the data of the acceleration increment signal acc are stored. This procedure is entirely applicable to the other inputs. As shown in FIG. 48, the signals R₁ through R₆ have nothing to do with the input signals and they simply control the sequence of computations. Since the codes of the vacuum sensor V_a are employed for computing the fuel injection quantity qv and also for computing the spark advance θ_v according to the engine intake manifold vacuum, the NAND element 3314 generates the signal

J_v. However, since the comparison operation for the spark advance θ_v must be made with entirely different value, the separate signals J_{qv} and J_{θv} are generated. On the other hand, the same timing signal R'₁ is employed in the computation of both the steady state fuel injection quantity q and the total spark advance θ_T of the engine as will be explained later. And in this case, the adder operates on the contents of the memories and not on the contents of the coders. This situation is shown in FIG. 49. FIG. 49 is referred to, since it is related to the computation of the steady state fuel injection quantity q and the contents of the memories are the values of qA_{cc}, qv and qA/F.

FIG. 52 illustrates the interconnections between the memories and the adder. In this figure, numerals 3320 through 3325 designate NAND elements for determining the contents of the memories; 3326, 3327 and 3328 NAND elements which function upon receipt of the signals from the NAND elements 3320 through 3325; 3329 through 3334 NAND elements for resetting the contents of the memories 3336 and 3337 NAND elements; 3338 and 3339 NAND elements for detecting whether the contents of the memories should be inverted; 3340 an inverter; 3341 a NAND element; M_a, M_b and M_c memories. If the computation of the fuel injection quantity q required for an engine is performed without involving any computation of the spark advance for the engine so that the memories store information as needed and they are reset as soon as the relevant computations are over, sharing of the memories is possible. Furthermore, if the air-fuel ratio change signal qA/F is stored in the memory M_c in the course of the computation of the steady state injection quantity q and the memory M_c is utilized in the manner shown in FIG. 49, the memory M_c may be reset when R_q = R_s = 1 so that it is used again at R_q = R_T = 1 during the computation. When computing the vacuum spark advance θ_v, the content of the memory N_a must be inverted and the inverter 3340 is inserted to effect this inversion. While the foregoing explanation has been made only in respect of the least significant digits, the whole circuit may be connected in exactly the same manner to effect the required addition.

FIG. 53 illustrates the sequence of operations of the whole system on the basis of the description made hereinbefore. Initially, the outputs of the flip-flops FF₄, FF₅ and FF₆ are all "L"s and when R₁ = 1, then J_{Acc} = 1 initiating the computation of qA_{cc}. This computational pattern is the same as shown in FIG. 33. Then, the output code of the acceleration sensor A_{cc} is suitably selected as qA_{cc} on which an addition is performed, and the result of this addition is stored in a memory M_{qAcc}, that is, the memory M_a in FIG. 52. Simultaneously, the air-fuel ratio change signal qA/F is stored in the memory M_c. Next, at J_{qv} = 1, the codes established according to the engine intake manifold are suitably selected and added so that the result of the addition is stored as qv in a memory M_{qv} which is the memory M_b. Then, at the signal J_q, all of the thus stored qA_{cc}, qA/F and qv are introduced into the memories according to the computation pattern shown in FIG. 49 and the addition is performed according to the addition pattern shown in FIG. 48. The result of the addition is restored as q in a memory M_q, i.e., the memory M_c. Then, at J_T = 1, the pattern by which the volume of fuel injection is corrected for the engine temperature is determined. This computational scheme is established as a pattern which deter-

mines a percentage by which the steady state fuel injection quantity q is increased, and it is then stored in the memory MT shown in FIG. 39. Consequently, at $J_{\theta} = 1$, the said pattern P is coupled to the gate circuit J_i for the codes, and the previously stored q is established in the various coders according to the pattern in the gate circuit J_i , so that the sum of these codes is formed to determine the total injection quantity Q. The value of this total injection quantity Q is transferred at $R_q = R_7 = 1$ to the memory M_q shown in FIG. 32, from which it is coupled to the injection circuit. The output of the vacuum sensor V_a is converted into the codes for the second time. This conversion is determined according to $J_{\theta v}$ in FIG. 36, and the result of the addition is set up as the inverted code of the vacuum spark advance. This value is stored as θ_v in a memory $M_{\theta v}$, i.e., the memory M_a so that it is inverted as shown in FIG. 52 when it is to be supplied to the output circuit. Then, at $R_{\theta R} = 1$, the spark advance according to the engine speed is computed and its value is stored in the memory M_b . Thereafter, at $R_{\theta} = 1$, the sum of the vacuum advance $\theta_v = \bar{M}_a$ and the rotational advance θ_R or the content of the memory M_b is formed to give the total spark advance θ_T which is in turn stored in the memory M_{θ} . At $R_{\theta} = R_7 = 1$, the total spark advance θ_T is transferred as the output, whereupon all the memories are reset by the second clock pulses.

In the foregoing explanation, the manner in which the memories are reset and the addition procedures are not described in detail. The whole cycle of operations starts at $R_{acc} = R_1 = 1$ and ends at $R_{\theta} = R_8 = 1$ and a new cycle of operations is initiated upon arrival of the succeeding clock pulses.

Embodiment 5:

According to the present embodiment, a system is provided in which a single operational circuit adapted to control the fuel injection system, the ignition system and the like which have direct effects on the performance of an engine, is also employed to perform the necessary computational operations to control the power and drive systems which are not directly related to the operation of the engine, such as, the automatic transmission with a fluid torque converter, the anti-lock device and the direction indicator. The system of the present embodiment thus contemplates the standardization of the operational circuit employed in vehicles, particularly automotive vehicles to thereby eliminate unnecessary complexity and disadvantages which may arise if a plurality of operational circuit are incorporated.

According to the system of the present embodiment, it is designed such that one cycle of computational operations are completed during a time interval in which no ignition spark is produced by any spark plug in the engine, thereby eliminating the undesired effect of the ignition spark on the computations to prevent any malfunctioning.

The system of the present embodiment will now be explained with reference to the drawings. In the first place, the general construction of the system is identical to that of the system of the fourth embodiment as explained with reference to FIG. 32. The conversion procedures of the acceleration increment signal qA_{cc} and the air-fuel ratio change signal qA/F are also the same as described with reference to FIGS. 33, 34 and 35.

The construction and operation of the arrangement illustrated in FIG. 54 are the same as those as described in connection with the fourth embodiment.

In FIG. 54, numerals 4110 through 4114 designate inverters; 4112 through 4114 NAND elements which open the relevant gate circuits depending on the region of the output signal of a vacuum sensor V_a on the graph of FIG. 37 (the fourth embodiment); 4117 through 4119 NAND elements which open the relevant gate circuits depending on the region of the output signal of the vacuum sensor V_a on the graph of FIG. 38.

Referring now to FIG. 57, there is illustrated an arrangement for determining the operating characteristic to control the fluid torque converter automatic transmission installed in an automobile. While the computational operations for the control of this automatic transmission have nothing to do with the control of the fuel injection and the spark advance of the engine as described hereinbefore, the procedures by which the parameters of the various parts of the automobile indicating the conditions of the engine and the automobile are derived as binary code signals and the operating characteristics are then determined utilizing these binary code signals, are all the same. In the system which will be described hereinafter, the same operational circuit as employed for the previously described control of the engine is also utilized for the control of the automatic transmission. In FIG. 57, designated as Φ is a throttle opening sensor for producing a binary code signal ϕ corresponding to the opening of the engine throttle valve; MAX, a coder for producing a reference code in which only the most significant position contains an "H" and all the remaining lower order positions contain "L"s; $(AS + B) + 1$ a coder for producing a gear shifting code $(as + b) + 1$; S a sensor for producing a binary code signal corresponding to the vehicle speed or the slip factor between the input and output shafts of the torque converter (in the discussion to follow, this will be referred to as a vehicle speed sensor for producing a binary code signal corresponding to the vehicle speed); C_0 a coder; LS_1 , LS_2 , LS'_2 and LS_3 discriminators for determining whether the binary coded output signal s of the vehicle speed sensor S is greater or smaller than predetermined values; J_1 , J_2 , J'_2 and J_3 gate circuits which enable the coder C_0 to produce codes. Designated as A_6 is an adder which forms the sum of the codes from the coder C_0 , and the output binary code $(as + b) + 1$ of the coder $(AS + B) + 1$ represents the result of the addition of the codes in the adder A_6 ; A_7 an adder (if the addition in this adder is performed at a time different from that of the adder 6 which forms the sum of the codes from the coder C_0 , both the additions can be performed by the same adder); G_1 , G_2 and G_3 gear position signal generators for producing gear position signals corresponding to the conditions in the automatic transmission in the first-speed, second-speed and third-speed, the gear position signal generator including actuators for changing the engagement of the gears into the first-speed, second-speed and third-speed gears upon application of an "H" signal thereto; H_1 , H_2 and H_3 hold circuits for the gear position signal generators G_1 , G_2 and G_3 ; MG a gear shift changing memory for receiving the most significant position signal which is either "H" or "L"; 4350 an inverter; 4351, 4352, 4353 and 4354 NAND elements for the gear shifting; 4355, 4356 and 4357 NAND elements for the gear shifting; T_{01} a gear shifting

signal, i.e., a gearshift timing signal for the gear shifts from the 1st to second speed, the second to third speed and the third to second speed; T_{02} a gearshift timing signal for the gear shift from the second to the first speed; $\bigcirc$, $\bigcirc$ and $\bigcirc$ terminals for connection to the inputs of the corresponding NAND elements 4355, 4356 and 4357.

With the arrangement described above, the vehicle speed sensor S for detecting the car speed first produces a binary code signal. In this case, as shown in FIG. 58 (the abscissa = the binary coded output signal s of the vehicle speed sensor S, the ordinate = the binary coded output signal ϕ of the throttle opening sensor Φ), it is prearranged so that the gear position is determined according to the relation between the vehicle speed and the throttle opening. In FIG. 58, a line I designates a gear shift up line from the first to second speed; II a gear shift up line from the second to third speed; III a gear shift down line from the second to first speed; IV a gear shift down line from the third to second speed. Now, if the gears are in the first speed and the binary coded output signal of the vehicle sensor S indicates that $s_2 > s$, then the gears are unconditionally retained in the first speed; if $s_2 < s < s_5$, then, in relation with the opening of the engine throttle valve, and depending on whether the condition is located above or below the shift up line I on the graph of FIG. 58, the gears are retained in the first speed if the condition is above the line I, while the upshift to the second speed is effected if the condition is located below the line I. On the other hand, if the binary coded output signal s of the vehicle sensor S indicates that $s > s_5$, then the gears are unconditionally shifted to the second speed. Similarly, the gear positions are determined as shown in Table 1.

TABLE 1

Gear position before shift	Vehicle speed sensor S output	Gear position after shift
G_1	Binary code s	G_1
g_1	$s < s_2$	g_1
g_1	$s_2 < s < s_5$	Upshift g_1 (above line I), g_2 (below I)
g_1	$s > s_5$	g_2
g_2	$s < s_4$	g_2
g_2	$s_4 < s < s_7$	Upshift g_2 (above line II), g_3 (below II)
g_2	$s > s_7$	g_3
g_2	$s < s_1$	g_1
g_2	$s_1 < s < s_4$	Downshift g_1 (above line III), g_2 (below III)
g_2	$s > s_4$	g_2
g_3	$s < s_3$	g_2
g_3	$s_3 < s < s_6$	Downshift g_2 (above line IV), g_3 (below IV)
g_3	$s > s_6$	g_3

The gear positions as shown in the above table must be obtained in relation with the various values of the binary coded output signal s of the vehicle speed sensor S. Accordingly, upon arrival of the output code s of the vehicle speed sensor S, if the gears are in the first speed position g_1 , the discriminator LS_1 examines whether the condition is located above or below the shift up line I in FIG. 58. Now, if the value of the output binary code s of the vehicle sensor S is smaller than s_2 , the comparison between s and s_2 alone is sufficient to determine that the first speed gear is to be maintained. In like manner, if $s > s_5$, then the upshift to the second speed is directed by the comparison between s and s_5 alone. All these operations are performed by the discriminator LS_1 . On the other hand, if $s_2 < s < s_5$, the value of s must be converted so that the gear position is determined according to the opening of the throttle valve. When the gear positions indicate the second and third speeds, the discriminators LS_2 , LS'_2 and LS_3 similarly perform the required comparison operations. With the gears in the second speed, however, the gear shift signal produced must be either a 2-3 upshift signal or a 2-1 downshift signal. Therefore, the discriminators LS_2 and LS'_2 perform the comparison operation on these two possibilities.

Next, explanation will be made of the situation in which there is the condition $s_2 < s < s_5$ with the gears in the first speed. Firstly, that portion of the gear shift up line I which corresponds to the conditions $s_2 < s < s_5$ can be given as $a_{18} + b_1$. This is obtainable by performing the characteristic conversion operation on the binary coded output signal s of the vehicle sensor S in the manner as described in relation with the computation of the amount of fuel injection and the amount of spark advance. On the other hand, since no gearshift takes place in the region to the left of the gear shift up line I, the relation between the binary coded output signal ϕ of the throttle opening sensor Φ and the above-mentioned portion $a_{18} + b_1$ is determined by $\phi - (a_{18} + b_1) \approx 0$. If $\phi - (a_{18} + b_1) > 0$, the portion is on the left side of the gear shift up line I and so the first speed gear is maintained. If $\phi - (a_{18} + b_1) < 0$, the portion is on the right side of the gear shift up line I and in this case the gearshift to the second speed is effected. When $\phi - (a_{18} + b_1) < 0$, then a negative code is produced. Then, the coder MAX_1 for producing a reference code produces a code max_1 which has more digits than any of the codes ϕ and $(a_{18} + b_1)$ with the most significant position containing an "H" and all the lower order positions containing "L"s, and now it is possible to compute $max_1 + \phi - (a_{18} + b_1)$. In this case, if $\phi - (a_{18} + b_1) < 0$, then the "H" in the most significant position of the code max_1 changes to "L". In this way, the comparison $\phi - (a_{18} + b_1) \approx 0$ can be performed. In this connection, the computation $\phi - (a_{18} + b_1)$ requires the provision of a subtractor. To perform this subtraction with an adder, it is only necessary to produce the inverted code $(as + b) + 1$ of the code $a_{18} + b$ and add this to the code ϕ . This code is then added to the code max_1 so that by examining whether the most significant position of the code max_1 retains "H," the comparison $\phi - (as + b) \approx 0$ can be performed. This operation will be explained hereunder.

In operation, the output binary code s of the vehicle speed sensor S is first introduced and it is determined that the gear position is the first speed gear g_1 . Then,

as the discriminator LS_1 finds that $s_2 < s < s_5$, the codes produced in the coder C_0 according to the predetermined pattern are added in the adder A_6 , so that the shift coder $(AS + B) + 1$ produces the code $(a_{1s} + b_1) + 1$. Then, the sum of this value and those of ϕ and $\max_1$ are formed in the adder A_7 , and only that particular digit position of $\max_1$ into which an "H" was previously introduced is stored in the memory MG. If the content of the memory MG is "L," then it indicates that the comparison $\phi < (a_{1s} + b_1)$ is met and hence the gear shift to the second speed is directed. At this time the gears are still in first, so that the gear position signal generator G_1 is in the "H" state and hence the hold circuit H_1 is also in the "H" state, and moreover the 1 - 2 upshift timing signal T_{01} is also "H." Consequently, only the NAND element 4351 produces an "L" output. Whereupon, the NAND element 4356 produces an "H" output, thereby changing the gear into second. In this case, if the hold circuit H_2 is allowed to assume the "H" state upon the upshift to the second speed, a further upshifting into the third speed may result. To prevent this, a preset time delay is provided for each of the hold circuits H_1 , H_2 and H_3 so that when the hold circuit H_1 is in the "H" state, this "H" output of the hold circuit H_1 is not permitted to appear at the output of the hold circuit H_2 .

The circuit which introduces such a preset time delay is illustrated in FIG. 59 by way of example. In this figure, designated as g_1 is the output of the gear position signal generator G_1 representing the first speed gear; 4358 a resistor, 4359 a capacitor, 4360 a NAND element; 4361 an inverter; Out H_1 and output terminal. In operation, when the first speed gear signal g_1 is applied to the hold circuit H_1 , the capacitor 4359 is charged by way of the resistor 4358. Eventually, the capacitor 4359 charged up to a level equal to the "H" level of the NAND element 4360 so that the output of the NAND element 4360 changes from "H" to "L." This "L" output is then inverted by way of the inverter 4361 to deliver an "H" output at the output terminal Out H_1 . As compared with the first speed gear signal g_1 , this "H" output appears after a delay determined by the time constant of the resistor 4358 and the capacitor 4359. By making this delay time larger than the shift commanding time, the desired effect can be attained. As with the upshift from the second speed to the third speed, the upshift from the first speed to the second speed is effected similarly depending upon the result of the comparison operation performed on $\phi - (a_{2s} + b_2) \geq 0$ according to the gear shift up line II. Furthermore, the downshift from the third speed to the second speed takes place when the comparison $\phi - (a_{3s} + b_4) > 0$ is found. In this connection, the result of the comparison operation is reversed in relation to that which is obtained when the 1 - 2 upshift occurs. Consequently, if $s_3 < s < s_6$ in the third speed, then the computation $\phi + \max_1 + (a_{4s} + b_4) + 1$ is performed, and the gearshift command is issued if the stored code of the memory MG is "H." This comparison is performed by means of the NAND element 4352, so that when the output of the NAND element 4352 assumes "L," the NAND element 4356 produces an "H" output to thereby effect the downshift to the second speed. Similarly, the downshift from the second to the first speed takes place depending upon the result of the comparison $\phi + (a_{3s} + b_4) \geq 0$ performed according to the shift down line III.

Next, the operation of producing the code $(as + b) + 1$ will be explained with reference to FIG. 61. In this figure, designated as S is the vehicle speed sensor; S_V a coder for inverting the binary coded output signal s of the vehicle speed sensor S to produce the five-place code $\bar{s}_5$; S_{IV} a coder for producing the inverted four-place code $\bar{s}_4$; S_{III} , S_{II} and S_I similar coders for producing the inverted three-place code $\bar{s}_3$, two-place code $\bar{s}_2$ and single-place code $\bar{s}_1$, respectively; K_I a coder for producing the constant code K_{21} which has nothing to do with the binary coded output signal s of the vehicle speed sensor S for the code $(as + b) + 1$, but related to the gear shift up line I shown in FIG. 58; K_{II} , K_{III} and K_{IV} coders for producing the constant codes K_{22} , K_{23} and K_{24} and related to the lines II, III and IV shown in FIG. 58. In this connection, the computational operations relating to these lines are not performed at the same time. Designated S_{Ks} a coder into which the constant codes K_{21} , K_{22} , K_{23} and K_{24} in the coders K_I , K_{II} , K_{III} and K_{IV} are transferred; A_8 an adder; J_{s5} a command signal for initiating the setting up of the five-place code in the coder S_V ; J_{s4} , J_{s3} , J_{s2} and J_{s1} similar command signals for initiating the setting up of the three-place, two-place and single-place codes; J_{K21} a coding command signal for initiating the setting up of the constant code K_{21} in the coder K_I when the comparison operation is to be performed according to the gear shift up line I in FIG. 58; J_{K22} , J_{K23} and J_{K24} similar coding command signals for initiating the setting up of the constant codes related to the lines II, III and IV in FIG. 58. In operation, upon arrival of the binary coded output signal s from the vehicle speed sensor S, some of the coding command signals J_{s5} through J_{K24} are generated according to either one of the discriminators LS_1 , LS_2 and LS_3 , so that some of the coders S_V through S_I produce the output codes. As previously mentioned, only a selected one of the coders K_I through K_{IV} produces its output code at a time and therefore only one of the codes K_{21} through K_{24} is applied as an input code signal to the coder S_{Ks} . Therefore, the connection among the coders K_I through K_{IV} and the coder S_{Ks} are established by way of an OR or NOR circuit. When the constant code is set up in the coder S_{Ks} in this way, the adder A_8 forms the sum of this constant code and those codes produced by the selected ones of the coders S_V through S_I , thereby producing the code $(as + b) + 1$.

The operation of the system of this embodiment will be explained in more detail with reference to FIG. 62. In this figure, designated as H_1 , H_2 and H_3 are hold circuits; J_{T0a} command signals for initiating the comparison of the binary coded output signal s of the vehicle speed sensor S and the values at the points S_1 , S_2 , S_3 , S_4 , S_5 , S_6 and S_7 in FIG. 58; J_{T0b} are similar command signals for initiating the comparison of the signal s and the values S_1 and S_4 . While the shifts from the first or third speed to any other speed gears can be determined with a single comparison operation, with the gears in second the gearshift may be either upshift to the third speed or downshifted to the first speed, and therefore the comparison operation must be performed twice. For this reason, in the second speed gear position the decision on the downshift to the first speed is performed at a time different from that of the decision in any other speed positions. Designated as $S - S_5$ a discriminator which produces an "H" when the binary coded output signal of the vehicle speed sensor S is greater than s_5 and an "L" when s is smaller than s_5 ; $S - S_2$ a discrimina-

tor for similarly producing an "H" when $s > s_2$; S-7, S-4, S-S₁, S-S₆ and S-S₃ similar discriminators for producing an "H" signal when the value of s is greater than the minuend; 4370 through 4377 inverters; 4378 a NAND element which receives the "H" signal from the discriminator S-S₅ to produce an "L" signal and whose output is shown as connected to the input terminal 2 of the NAND element 4356 in FIG. 57. Similarly the outputs of NAND elements 4383, 4384 and 4389 are connected to the input terminal ○ of the NAND element 4356. In like manner, the outputs of the NAND elements 4380 and 4386 are connected to the input terminal ○ of the NAND element 4357, and the outputs of the NAND elements 4381 and 4387 are connected to the input terminal ○ of the NAND element 4355. Numeral 4379 designates a NAND element for producing an "L" output when it detects that $s_2 < s < s_3$; 4380 a NAND element for producing an "L" output when $s < s_2$; 4381 through 4389 similar NAND elements, 4381 producing an "L" signal when $s > s_7$, 4382 when $s_4 < s < s_7$, 4383 when $s < s_4$, 4384 when $s > s_4$, 4385 when $s_1 < s < s_4$, 4386 when $s < s_1$, 4387 when $s > s_6$, 4388 when $s_2 < s < s_6$, 4389 when $s < s_3$, the numbers ○, ○ and ○ being attached at the output terminals of some of these NAND elements and these NAND elements being connected to the input terminals ○, ○ and ○ of the NAND elements 4357, 4356 and 4355 in FIG. 57 or the input terminals of NAND elements which will be explained hereinafter. Numeral 4390 designates a NAND element which generates the command signal J_{s5} for initiating the setting up of the five-place code in the coder SV shown in FIG. 61; 4391 through 4394 similar NAND elements for generating command signals J_{s4} , J_{s3} , J_{s2} and J_{s1} ; 4395 a NAND element which generates the command signal J_{K21} for initiating the setting up of the constant code in the coder K_I; 4396, 4397 and 4398 NAND elements for generating the command signals J_{K22} , J_{K23} and J_{K24} for setting up the constant codes K_{II} , K_{III} and K_{IV} , respectively.

With the construction described above, if the gear position indicates the first speed gear and the output of the gear position signal generator G₁ is "H," then the discriminators S-S₅ and S-S₂ come into operation according to the discrimination command signals J_{70a} . Now, if the binary coded output signal s of the vehicle speed sensor S is $s > s_5$, then the discriminator S-S₅ produces at its output an "H" signal and the output of the NAND element 4378 changes from "H" to "L," so that this "L" signal is transferred to the input terminal ○ of the NAND element 4356 shown in FIG. 57 to thereby effect the upshift to the second speed gear.

On the other hand, if $s_2 < s < s_5$, the discriminator S-S₅ produces an "H" output and the discriminator S-S₂ produces an "L" output and hence the NAND element 4379 assumes the "L" output state, so that the output of the NAND elements 4390, 4392, 4394 and 4395 change from "L"s to "H"s. As a result, the coders S_V, S_{III}, S_{II}, S_I and K_I invert the binary coded output signal of the vehicle speed sensor S and produce the five-place code $\bar{s}_5$, three-place code $\bar{s}_3$, two-place code $\bar{s}_2$ and single-place code $\bar{s}_1$, respectively, and the coder K_I also produces the constant code K_{21} , whereby the sum of these codes is formed. Then, if $s < s_2$, the discriminator S-S₅ produces an "L" output and the discriminator S-S₂ produces an "L" output and hence only the NAND element 4380 produces an "L" output, so that the NAND element 4357 shown in FIG. 57 produces an

"H" output and the gears are retained in the first speed. With the gears in the second and third speeds, similar discrimination operations are performed. When the gears are in the second speed, two gear shifts, i.e., the downshift and upshift are possible, and therefore all the necessary discrimination operations are performed according to the discrimination command signals J_{70a} and J_{70b} , respectively.

In the foregoing explanation, the determination of the regions on the graph are performed with separately provided discriminators. However, the determination of whether any condition under consideration is located above or below the gearshift lines I, II and III respectively is after all a matter of the discrimination operation on the input codes. Thus, in like manner the discrimination of the input codes can be performed by means of the adder. For example, considering the comparison operation on the values of s_1 and s , this can be determined by first performing the operation $s + \max_1 + \bar{s}_1 + 1$ and then detecting whether there is still an "H" in the most significant position of the code $\max_1$ where there previously was an "H." In this way, the adder can also be employed as a discriminator. This is similarly applicable to those operations relating to the discriminators employed for the determination of other regions.

As will be apparent from the foregoing explanation, each time the operation of addition is performed in the computation of the acceleration increment qA_{cc} , the fuel injection quantity qv according to the intake manifold vacuum, the steady state injection quantity q , the temperature increment mt , the vacuum spark advance θ_v , the rotational spark advance θ_R , the total spark advance θ_T , and the automatic transmission shift instruction; the addition is performed according to the similar addition pattern. A method of computation for performing these additions in a coordinated manner will be explained hereunder.

To begin with, the block diagram of this addition pattern is identical with that shown in FIG. 45 (the fourth embodiment). The circuit for determining the timing and sequence of computations is shown in FIG. 63. In this figure, designated as FF₁, FF₂ and FF₃ are flip-flop circuits which are set by the application of clock pulses P_c; FF₄, FF₅, FF₆ and FF₇ flip-flop circuits connected in series with the flip-flops FF₁, FF₂ and FF₃; 4250, 5251 and 4252 inverters; 4253 through 4260 NAND elements which function successively according to the outputs of the flip-flops FF₁, FF₂ and FF₃; 4261 through 4268 inverters; 4270 through 4273 inverters; 4274 through 4290 NAND elements; 4291 through 4306 inverters; R₁ through R₈ signals which successively assume the "H" output state according to the output codes of the flip-flops FF₁, FF₂ and FF₃ and hence the output of the inverters 4291 through 4309 also assume successively the "H" state, so that signals R_{Acc} , R_{qv} , R_q , R_T , R_Q , $R_{\theta v}$, $R_{\theta R}$, R_{θ} , R_{Ta} , R_{Tb1} , R_{Tb} , R_{Tb1} , ..., R_E successively change to "H." Assuming now that all the flip-flops FF₁ through FF₇ are at "L," then the memories are reset altogether. In this state, since R_{Acc} is in the "H" state, at $R_1 = 1$ the application of the first train of clock pulses initiates the conversion of the output code of the acceleration sensor A_{cc} by way of the circuit shown in FIG. 55 and the succeeding operations are performed in the manner as described with reference to FIG. 48 (the fourth embodiment). Then at $R_E = 1$ and $R_7 = 1$, the process is completed and all the flip-

flops are restored to "L," and as also shown in FIG. 56 all the memories are restored to "L" to get ready for further inputs.

The circuit for determining the sequence of these computational operations as well as the manner of coupling the various gate signals are shown in FIG. 64. In this figure, numerals 4310 through 4321 designate NAND elements for producing the gate signals; 4322 through 4333 inverters; 4334 a NAND element for establishing the engine intake manifold vacuum; 4335 a NAND element for establishing the vehicle speed for automatic transmission; 4336 a NAND element for initiating the addition of the contents of the memories. Now, if it is time for the increased amount of fuel supply for acceleration to be computed, the acceleration increment signal a_{cc} must be introduced into the coder, that is, in FIG. 55 the condition $J_{Acc} = 1$ is necessary. For this reason, it is prearranged so that when both the output signals R_1 and R_{Acc} change to "H" simultaneously, then $J_{Acc} = 1$. Whereupon, all the data relating to the acceleration increment signal a_{cc} are stored in the memories. This is exactly the same with the other inputs. R_2 through R_7 have nothing to do with the respective input signals and only the computational operations are performed at the R_2 through R_7 as shown in FIG. 48 (the fourth embodiment). Since the codes of the vacuum sensor V_a are utilized in the computation of both the fuel injection quantity qv and the engine intake manifold vacuum advance θ_v , the NAND element 4334 is provided to generate the signal J_{va} . On the other hand, the comparison operation for the spark advance θ_i must be performed against entirely different values, and therefore the signals J_{qv} and J_{θ_v} are separately generated. Further, as will be explained later, the same command signal J_M is employed for the addition procedures of the steady state fuel injection quantity q , the total spark advance θ_T required for the engine and the code $(\bar{a}\bar{s} + \bar{b}) + 1$. In this case, the addition is performed on the contents of the memories and not on the contents of the coders. This process is the same as shown in FIG. 56. This figure is referred to, since it relates to the computation of the steady state injection quantity q and the contents of the memories consist of the values of qA_{cc} , qv and qA/F .

Referring now to FIG. 65, there are shown those memories which store the signals qA_{cc} , qv , qA/F , q , θ_v , θ_R , and ϕ before the addition is performed on these signals and the gate inputs to these memories. In FIG. 65, numeral 4400 designates a gate timing NAND element for the memory M_a ; 4401 a NAND element which determines the content of the memory M_a . Since the memory M_5 shown in FIG. 48 (the fourth embodiment) is employed during addition, the content of the memory M_5 is transferred to the memory M_a through the NAND element 4401 when it is opened by the NAND element 4400; 4402 an inverter; 4403 a reset timing NAND element for the memory M_a ; 4404 a similar reset timing NAND element; 4405 an inverter; 4406 and 4407 NAND elements which determine whether the content of the memory M_a must be inverted; 4408 an inverter; 4409 a NAND element which transfers the output of the memory M_a to the adder. Numerals 4410 and 4411 timing NAND elements which determine the content of the memory M_b ; 4412 and 4413 NAND elements which represent the content of the memory M_b ; 4414 a NAND element connected to the memory M_b ; 4416 a NAND element for resetting the memory M_b ;

4417 an inverter; 4420, 4421, 4422 and 4423 input NAND elements for the memory M_c ; 4429 an input NAND element; 4424, 4425, 4426 and 4427 NAND elements for resetting the memory M_c ; 4428 a resetting NAND element.

With the arrangement described above, assume that $R_{Acc} = 1$ and $R_7 = 1$. Then, since at this time the result of the addition, i.e., qA_{cc} is contained in the memory M_5 , $\bar{R}_{Acc} = 0$ and $R_7 = 1$ so that the content of the memory M_5 is transferred to the memory M_a by way of the inverter 4402. This $\bar{R}_{Acc}$ is the inverted signal of R_{Acc} and the output signal of the NAND element 4274 in FIG. 63. Then, at $R_q = 1$, the content of the memory M_a must be added. When $R_q = 1$ and $R_1 = 1$, R_{θ_v} is not in the "H" state, that is, $R_{\theta_v} = 0$ and therefore $\bar{R}_{\theta_v} = 1$. In other words, it is transferred by way of the NAND elements 4406 and 4409 to the NAND element 4240 shown in FIG. 56. Since $J_M = 1$ in FIG. 56, the content of the memory M_a is transferred to the memory M_2 and added therein.

With the addition procedures for the spark advance θ , $R_{\theta} = 1$, $R_1 = 1$ and $J_M = 1$ and thus the content of the memory M_a is inverted and transferred to the memory M_2 . Next, consider the memory M_b whose content consists of the sum of qv and θ_R and the value of ϕ . Since the sum of qv and θ_R is in the memory M_5 as a result of the previous addition, connections are provided by way of the NAND elements 4412 and 4413 to the memory M_b so that the content of the memory M_5 is transferred to the memory M_b and ϕ is also directly introduced into the memory M_b . The content of the memory M_c comprises the steady state fuel injection quantity q , the air-fuel ratio change signal qA/F and the code $\max_1$ and only the value of the steady state fuel injection quantity q is contained in the memory M_5 . Thus, these values are transferred to the memory M_c by separate NAND elements 4420, 4421, 4422 and 4423.

The contents of the memories M_a , M_b and M_c must be reset upon completion of the addition. The required reset signal is supplied to the memory M_a by way of the NAND elements 4403 and 4404 and the inverter 4405, to the memory M_b by way of the NAND elements 4415 and 4416 and the inverter 4417, and to the memory M_c by way of the NAND elements 4424, 4425, 4426, 4427 and 4428. While the foregoing explanation has been made only in respect to the least significant digits, any of the higher order digits can be stored in exactly the same manner.

Based on the foregoing description, the sequence of the operations as a whole are illustrated in FIG. 60. To begin with, the outputs of the flip-flops FF_4 , FF_5 , FF_6 and FF_7 are all at "L" so that when $R_1 = 1$, $J_{Acc} = 1$ thereby initiating the computation of qA_{cc} . The pattern of this computation is the same as shown in FIG. 33 (the fourth embodiment). The output codes of the acceleration sensor which are suitably selected to provide the signal qA_{cc} are added and the result of this addition is stored as qA_{cc} in a memory $M_{qA_{cc}}$, i.e., the memory M_a in FIG. 65. Simultaneously, the air-fuel ratio change signal qA/F is stored in the memory M_c . Then, at $J_{qv} = 1$, the codes for the engine intake manifold vacuum are suitably selected and added so that the result obtained is stored as qv in a memory M_{qv} , i.e., the memory M_b . At the signal J_q , all the signals qA_{cc} , qA/F and qv as stored in the memories in the manner described above are restored according to the pattern of FIG. 56 and are

then added according to the pattern shown in FIG. 48 (the fourth embodiment). The result obtained from this addition is, as the signal q , transferred to a memory M_q , that is, the memory M_c . Thereafter, at $J_i = 1$, a pattern is determined by which the volume of fuel injection is compensated for according to the engine temperature. This scheme is computed to provide a pattern for determining a percentage by which the value of the steady state fuel injection quantity q is to be multiplied. This pattern is then stored in the memory MT in FIG. 39 (the fourth embodiment). Accordingly, at $J_q = 1$, the pattern is coupled to the designated coder, while the previously stored value q is applied according to the pattern in the designated coder to the corresponding coders to produce the relevant codes which are in turn added together to determine the value of the total fuel injection quantity Q . At $R_q = R_i = 1$, this value of the total fuel injection quantity Q is transferred to a memory M_q in FIG. 32 (the fourth embodiment) from which it is supplied to the injection circuit. Then, the output of the vacuum sensor V_a is converted into the codes. The pattern at this time is determined by the signal $J_{\theta v}$ in FIG. 54 and the result of the addition is converted into the inverted code representing the vacuum spark advance. This value is stored as θ_v in a memory $M_{\theta v}$, i.e., the memory M_a and as shown in FIG. 64 it is inverted when delivered to the output circuit. At $R_{\theta R} = 1$, the spark advance according to the engine speed is computed and the result is stored in the memory M_b . Then, at $R_{\theta} = 1$, the sum of the vacuum spark advance $\theta_v = M_a$ and the rotational advance θ_R , i.e., the content of the memory M_b is formed and the sum is stored as the total spark advance θ_T in the memory M_{θ} shown in FIG. 32 (the fourth embodiment). When $R_{\theta} = R_7 = 1$, the output, i.e., the total spark advance θ_T is read out. Thereafter, at $J_{T0} = 1$, the computational operation relating to the automatic transmission is initiated. In the first step of the operation, the value of the binary coded output signal s of the vehicle sensor S is examined to determine whether the gear should be shifted unconditionally or left unchanged, or whether the value lies in a region which necessitates a further computation for its determination. When no further computation is necessary, a command signal is issued to leave the gear unchanged. If any further computation is necessary, the computation $T_0 = (as + b) + 1$ is first performed. Then, at J_{Ta1} and J_{Tb1} , $GS = \max_1 + T_0 + \phi$ is computed. Consequently, the gearshift is directed depending on whether an "H" is retained in the most significant position of the code $\max_1$ where there previously was an "H" and depending also on the gear position at this time. The procedure of this discrimination operation is the same as illustrated in FIG. 57.

In the foregoing discussion, no detailed explanation of the manner of resetting the memories and the addition procedures is given. The cycle of the operations starts at $R_{Acc} = R_1 = 1$ and ends at $R_E = R_8 = 1$, and another cycle is newly initiated upon the application of the next train of clock pulses.

Referring now to FIGS. 66 and 67, there is shown a sequence which generates clock pulses to determine the sequence of operations. In FIG. 66, designated as P_i is an ignition signal; P_d a signal which is delayed a definite time T_d with respect to the ignition signal P_i ; P_c a clock pulse; R_E and R_7 the same signals as designated by the identical letters in FIG. 63; CL a clock pulse generator, 4430 a NAND element whose inputs are the

signals R_E and R_7 , 4431 a signal delay circuit. With the construction as described, the application of the ignition signal P_i causes a monostable multivibrator or the delay circuit shown in FIG. 59 to generate the pulse P_d which lags behind the ignition signal P_i by a definite time. Then, since $R_E = R_7 = 1$, the clock pulse generator CL comes into operation producing the clock pulses P_c at its output. This process is illustrated in FIG. 67. In this figure, designated as T_d is the time delay between the arrival of the ignition pulse P_i and the generation of the pulse P_d . Following the generation of the pulse P_d , the clock pulses P_c are generated which are shown as corresponding to the signals R_{Acc} , R_8 , R_{Acc} , R_1 , ..., R_E , R_6 and R_E , R_7 , respectively. At the signals R_E , R_7 , the clock pulse generator CL stops the generation of its output pulses P_c . The method employed to intermittently generate the clock pulses P_c is illustrated in FIG. 68. In this figure, numeral 4432 designates a reset/set flip-flop (hereinafter referred to as a R-S flip-flop); 4433 a NAND element; osc a clock pulse oscillator. The pulse P_d assumes an "L" level only during a predetermined time. With the construction described above, the truth table of the R-S flip-flop 4432 is shown in Table 2, where P_d is the pulse applied to the input terminal S, $\overline{R_E} \cdot \overline{R_7}$ the output signal of the NAND element which is applied to the input terminal R, and Q is the output signal of the flip-flop 4432.

TABLE 2

P_d (S)	$\overline{R_E} \cdot \overline{R_7}$ (R)	Q
0	1	1
1	1	1
1	0	0
1	1	1
0	1	1

In the first place, when the pulse P_d assumes the "L" level thereby initiating the computation, the flip-flop 4432 produces an "H" output. Eventually, the pulse P_d terminates so that it assumes the "H" state. In this situation, the output signal Q stays unchanged and thus the output signal $Q = 1$. Meantime, the NAND element 4433 inverts the output signal of the oscillator osc and generates the clock pulses P_c . Then, when the negation of the logical product of R_E and R_7 in the NAND element 4430 changes to "L", that is, when $R_E = R_7 = 1$, the output signal Q changes to "L." In this state, the output of the NAND element 4433 remains in the "H" state independent of the output of the oscillator osc. Under these circumstances, even if, owing to a noise of some kind, an output is applied to the input terminal R which would apparently cause the signal $\overline{R_E} \cdot \overline{R_7}$ to change from "H" to "L," the output signal Q remains in the "L" state, and the signal at the output terminal Q changes to "H" only when it is the time that another computation is to be initiated and the pulse P_d assumes the "L" level again, thereby starting the computation. The clock pulses P_c are produced after a delay of the predetermined time t_d with respect to the arrival of the ignition signal P_i and they are terminated on completion of the computation. In other words, the initiation of the computation lags the ignition time by the time t_d and it ends before the next ignition occurs. The applications of the next pulse P_d initiates a further computation.

While in the above description of the present embodiment, the fluid torque converter automatic trans-

mission has been explained as an example of such automobile equipment which is not directly related to the fuel injection system and the ignition system which determine the operating conditions of an engine, it is the same with any other device, such as, a device for controlling the amount of air drawn into the engine, security systems including an anti-skid device and a turns signal which ensure a safe drive, and an air conditioning system and the like which make the driver feel still more comfortable in his compartment.

According to the system of the present embodiment, in addition to the various input codes required for the control of both the fuel injection system and the ignition system, other binary codes are also obtained which correspond to the parameters of such devices as the automatic transmission and anti-skid device which have no direct effects on the operation of the automobile engine, and the latter input codes are operated according to similar methods of computation as used with those of the fuel injection and ignition systems. Thus, with the present system only a single operational circuit is employed, that is, the operational circuit is adapted to perform all the necessary computations to determine the correct amount of fuel injection and the spark advance is also utilized to perform, in addition to those computational operations necessary for operating the engine, such operations as needed for the control of various devices and systems which have no direct relation to the operation of the engine. Consequently, there is no need to incorporate any other operational circuits with the result that not only a reduced cost is ensured, owing to the reduced number of component parts used, but also considerably improved mass productivity and miniaturization of the system can be achieved. This effect should be tremendous in the light of the existing tendency toward an increased number of such devices and systems which have no direct relation to the operation of the engine.

According to the system of the present embodiment, every computation is started by a signal which lags the ignition time of an engine by a predetermined time and it ends before the next ignition time arrives. This eliminates any error in the computations due to the introduction of the ignition noise. This solution is particularly important as a remedial measure against noise that interferes with the operational circuit, and moreover it eliminates any need to incorporate a specially designed noise suppressor and remedial arrangements in the design of the circuit, thereby ensuring accurate computations.

Furthermore, since the characteristics are corrected at every ignition cycle of the engine, the characteristics which are both essential and sufficient can be obtained at all times, and this is particularly true with the spark advance and fuel injection quantity requirements of the engine.

Embodiment 6:

The system according to a sixth embodiment of the present invention relates only on the fuel injection control and not on the control of the ignition timing of an engine.

Referring now to FIG. 69, there is illustrated a block diagram showing the general construction of the present system. In this figure, designated as S_i' is a start signal for indicating the start of an engine; V_a' an input signal (hereinafter referred as a manifold vacuum signal) corresponding to the value of the engine intake

manifold vacuum; T' an input signal corresponding to the engine temperature showing its degree of heat; A_c' an input signal (hereinafter referred to as an acceleration signal) corresponding to the opening velocity of the engine throttle valve; A/F an input signal (hereinafter referred to as an air-fuel ratio change signal) corresponding to the electrically detected value of the engine throttle opening exceeding a predetermined value. Numeral **5001** designates a coder for establishing the volume of fuel injection according to the engine intake manifold vacuum; **5002** a coder for increasing the volume of fuel injection at the start of the engine; **5003** a coder for increasing the volume of fuel injection when the engine is not warmed up; **5004** a coder for increasing the supply of fuel for acceleration, that is, for increasing the amount of fuel injection when the engine throttle valve is quickly opened; **5005** a coder for establishing the additional amount of fuel to change the air-fuel ratio from the economy air-fuel ratio to the maximum power air-fuel ratio as the full throttle operation of the engine is approached; **5006** an adder which forms the sum of the output signals of the coders **5001**, **5002**, **5003**, **5004** and **5005**; **S** the output signal of the adder **5006**, the actual injection of fuel being effected according to the value of the output signal **S**.

With the construction described above, all the input signals S_i' , V_a' , T' , A_c' and A/F are derived in the form of binary coded digital signals. In other words, although not shown in this figure, there are provided the corresponding sensors mounted on the engine to produce these signals and there are also provided the corresponding converters which convert the outputs of these sensors into the binary codes which are in turn supplied to the coders as their input signals. To start with, when the coder **5001** receives its input, i.e., the manifold vacuum signal V_a' , the coder **5001** establishes the volume of fuel injection which corresponds to the input signal V_a' . As will be explained in detail at a later time, the function of the coder **5001** is to select a suitable function according to the value of the manifold vacuum signal V_a' . The other coders operate in exactly the same manner.

Then, when the engine is starting, the start signal S_i' is supplied to the coder **5002** so that the coder **5002** establishes the amount of fuel to be increased in proportion to the start signal S_i' . In this case, the output signal of the adder **5006** represents the condition which corresponds $S_i' = 1$, and the rate of increase in the fuel quantity delivered is computed on the basis of this output signal according to the degree of warmth of the engine. Then, the signal T' representing the degree of heat of the engine is supplied to the coder **5003** as its input so that the rate of increase in the fuel quantity is also established. In this case, the rate of increase is determined irrespective of whether the start signal $S_i' = 1$ or $S_i' = 0$. Net, the fuel quantity is increased for acceleration of the engine. In other words, when the output power of the engine must be increased rapidly, the acceleration signal A_c' is supplied to the coder **5004** so that the coder **5004** functions to increase the amount of fuel in proportion to the amount of air drawn into the engine. More particularly, the coder **5004** functions such that when the throttle valve is quickly opened, the fuel quantity is increased in several steps according to the position of the throttle valve. As the throttle opening approaches its full throttle position, the coder **5005** comes into operation to determine a definite amount of

the additional fuel supply according to the air-fuel ratio change signal A/F' which is generated upon detection of the relative pressure to the atmospheric pressure or the throttle opening. In other words, with the throttle valve approaching its full throttle operation, the air-fuel ratio change signal $A/F' = 1$. Consequently, the coder 5005 establishes the additional amount of fuel supply, so that the fuel quantity thus established moves from the locus indicating the minimum rate of fuel consumption of the engine for its output power to a locus indicating the maximum power.

The output signals of the coders 5001, 5002, 5003, 5004 and 5005 are added altogether in the adder 5006, and the output signal S which is the sum of the addition now represents the total amount of fuel injection. The output signal S is applied to the fuel injection system as its input. This situation is shown in FIG. 70.

In FIG. 70, the abscissa represents the engine intake manifold vacuum V_a and the ordinate represents the fuel injection quantity q . In the figure, the curve V_a represents the required basic fuel quantity characteristic; T the characteristic corresponding to the curve V_a plus the fuel quantity increment according to the engine temperature; S_t the characteristic corresponding to the curve T plus the required increment for starting the engine; A/F the characteristic which shows that the required basic fuel quantity characteristic represented by the curve V_a is increased by a definite amount; A_c the characteristic which similarly shows that the required basic fuel quantity characteristic V_a is increased by a definite amount. The additional amount of fuel for a cold engine and the additional fuel for starting up the engine must be calculated in terms of percentages to the basic fuel injection characteristic according to the engine intake manifold vacuum V_a . Moreover, the additional fuel for starting must be calculated in terms of percentages to the basic fuel injection quantity according to the degree of the engine temperature. The procedures for calculating such additional fuel will be explained in detail hereunder.

FIG. 71 illustrates a block diagram of an arrangement for calculating the basic fuel injection characteristic V_a . The method of calculating the volume of fuel injection according to the engine intake manifold vacuum alone will be first explained. In FIG. 70, designated as V_a' is a binary coded digital input representing the engine intake manifold vacuum converted into an electrical signal; $F(V_{a\alpha})$ a first discriminator for determining whether the input V_a' is greater or smaller than the value at the point designated as $V_{a\alpha}$ in FIG. 70; $F(V_{a\beta})$ a second discriminator for determining whether the input V_a' is greater or smaller than the value at the point designated as $V_{a\beta}$ in FIG. 70; 5101 a logical element for producing an "L" output when the input V_a' is greater than the values at the points $V_{a\alpha}$ and $V_{a\beta}$; 5102 an inverter; 5103 a logical element for producing an "H" output when the comparison $V_{a\beta} < V_a' < V_{a\alpha}$ is found; 5104 and 5105 inverters; 5106 a logical element for producing an "L" output when the comparison $V_a' < V_{a\beta}$ is found. Designated as V_{a5} is a coder into which the value of the binary coded five-place input V_a' is transferred in its original form; V_{a4} , V_{a3} , V_{a2} and V_{a1} coders for shifting the five-place input V_a' to the right by the corresponding places to produce the four-place, third-place, two-place and single-place codes, respectively; V_{a0} a coder for setting up a constant code; J_{i5} a connecting circuit for coupling the

coder V_{a5} to an adder; J_{i4} , J_{i3} , J_{i2} , J_{i1} and J_{i0} circuits for coupling the coders V_{a4} , V_{a3} , V_{a2} , V_{a1} and V_{a0} to the adder 5113. Numeral 5107 designates a logical element for controlling the connecting circuit J_{i5} to connect it to the adder 5113; 5108, 5109, 5110, 5111, 5112 logical elements for controlling the connecting circuits J_{i4} , J_{i3} , J_{i2} , J_{i1} and J_{i0} to connect them to the adder 5113.

In operation, when the binary coded digital input V_a' is applied, the coders, V_{a5} , V_{a4} , V_{a3} , V_{a2} , V_{a1} and V_{a0} produce their respective codes. At the same time, the value of the input V_a' is compared with the value at the point $V_{a\alpha}$ in the discriminator $F(V_{a\alpha})$. Now, if the value of V_a' is smaller than that of $V_{a\alpha}$, it is further compared with $V_{a\beta}$ in the second discriminator $F(V_{a\beta})$ to examine whether V_a' is greater or smaller than $V_{a\beta}$. If the result of the comparison indicates that $V_a' > V_{a\beta}$, then the conditions $V_a' > V_{a\alpha}$ and $V_a' > V_{a\beta}$ exist and hence $F(V_{a\alpha}) = F(V_{a\beta}) = 1$, so that the logical element 5101 produces an "L" signal. When this happens, each of the logical elements 5107, 5109, 5110, 5111 and 5112 connected to the output of the logical element 5101 produces an "H" signal, so that the coders V_{a5} , V_{a4} , V_{a3} , V_{a2} , V_{a1} and V_{a0} are now ready to be connected to the adder 5113. In other words, the connecting circuits J_{i5} , J_{i4} , J_{i3} , J_{i2} , J_{i1} and J_{i0} are now placed in a condition for connection with the adder 5113. The commands for coupling the J_{i5} , J_{i4} , J_{i3} , J_{i2} , J_{i1} and J_{i0} are issued by way of a separate circuit. Consequently, when $V_a' > V_{a\alpha}$, the fuel injection quantity q is given as $q = V_{a5} + V_{a4} + V_{a3} + V_{a2} + V_{a1} + V_{a0}$ and this value is supplied to the injection circuit. Similarly, when $V_{a\beta} < V_a' < V_{a\alpha}$ and fuel injection quantity q is given as $q = V_{a4} + V_{a3}$, and when $V_a' < V_{a\beta}$, $q = V_{a0}$. Now, since the input V_a' is the five-place binary number there exists the relation $V_{a5} \approx 2V_{a4} \approx 4V_{a3}$. Thus, the value of q may be determined on the basis of V_{a5} as follows:

$q = 1.0 V_{a5}, 1.25 V_{a5}, 1.5 V_{a5}, 1.75 V_{a5}, 0.75 V_{a5}, 0.5 V_{a5}$ and $0.25 V_{a5}$. The value of V_{a0} may also be added to these values to obtain the value of q .

The operation described above will not be explained in detail with reference to an actual circuit. The circuit construction of the first and second discriminators $F(V_{a\alpha})$ and $F(V_{a\beta})$ will be as shown in FIG. 72. In this figure, numerals 5120, 5122, 5124 and 5126 designate NAND elements which decide whether the signal in each of the positions 2^0 through 2^4 is "H" or "L"; 5121, 5123 and 5125 inverters for inverting the signal from "L" to "H" and vice versa; 5128, 5130, 5131 and 5132 NAND elements which perform the comparison operation on the respective digits to give an indication of agreement or disagreement; 5129 an inverter; 5133 and 5134 NAND elements.

With the construction described above, the operation of the first discriminator $F(V_{a\alpha})$ will be explained by way of example. With the present value of $V_{a\alpha}$ which is represented in the binary code as 10110 in the first discriminator $F(V_{a\alpha})$, the comparison operation is performed in the following manner to see whether the value of V_a' is greater than this preset value. To start with, an "H" signal is applied to one of the input terminals of the NAND elements 5120, 5122, 5124 and 5126, respectively, and the five-place signal V_{a5} at the top is applied to the other terminal of the NAND element 5120. Then, if V_{a5} is "H," the NAND element 5120 produces an "L" output and this is received by the NAND element 5128 which in turn produces an

"H" output. On the other hand, the output of the NAND element 5120 is inverted by way of the inverter 5121, so that if V_{a5} is "H", the output of the inverter 5121 is "H". Next, if V_{a4} is "H", the output of the inverter 5129 is "L" and hence the NAND element 5122 produces an "H" output. In this case, the output of the NAND element 5130 is "L" and hence the output of the NAND element 5134 is "H," so that when an "H" output appears at the output terminal L_a of the NAND element 5134, it is, then established that the value of $V_{a'}$ is greater than V_{aa} , that is, $V_{a'} > 10110$ ($V_{a'} > V_{aa}$). Similarly, the comparison operation is performed on the three-place and two-place numbers, respectively, so that if $V_{a'} > V_{aa}$, an "L" signal appears at either one of the input terminals of the NAND element 5134 producing an "H" signal at the output terminal L_a . On the other hand, if $V_{a'} < V_{aa}$, an "L" signal is introduced at either one of the input terminals of the NAND element 5133 and hence an "H" signal is produced at the output terminal SM. Next, regarding the singleplace code, if $V_{a1} = 1$, then $V_{a'} > V_{aa}$ and if $V_{a1} = 0$, then $V_{a'} = V_{aa}$. Thus, if the break points of the characteristic curves V_a , T and S_t in FIG. 70 are chosen so that $V_a \geq V_{aa}$, the discriminators for V_{a1} may be dispensed with. Accordingly, the circuit is prearranged so that if the value of $V_{a'}$ agrees with respect to the four most significant digits 1011 of the preset binary number 10110 in the first discriminator $F(V_{aa})$, then the condition $V_{a'} \geq V_{aa}$ is present. It is also prearranged so that the comparison on the most significant bit is performed by comparing the output of the NAND element 5120 with "H" to make a discrimination between "H" and "L," while the comparison operation on the lower bits is performed only when there is found no agreement thereabout since the existence of agreement on any higher order bit is indicated by the "H" output of the corresponding inverter.

The second discriminator $F(V_{a\beta})$ may be constructed in exactly an identical manner. In other words, what is needed is simply to construct an identical circuit excepting that it employs a different binary number in place of the preset binary number 10110 in the first discriminator. It is also possible to dispense with the comparison operation on the least significant bit, if it is prearranged in the same manner as described above that the condition $V_{a'} \geq V_{a\alpha} ; \beta$ is met when the comparison of the least significant bit produces an "H."

While there has been explained the method of determining the volume of fuel injection according to the engine intake manifold vacuum, as already mentioned, in practice the volume of fuel injection must be increased according to the operating conditions of the engine such as the engine temperature and the start up of the engine so as to obtain a highly efficient operation of the engine. In other words, when the weather is cold so that the engine gets cold, the engine torque is considerably reduced. In this case, there is the danger that the engine tends to stall if the amount of fuel that is determined according to the engine intake manifold vacuum is simply injected. The result of the experiments has shown that this deficiency of a cold engine can be considerably remedied by increasing the volume of fuel injection before and after starting the engine. The method of computing the additional fuel supply for starting and the warming up operation of the engine ac-

cording to the engine intake manifold vacuum will be explained hereunder.

The method of computation which will be explained hereinafter employs as a basis the amount of fuel injection (with no increase for the warming up operation) determined according to the engine intake manifold vacuum under normal operating conditions of the engine, and any increase in the fuel quantity is determined proportionally, that is, in terms of percentages to the basic fuel injection quantity. Moreover, such percentages may be varied as desired according to the temperature of the engine as well as other engine operating conditions, and at the same these computational operations may be performed on the binary coded digital inputs in a rational manner.

Referring now to FIG. 73, there is illustrated a block diagram of an arrangement for computing, in terms of the binary codes, the basic fuel injection quantity according to the engine intake manifold vacuum and the additional fuel supply for the starting and warming up operation of the engine. In FIG. 73, designated as T' a binary coded digital input corresponding to the engine temperature which is derived by detecting the temperature of the cooling water for the engine, the engine oil temperature, etc.; $I(\alpha)$, $T(\beta)$, $T(\gamma)$ and $T(\delta)$ temperature discriminators for discriminating one of the five engine temperature ranges in which the input engine temperature falls. As for the detailed construction of the temperature discriminators, they may be similarly constructed with the circuit shown in FIG. 72. Designated as $V_{a'}$ is a binary coded digital signal corresponding to the engine intake manifold vacuum; $F(V_{aa})$ and $F(V_{a\beta})$ discriminators which are the same as shown in FIG. 71; 5201, 5202, 5203 and 5204 inverters; 5205 through 5209 and NAND elements which perform their function under the control of the discriminators $T(\alpha)$, $T(\beta)$, $T(\gamma)$ and $T(\delta)$; 5215 an inverter which detects that the engine is not starting; S_t' the start signal which indicates that the engine is starting; 5216 through 5220 logical elements which function upon detection of the start signal and the engine temperature range signal; K_1 , K_2 , ..., K_{10} coders for determining the fuel injection quantity calculating schemes (hereinafter referred to as a pattern) according to the requirements of the engine, on which a detailed explanation will be made later; K_{11} , K_{12} and K_{13} similar coders for determining the fuel injection quantity calculating patterns under normal operating conditions of the engine; C_1 , C_2 , ..., C_{12} the output constant codes of the coders K_1 , K_2 , ..., K_{13} which are the inputs to overall constant coders S_3 and S_4 ; S_1 and S_2 coders which receive the patterns from the selected ones of the coders K_1 through K_{10} and K_{11} through K_{13} respectively, to produce the corresponding codes; A_1 an adder which performs the operation of addition on the established patterns; A_2 an adder which performs the final addition to determine the volume of fuel injection; F_u an injection circuit which injects the fuel according to the output of the adder A_2 ; A_c a coder for establishing the additional amount of fuel for acceleration; AF a coder for establishing the additional amount of fuel for near-full throttle operation.

Referring now to FIG. 74, there are illustrated by way of example detailed circuit diagrams of the coders K_1 , K_2 and K_{11} of the coders K_1 through K_{12} for establishing the patterns, and the circuit diagram of the overall coders S_1 and S_2 .

FIG. 75 illustrates a coder in which the input code corresponding to the engine intake manifold vacuum is shifted to the left or right to produce binary codes having varying number of digits.

Referring to FIG. 75, designated as V_1 is the first-place digit, i.e., the least significant digit of the six-place digital input corresponding to the engine intake manifold vacuum; $V_2, V_3, \dots, V_6$ higher order digits of the same six-place input, respectively; 5301 through 5306 input inverters; V_{a7} a coder for producing a seven-place code; $V_{a6}, \dots, V_{a1}$ coders for producing the six-place through single-place codes having as many digits as indicated by their respective suffixes; 5307 a NAND element for setting up the seventh-place digit or the most significant digit of the seven-place code to be produced by the coder V_{a7} ; 5308, 5309, ..., 5313 NAND elements for setting up the corresponding digits of the seven-place code in the coder V_{a7} ; 5314, 5315, ..., 5319 similar NAND elements for the six-place number coder; 5320 through 5324 similar NAND elements for the five-place number coder V_{a5} ; 5325 through 5328 similar NAND elements for the four-place number coder V_{a4} ; 5329 through 5331 similar NAND elements for the three-place number coder V_{a3} ; 5332 and 5333 similar NAND elements for the two-place number coder V_{a2} ; 5334 a similar NAND element for the single-place number coder V_{a1} . In operation, the input codes V_5 through V_1 are supplied to the seven-place number coder V_{a7} such that the largest input code V_{a6} is set up in the highest order NAND element 5307. In like manner, the input code V_5 is set up in the NAND element 5308, V_4 in the NAND element 5309, V_3 in the NAND element 5310, V_2 in the NAND element 5311 and V_1 in the NAND element 5312. The NAND element 5313 has no corresponding input and therefore it is preset to always produce an "L" output. Similarly, the input codes are supplied to the six-place number coder V_{a6} such that the input codes are set up in the like significance NAND elements as indicated by the suffix of the input codes, while the input codes supplied to the five-place number coder V_{a5} are shifted one place to the right and then set up, thus shifting out the least significant digits. In like manner, the input codes are set up in the four-place number coder V_{a4} through the single-place number coder V_{a1} each thereof shifting out the corresponding number of least significant digits of the input codes. Accordingly, there is the relation $V_{a7} \approx 2 V_{a6} \approx 4 V_{a5} \approx 8 V_{a4} \approx 16 V_{a3} \approx 36 V_{a2} \approx 64 V_{a1}$.

Next, the coders for establishing the computational patterns and the circuit for forming the sum of these patterns will now be explained with reference to FIG. 74. In this figure, numerals 5205, 5216 and 5223 designate the same NAND elements as designated by the identical reference numerals in FIG. 73, which perform their respective function upon receipt of the output from the corresponding discriminators; 5295, 5296 and 5297 inverters; 5250, 5251, 5252, 5253 and 5254 NAND elements for establishing the addition pattern when the output of NAND element 5205 is "H"; 5260 through 5264 NAND elements which perform their function upon receipt of the output of the NAND element 5216; 5280 through 5284 NAND elements which perform their function upon receipt of the output of the NAND element 5223; 5270 a NAND element which performs its function upon receipt of the output of the NAND elements 5250, 5260 and other similar NAND

elements of the pattern coders; 5271 through 5274 NAND elements which perform their function upon receipt of the output from the NAND elements of the corresponding digit positions, the NAND elements 5270 through 5274 performing their function according to different conditions; 5290 through 5294 NAND elements which perform their function upon receipt of the output of the NAND elements 5280 through 5284 and other corresponding NAND elements. The adder A_1 comes into operation when it receives the outputs of the above-mentioned two sets of the NAND elements and the ultimate pattern of addition is formed in this adder.

The operation of the circuit, shown in FIG. 74, will now be explained. Assume that the NAND elements 5205 and 5223 are now in the established states and hence the outputs of the inverters 5295 and 5297 are all at "H." Then, the coder K_1 generates its pattern 10101 by means of the NAND elements 5250 through 5254. In this situation, the other pattern coders $K_2, \dots, K_{12}$ are all in the "L" state. Consequently, the output of the overall coder S_1 is set up as 10101. On the other hand, since the NAND element 5223 is in the established state, the overall coder S_2 generates its code 01101 in the similar manner as S_1 . Consequently, the adder A_1 produces its output 100010 which is the sum of the two input codes 10101 and 01101. Thus, the addition pattern is determined as 100010 and this is compared with the previously established codes to determine the final pattern. In this case, the "H" in the most significant position of the aforesaid sum represents the code V_{a7} and the "H" in the next least significant position represents the code V_{a3} , and therefore the final pattern is given as $V_{a7} + V_{a3}$. This process will be explained hereunder with reference to FIG. 73.

To begin with, when the binary coded digital input T' corresponding to the engine temperature is applied from the converter, the comparison operation is performed on the input T' in the temperature discriminators $T(\alpha), T(\beta), T(\gamma)$ and $T(\delta)$ to determine the temperature range in which the value of the input T' falls. Depending on the result of this discrimination operation, if the engine has not started a selected one of the NAND elements is placed in its established state, so that a selected one of the pattern coders K_1, K_3, K_5, K_7 and K_9 generates its output code. In this case, if the NAND element 5205 is in its established state, it follows as shown in FIG. 74. On the other hand, if the engine is starting, then the start signal $S_1' = 1$ and therefore one of the coders K_2, K_4, K_6, K_8 and K_{10} generates its output code. Thus, only one of the coders K_1 through K_{10} generates its output to provide a sole input to the overall coder S_1 . Similarly, the arrival of the binary coded digital input V_a' corresponding to the engine intake manifold vacuum places one of the NAND elements 5223, 5224 and 5225 in an established state, so that one of the coders K_{11}, K_{12} and K_{13} which corresponds to that particular one of the NAND elements produces its output and this is supplied to the overall coder S_2 , whereupon the adder A_1 performs the addition as described with reference to FIG. 74. On the other hand, the constant codes C_1 through C_{10} which have nothing to do with the engine intake manifold vacuum as with the constant codes C_{11} through C_{13} , are also introduced into the overall constant coders S_3 and S_4 in the same manner as the overall coder S_1 . In this case, since these constants have no relation with the in-

take manifold vacuum, only those values are applied to the coders S_3 and S_4 which are added in the final addition and reflected as such in the finally calculated fuel injection quantity. Consequently, the result of the addition performed according to the addition pattern obtained in the adder A_1 and the inputs from the overall coders S_3 and S_4 are added in the adder A_2 to establish the ultimate volume of fuel injection, so that the output of the adder A_2 is supplied to the injection circuit which in turn injects the fuel according to the output of the adder A_2 . Although not shown in FIG. 73, depending on the operating conditions of the engine, as shown in FIG. 69, the additional fuel for acceleration according to the acceleration signal A_c' as well as the additional fuel for effecting the change from the economy air-fuel ratio to the maximum power air-fuel ratio can be accomplished by means of the air-fuel ratio change signal A/F' .

As described above, according to the fuel injection control system of the present embodiment, at least information relating to the temperature of the engine, the starting and the engine intake manifold vacuum are converted into binary coded digital signals so that the necessary computational operations are performed on these digital signals to control the injection of fuel. Embodiment 7:

A seventh embodiment of the present invention relates to another form of the fuel injection control system which does not involve the control of the ignition timing of an engine.

Referring now to FIG. 76, there is illustrated a block diagram of the system of the present embodiment. In this figure, numeral 6100 designates a sensor circuit; 6100 a vacuum sensor for producing a DC output voltage corresponding to the amount of the vacuum developed in the intake manifold of an engine; 6130 a temperature sensor for detecting the temperature of the engine to produce a DC output voltage corresponding to the detected engine temperature; 6140 a timing sensor for producing a pulse signal voltage corresponding to the rotation of the shaft correlated to the rotating shaft of the engine; 6200 an A - D converter circuit for converting the DC output voltages of the vacuum sensor 6110 and the temperature sensor 6130 into the corresponding binary coded digital signals; 6210 an A - D converter for converting the DC output voltage of the vacuum sensor 6110 into the binary digital signal; 6230 an A - D converter for converting the DC output voltage of the temperature sensor 6130 into the binary digital signal; 6300 a function generator comprising a function generator 6310 adapted to convert the output binary digital signal of the A - D converter 6210 into another binary digital signal to suit the fuel requirement of the engine, and a function generator 6330 for converting the binary coded output signal of the A - D converter 6230 into another binary coded signal to increase or decrease the volume of fuel injection by a proper amount according to variations of the engine temperature; 6500 an operational circuit which performs an addition or subtraction on the binary coded output signals of the function generators 6310 and 6330 to obtain a binary coded injection signal corresponding to the duration of fuel injection from the binary coded output signal of the converter 6210 for the vacuum sensor 6110 and the binary coded output signal of the converter 6230 for the temperature sensor 6130; 6700 a memory circuit (hereinafter simply re-

ferred to as a memory) for storing the binary coded output signal of the operational circuit 6500 corresponding to the duration of the fuel injection based on the volume of fuel injection calculated in the operational circuit 6500; 6800 a distributor circuit adapted to be actuated with the output signals of the timing sensor 6140 to distribute to the engine cylinders the content, i.e., the digital signal stored in the memory 6700; 6820 a counter circuit (hereinafter simply referred to as a counter) adapted to come into operation upon receipt of the output signal of the distributor 6800 to count the duration of the fuel injection so that it stops the counting operation when its count attains the content of the memory 6700 and simultaneously erases the content of the memory 6700; 6840 a clock pulse generator which generates pulse signals having a predetermined frequency upon actuation of the counter 6820 so that the counter 6820 counts the number of the pulse signals to indicate the duration of the fuel injection; 6920 a solenoid valve mounted in the engine intake manifold to start the injection of fuel with the output signal of the counter 6820, that is, when the counter 6820 starts counting and stop the injection of fuel when the counter 6820 completes and stops its counting operation.

With the construction described above, the operation of the fuel control system of the present embodiment will be explained. The operational circuit 6500 performs an operation on the binary coded output signal of the vacuum sensor 6110 which is converted by the function generator 6310 and the binary coded output signal of the temperature sensor 6130 which is converted by the function generator 6330, and the binary coded signal derived from this operation, i.e., the binary coded signal corresponding to the duration of the fuel injection is stored in the memory 6700. Whereupon, the distributor 6800 comes into operation upon receipt of the output signals of the timing sensor 6140 and the counter 6820 starts to count the clock pulse signals from the clock pulse generator. Concurrently, the solenoid valve 6920 is energized so that the solenoid valve 6920 starts to inject fuel into a cylinder. Thereafter, when the binary coded signal counted by the counter 6820 attains the value of the digital signal stored in the memory 6700, the counter 6820 stops the operation and simultaneously it erases the content of the memory 6700 and de-energizes the solenoid valve 6920 to stop the injection of the fuel.

The same operational process is repeated each time the timing sensor 6140 produces its output signal pulse and the solenoid valve 6920 injects the amount of the fuel corresponding to the output signals of the vacuum sensor 6110 and the temperature sensor 6130.

Next, the construction of the fuel injection distribution circuit incorporated in the fuel control system described above will be explained with reference to FIG. 77. In this figure, numeral 6500 designates the operational circuit, 6700 the memory; 6830 a comparator circuit; 6830A₁ and 6830A₂ comparators adapted to de-energize solenoid valves 6920A₁ and 6920A₂, respectively, and erase the content of the memory 6700 when the duration of the fuel injection is found to be equal to the content of the memory 6700; 6820 the counter for counting the duration of the fuel injection comprising counters 6820A₁ and 6820A₂; 6810 the distributor circuit for distributing the clock pulses to the counters 6820A₁ and 6820A₂, respectively, upon re-

ceipt of the output signals of the timing sensor 6140; 6840 the clock pulse generator; 6140 the timing sensor.

The construction and operation of the fuel injection distribution circuit illustrated in the above block diagram will be explained in more detail with reference to FIG. 78. In this figure, numeral 6500 designates the operational circuit; 6501 through 6508 output terminals for the binary coded output signal of the operational circuit 6500; 6700 the memory; 6711 through 6718 flip-flops which are set upon receipt of the corresponding output binary code produced at the output terminals 6501 through 6508 of the operational circuit 6500; 6830A₁ the comparator comprising constituent elements 6831A through 6838A each thereof producing a low level (L) signal voltage at its output terminal Z when its signal inputs at its two input terminals X and Y are simultaneously at a high level (H) or a low level (L) and generating a low level (L) signal at the output terminal B by way of a NAND element 6839A when the signal voltages at all the output terminals Z of the elements 6831A through 6839A are at the H level; 6820A₁ the counter for counting the clock pulses applied at the input terminal C; 6821 through 6828 flip-flops constituting the counter 6820A₁; D an inverter which inverts the output signal of the comparator 6830A₁ so that the content of the memory 6700 and the count of the counter 6820A₁ are erased when the signal level at the output terminal of the comparator 6830A₁ is at L.

The constituent elements of the comparator 6830A₁ are identical to those which are described with reference to FIG. 17 in connection with the explanation of the second embodiment. The NAND element 6839A is also identical with the one explained in the description of the second embodiment.

The operation of the fuel injection distribution circuit shown in FIGS. 76 through 78 will now be explained. To begin with, the binary coded signal produced at the output terminals 6501 through 6508 of the operational circuit 6500 are stored in the flip-flops 6711 through 6718 constituting the memory 6700. Then, as the clock pulses are applied from the clock pulse generator 6840 to the input terminal C of the counter 6820A₁, the flip-flops 6821 through 6828 are successively set to count the input clock pulses in binary form. Thereafter, when the binary coded signal at the respective single output terminals Y of the flip-flops constituting the counter 6820A₁ differ entirely from the binary coded signal appearing at the respective single output terminals X of the flip-flops 6711 through 6718 constituting the memory 6700, the output terminal B of the comparator 6830A₁ assumes the L level, whereby with the signal of the H level as inverted by the inverter D, the flip-flops 6821 through 6828 of the counter 6820A₁ and the flip-flops 6711 through 6718 of the memory 6700 are reset and cleared to erase their contents, and simultaneously the distributor 6810 stops its operation upon receipt of the output pulse signal from the output terminal B and the application of the clock pulses to the input terminal C also ceases.

While the counter 6820 A₁ for one of the engine cylinders has been explained by way of example, the operation of the counter 6820 A₂ for other cylinder and that of the similar counters provided for the remaining cylinders are the same as that of the operation of the counter 6820 A₁. In other words, the time that each of

these counters comes into operation is determined by the distributor 6810, and when a comparator provided for each counter finds that the count of the counter is equal to the content of the corresponding memory, the counter stops the operation.

The construction and operation of the distributor 6810 are the same as explained with reference to FIGS. 20 and 21 in connection with the description of the second embodiment.

In the foregoing explanation of the operation, the contents of the memories are erased at times T₁, T₂, ..., ..., at which the fuel injection stops and thereafter their contents remain at zero. However, since the corresponding counters are already set to count the clock pulses at times t₁, t₂, ..., t₆ and therefore the contents of the memories are not equal to those of the corresponding counters. Thus, it is apparent that even if the contents of the memories are cleared while the counters are in operation, this erasing of the memory contents will never cause the counters to stop their operation thereby stopping the injection of the fuel.

Embodiment 8:

A eighth embodiment of the present invention relates to a fuel control system in which only the ignition timing (the amount of spark advance) of an internal combustion engine is controlled.

Referring now to FIG. 79 illustrating a block diagram of the general construction of the present system, numeral 7110 designates a vacuum sensor to produce a DC output voltage corresponding to the amount of the vacuum in the intake manifold of an internal combustion engine which is not shown; 7120 an engine speed sensor to produce a DC output voltage corresponding to the number of revolutions of the engine shaft; 7140 a timing sensor mounted on the rotating shaft correlated to the engine shaft to produce pulse signal voltages (hereinafter referred to as timing signals) according to the speed of the engine; 7150 an angular sensor mounted on the rotating shaft correlated to the engine shaft to produce 180 pulse signals (hereinafter referred to as angular signals) for every rotation of the rotating shaft, that is, one angular signal for every two rotational degrees; 7210 an A - D converter for converting the DC output voltage of the vacuum sensor 7110 into a binary coded digital signal; 7220 an A - D converter for converting the DC output voltage of the engine speed sensor 7120 into a binary coded digital signal; 7310 a function generator for the vacuum sensor 7110 which converts the binary coded output signal of the A - D converter 7210 into another binary coded digital signal suited to the ignition timing, i.e., the vacuum spark advance characteristic required for the engine; 7320 a function generator for the engine speed sensor which converts the binary coded output signal of the A - D converter 7220 into another binary coded signal to suit the ignition timing characteristic, i.e., the rotational spark advance characteristic required for the engine; 7400 an operational circuit which operates on the binary coded output signal of the function generator 7310 for the vacuum sensor 7110 and the binary coded output signal of the function generator 7320 for the engine speed sensor 7120 so as to produce another binary coded signal corresponding to the required ignition timing, i.e., the spark advance characteristic; 7500 a memory circuit (hereinafter referred to as a memory) which stores the binary coded output signal of the operational circuit 7400 corresponding to the required igni-

tion timing of the engine; 7600 a distributor for distributing the digital signal stored in the memory 7500 to the spark plugs of the engine cylinders according to the output signals of the timing sensor 7140; 7700 a counter circuit (hereinafter referred to as a counter) which counts the angular signals from the angular sensor 7150 so that it stops the counting operation and erases the content of the memory 7500 when the count is found to be equal to the content of the memory 7500; 7800 an ignition system which is designed so that when the counter 7800 starts to count and then completes and stops the operation, by way of the distributor rotor (not shown) adapted to rotate in correlated relation to the engine shaft, a spark signal is supplied to the spark plug mounted on the engine cylinder to produce an ignition spark.

With the construction described above, the operation of the system of the present embodiment will be explained. When the counter 7700 completes and stops its counting operation, the ignition system comes into operation to cause the spark plug mounted at the engine cylinder to produce an ignition spark as previously mentioned. On the other hand, the binary coded output signal of the function generator 7310 and the binary coded output signal of the function generator 7320 are applied to the operational circuit 7400 so that the operational circuit 7400 produces a binary coded digital signal corresponding to the required spark advance characteristic of the engine and this digital signal is then stored in the memory 7500. Then, the counter 7700 restarts its operation and counts the angular signals from the angular sensor 7150. Thereafter, when the content of the memory 7500 and the value of the binary coded signal representing the count of the counter 7700 are found to be equal to each other, a current is supplied to the ignition system so that an electrical spark is produced by the spark plug and simultaneously the content of the memory 7500 is erased. This process is repeated every time the timing sensor 7140 generates its timing signal and the ignition system 7800 produces an ignition spark according to the spark timing corresponding to the binary coded output signals of the vacuum sensor 7110 and the engine speed sensor 7120.

Next, the construction of the principal part of the present system as well as its operation will be explained. Referring to FIGS. 80 and 81, like reference numerals used in FIG. 79 designate like component parts; 7400 the operational circuit; 7401 through 7406 the output terminals of the operational circuit 7400; 7500 the memory comprising flip-flops 7501 through 7506 which store the digital signal produced at the output terminals 7401 through 7406 of the operational circuit 7400; 7600 the distributor designed so that when the output signal of the timing sensor 7140 is applied at one of its input terminals, it comes into operation to supply to the counter 7700 the angular signals applied to one of the other input terminals from the angular sensor 7150, and then it stops the operation to interrupt the supply of the angular signals to the counter 7700 upon receipt of the output signal of a comparator 7900 which will be explained later; 7611 a set/reset flip-flop (hereinafter simply referred to as a S.R.F.F.); 7612 and 7613 inverters which invert the signal level at the output terminal with respect to the input terminal; 7614 a two-input NAND element which conducts to supply angular signals to the counter 7700 when the single output terminal of the S.R.F.F. assumes the H

level; 7700 the counter comprising the flip-flops 7701 through 7706 to count the angular signals; 7800 the ignition system which receives the output signal of the comparator 7900 that will be explained later to distribute this output signal by way of the distributor rotor to the spark plug of the engine cylinder to produce an ignition spark; 7900 the comparator designed so that when it finds the count of the counter 7700 to be equal to the content of the memory 7500, it produces an output signal and at the same time it stops the operation of the counter 7700, resets the counter 7700 and also clears the content of the memory 7500; 7901 through 7906 the comparator elements constituting the comparator 7900 each of which produces an output signal at its output terminal Z when the binary coded signal from the flip-flops 7501 through 7506 of the memory 7500 and the binary coded signal from the flip-flops 7701 through 7706 of the counter 7700 are found to be equal to each other; 7907 a seven-input NAND element which produces its output signal only when all of the comparator elements 7901 through 7906 produce their output signals and when the angular signals assume the H level; 7908 a S.R.F.F. designed so that when the output signal of the seven-input NAND element 7907 is applied to one of its input terminals, it is set to produce a high level (H) output signal at the output thereof and thereafter it is reset only when the angular signal is applied to the other input terminal, so that the H level output signal at the output terminal is reset to the L level. The H level output signal produced at the output terminal of the S.R.F.F. clears the contents of the flip-flops 7501 through 7506 of the memory 7500 and the counts of the flip-flop 7701 through 7706 of the counter 7700. Numerals 7909 and 7910 designate two-input NAND elements constituting the S.R.F.F. 7908; 7911 the output terminal of the comparator 7900; 7615 the output terminal of the distributor; 7616 the output terminal of the S.R.F.F. 7611; 7617 the output terminal of the distributor which assumes the H level when the output signal voltage appears at the output terminal 7911 of the comparator 7900.

The arrangement of the comparator elements 7901 through 7906 of the comparator 7900 is the same as explained in connection with the description of the second embodiment (FIG. 17).

Next, the operation of the principal part of the present system as illustrated in FIGS. 79 through 81 will be explained with reference to FIG. 82. In this figure, designated as α and β are the voltage waveforms produced at the two output terminals of the timing sensor 7140; P the input voltage waveform at the input terminal of the inverter 7612 and this signal voltage P sets the S.R.F.F. 7611 so that the signal voltage designated as Q appears at the output terminal 7616 of the S.R.F.F. 7611; R the output signal voltage waveform at the output terminal 7615 of the distributor 7600; S the signal voltage waveform at the output terminal 7911 of the comparator 7900. As the S.R.F.F. 7611 is set with the output signal α of the timing sensor 7140 at time t_1 so that the signal voltage Q appears at the output terminal 7616, the angular signal voltage designated as R appears at the output terminal of the two-input NAND element 7614; i.e., the output terminal 7615 of the distributor 7600. Whereupon, the flip-flops 7701 through 7706 of the counter 7700 count the angular signals and eventually at time T_{11} the count of the counter 7700 attains the value of the content of the memory 7500 so

that the signal voltage S appears at the output terminal of the comparator 7900. Consequently, at the time T_{11} , the ignition system 7800 receives the signal voltage S and comes into operation to cause the spark plug to produce an ignition spark. Concurrently, the signal voltage S at the output terminal 7911 resets the flip-flops 7501 through 7506 of the memory 7500 and the flip-flops 7701 through 7706 of the counter 7700, whereby the content of the memory 7500 and the count of the counter 7700 are cleared. At the same time, the signal voltage S is inverted by the inverter 7613 and it is then applied to the S.R.F.F 7611 to reset it with the result that the signal voltage Q at the output terminal 7616 terminates, thereby extinguishing the angular signal pulse at the output terminal 7615.

The process of operations as described above is repeated thereafter at times $t_2, t_3, \dots, t_6$, thereby maintaining the continued operation of the engine. In this connection, while the ignition spark occurs at the time T_{11} which lags the time t_1 by the time from T_{11} to t_1 , this time T_{11} occurs earlier than the time t_2 . Put in another way, the "retard" with respect to the time t_1 of the timing signal from the timing sensor 7140 means "advance" with respect to the time t_2 . Thus, in distributing the high voltage surge produced by the ignition system 7800 to the spark plug, it is possible to arrange to have the ignition spark occur with a "positive" spark advance so that by computing the delay time (spark retard) of from time T_{11} to time t_1 , the lead time (spark advance) of from t_2 to T_{11} can be computed.

Embodiment 9:

A ninth embodiment of the present invention relates to a fuel control system, and more particularly an analog to a digital converter which constitutes a constituent element of the system and which converts the input analog signals corresponding to the parameters of an internal combustion engine into digital binary codes.

Referring now to FIG. 83 illustrating a block diagram showing the general construction of the present converter, numeral 8101 designates a reference rotational position (engine crankshaft) signal generator; 8102 a shaping circuit for converting the output signal of the reference rotational position signal generator 8101 into a voltage waveform representing, for example, the degree of crankshaft rotation at the top dead center of the engine cylinder; 8103 an integrator for integrating the output signal of the reference rotational position signal generator 8101; 8104 a level detector; 8105 a shaping circuit for producing the voltage waveform representing, for example, the degree of crankshaft rotation at the top dead center of a specified cylinder selected by the level detector 8105; 8106 a rotational position signal generator for generating the voltage waveform synchronized with the rotation of the engine crankshaft along with the reference rotational position signal generator 8101; 8107 a shaping circuit; 8108 an integrator constituting an engine speed sensor with the shaping circuit 8107; 8109, 8113 and 8114 differential amplifiers; 8110 a start detector; 8111 a vacuum sensor for producing an analog signal voltage corresponding to the degree of the engine intake manifold vacuum; 8112 a temperature sensor for producing an analog signal voltage corresponding to the temperature of the engine; 8115 an analog switch for effecting the time-sharing of an analog to a digital converter; 8116 a clock pulse generator; 8117 an binary code analog to digital converter (hereinafter referred to as an A - D con-

verter). In each of FIGS. 87(A), (B), (C), (D), (E) and (F), the abscissa represents the crank angles θ .

With the construction described above, the operation of the converter of the present embodiment will be explained. The voltage waveform produced by the reference rotational position signal generator 8101 as shown in FIG. 87(A) is applied to the shaping circuit 8102 where it is shaped to produce, as shown in FIG. 87(B), pulses at the reference rotational angles $\theta_1, \theta_2, \theta_3$ and θ_4 for the upper dead centers of the engine cylinders. On the other hand, the output of the reference rotational position signal generator 8101 is also applied to the integrator 8103 for integration and it is then applied to the level detector 8104 which distinguishes between the pulse A_1 having a higher crest value and the pulse A_2 having a lower crest value in FIG. 87(A), so that the pulses A_1 are selected and supplied to the shaping circuit 8105 to produce the pulses as shown in FIG. 87(C). In other words, the upper dead center of the specified cylinder is indicated. The rotational position signal generator 8106 is synchronized with the rotation of the engine along with the reference rotational position signal generator 8101 and it produces pulses whose waveform is shown in FIG. 87(D) and these pulses are then shaped in the shaping circuit 8107 to produce a larger number of pulses whose waveshapes are shown in FIGS. 87(E) and (F). By counting the number of these pulses, the degree of crankshaft rotation can be detected. The pulse having the voltage waveform shown in FIG. 87(E) is also applied from the shaping circuit 8107 to the integrator 8108 and the integrated pulse is then supplied to the differential amplifier 8109 where it is amplified to produce a signal voltage proportional to the engine speed. The start detector 8100 receives this signal voltage and compares it with the reference value to detect the start of the engine. The output analog voltages of the vacuum sensor 8111 and the temperature sensor 8112 are supplied to the differential amplifiers 8113 and 8114, respectively, so that their signal levels are adjusted to the operating level ranging from 0 to 7 V and these signal voltages are applied to the analog switch 8115 in addition to the output signal voltage of the differential amplifier 8109. The analog switch 8115 receives the clock pulses from the clock pulse generator 8116 to successively transmit the analog signals from the differential amplifiers 8109, 8113 and 8114 to the single A - D converter 8117 in a time-shared manner, and the A - D converter 8117 successively converts the input analog signals into the corresponding binary coded and send them out.

Next, the construction of the reference rotational position signal generator 8101, the rotational position signal generator 8106 and the binary code A - D converter 8117, respectively, will be explained in detail. Referring first to FIGS. 84A and 84B illustrating the reference rotational position signal generator 8101, numeral 8101a designates a distributor mounted to the engine (not shown); 8101b a distributor housing; 8101c a distributor shaft adapted to rotate in synchronism with the engine; 8101d and 8101e rotating field poles securely mounted on the distributor shaft 8101c through the intermediary of a sleeve 8101f made of a non-magnetic material, the rotating field pole 8101d having four salient poles 8101g, 8101h, 8101i and 8101j formed on the outer periphery thereof, and the rotating field pole 8101e having no such salient poles. Among the four salient poles of the rotating field pole

8101*d*, the salient pole 8101*g* is made specific and shaped so that it projects upward from the horizontal plane of the rotating field pole 8101*d*, while the remaining salient poles 8101*h*, 8101*i*, and 8101*j* are made smaller than the specific salient pole 8101*g* and disposed on the same plane. Numeral 8101*k* designates a permanent magnet so magnetized that the south pole is retained on the top and the north pole on the bottom in FIG. 84A, the permanent magnet 8101*k* being mounted between the rotating field poles 8101*d* and 8101*e* and secured on the shaft 8101*c* through the intermediary of the sleeve 8101*f*. Numeral 8101*l* designates a stationary field pole securely mounted on the inner wall of the non-magnetic housing 8101*b* of the distributor 8101*a*, the stationary field pole 8101*l* having four salient poles 8101*m*, 8101*n*, 8101*o* and 8101*p* of which the salient pole 8101*m* is made specific and so shaped that it projects upwardly to face the specific salient pole 8101*g* of the rotating field pole 8101*d*, while the remaining salient poles 8101*n*, 8101*o* and 8101*p* are disposed on the same plane and made smaller than the specific salient pole 8101*m*. Numeral 8101*q* designates an armature winding mounted in a recessed portion 8101*r* of the stationary field pole 8101*l*.

With the construction described above, the action which takes place when the shaft 8101*c* of the distributor 8101*a* rotates in synchronism with the engine will now be explained. To begin with, when the rotating field poles 8101*d* and 8101*e* and the stationary field pole 8101*l* assume the relative positions as shown in FIGS. 84A and 84B, the salient poles 8101*g*, 8101*h*, 8101*i* and 8101*j* of the rotating field pole 8101*d* face the respective salient poles 8101*m*, 8101*n*, 8101*o* and 8101*p* of the stationary field pole 8101*l*, so that the magnetic flux in the permanent magnet 8101*k* flows through these opposed salient poles and hence the magnetic flux interlinking the armature winding 8101*q* assumes a considerably large value, thereby producing the pulses which have a higher crest value as shown by A₁ in FIG. 87(A). Then, consider the situation in which the distributor shaft 8101*c* rotates through 90 degrees from its position shown in FIGS. 84A and 84B. This changes the relative positions of the poles. In other words, the rotating field pole 8101*d* and the stationary field pole 8101*l* are now positioned so that the salient poles 8101*g*, 8101*h*, 8101*i* and 8101*j* now face the salient poles 8101*n*, 8101*o*, 8101*p* and 8101*m*, respectively. However, since the specific salient pole 8101*g* of the rotating field pole 8101*d* and the specific salient pole 8101*m* of the stationary field pole 8101*l* are projected upward to stand out from the rest as shown in FIG. 84A, in fact that specific salient pole 8101*g* is not facing the salient pole 8101*n* and the salient pole 8101*j* is also not facing the specific salient pole 8101*m*. Consequently, the flux which interlinks the armature winding 8101*q* is correspondingly reduced and hence the reduced output voltage is obtainable when these poles are relatively positioned like this. Similarly, when the distributor shaft 8101*c* rotates through another 90 degrees, the reduced output voltage is obtained and this is the same when the shaft 8101*c* rotates through still another 90 degrees, thus producing the pulses having the lower crest value as shown by A₂ in FIG. 87(A). The same series of operations is repeated for each revolution of the shaft 8101*c*

and the armature winding 8101*q* produces two kinds of pulses, i.e., the pulses A₁ and A₂.

Referring now to FIG. 85, the construction of the rotational position signal generator 8106 will be explained. In this figure, numeral 8106*a* designates a ring gear integral with a fly wheel and rotatable in synchronism with the rotation of the engine; 8106*b* an armature winding; 8106*c* a permanent magnet; 8106*d* an output terminal for delivering the output waveform. Now, as the ring gear 8106*a* rotates with the engine so that the magnetic path between the permanent magnet 8106*c* and the ring gear 8106*a* changes to vary the magnetic flux which interlinks with the armature winding 8106*b*, the pulses whose waveform is shown in FIG. 87(D) appear at the output terminal 8106*d*. These pulses are then shaped in the shaping circuit 8107 to produce the pulses shown in FIG. 87(F). If the number of the teeth in the ring gear 8106*a* is *n*, then every pulse counted indicates that the engine crankshaft has rotated through (360/*n*) degrees.

Referring now to FIG. 86, the construction of the binary code A - D converter 8117 will be explained. In the figure, numeral 8117*a* designates an input terminal for analog signal voltages; 8117*b*, 8117*c*, 8117*d*, ..., 8117*n'* output terminals for digital signal voltages; 8117*e* a reference constant voltage source; 8117*f*, 8117*g*, 8117*h*, ..., 8117*n* circuits each of which is provided to produce a signal of one bit generated by the binary code A - D converter 8117, the *n* circuits being provided corresponding to the *n* digits contained in the digital signal produced by the converter. Numeral 8117*i* designates a comparator amplifier; 8117*j* a feedback resistor; 8117*k* and 8117*l* output resistors; 8117*m* a differential amplifier; 8117*o* a feedback resistor; 8117*p* an output resistor. With the construction described above, the operation of the A - D converter will be explained. In the first place, it is assumed that the output of the comparator amplifier 8117*i* is represented by the two binary digits "H" or "L," with the "H" output = 3.5 V and the "L" output = 0 V. The output of the reference constant voltage source 8117*e* is set to 3.5 V and the output analog voltages from the differential amplifiers 8109, 8113 and 8114 are controlled by these amplifiers to be same level, i.e., the same output range between 0 V and 7 V. The input analog signal voltage applied by way of the input terminal 8117*a* is first compared with the reference voltage of 3.5 V in the comparator 8117*i*. If the result of the comparison shows that the input analog signal voltage is greater than the reference voltage 3.5 V, the comparator 8117*i* produces an "H" signal, that is, the output voltage of the comparator 8117*i* is 3.5 V. this output signal is taken out of the digital output terminal 8117*b* as the most significant digit of the *n* digit binary code into which the analog input signal is to be converted. This output of 3.5 V is also applied to the differential amplifier 8117*m* as its one input signal so that it is subtracted from the input analog signal voltage introduced by way of the analog signal input terminal 8117*a*. If the gain of the differential amplifier 8117*m* is chosen to be 2, then the output voltage is given as the output voltage {(input analog signal voltage) - (reference voltage)} × 2. Thus, if the input analog signal voltage is smaller than the reference voltage of 3.5 V, then {(input analog signal voltage) - 0} × 2, so that the output at the digital output terminal 8117*d* is 0 V. The output of the differential amplifier 8117*m* which is now amplified by

the factor of 2 is applied to the comparator for the next most significant digit and it is compared with the same reference voltage of 3.5 V. By repeating this process *n* times, the required digital binary code is obtained.

In the embodiment described above, the differential amplifiers 8109, 8113 and 8114 are used as level adjusting circuits. However, these level adjusting circuits may comprise ordinary amplifiers whose input biasing and gain are properly modified. Furthermore, the sensors may include those sensors which detect the engine throttle valve positions, the opening speed of the throttle valve and the like as analog signals.

As described above, the converter of the present embodiment comprises a plurality of level adjusting circuits adapted to adjust a plurality of input analog signals corresponding to the engine parameters into the same range of voltage levels, an analog switch which receives the clock pulses to successively transmit a plurality of the output analog signals from the plurality of the level adjusting circuits to the succeeding stage in a time-sharing manner, and a binary code A - D converter which converts the output analog signals of the analog switch circuit into the binary coded digital signals. Thus, it is possible to obtain binary coded digital signals which are not affected by any variations of the power supply voltage, ambient temperature and the like and which correspond accurately to the various parameters of an engine. Moreover, when these binary coded digital signals are used as the inputs in the calculation of the volume of fuel injection, the amount of spark advance and the like, there is no danger that variations of the power supply voltage, ambient temperature and the like may result in any errors in the calculations. Furthermore, since the analog switch circuit is employed to transmit a plurality of input analog signals to the succeeding stage in a time-sharing manner, the analog to digital conversion can be performed with the single binary code A - D converter irrespective of the number of input analog signals applied. Thus, the converter according to the present embodiment is very simple in construction and extremely inexpensive.

1. A fuel control system for internal combustion engines in which the fuel is supplied through an electromagnetic valve to each cylinder of the engine by an amount which is predetermined as a non-linear function of at least one operational parameter of the engine, said system comprising:

vacuum sensor means responsive to the intake manifold vacuum of the engine for producing an analog voltage signal proportional to said vacuum;

a first analog to digital converter connected in circuit with said vacuum sensor for converting said analog voltage signal to a first digital signal in a binary code of a predetermined number of places;

a first discriminator connected in circuit with said first analog to digital converter for detecting one of a plurality of predetermined pressure ranges within which said vacuum represented by said first digital signal stands, and producing a number of output signals as determined by said detected pressure range;

first circuit means including a plurality of first shifted code setting circuits for each producing digital signals in binary codes which indicate respectively numbers represented by binary codes obtained by shifting said binary code of said first digital signal to the right successively by one place each shift, a

first constant code setting circuit for producing a predetermined constant value, and first selecting means for selecting a number of circuits from said first shifted code setting and said first constant code setting circuits in accordance with said number of output signals of said first discriminator and permitting said digital signals produced by the selected circuits to pass therethrough;

a first adder connected to said first circuit means for receiving said digital signals passed through said selecting means and adding them to produce an injection digital signal; and

injection circuit means for energizing said electromagnetic valve of each cylinder, thereby effecting a fuel injection for a time interval whose duration is determined by said injection digital signal.

2. A fuel control system according to claim 1, wherein said injection circuit means comprise:

a memory circuit in circuit with said first adder for retaining said output digital signal of said first adder in a form of a binary code;

a clock pulse generator for producing clock pulses with a predetermined frequency;

means for producing a timing pulse which determines the starting of fuel injection during each cycle for each cylinder;

a counter for counting said clock pulses transmitted thereto and producing an output digital signal in a binary code corresponding to the count;

a comparator for producing an output signal for ending the energization of said electromagnetic valve under coincidence of the digital signal retained in said memory and that of said counter, and

a distributor comprising means responsive to said timing pulse for starting and continuing energization of the electromagnetic valve of said each cylinder and simultaneously permitting said clock pulses, being transmitted to said counter from said clock pulse generator to pass therethrough and means responsive to an output signal of said comparator for ending the energization of said electromagnetic valve and simultaneously preventing thereafter said clock pulse from being transmitted to said counter.

3. A fuel control system according to claim 1, further comprising:

a speed sensor responsive to the speed of the engine for producing an analog voltage signal proportional to the engine speed;

an inverter circuit connected in circuit with said vacuum sensor for producing an analog voltage inversely proportional to said vacuum;

a second analog to digital converter connected in circuit with said inverter circuit for converting said analog voltage signal produced by said inverter circuit to a second digital signal in a binary code of a predetermined number of places;

a third analog to digital converter connected in circuit with said speed sensor for converting said analog voltage signal produced by said speed sensor to a third digital signal of a binary code of a predetermined number of places;

a second discriminator connected in circuit with said second analog to digital converter for detecting one of a plurality of predetermined pressure ranges within which the vacuum represented by said second digital signal stands and producing a number

of output signals as determined by said detected pressure range;

a third discriminator connected in circuit with said third analog to digital converter for detecting one of a plurality of predetermined speed ranges within which said engine speed represented by said third digital signal stands and producing a number of output signals determined by said detected speed range;

second circuit means including a plurality of second shifted code setting circuits for producing digital signals of binary codes which indicate respectively numbers represented by binary codes obtained by shifting said binary code of said second digital signal to the right successively by one place each shift, a second constant code setting circuit for producing a digital signal of a binary code indicating a predetermined constant value, and second selecting means for selecting a number of circuits from said second shifted code setting and second constant code setting circuits in accordance with said number of output signals of said second discriminator and permitting said digital signals of the selected circuits to pass said second selecting means;

third circuit means including a plurality of third shifted code setting circuits for producing digital signals in binary codes which indicate respectively numbers represented by binary codes obtainable by shifting said binary code of said third digital signal to the right successively by one place each shift, a third constant code setting circuit for producing a digital signal of a binary code indicating a predetermined constant value, and third selecting means for selecting a number of circuits from said third shifted code setting and third constant code setting circuits in accordance with said number of output signals of said third discriminator and permitting said digital signals of said selected circuits to pass through said third selecting means;

a second adder connected in circuit with said third circuit means and said second circuit means for receiving said digital signals produced by said second and third circuit means and adding them to produce an ignition digital signal; and

ignition circuit means for advancing an ignition of each cylinder by a time determined by said ignition digital signal.

4. A fuel control system according to claim 3, wherein said ignition circuit means comprise:

a memory circuit for retaining said output digital signal of said second adder in a form of a binary code;

an angular sensor for periodically producing pulses in accordance with rotations of the engine;

a timing sensor for producing a timing pulse responsive to a predetermined position each cycle of each cylinder;

a counter for counting pulses of said angular sensor transmitted thereto and producing an output digital signal of a binary code corresponding to the count;

a comparator for producing an output signal upon coincidence of said digital signal of said memory circuit and that of said counter;

a distributor comprising means responsive to said timing pulse for permitting said pulses of said angu-

lar sensor being transmitted therethrough to said counter; and

an ignition circuit for producing an ignition timing signal responsive to said output signal of said comparator.

5. A fuel control system according to claim 1 further comprising:

a temperature sensor responsive to the engine temperature for producing an analog voltage signal proportional thereto;

a second analog to digital converter connected in circuit with said temperature sensor for converting said analog voltage signal to a second digital signal in a binary code of a predetermined number of places;

a second discriminator connected in circuit with said analog to digital converter for detecting one of a plurality of predetermined temperature ranges within which said engine temperature represented by said second digital signal stands and producing a number of output signals determined by said detected temperature range;

a start sensor for producing a signal upon starting of the engine;

second circuit means comprising a plurality of second shifted code setting circuits for producing digital signals of binary codes which represent respectively numbers represented by binary codes obtained by shifting said binary code of said second digital signal to the right successively by one place each shift, a second constant setting circuit for producing a digital signal of a binary code indicating a predetermined constant value, and second selecting means for selecting a number of circuits from said second shifted code setting and said second constant setting circuits in accordance with said number of output signals of said second discriminator and said signal of said start sensor and permitting said digital signals produced by said selected circuits to pass therethrough; and

a first auxiliary circuit connected between said first adder and said injection circuit means and further connected to said second circuit means for correcting said injection digital signal produced by said first adder in accordance with said digital signals passed through said second selecting means and supplying said corrected injection digital signal to said injection circuit means.

6. A fuel control system according to claim 5 further comprising:

an engine speed sensor responsive to the engine speed for producing an analog voltage signal proportional to said engine speed;

a third analog to digital converter connected in circuit to said engine speed sensor for converting said analog signal to a third digital signal of a binary code of a predetermined number of places;

a third discriminator connected in circuit with said third analog to digital converters for detecting one of a plurality of predetermined speed ranges within which said engine speed represented by said third digital signal stands and producing a number of output signals determined by said detected speed range;

a fourth discriminator connected in circuit with said first analog to digital converters for detecting one of a plurality of predetermined pressure ranges

within which said vacuum represented by said first digital signal stands and producing a number of output signals determined by said detected pressure range;

third circuit means comprising a plurality of third shifted code setting circuits for producing digital signals of binary codes which indicate respectively numbers represented by binary codes obtainable by shifting said binary code of said third digital signal to the right successively by one place each shift, a third constant code setting circuit for producing a digital signal indicative of a predetermined constant value, and third selecting means for selecting a number of circuits from said third shifted code setting and third constant code setting circuits in accordance with said output signals of said third discriminator and permitting said digital signals of said selected circuits to pass therethrough;

fourth circuit means comprising fourth selecting means for selecting a number of circuits from said first shifted code setting and first constant code setting circuits in accordance with said output signals of said fourth discriminator and permitting said digital signals of said selected circuits determined by said fourth selecting means to pass therethrough;

means connected to said third and fourth circuit means for summing the signals passed therethrough to provide an ignition signal;

a first memory circuit for retaining a digital signal supplied thereto and connected to said injection circuit means for supplying the same with said digital signal memorized therein;

a second memory circuit for receiving said ignition signal and retaining that ignition; and

ignition circuit means connected to said second memory circuit for producing an ignition timing signal in accordance with said digital signal retained in said second memory circuit thereby effecting an ignition at a time determined by said retained digital signal.

7. A fuel control system according to claim 5 wherein said first auxiliary circuit comprises:

a second adder connected to said second circuit means for adding said digital signals produced by said second circuit means thereby producing a number of second addition digital signals determined by said addition;

adder circuit means connected to said first adder and said second adder and comprising a plurality of addition code setting circuits for producing digital signals of binary codes which indicate respectively numbers represented by binary codes obtainable by shifting a binary code of said injection digital signal produced by said first adder to the right successively by one place each shift, and adder selecting means for selecting a number of circuits from said addition code setting circuits in accordance with said number of second addition digital signals and permitting said digital signals of said selected circuits to pass therethrough, and

a third adder connected between said adder circuit means and said injection circuit means for receiving said digital signals passed through said adder selecting means and adding them totally thereby producing a digital signal which is supplied to said injection circuit means as an injection digital signal.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

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INVENTOR(S) : Hiroshi Yoshida, Moriyoshi Ando & Kazuo Oishi

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Under the Heading:

[30] Foreign Application Priority Data

Please add:

March 20, 1970	Japan.....23832/70
April 23, 1970	Japan.....34856/70
May 22, 1970	Japan.....44184/70

Signed and sealed this 27th day of May 1975.

(SEAL)
Attest:

RUTH C. MASON
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