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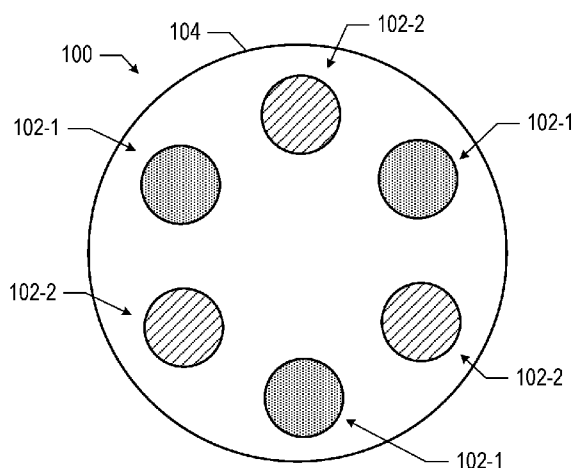


FIG. 1A

(57) **Abstract:** Disclosed herein are chemical mechanical polishing (CMP) conditioning disks, and related systems and techniques. For example, in some embodiments, a CMP conditioning disk may include: a support; a first pedestal extending from the support, the first pedestal having a first surface roughness (SR); and a second pedestal extending from the support, the second pedestal having a second SR different from the first SR.

CONDITIONING DISKS FOR CHEMICAL MECHANICAL POLISHINGTechnical Field

[0001] The present disclosure relates generally to chemical mechanical polishing (CMP), and more particularly, to CMP conditioning disks.

Background

[0002] Chemical mechanical polishing (CMP) typically includes rotating and translating a polishing pad on a wafer to remove material from the wafer and achieve a flat wafer surface. For example, a wafer may be polished to remove an oxide layer prior to a lithography step. The polishing process may degrade the polishing surface of CMP polishing pads; to "refurbish" a CMP polishing pad and mitigate a degradation in polishing performance, the polishing surface may be abraded using a CMP conditioning disk.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIG. 1A is a top view of an example chemical mechanical polishing (CMP) conditioning disk having multiple pedestals with different surface roughnesses (SRs), in accordance with various embodiments.

[0005] FIG. 1B shows example profiles of pedestal surfaces having different SRs, in accordance with various embodiments.

[0006] FIG. 2 is a side view of a CMP system including a CMP conditioning disk as disclosed herein, in accordance with various embodiments.

[0007] FIGS. 3-4 are top views of example CMP conditioning disks having multiple pedestals with different SRs, in accordance with various embodiments.

[0008] FIGS. 5-7 illustrate various example stages in the manufacture of a CMP conditioning disk as disclosed herein, in accordance with various embodiments.

[0009] FIG. 8 is a flow diagram of a method of manufacturing a CMP conditioning disk, in accordance with various embodiments.

[0010] FIG. 9 is a flow diagram of a method of using a CMP conditioning disk, in accordance with various embodiments.

[0011] FIGS. 10A and 10B are top views of a wafer and dies that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0012] FIG. 11 is a cross-sectional side view of an integrated circuit (IC) device that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0013] FIG. 12 is a cross-sectional side view of an IC device assembly that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0014] FIG. 13 is a block diagram of an example computing device that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

Detailed Description

[0015] Disclosed herein are chemical mechanical polishing (CMP) conditioning disks, and related systems and techniques. For example, in some embodiments, a CMP conditioning disk may include: a support; a first pedestal extending from the support, the first pedestal having a first surface roughness (SR); and a second pedestal extending from the support, the second pedestal having a second SR different from the first SR.

[0016] The CMP conditioning disk designs disclosed herein may improve performance versatility over conventional CMP conditioning disks. In such conventional disks, all of the abrasive portions typically have the same surface roughness (SR), and the "shapes" of the abrasive portions on the CMP conditioning disk are identical. This uniformity is often the result of a single chemical vapor deposition (CVD) or other manufacturing process that creates the abrasive portions.

[0017] However, optimal disk performance may be achieved when the aggressiveness of the CMP conditioning disk (measured, e.g., by pad cut rate and/or pad surface roughness) can be finely tuned to achieve a desired removal of waste byproduct in the CMP polishing pad and/or generate grooves in the CMP polishing pad for slurry delivery. Various ones of the embodiments disclosed herein may achieve such fine tuning by including multiple pedestals having different SRs, achieving performance parameters not achieved by conventional, uniform designs.

[0018] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0019] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order

dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0020] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges.

[0021] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale.

[0022] FIG. 1A is a top view of an example chemical mechanical polishing (CMP) conditioning disk 100 having multiple pedestals 102 with different surface roughnesses (SRs) extending from a support 104, in accordance with various embodiments. In particular, the pedestals 102-1 may have a first SR different from a second SR of the pedestals 102-2. Although six pedestals 102 are illustrated in FIG. 1A, and the pedestals 102-1 and 102-2 are arranged in alternating and regular manner, the CMP conditioning disk 100 may include fewer than or more than six pedestals and may include pedestals having different combinations of shapes, as desired.

[0023] As used herein, the "SR" of a pedestal 102 of a CMP conditioning disk 100 may refer to any suitable surface roughness metric or combination of such metrics (e.g., a profile surface roughness metric, an area surface roughness metric, any combination of such metrics, etc.). For example, the SR of a pedestal 102 may be the average roughness (known as "R_a"), calculated in accordance with:

$$\frac{1}{n} \sum_{i=1}^n |y_i|$$

[0024] where y_i is the vertical distance between the mean line and the i th data point in the surface profile, as known in the art. In some embodiments, the SR may be the root mean square roughness (known as "R_q"), calculated in accordance with:

$$\sqrt{\frac{1}{n} \sum_{i=1}^n (y_i)^2}$$

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[0025] In other embodiments, the SR may be the maximum valley depth, the maximum peak height, the maximum total height and the surface profile, or any other surface roughness parameter. In some embodiments, multiple surface roughness parameters may be combined (e.g., in a linear or nonlinear combination) to generate an SR. Various examples of particular SRs are used to illustrate the systems and techniques disclosed herein, but these are simply for illustrative purposes, and any suitable SR may be used to quantify the roughness of a pedestal 102.

[0026] In some embodiments, the pedestals 102 may be formed by abrasive material disposed on an otherwise "flat" support 104. For example, the pedestals 102 may be formed by embedding portions of abrasive material in the support 104 such that the portions extend away from the support 104. In other embodiments, the support 104 may include raised portions, and the pedestals 102 may include the raised portions and abrasive material disposed thereon. Examples of the latter embodiments are discussed below with reference to FIGS. 5-7.

[0027] The support 104 may be formed from any suitable material or materials. In some embodiments, the support 104 may be formed of a material that may be used as a substrate for growing an abrasive material for the pedestals 102 using chemical vapor deposition (CVD). For example, when the abrasive material for the pedestals 102 is CVD-grown diamond, the support 104 (e.g., raised portion of the support, as discussed below with reference to FIGS. 5-7) may be formed of a carbon- or silicon-based composite material, such as silicon carbide. In some embodiments, the pedestals 102 may have diamonds embedded in their surface. Although diamond is used as an example of an abrasive herein, other materials with hardnesses similar to diamond may be used, instead of or in addition to diamond, in various embodiments.

[0028] FIG. 1B illustrates profiles of surfaces having different SRs, in accordance with various embodiments. In particular, FIG. 1B illustrates a first profile 174-1 and a second profile 174-2 (along with the mean lines of each surface profile). The first profile 174-1 may correspond to one of the first pedestals 102-1 of the CMP conditioning disk 100 of FIG. 1A, for example, and the second profile 174-2 may correspond to one of the second pedestals 102-2 of the CMP conditioning disk 100 of FIG. 1A. In some embodiments, such surface profiles may be generated by a profilometer (e.g., using white light spectroscopy) or another suitable device. The SR of the surface represented by the first profile 174-1 may be greater than the SR of the surface represented by the second profile 174-2 (using any suitable SR metric).

[0029] As noted above, the SR of the pedestals 102-1 may be different from the SR of the pedestals 102-2. In some embodiments, the SR of at least one of the pedestals 102-1 may be 10% greater than the SR of at least one of the pedestals 102-2. In some embodiments, the SR of at least one of the pedestals 102-1 may be 15% greater than the SR of at least one of the pedestals 102-2. In some

embodiments, the SR of at least one of the pedestals 102-1 may be 20% greater than the SR of at least one of the pedestals 102-2. In some embodiments, the SR of at least one of the pedestals 102-1 may be 30% greater than the SR of at least one of the pedestals 102-2. These relative SRs may apply to any of the embodiments of the CMP conditioning disk 100, not just the embodiment illustrated in FIG. 1A.

[0030] Different SRs for different pedestals 102 in a CMP conditioning disk 100 may be achieved in any suitable manner. For example, CVD may be used, and the film grains used during CVD (e.g., diamond CVD) may determine the SR. The size of these grains may be determined by the CVD process conditions, such as temperature, time, deposition material source, etc., as known in the art. In some CVD diamond embodiments, for example, a rectangular deposition morphology may result in a higher SR than a rhomboid deposition morphology. This example is simply illustrative, and other parameters (e.g, CVD parameters) may control the SR of the resulting pedestal 102.

[0031] The amount of conditioning performed by the CMP conditioning disk 100 on a CMP polishing pad (e.g., the CMP polishing pad 158 of FIG. 2, discussed below) may be quantified by the pad cut rate (PCR), the amount of material removed from the CMP polishing pad by the CMP conditioning disk 100 (normalized by time of conditioning). The SR of the CMP conditioning disk 100 may correlate with the PCR of the CMP conditioning disk 100. In some embodiments, a 3X increase in the average roughness of the CMP conditioning disk 100 may yield an 8X increase in the PCR. The PCR of the conditioning disk 100 may be between the PCR of the conditioning disk 100 if all of the pedestals 102 had an SR equal to the SR of a pedestal 102-1, and the PCR of the conditioning disk 100 if all of the pedestals 102 had an SR equal to the SR of a pedestal 102-2. In some embodiments, the PCR of the CMP conditioning disk 100 may be between 1 and 15 $\mu\text{m}/\text{minute}$. In some embodiments, the PCR of the CMP conditioning disk 100 may be between 4 and 12 $\mu\text{m}/\text{minute}$. In some embodiments, the PCR of the CMP conditioning disk 100 may be between 5 and 10 $\mu\text{m}/\text{minute}$. These PCR ranges may apply to any of the embodiments of the CMP conditioning disk 100, not just the embodiment illustrated in FIG. 1A.

[0032] FIG. 2 is a side view of a CMP system 150 including a CMP conditioning disk 100, in accordance with various embodiments. The CMP system 150 may include a CMP conditioning disk 100 disposed on a first arm 152. The CMP conditioning disk 100 of the CMP system 150 may take the form of any of the CMP conditioning disks disclosed herein. The CMP conditioning disk 100 may be secured to the first arm 152 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. The first arm 152 may include mechanical linkages to allow the CMP conditioning disk 100 to translate "up and down" to bring the CMP conditioning disk 100 into contact with the CMP polishing pad 158 (discussed below). In some embodiments, the first arm 152

may include mechanical linkages to allow the CMP conditioning disk 100 to translate "side to side" while in contact with the CMP polishing pad 158. In some embodiments, the first arm 152 may include a rotor to allow the CMP conditioning disk 100 to rotate while in contact with the CMP polishing pad 158. The first arm 152 may include, for example, a head, as known in the art. In various embodiments, the CMP system 150 may include control circuitry (not shown) to allow a user to control the rotation rate of the CMP conditioning disk 100, the downward force exerted by the CMP conditioning disk 100 on the CMP polishing pad 158, the "side to side" translation of the CMP conditioning disk 100, and/or other operational properties of the CMP system 150.

[0033] The CMP system 150 may include a CMP polishing pad 158 disposed on a second arm 154. The CMP polishing pad 158 may be formed from a porous material, such as a hard elastomer or a polyurethane-based material. The CMP polishing pad 158 may include other additives to achieve a desired porosity, as known in the art. Different CMP polishing pads 158 may have different mechanical properties, such as hardness (e.g., with "soft" pads having a hardness between 10 and 20 MPa, and "hard" pads having a hardness between 200 and 1500 MPa). The CMP polishing pad 158 may be secured to the second arm 154 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. The second arm 154 may include mechanical linkages to allow the CMP polishing pad 158 to translate "up and down" to bring the CMP polishing pad 158 into contact with the CMP conditioning disk 100 and/or the wafer 160 (discussed below). In some embodiments, the second arm 154 may include mechanical linkages to allow the CMP polishing pad 158 to translate "side to side" while in contact with the CMP conditioning disk 100 and/or the wafer 160. In some embodiments, the second arm 154 may include a rotor to allow the CMP polishing pad 158 to rotate while in contact with the CMP conditioning disk 100 and/or the wafer 160. The second arm 154 may be, for example, a platen, as known in the art. In various embodiments, the CMP system 150 may include control circuitry (not shown) to allow a user to control the rotation rate of the CMP polishing pad 158, the "side to side" translation of the CMP polishing pad 158, and/or other operational properties of the CMP system 150, as noted above. The amount of conditioning performed by the CMP conditioning disk 100 on the CMP polishing pad 158 may be quantified by the pad cut rate (PCR), the amount of material removed from the CMP polishing pad 158 by the CMP conditioning disk 100 (normalized by time of conditioning).

[0034] The CMP system 150 may include a wafer 160 disposed on a third arm 156. The wafer 160 may have any suitable dimensions (e.g., 200, 300, or 450 mm in diameter). The wafer 160 may be secured to the third arm 156 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. In some embodiments, the wafer 160 may be disposed in a retainer ring to control the "side to side" movement of the wafer 160, and vacuum force may be

used to hold the wafer 160 against the third arm 156 to control the "up and down" movement of the wafer 160. The third arm 156 may include mechanical linkages to allow the wafer 160 to translate "up and down" to bring the wafer 160 into contact with the CMP polishing pad 158. In some embodiments, the third arm 156 may include mechanical linkages to allow the wafer 160 to translate "side to side" while in contact with the CMP polishing pad 158. In some embodiments, the third arm 156 may include a rotor to allow the wafer 160 to rotate while in contact with the CMP polishing pad 158. In various embodiments, the CMP system 150 may include control circuitry (not shown) to allow a user to control the rotation rate of the wafer 160, the "side to side" translation of the wafer 160, the downward force exerted by the third arm 156 on the CMP conditioning pad 158, and/or other operational properties of the CMP system 150, as noted above.

[0035] When the CMP conditioning disk 100 is brought into contact with the CMP polishing pad 158, and the two are rotated (and/or translated) relative to one another, the surfaces of the pedestals 102 of the CMP conditioning disk 100 may "dig" into the surface of the CMP polishing pad 158 and create grooves in the CMP polishing pad 158.

[0036] When the wafer 160 is brought into contact with the CMP polishing pad 158, and the two are rotated (and/or translated) relative to one another, the CMP polishing pad 158 may remove material from the wafer 160 and thereby polish the wafer 160. A slurry 162 may be disposed on the CMP polishing pad 158. When the wafer 160 is brought into contact with the CMP polishing pad 158, and the two are rotated (and/or translated) relative to one another, the slurry 162 may flow between the CMP polishing pad 158 and the wafer 160 to facilitate the polishing of the wafer 160. In some embodiments, a retainer ring holding the wafer 160 on the third arm 156 may include grooves to allow the slurry 162 to flow to the wafer 160 and away from the wafer 160 during polishing. The slurry 162 may also flow through grooves in the CMP polishing pad 158 formed by the CMP conditioning disk 100. The slurry 162 may take any suitable form known in the art (e.g., an oxide slurry). Control circuitry (not shown) included in the CMP system 150 may control the rate of flow of the slurry 162 from a slurry source (not shown) in some embodiments.

[0037] In some embodiments, the CMP conditioning disk 100 may be used to condition the CMP polishing pad 158 simultaneously with the CMP polishing pad 158 polishing the wafer 160. That is, the CMP conditioning disk 100 may be in contact with (and rotated relative to) the CMP polishing pad 158 at the same time that the wafer 160 may be in contact with (and rotated relative to) the CMP polishing pad 158. In other embodiments, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 100 before and/or after (but not simultaneously with) polishing the wafer 160 using the CMP polishing pad 158.

[0038] FIGS. 3-4 are top views of example CMP conditioning disks having multiple pedestals with different SRs, in accordance with various embodiments. FIG. 3 depicts a CMP conditioning disk 100 having multiple pedestals 102 of different shapes. The pedestal 102-1 may have a substantially trapezoidal footprint, the pedestals 102-2 may have circular footprints, and the pedestals 102-3 may have substantially trapezoidal footprints (like the pedestal 102-1). The SR of the pedestals 102-1 may differ from the SR of the pedestals 102-2 and the SR of the pedestals 102-3, and the SR of the pedestals 102-2 may differ from the SR of the pedestals 102-3. In other embodiments, the SR of the pedestals 102-1 may be the same as the SR of the pedestals 102-2 (but may differ in shape), the SR of the pedestals 102-2 may be the same as the SR of the pedestals 102-3 (but may differ in shape), and/or the SR of the pedestals 102-1 may be the same as the SR of the pedestals 102-3 (but may differ in shape). In some embodiments, abrasive material may be disposed only in the pedestals 102 of the embodiment of FIG. 3, and not on the rest of the support 104. In some embodiments, the pedestals 102 may include raised portions on which abrasive material is disposed (see, e.g., FIGS. 5-7), while in other embodiments, the pedestals 102 may be formed from an abrasive material disposed on an otherwise "flat" support 104. Although five pedestals 102 are illustrated in FIG. 3, the CMP conditioning disk 100 may include fewer than or more than five pedestals, and may include pedestals having different combinations of shapes, as desired.

[0039] FIG. 4 depicts a CMP conditioning disk 100 having multiple elongated pedestals 102 in a regular arrangement. The pedestals 102-1 may have a different SR than the pedestals 102-2. Each of these pedestals 102 may have the shape of a vane or ridge, as shown. In some embodiments, abrasive material may be disposed only in the pedestals 102 of the embodiment of FIG. 4, and not on the rest of the support 104. In some embodiments, the pedestals 102 may include raised portions on which abrasive material is disposed (see, e.g., FIGS. 5-7), while in other embodiments, the pedestals 102 may be formed from an abrasive material disposed on an otherwise "flat" support 104. The support 104 of FIG. 4 has a circular footprint (corresponding to the footprint of the CMP conditioning disk 100). Although eight pedestals 102 are illustrated in FIG. 4, the CMP conditioning disk 100 may include fewer than or more than eight pedestals, and may include pedestals having different combinations of shapes or in different arrangements (e.g., non-alternating), as desired.

[0040] The CMP conditioning disks 100 disclosed herein may be manufactured using any suitable techniques. FIGS. 5-7 illustrate various example stages in the manufacture of a CMP conditioning disk 100, in accordance with various embodiments.

[0041] FIG. 5 is a side cross-sectional view of a support 104. The support 104 may have two or more raised portions 110 extending from a base 108. Two raised portions 110-1 and 110-2 are illustrated in FIG. 5, but the support 104 may include more raised portions 110. In some

embodiments, the raised portions 110 and the base 108 may be integrally formed (e.g., by three-dimensional printing, molding, laser engraving, or otherwise machining the raised portions 110 and the base 108 from a single block of material). In other embodiments, the raised portions 110 may be secured to the base 108 using an adhesive, a mechanical fastener, a friction fit, or any other suitable technique. The base 108 and the raised portions 110 may be formed of a same material or of different materials. The shape of the footprint of the raised portions 110 may be any desired shape, such as circular (e.g., for a substantially cylindrical, conical, or semispherical raised portion 110), a polygon (e.g., a triangle, rectangle, or higher-order polygon), or any other desired shape. In some embodiments, different raised portions 110 in a support 104 may have different shapes (e.g., different profiles or footprints). In other embodiments, the support 104 may not include any raised portions 110. More generally, the support 104 may take the form of any of the embodiments disclosed herein.

[0042] FIG. 6 is a side cross-sectional view of an assembly 600 subsequent to providing an abrasive material 112-1 on the raised portion 110-1 of the support 104 of FIG. 5 to form the pedestal 102-1. The abrasive material 112-1 may be any abrasive material suitable for conditioning the surface of the CMP polishing pad 158 (e.g., as discussed above with reference to FIG. 2). In some embodiments, the abrasive material 112-1 may include a diamond film. In such embodiments, the diamond film may be formed by chemical vapor deposition (CVD), for example. In some embodiments, the abrasive material may be any other suitable abrasive and may be secured to the raised portion 110-1 by any suitable mechanism (e.g., adhesive). In embodiments in which the abrasive material 112-1 is to be used to form multiple pedestals 102, multiple portions of the abrasive material 112-1 may be provided on the support 104 simultaneously, in sequence, or in any desired order.

[0043] FIG. 7 is a side cross-sectional view of a CMP conditioning disk 100 subsequent to providing an abrasive material 112-2 on the raised portion 110-2 of the assembly 600 of FIG. 6 to form the pedestal 102-2. The abrasive material 112-2 may be any abrasive material suitable for conditioning the surface of the CMP polishing pad 158 and may take any of the forms discussed above with reference to the abrasive material 112-1. In embodiments in which the abrasive material 112-2 is to be used to form multiple pedestals 102, multiple portions of the abrasive material 112-2 may be provided on the support 104 simultaneously, in sequence, or in any desired order. The SR of the abrasive material 112-2 (and thus the SR of the pedestal 102-2) may be different from the SR of the abrasive material 112-1/pedestal 102-1.

[0044] In some embodiments, the abrasive materials 112 discussed above with reference to FIGS. 6 and 7 may not be deposited on the raised portions 110, but may be embedded into the raised portions 110 (or other portions of the support 104). For example, diamond or another similarly hard

material may be embedded into the surfaces of the raised portions 110, using any suitable technique.

[0045] FIG. 8 is a flow diagram of a method 800 of manufacturing a CMP conditioning disk, in accordance with various embodiments. Although various operations are arranged in particular order and illustrated once each, various ones of the operations may be repeated or performed in any suitable order.

[0046] At 802, a support may be provided. For example, the support 104 may be provided. In some embodiments, the support 104 may include raised portions (e.g., the raised portions 110 discussed above with reference to FIGS. 5-7). In some embodiments, the support 104 may not include raised portions.

[0047] At 804, a first abrasive material of a first pedestal may be provided on the support of 802. For example, the abrasive material 112-1 of the pedestal 102-1 of the assembly 600 of FIG. 6 may be provided on the support 104.

[0048] At 806, a second abrasive material of a second pedestal may be provided on the support of 802. The SR of the first abrasive material may be different from the SR of the second abrasive material. For example, the abrasive material 112-2 of the pedestal 102-2 of the CMP conditioning disk 100 of FIG. 7 may be provided on the support 104, and the abrasive material 112-2 may have a different SR than an SR of the abrasive material 112-1.

[0049] FIG. 9 is a flow diagram of a method 900 of using a CMP conditioning disk, in accordance with various embodiments. Although various operations are arranged in particular order and illustrated once each, various ones of the operations may be repeated or performed in any suitable order.

[0050] At 902, a CMP conditioning disk may be brought into contact with a CMP polishing pad. The CMP conditioning disk may include a first pedestal having a first SR and a second pedestal having a second SR different from the first SR. For example, the CMP conditioning disk 100 may be brought into contact with the CMP polishing pad 158 of the CMP system 150 (FIG. 2). The CMP conditioning disk 100 may include a first pedestal 102-1 having a first SR and a second pedestal 102-2 having a second SR different from the first SR. The CMP conditioning disk of 902 may take any suitable form, such as any of the forms disclosed herein.

[0051] At 904, the CMP conditioning disk may be rotated to polish the CMP polishing pad. For example, the CMP conditioning disk 100 and the CMP polishing pad 158 of the CMP system 150 may be rotated and/or translated relative to one another (e.g., using the first arm 152 and the second arm 154) to polish the CMP polishing pad 158.

[0052] Devices processed using the CMP systems and techniques disclosed herein (e.g., polished by CMP polishing pads conditioned by the CMP conditioning disks disclosed herein) may be included in any suitable electronic device. FIGS. 10-13 illustrate various examples of apparatuses that may include devices processed using the CMP systems and techniques disclosed herein.

[0053] FIGS. 10A-B are top views of a wafer 1000 and dies 1002 that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein. In particular, the wafer 1000 may be the wafer 160 polished in the CMP system 150 of FIG. 2. The wafer 1000 may be composed of semiconductor material and may include one or more dies 1002 having IC structures formed on a surface of the wafer 1000. Each of the dies 1002 may be a repeating unit of a semiconductor product that includes any suitable IC. After the fabrication of the semiconductor product is complete (e.g., after the semiconductor product is polished in accordance with any of the techniques disclosed herein), the wafer 1000 may undergo a singulation process in which each of the dies 1002 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices processed using the CMP systems and techniques disclosed herein may take the form of the wafer 1000 (e.g., not singulated) or the form of the die 1002 (e.g., singulated). The die 1002 may include one or more transistors (e.g., some of the transistor(s) 1140 of FIG. 11, discussed below) and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components. In some embodiments, the wafer 1000 or the die 1002 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1002. For example, a memory array formed by multiple memory devices may be formed on a same die 1002 as a processing device (e.g., the processing device 1302 of FIG. 13) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0054] FIG. 11 is a cross-sectional side view of an IC device 1100 that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein. The IC device 1100 may be formed on a substrate 1102 (e.g., the wafer 1000 of FIG. 10A) and may be included in a die (e.g., the die 1002 of FIG. 10B). The substrate 1102 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. The substrate 1102 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 1102 may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V,

or IV may also be used to form the substrate 1102. Although a few examples of materials from which the substrate 1102 may be formed are described here, any material that may serve as a foundation for an IC device 1100 may be used. The substrate 1102 may be part of a singulated die (e.g., the dies 1002 of FIG. 10B) or a wafer (e.g., the wafer 1000 of FIG. 10A).

[0055] The IC device 1100 may include one or more device layers 1104 disposed on the substrate 1102. The device layer 1104 may include features of one or more transistors 1140 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 1102. The device layer 1104 may include, for example, one or more source and/or drain (S/D) regions 1120, a gate 1122 to control current flow in the transistors 1140 between the S/D regions 1120, and one or more S/D contacts 1124 to route electrical signals to/from the S/D regions 1120. The transistors 1140 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 1140 are not limited to the type and configuration depicted in FIG. 11 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0056] Each transistor 1140 may include a gate 1122 formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0057] The gate electrode layer may be formed on the gate dielectric layer and may include at least one P-type work function metal or N-type work function metal, depending on whether the transistor 1140 is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel,

and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide).

[0058] In some embodiments, when viewed as a cross-section of the transistor 1140 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0059] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0060] The S/D regions 1120 may be formed within the substrate 1102 adjacent to the gate 1122 of each transistor 1140. The S/D regions 1120 may be formed using either an implantation/diffusion process or an etching/deposition process, for example. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate 1102 to form the S/D regions 1120. An annealing process that activates the dopants and causes them to diffuse farther into the substrate 1102 may follow the ion implantation process. In the latter process, the substrate 1102 may first be etched to form recesses at the locations of the S/D regions 1120. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the S/D regions 1120. In some implementations, the S/D regions 1120 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 1120 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further

embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 1120.

[0061] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 1140 of the device layer 1104 through one or more interconnect layers disposed on the device layer 1104 (illustrated in FIG. 11 as interconnect layers 1106-1110). For example, electrically conductive features of the device layer 1104 (e.g., the gate 1122 and the S/D contacts 1124) may be electrically coupled with the interconnect structures 1128 of the interconnect layers 1106-1110. The one or more interconnect layers 1106-1110 may form an interlayer dielectric (ILD) stack 1119 of the IC device 1100.

[0062] The interconnect structures 1128 may be arranged within the interconnect layers 1106-1110 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 1128 depicted in FIG. 11). Although a particular number of interconnect layers 1106-1110 is depicted in FIG. 11, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0063] In some embodiments, the interconnect structures 1128 may include trench structures 1128a (sometimes referred to as "lines") and/or via structures 1128b (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The trench structures 1128a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 1102 upon which the device layer 1104 is formed. For example, the trench structures 1128a may route electrical signals in a direction in and out of the page from the perspective of FIG. 11. The via structures 1128b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 1102 upon which the device layer 1104 is formed. In some embodiments, the via structures 1128b may electrically couple trench structures 1128a of different interconnect layers 1106-1110 together.

[0064] The interconnect layers 1106-1110 may include a dielectric material 1126 disposed between the interconnect structures 1128, as shown in FIG. 11. In some embodiments, the dielectric material 1126 disposed between the interconnect structures 1128 in different ones of the interconnect layers 1106-1110 may have different compositions; in other embodiments, the composition of the dielectric material 1126 between different interconnect layers 1106-1110 may be the same.

[0065] A first interconnect layer 1106 (referred to as Metal 1 or "M1") may be formed directly on the device layer 1104. In some embodiments, the first interconnect layer 1106 may include trench structures 1128a and/or via structures 1128b, as shown. The trench structures 1128a of the first interconnect layer 1106 may be coupled with contacts (e.g., the S/D contacts 1124) of the device layer 1104.

[0066] A second interconnect layer 1108 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 1106. In some embodiments, the second interconnect layer 1108 may include via structures 1128b to couple the trench structures 1128a of the second interconnect layer 1108 with the trench structures 1128a of the first interconnect layer 1106. Although the trench structures 1128a and the via structures 1128b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 1108) for the sake of clarity, the trench structures 1128a and the via structures 1128b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0067] A third interconnect layer 1110 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 1108 according to similar techniques and configurations described in connection with the second interconnect layer 1108 or the first interconnect layer 1106.

[0068] The IC device 1100 may include a solder resist material 1134 (e.g., polyimide or similar material) and one or more bond pads 1136 formed on the interconnect layers 1106-1110. The bond pads 1136 may be electrically coupled with the interconnect structures 1128 and configured to route the electrical signals of the transistor(s) 1140 to other external devices. For example, solder bonds may be formed on the one or more bond pads 1136 to mechanically and/or electrically couple a chip including the IC device 1100 with another component (e.g., a circuit board). The IC device 1100 may have other alternative configurations to route the electrical signals from the interconnect layers 1106-1110 than depicted in other embodiments. For example, the bond pads 1136 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0069] FIG. 12 is a cross-sectional side view of an IC device assembly 1200 that may include components processed using any of the CMP systems and techniques disclosed herein. The IC device assembly 1200 includes a number of components disposed on a circuit board 1202 (which may be, e.g., a motherboard). The IC device assembly 1200 includes components disposed on a first face 1240 of the circuit board 1202 and an opposing second face 1242 of the circuit board 1202; generally, components may be disposed on one or both faces 1240 and 1242.

[0070] In some embodiments, the circuit board 1202 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1202. In other embodiments, the circuit board 1202 may be a non-PCB substrate.

[0071] The IC device assembly 1200 illustrated in FIG. 12 includes a package-on-interposer structure 1236 coupled to the first face 1240 of the circuit board 1202 by coupling components 1216. The coupling components 1216 may electrically and mechanically couple the package-on-interposer structure 1236 to the circuit board 1202, and may include solder balls (as shown in FIG. 12), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0072] The package-on-interposer structure 1236 may include an IC package 1220 coupled to an interposer 1204 by coupling components 1218. The coupling components 1218 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1216. Although a single IC package 1220 is shown in FIG. 12, multiple IC packages may be coupled to the interposer 1204; indeed, additional interposers may be coupled to the interposer 1204. The interposer 1204 may provide an intervening substrate used to bridge the circuit board 1202 and the IC package 1220. The IC package 1220 may be or include, for example, a die (the die 1002 of FIG. 10B), an IC device (e.g., the IC device 1100 of FIG. 11), or any other suitable component. Generally, the interposer 1204 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1204 may couple the IC package 1220 (e.g., a die) to a ball grid array (BGA) of the coupling components 1216 for coupling to the circuit board 1202. In the embodiment illustrated in FIG. 12, the IC package 1220 and the circuit board 1202 are attached to opposing sides of the interposer 1204; in other embodiments, the IC package 1220 and the circuit board 1202 may be attached to a same side of the interposer 1204. In some embodiments, three or more components may be interconnected by way of the interposer 1204.

[0073] The interposer 1204 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 1204 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1204 may include metal interconnects 1208 and vias 1210, including but not limited to through-silicon vias (TSVs) 1206. The interposer 1204 may further include embedded devices 1214, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1204. The package-on-interposer structure 1236 may take the form of any of the package-on-interposer structures known in the art.

[0074] The IC device assembly 1200 may include an IC package 1224 coupled to the first face 1240 of the circuit board 1202 by coupling components 1222. The coupling components 1222 may take the form of any of the embodiments discussed above with reference to the coupling components 1216, and the IC package 1224 may take the form of any of the embodiments discussed above with reference to the IC package 1220.

[0075] The IC device assembly 1200 illustrated in FIG. 12 includes a package-on-package structure 1234 coupled to the second face 1242 of the circuit board 1202 by coupling components 1228. The package-on-package structure 1234 may include an IC package 1226 and an IC package 1232 coupled together by coupling components 1230 such that the IC package 1226 is disposed between the circuit board 1202 and the IC package 1232. The coupling components 1228 and 1230 may take the form of any of the embodiments of the coupling components 1216 discussed above, and the IC packages 1226 and 1232 may take the form of any of the embodiments of the IC package 1220 discussed above. The package-on-package structure 1234 may be configured in accordance with any of the package-on-package structures known in the art.

[0076] FIG. 13 is a block diagram of an example computing device 1300 that may include one or more components processed using the CMP systems and techniques disclosed herein. For example, any suitable ones of the components of the computing device 1300 may include a die (e.g., the die 1002 (FIG. 10B)) processed using the CMP systems and techniques disclosed herein. A number of components are illustrated in FIG. 13 as included in the computing device 1300, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 1300 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0077] Additionally, in various embodiments, the computing device 1300 may not include one or more of the components illustrated in FIG. 13, but the computing device 1300 may include interface circuitry for coupling to the one or more components. For example, the computing device 1300 may not include a display device 1306, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 1306 may be coupled. In another set of examples, the computing device 1300 may not include an audio input device 1324 or an audio output device 1308, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 1324 or audio output device 1308 may be coupled.

[0078] The computing device 1300 may include a processing device 1302 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any

device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 1302 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 1300 may include a memory 1304, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 1304 may include memory that shares a die with the processing device 1302. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0079] In some embodiments, the computing device 1300 may include a communication chip 1312 (e.g., one or more communication chips). For example, the communication chip 1312 may be configured for managing wireless communications for the transfer of data to and from the computing device 1300. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0080] The communication chip 1312 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultra mobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 1312 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 1312 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip

1312 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 1312 may operate in accordance with other wireless protocols in other embodiments. The computing device 1300 may include an antenna 1322 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0081] In some embodiments, the communication chip 1312 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 1312 may include multiple communication chips. For instance, a first communication chip 1312 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1312 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 1312 may be dedicated to wireless communications, and a second communication chip 1312 may be dedicated to wired communications.

[0082] The computing device 1300 may include battery/power circuitry 1314. The battery/power circuitry 1314 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the computing device 1300 to an energy source separate from the computing device 1300 (e.g., AC line power).

[0083] The computing device 1300 may include a display device 1306 (or corresponding interface circuitry, as discussed above). The display device 1306 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0084] The computing device 1300 may include an audio output device 1308 (or corresponding interface circuitry, as discussed above). The audio output device 1308 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0085] The computing device 1300 may include an audio input device 1324 (or corresponding interface circuitry, as discussed above). The audio input device 1324 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0086] The computing device 1300 may include a global positioning system (GPS) device 1318 (or corresponding interface circuitry, as discussed above). The GPS device 1318 may be in

communication with a satellite-based system and may receive a location of the computing device 1300, as known in the art.

[0087] The computing device 1300 may include an other output device 1310 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1310 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0088] The computing device 1300 may include an other input device 1320 (or corresponding interface circuitry, as discussed above). Examples of the other input device 1320 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0089] The computing device 1300 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultra-mobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 1300 may be any other electronic device that processes data.

[0090] The following paragraphs provide various examples of the embodiments disclosed herein.

[0091] Example 1 is a chemical mechanical polishing (CMP) conditioning disk, including: a support; a first pedestal extending from the support, the first pedestal having a first surface roughness (SR); and a second pedestal extending from the support, the second pedestal having a second SR different from the first SR.

[0092] Example 2 may include the subject matter of Example 1, and may further specify that the first pedestal and the second pedestal each include diamond.

[0093] Example 3 may include the subject matter of Example 2, and may further specify that the first pedestal and the second pedestal each include a diamond film formed by chemical vapor deposition (CVD).

[0094] Example 4 may include the subject matter of any of Examples 1-3, and may further specify that the first and second SRs are average roughnesses, and the second SR is at least 20% greater than the first SR.

[0095] Example 5 may include the subject matter of any of Examples 1-4, and may further specify that the first and second SRs are average roughnesses, and the second SR is at least 30% greater than the first SR.

[0096] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the CMP conditioning disk has a pad cut rate (PCR) between 1 and 15 millimeters/minute.

[0097] Example 7 may include the subject matter of any of Examples 1-6, and may further specify that the first and second pedestals have different shapes.

[0098] Example 8 may include the subject matter of any of Examples 1-7, and may further specify that the first and second pedestals have elongated footprints.

[0099] Example 9 may include the subject matter of any of Examples 1-7, and may further specify that the first pedestal has a circular footprint.

[0100] Example 10 is a chemical mechanical polishing (CMP) system, including: a CMP conditioning disk disposed on a first arm, wherein the CMP conditioning disk includes a first pedestal having a first abrasive material, and a second pedestal having a second abrasive material, and wherein the first abrasive material has a surface roughness (SR) different from an SR of the second abrasive material; and a CMP polishing pad disposed on a second arm; wherein the first and second arms allow the CMP conditioning disk to come into contact with, and rotate relative to, the CMP polishing pad.

[0101] Example 11 may include the subject matter of Example 10, and may further specify that the SR of the second abrasive material is at least 20% greater than the SR of the first abrasive material.

[0102] Example 12 may include the subject matter of Example 11, and may further specify that the SRs of the first and second abrasive materials are average roughnesses.

[0103] Example 13 may include the subject matter of any of Examples 10-12, and may further include a wafer disposed on a third arm, wherein the second and third arms allow the wafer to come into contact with, and rotate relative to, the CMP polishing pad.

[0104] Example 14 may include the subject matter of any of Examples 10-13, and may further specify that the CMP conditioning disk includes at least five pedestals.

[0105] Example 15 may include the subject matter of any of Examples 10-14, and may further specify that the CMP conditioning disk has a pad cut rate (PCR) between 4 and 12 microns/minute.

[0106] Example 16 is a method of manufacturing a chemical mechanical polishing (CMP) conditioning disk, including: providing a support; providing, on the support, a first abrasive material of a first pedestal; and providing, on the support, a second abrasive material; wherein the first abrasive material has a surface roughness (SR) different from the SR of the second abrasive material.

[0107] Example 17 may include the subject matter of Example 16, and may further specify that providing the first abrasive material comprises performing chemical vapor deposition (CVD) of the first abrasive material.

[0108] Example 18 may include the subject matter of Example 17, and may further specify that performing CVD of the first abrasive material comprises performing CVD of the first abrasive material on a raised portion of the support.

[0109] Example 19 may include the subject matter of any of Examples 16-18, and may further specify that the SR of the second abrasive material is at least 10% greater than the SR of the first abrasive material.

[0110] Example 20 may include the subject matter of any of Examples 16-19, and may further specify that the support includes a plurality of raised portions.

[0111] Example 21 may include the subject matter of any of Examples 16-20, and may further specify that the first pedestal and a second pedestal are of the same shape.

[0112] Example 22 is a method, including: bringing a chemical mechanical polishing (CMP) conditioning disk into contact with a CMP polishing pad, wherein the CMP conditioning disk includes a first pedestal having a first surface roughness (SR), and a second pedestal having a second SR different from the first SR; and rotating the CMP conditioning disk to condition the CMP polishing pad.

[0113] Example 23 may include the subject matter of Example 22, and may further specify that the CMP conditioning disk has a pad cut rate (PCR) between 5 and 10 microns/minute.

[0114] Example 24 may include the subject matter of any of Examples 22-23, and may further include translating the CMP conditioning disk, while rotating the CMP conditioning disk, to condition the CMP polishing pad.

[0115] Example 25 may include the subject matter of any of Examples 22-24, and may further include using the CMP polishing pad to polish a wafer.

[0116] Example 26 may include the subject matter of any of Examples 22-25, and may further specify that the first and second pedestals include diamond.

[0117] Example 27 is a method, including: bringing the chemical mechanical polishing (CMP) conditioning disk of any of Examples 1-9 into contact with a CMP polishing pad; and rotating the CMP conditioning disk to condition the CMP polishing pad.

Claims:

1. A chemical mechanical polishing (CMP) conditioning disk, comprising:
a support;
a first pedestal extending from the support, the first pedestal having a first surface roughness (SR);
and
a second pedestal extending from the support, the second pedestal having a second SR different from the first SR.
2. The CMP conditioning disk of claim 1, wherein the first pedestal and the second pedestal each include diamond.
3. The CMP conditioning disk of claim 2, wherein the first pedestal and the second pedestal each include a diamond film formed by chemical vapor deposition (CVD).
4. The CMP conditioning disk of claim 1, wherein the first and second SRs are average roughnesses, and the second SR is at least 20% greater than the first SR.
5. The CMP conditioning disk of claim 1, wherein the first and second SRs are average roughnesses, and the second SR is at least 30% greater than the first SR.
6. The CMP conditioning disk of claim 1, wherein the CMP conditioning disk has a pad cut rate (PCR) between 1 and 15 microns/minute.
7. The CMP conditioning disk of any of claims 1-5, wherein the first and second pedestals have different shapes.
8. The CMP conditioning disk of any of claims 1-5, wherein the first and second pedestals have elongated footprints.
9. The CMP conditioning disk of any of claims 1-5, wherein the first pedestal has a circular footprint.
10. A chemical mechanical polishing (CMP) system, comprising:
a CMP conditioning disk disposed on a first arm, wherein the CMP conditioning disk includes a first pedestal having a first abrasive material, and a second pedestal having a second abrasive material, and wherein the first abrasive material has a surface roughness (SR) different from an SR of the second abrasive material; and
a CMP polishing pad disposed on a second arm;
wherein the first and second arms allow the CMP conditioning disk to come into contact with, and rotate relative to, the CMP polishing pad.
11. The CMP system of claim 10, wherein the SR of the second abrasive material is at least 20% greater than the SR of the first abrasive material.
12. The CMP system of claim 11, wherein the SRs of the first and second abrasive materials are average roughnesses.

13. The CMP system of claim 10, further comprising:
a wafer disposed on a third arm, wherein the second and third arms allow the wafer to come into contact with, and rotate relative to, the CMP polishing pad.
14. The CMP system of any of claims 10-13, wherein the CMP conditioning disk includes at least five pedestals.
15. The CMP system of any of claims 10-13, wherein the CMP conditioning disk has a pad cut rate (PCR) between 4 and 12 microns/minute.
16. A method of manufacturing a chemical mechanical polishing (CMP) conditioning disk, comprising:
providing a support;
providing, on the support, a first abrasive material of a first pedestal; and
providing, on the support, a second abrasive material;
wherein the first abrasive material has a surface roughness (SR) different from the SR of the second abrasive material.
17. The method of claim 16, wherein providing the first abrasive material comprises performing chemical vapor deposition (CVD) of the first abrasive material.
18. The method of claim 17, wherein performing CVD of the first abrasive material comprises performing CVD of the first abrasive material on a raised portion of the support.
19. The method of any of claims 16-18, wherein the SR of the second abrasive material is at least 10% greater than the SR of the first abrasive material.
20. The method of any of claims 16-18, wherein the support includes a plurality of raised portions.
21. The method of any of claims 16-18, wherein the first pedestal and a second pedestal are of the same shape.
22. A method, comprising:
bringing a chemical mechanical polishing (CMP) conditioning disk into contact with a CMP polishing pad, wherein the CMP conditioning disk includes a first pedestal having a first surface roughness (SR), and a second pedestal having a second SR different from the first SR; and
rotating the CMP conditioning disk to condition the CMP polishing pad.
23. The method of claim 22, wherein the CMP conditioning disk has a pad cut rate (PCR) between 5 and 10 microns/minute.
24. The method of any of claims 22-23, further comprising:
translating the CMP conditioning disk, while rotating the CMP conditioning disk, to condition the CMP polishing pad.

25. The method of any of claims 22-23, further comprising:
using the CMP polishing pad to polish a wafer.

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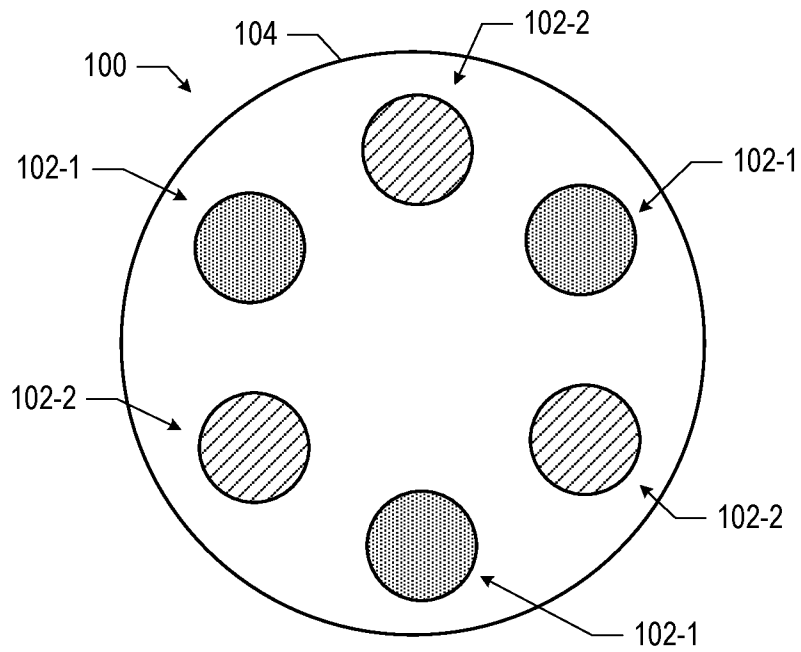


FIG. 1A



FIG. 1B

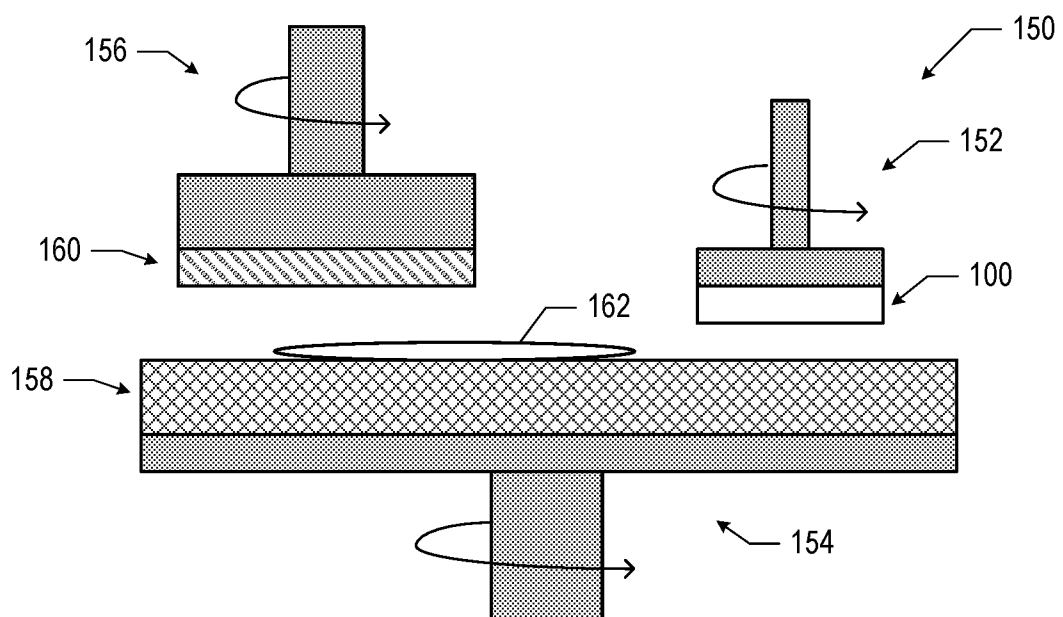


FIG. 2

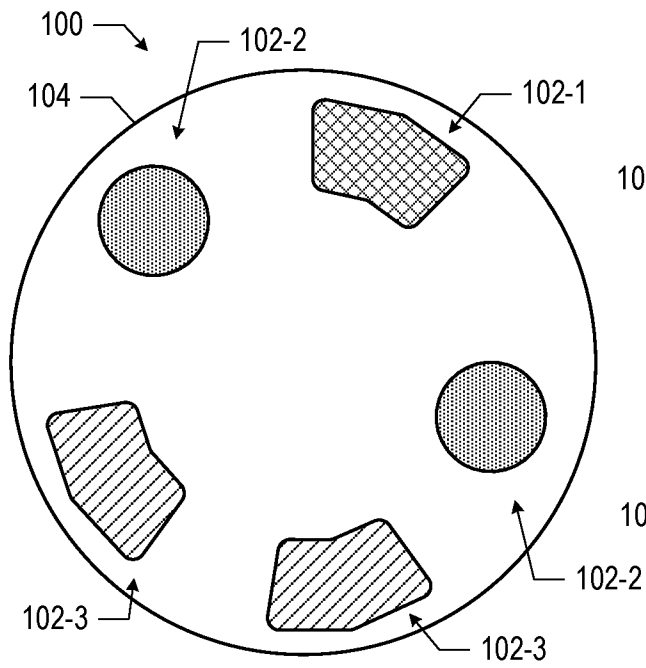


FIG. 3

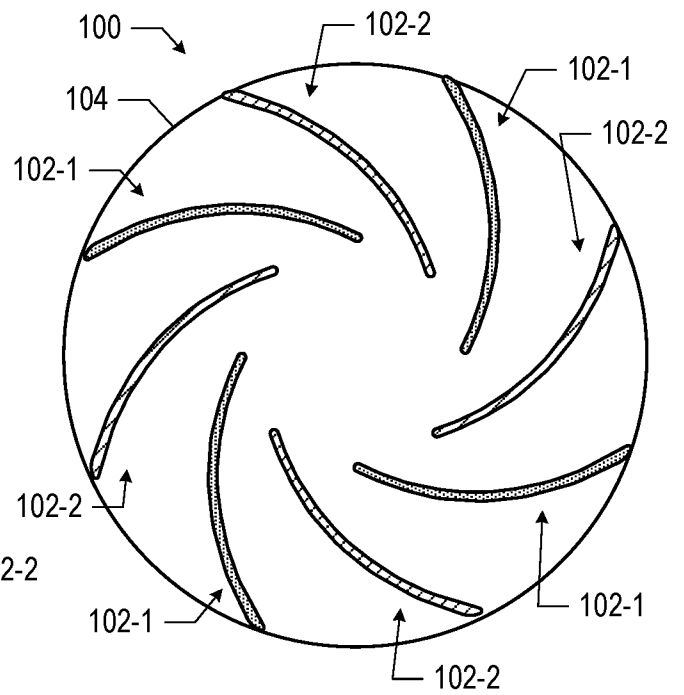


FIG. 4

FIG. 5

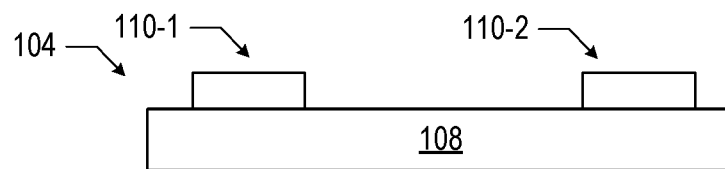


FIG. 6

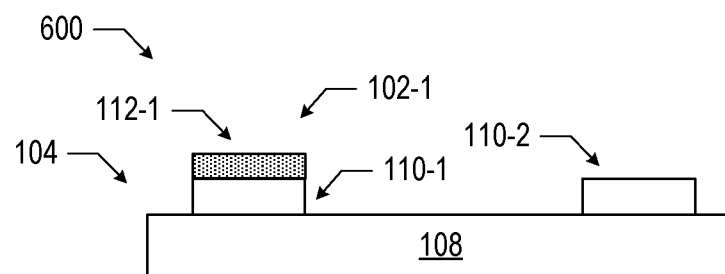
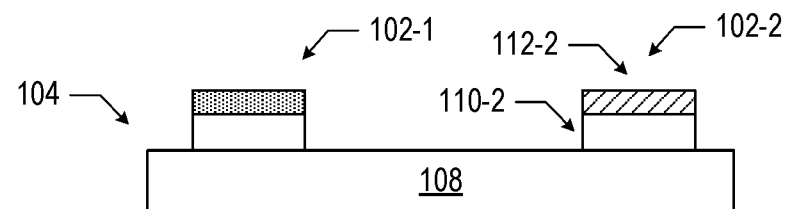


FIG. 7



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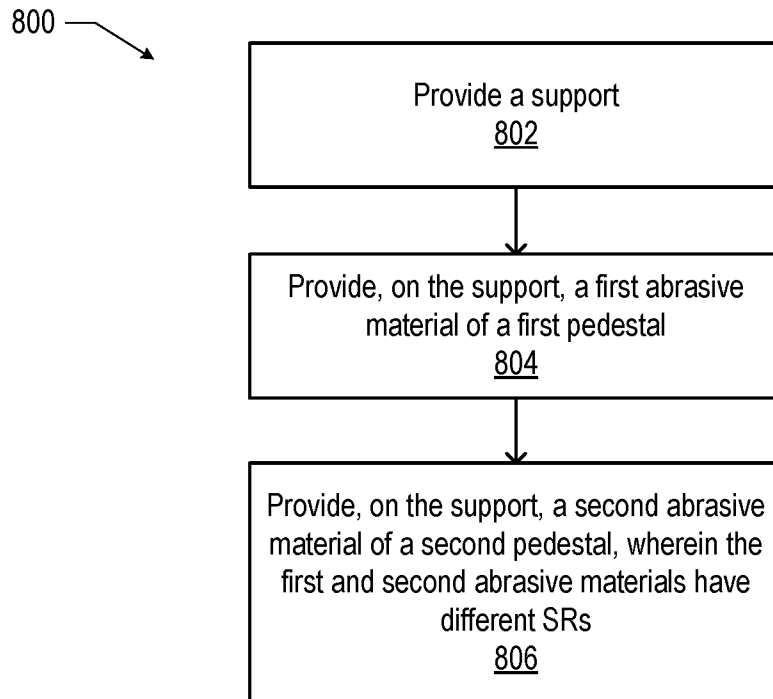


FIG. 8

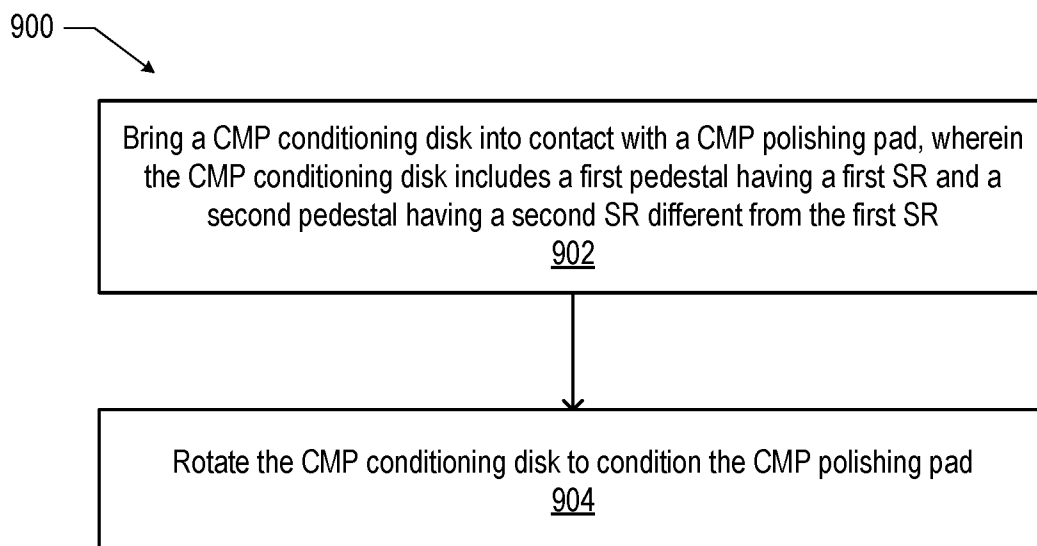


FIG. 9

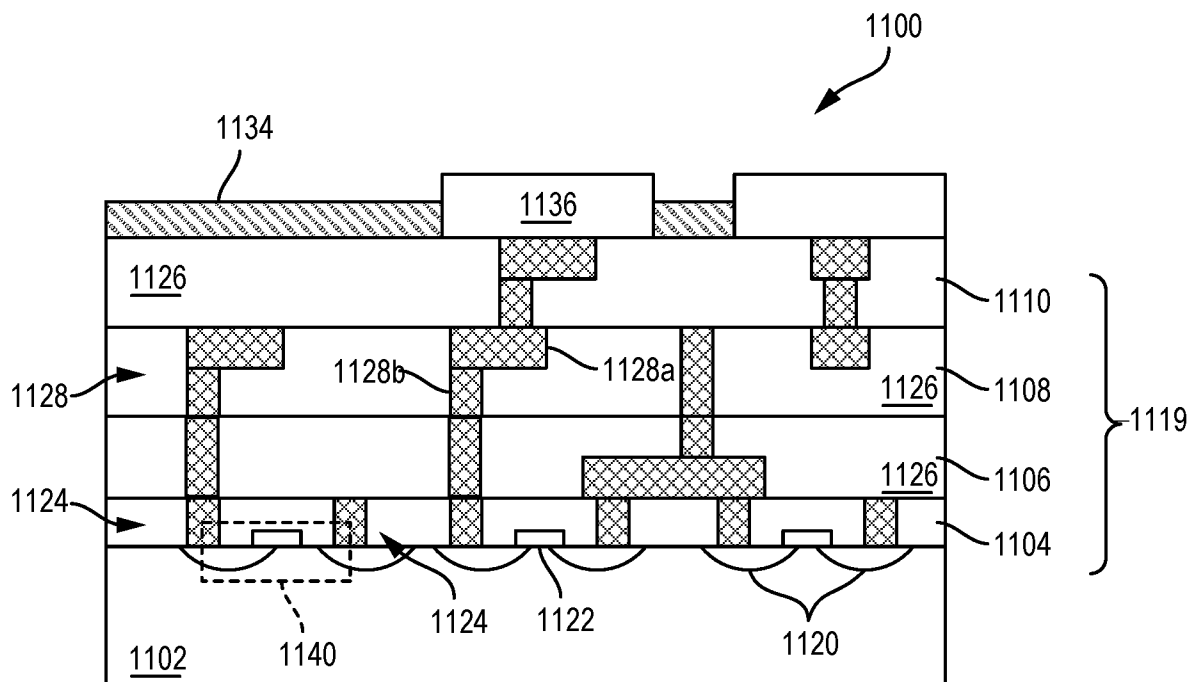
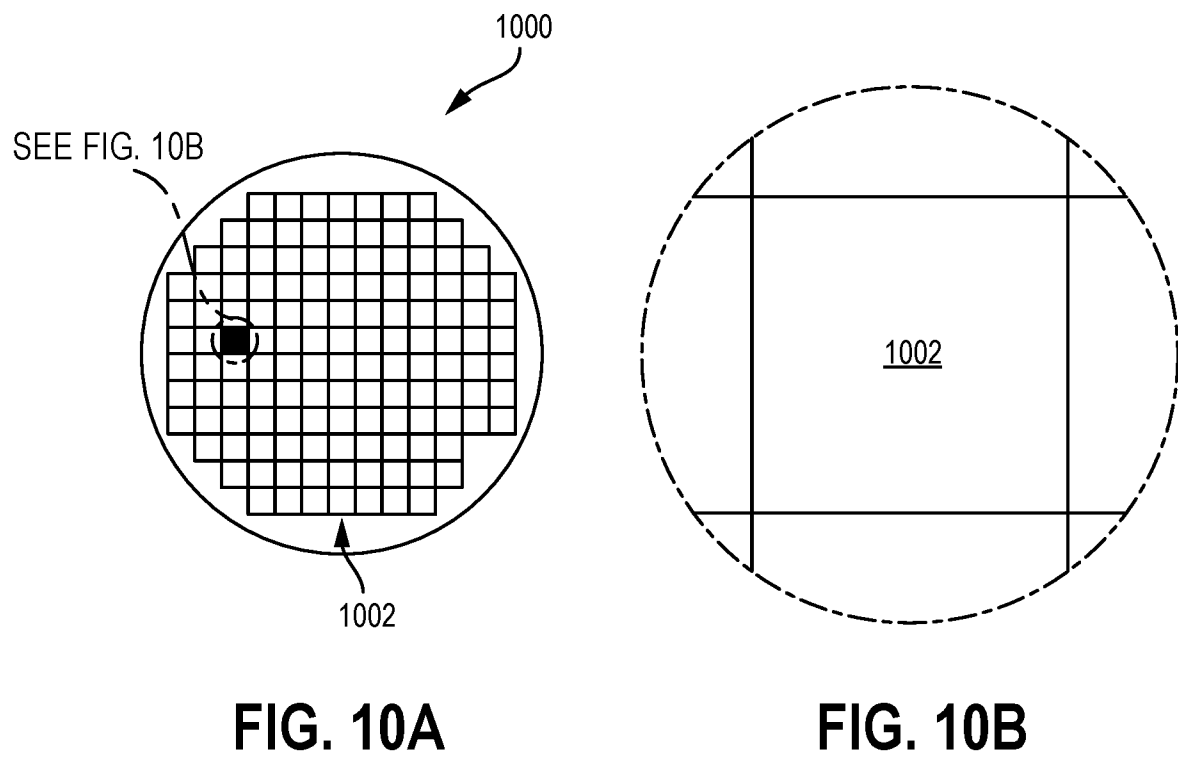


FIG. 11

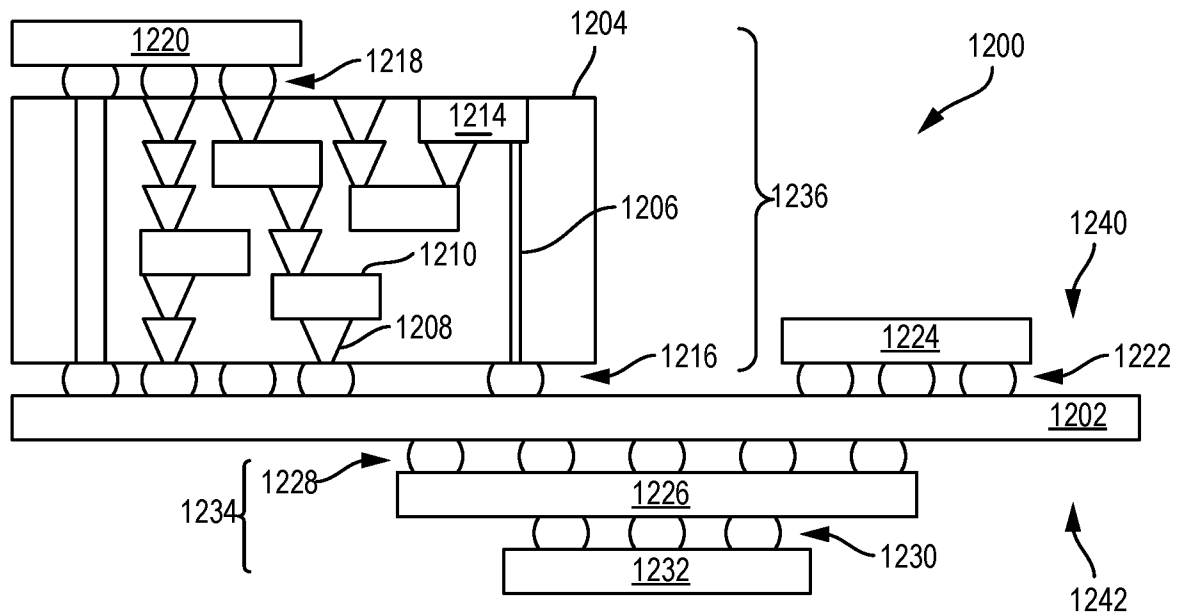


FIG. 12

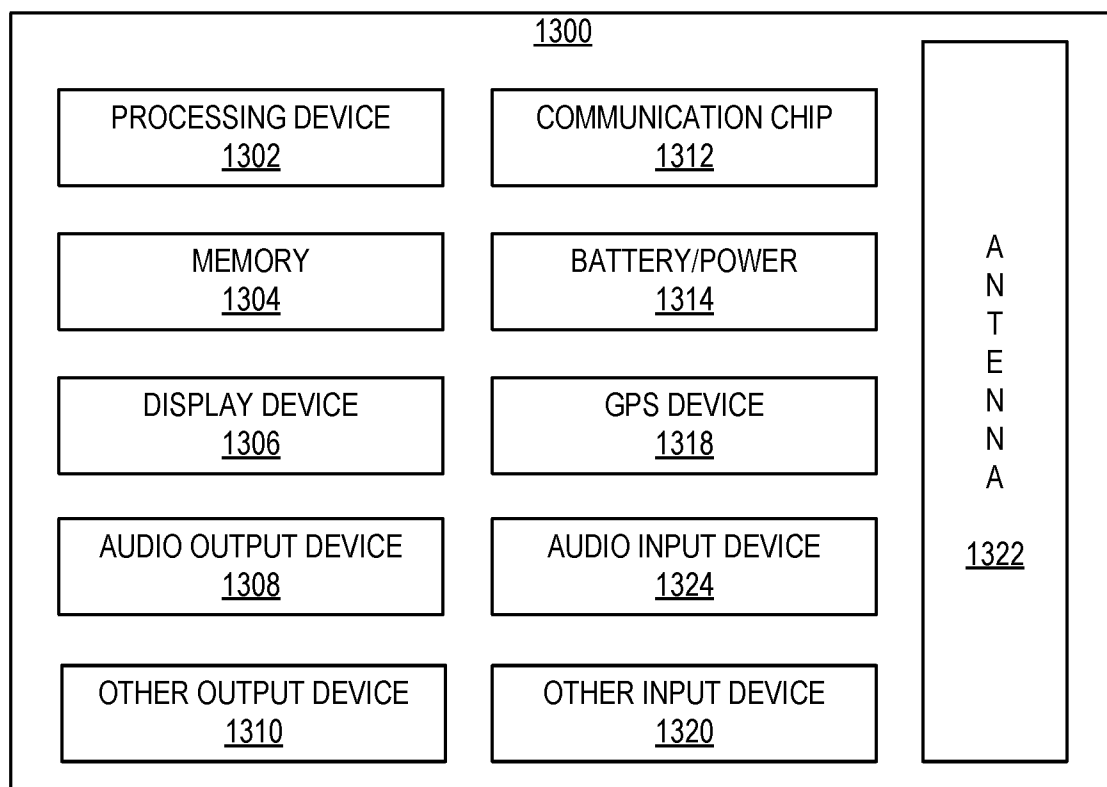


FIG. 13

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/304(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/304; B24B 53/017; B24B 53/00; H01L 21/306; B24B 55/00; B24B 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: CMP, conditioner, pad, head, surface roughness, abrasive material

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014-0113532 A1 (JOSEPH SMITH et al.) 24 April 2014 See paragraphs [0003]-[0007], [0059]-[0087], [0123], claims 1-14, 16, 17 and figures 1, 5A-7F, 17.	1-21
Y		22-25
Y	US 2014-0148008 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 29 May 2014 See paragraph [0019], claim 1 and figure 1.	22-25
A	US 6361414 B1 (MIKE RAVKIN et al.) 26 March 2002 See column 3, line 9 - column 5, line 7, claim 1 and figure 1.	1-25
A	KR 10-2012-0035370 A (SAMSUNG ELECTRONICS CO., LTD.) 16 April 2012 See paragraphs [0020]-[0036], claims 1-4 and figures 1, 2.	1-25
A	US 2004-0203325 A1 (TIMOTHY J. DONOHUE) 14 October 2004 See paragraphs [0023]-[0036], claims 1-16 and figures 1-4.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

11 November 2016 (11.11.2016)

Date of mailing of the international search report

14 November 2016 (14.11.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/019005

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