

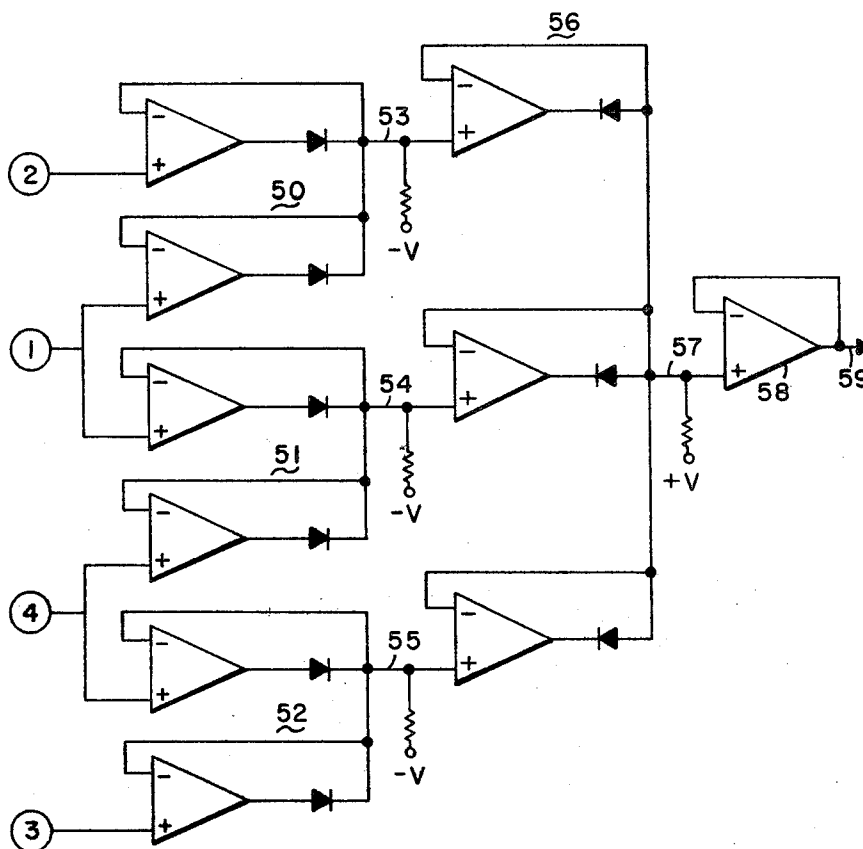
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Assistant Examiner—L. N. Anagnos
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[54] **SIGNAL SELECTOR**
11 Claims, 12 Drawing Figs.
 [52] U.S. Cl..... **307/204,**
 307/219, 307/235, 328/137, 328/147, 328/154
 [51] Int. Cl..... **G06g 11/08,**
 H03k 19/30
 [50] Field of Search..... **307/204,**
 219, 235; 340/146.1, 213; 318/564

ABSTRACT: A signal selecting means to which a plurality of signals of variable amplitude and sign are applied and which develops an output signal corresponding in magnitude and sign to preselected ones, depending on algebraic rank, of the midvalue applied signals, exclusive of the most algebraically positive and negative ones of the input signals. The output signal magnitude is controlled by a predetermined permutation of midvalue selections and in a manner that obviates transients on the output line as control is transferred to the various ones of the midvalue input signals.



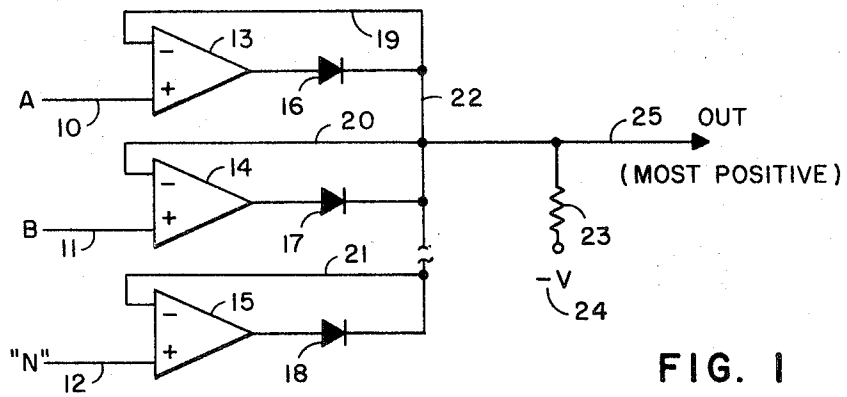


FIG. 1

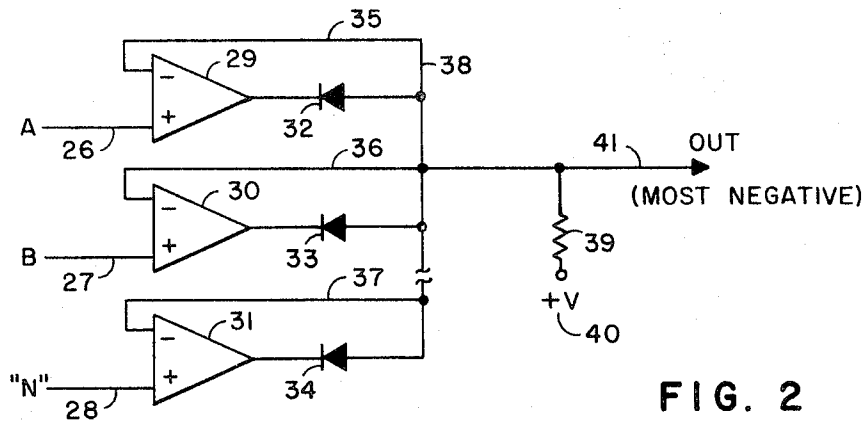


FIG. 2

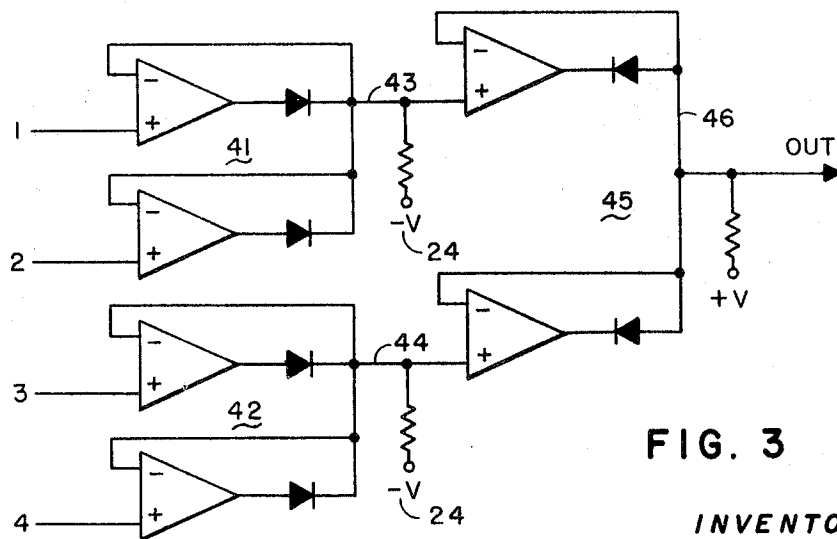
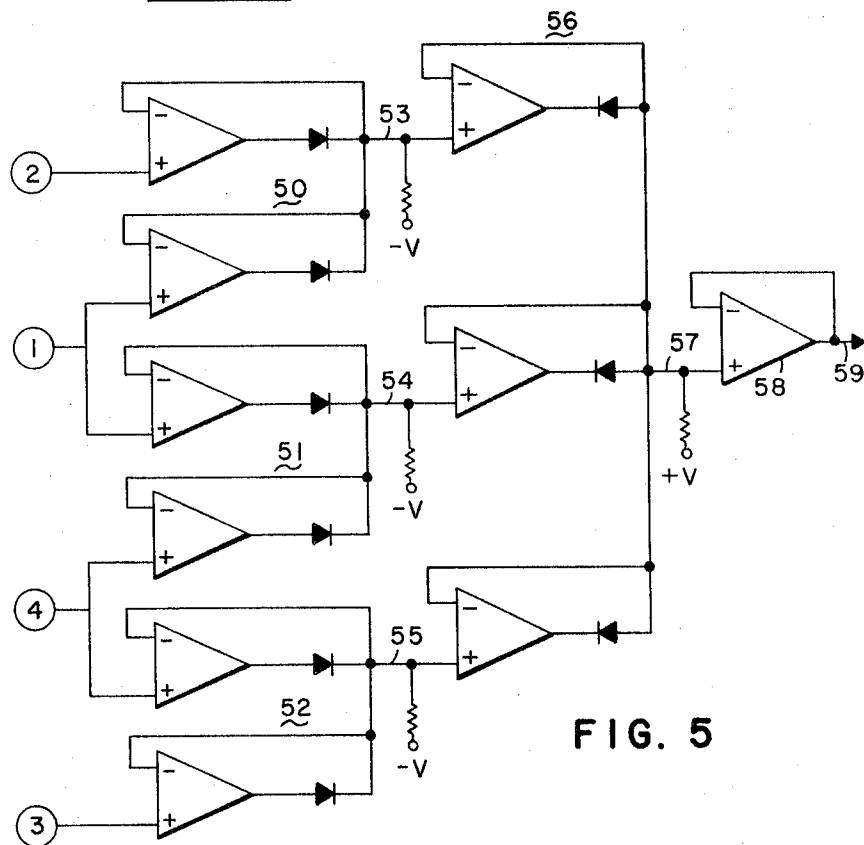
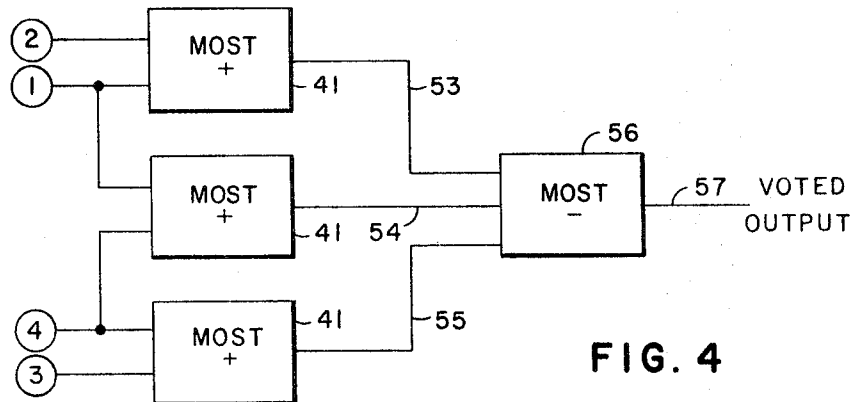


FIG. 3

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MOST +

1	1	2	2	2	2	3	3	3	3	4	4	1	1	1	1	2	2	3	3	4	4	4	4
2	2	1	1	3	3	2	2	4	4	3	3	3	3	4	4	4	4	1	1	1	1	2	2
3	4	3	4	1	4	1	4	1	2	1	2	2	4	2	3	1	3	2	4	2	3	1	3
4	3	4	3	4	1	4	1	2	1	2	1	4	2	3	2	3	1	4	2	3	2	3	1

MOST -
ALGEBRAIC
RANK

FIG. 6

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FIG. 6

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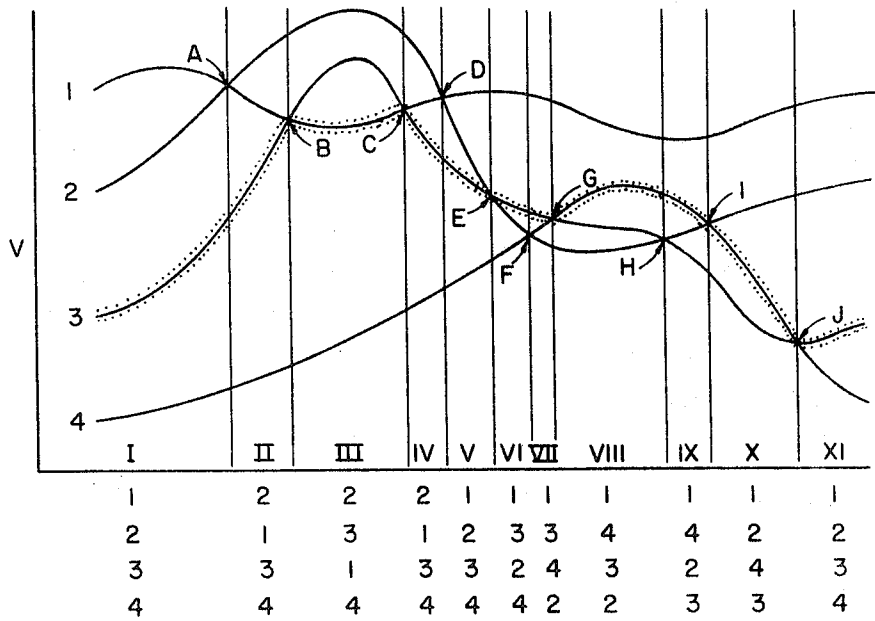


FIG. 7

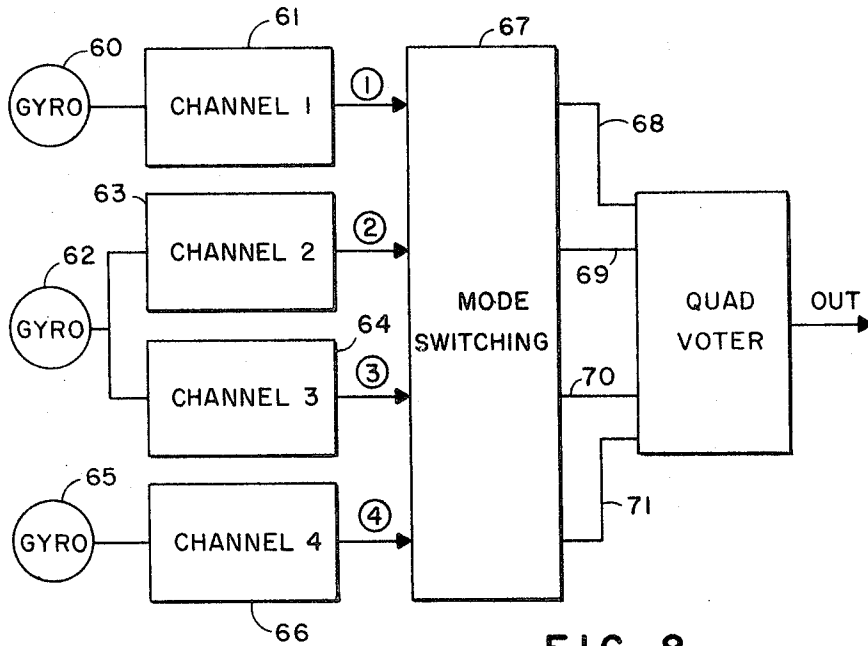


FIG. 8

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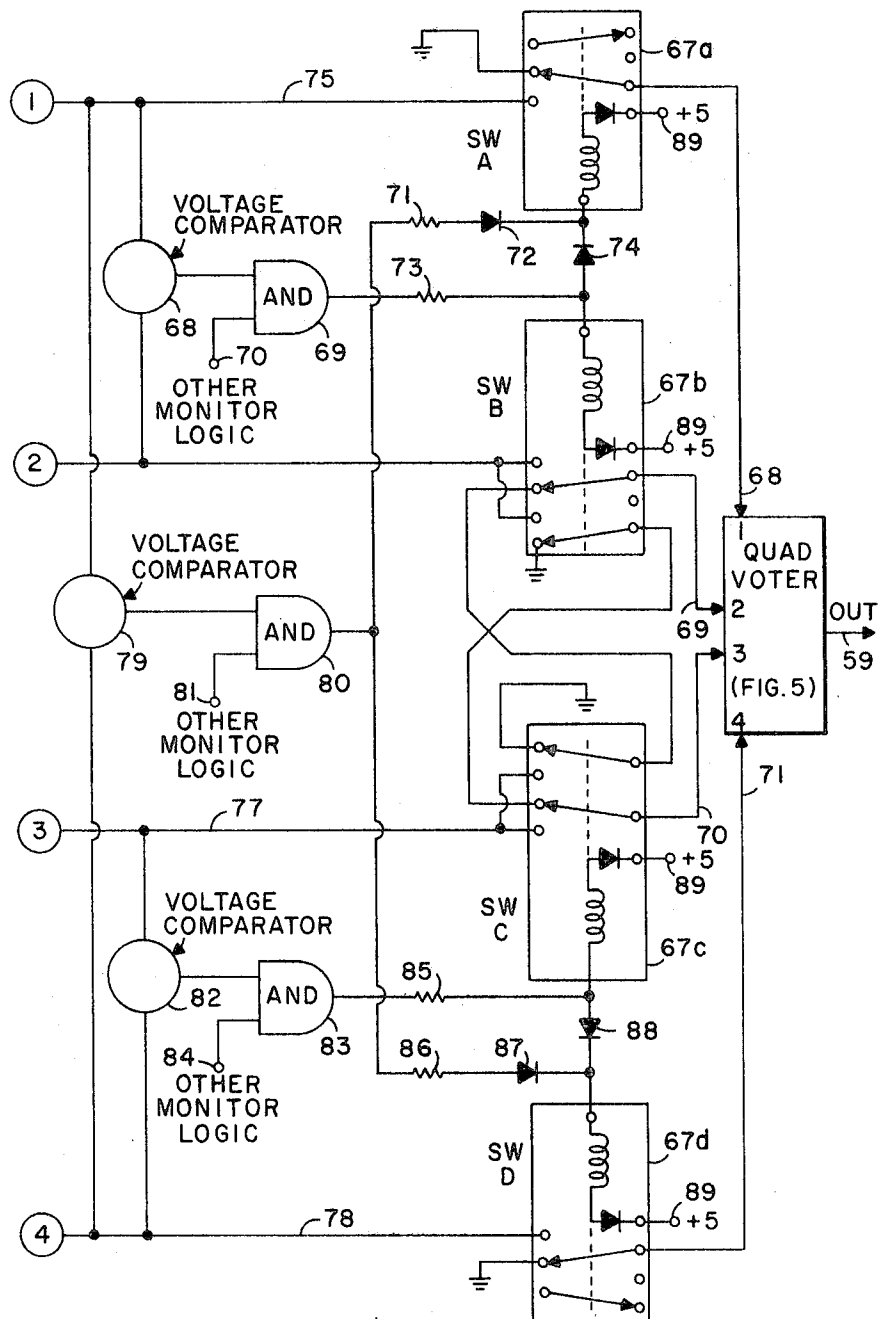
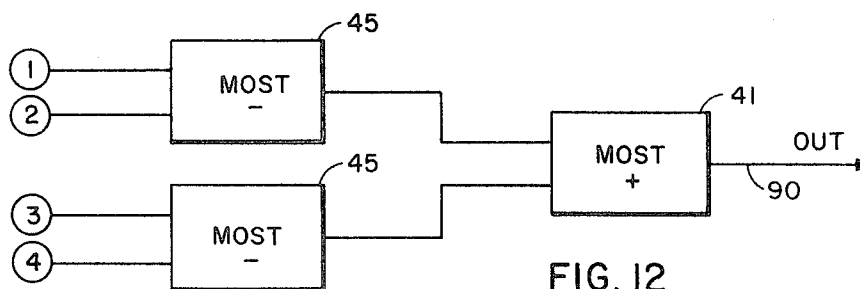
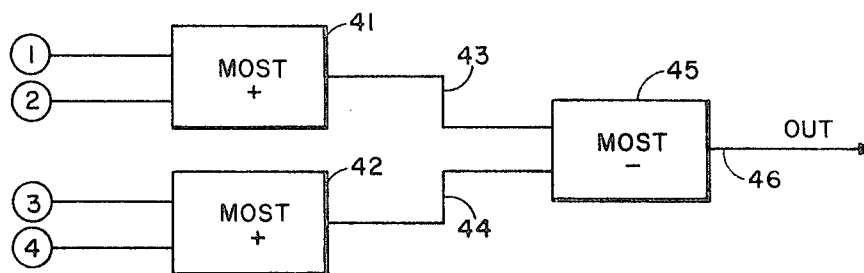
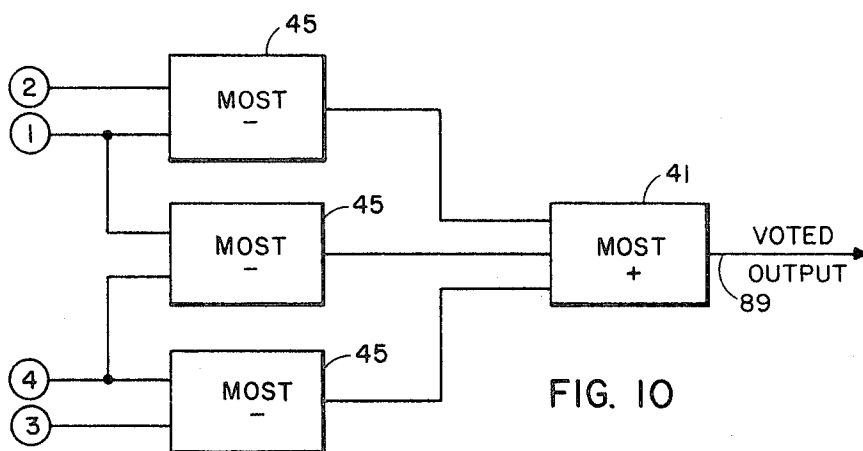


FIG. 9

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SIGNAL SELECTOR

This invention relates generally to signal selection and more particularly to a means for selecting for application on a common output line a particular one of a plurality of input signals whose algebraic rank as concerns relative magnitude lies between the most algebraically positive and the most algebraically negative ones of a plurality of input signals.

The signal selecting means of this invention relates still more particularly to that segment of the art referred to as electronic "voters" wherein a plurality of input signals are applied to a translating means and a particular one of the input signals is applied to a common output line based on a logical selection process—that is, by a process which in some manner eliminates those of the input signals which would be deemed to be unreliable. In the present case the system eliminates the most algebraically extreme signals of a plurality of input signals. For example, the highest or most positive one of a plurality of input signals is prevented from appearing on the output as is the least positive or most negative one of the input signals in an algebraic sense.

The present invention finds special usage in aircraft guidance control systems wherein the demands of current aircraft control problems necessitate the development of redundant command signals. For example, a roll command signal as would be applied to a servosystem to control the ailerons of an aircraft is computed from various input parameters a number of independent or quasi-independent times. The computation thus might comprise four independent computations or in a particular situation, four computations with one or more of the computations being peculiarly dependent on a particular failure such as a common input source employed in the computation. The signal selector or voter is then employed with appropriate logic circuitry to assure that those of the computations exhibiting extreme magnitudes—that is, the highest and the lowest—are prevented from being applied to the aircraft control servosystem so as to prevent intolerable "hard-over" control situations.

The present invention is featured in the provision of a signal selecting means to which a plurality of signals are applied and which assures that those of the input signals exhibiting the extremes in magnitude in an algebraic sense are prevented from being coupled to the output. The object of the present invention is accordingly the provision of an electronic signal selector to which a plurality of signals are applied and which will automatically "elect" one of the midvalue signals of a plurality of input signals being applied and which excludes those of the input signals whose magnitudes represent the algebraic extremes of the plurality of input signals.

A further object of the present invention is to provide a signal translating means to prevent the highest and the lowest ones of a plurality of signals from being translated to a common output line and wherein the output line exhibits at all times a magnitude corresponding to one of the midvalue signal magnitudes of the plurality of input signals and which automatically "switches" between predetermined midvalue ones of the input signals in a manner preventing switching transients from appearing on the common output line.

The present invention is featured in a unique utilization of differential operational amplifiers in two basic circuitries which respectively pass the most positive one of a plurality of input signals and the most negative one of a plurality of input signals so as to eliminate the magnitude extremes from the output.

The present invention is further featured in a means whereby basic mode of operation is based on all input signals being deemed reliable, with lesser sophisticated modes of operation being instituted upon failure of one or more of the input signals to automatically convert the electing system. The lesser sophisticated, yet logically reliable, means of electing the best available computed control signal assures continued automatic operation.

These and other features and objects of the present invention will become apparent upon reading the following description in conjunction with the accompanying drawings in which:

FIG. 1 is a functional diagram of a basic signal translating means as employed in the present invention by means of which the most algebraically positive one of a plurality of input signals is translated to a common output line;

FIG. 2 is a basic functional diagram of a signal translating means as employed in the present invention by means of which the most algebraically negative one of a plurality of input signals is translated to the common output line;

FIG. 3 is a functional diagram of a combination of the signal translating means of FIGS. 1 and 2 into a system providing a selection of one of the midvalue signals of a plurality of input signals exclusive of the most algebraically positive and negative ones of the input signals;

FIG. 4 is a further functional diagram illustrating the application of signal selecting means in a further embodiment so as to select one of the midvalue signals of a plurality of input signals exclusive of the most algebraically positive and negative ones;

FIG. 5 is a functional diagram of a signal translating means in accordance with the present invention by means of which midvalue ones of four input signals are selected in a predetermined selection basis based on comparative algebraic rank of the input signals;

FIG. 6 is a tabular representation illustrating permutations of algebraic ranks of four input signals and the particular midvalue elections made in accordance with the circuitry of FIG. 5;

FIG. 7 is a graphical representation of four variable input signals illustrating the application of various times of particular ones of two midvalue signals to the common output line;

FIG. 8 is a functional diagram of an overall control system employing four channels and including the selector in accordance with the present invention as combined with a mode switching means;

FIG. 9 is a functional schematic diagram of a system of mode switching as may be employed in a control system such as outlined in FIG. 8; and

FIGS. 10, 11 and 12 represent further functional diagrams of combinations of signal translators to arrive at midvalue selection in accordance with the present invention.

The present invention functions basically to prevent the application of the extreme ones of a plurality of redundantly computed control signals from being applied to an activator control circuit. The application of this type of circuitry is particularly important in aircraft control where the safety demands of automatically controlled equipment which will bring an aircraft safely to touchdown dictate that control computations be made in a plural sense and that the logically best one of the computed signals is at all times the signal which is effective in actually controlling the aircraft. This philosophy of course eliminates the possibility of "hard-over" signals; that is, extreme magnitude control signals which would cause a violent maneuver from ever being applied to the control circuitry, per se. The system philosophy also enables continued automatic control of the aircraft in the circumstances where one or more of the redundantly computed control signals fail for one reason or another. Accordingly, the present invention will be described with particular emphasis on automatic control of aircraft though it is not to be so limited since the control philosophy would equally be valuable in other types of control systems where continued automatic control is necessary and the application of extreme signals to the actual controlling device is prohibited.

The basic purpose of the present invention then is to eliminate the possibility of the highest and lowest of a plurality of redundantly computed control signals from being effective in the ultimate control and to select predetermined ones of the midvalue signals of the plurality of control signals for actual control application. The invention accordingly will be described in a general sense as to elimination of the highest

and the lowest signal, and also in a specific sense to meet a particular control criteria whereby the election process may be uniquely tailored to provide the logically best control under circumstances where, for one reason or another, one or certain ones of the input signals may not be given a full "vote" from a reliability standpoint due to a particular system configuration.

FIG. 1 illustrates a basic functional system in accordance with the invention by means of which the most algebraically positive one of a plurality of input signals is applied to a common output line in a manner analogous to continuously switching the most positive one of a plurality of input signals to the output lines but in a manner which prevents switching transients, the latter function being accomplished by a novel electronic "switching" selection process wherein the output is caused to assume a potential corresponding to that of the most positive one of the plurality of input signals at any instant in time. The "switching" is so accomplished that a newly "elected" input signal is applied to the output line at that time when its potential is equal to that of the preceding or last selected one of the input signals, thus obviating any switching transient.

With reference to FIG. 1, a "most positive" signal selector is illustrated as comprising a plurality of differential operational amplifiers 13, 14 and 15, first inputs 10, 11 and 12 to which comprise input signals A, B and "N." The output of each of these differential amplifiers is connected through a diode member and back to the second input of the differential amplifier. Thus, the output of differential amplifier 13 is connected to the anode electrode of a diode 16 the cathode electrode of which is connected to a feedback line 19 as a second input to the differential amplifier. The output from differential amplifier 14 is likewise connected to the anode electrode of a further diode 17 the cathode electrode of which is connected to a feedback line 20 as a second input to amplifier 14. The output from differential amplifier 15 is likewise connected to the anode electrode of diode member 18 the cathode electrode of which is connected through a feedback line 21 as a second input to amplifier 15. The feedback lines 19, 20, 21, which function as the second inputs to the respective differential amplifiers, are connected in common by means of a line 22. The figure illustrates that any number of input signals including a first signal A and a last signal "N" may be likewise connected into circuit, with all the operational amplifiers having their second inputs connected in common by means of line 22. Line 22 is connected through a common resistive member 23 to a negative DC voltage source 24 and the common output line 22 constitutes the output 25 of the signal selector.

The differential operational amplifiers 13, 14, and 15 of FIG. 1 are connected in a voltage follower configuration each having the output fed back to the input with the feedback taken around each of the diode members to eliminate the effect of the diode voltage drop. The inputs indicated "+" and "-" are respective noninverting and inverting terminals. In operation the diodes 16, 17, and 18 are so polarized in conjunction with the negative DC source 24 that the output line 22 assumes the potential of the most algebraically positive one of the input signals 10, 11, and 12 at any instant in time. The input signal 11 is less in magnitude than the DC voltage 24. For example, the source 24 might be -12 volts and the input signal variable between ± 8 volts. The very slightest differential between the two inputs forces the differential amplifiers into saturation due to the extremely high gain of the amplifier. Thus, in operation the most positive input signal controls the instantaneous potential of line 22 since those input signals of a lesser positive amplitude force their associated amplifier into negative saturation due to a maintained differential between the "+" and "-" input terminals while variations in the inputs of lesser magnitudes are not effective in changing total output current. Variations in the most positive input cause the common line voltage to vary accordingly since the associated differential amplifier here operates as an instantaneous voltage follower and does not saturate with application of input signal within its operating range.

FIG. 2 illustrates a further basic functional element of the present invention as a signal development means which applies the most algebraically negative one of a plurality of input signals to a common output line. The circuitry is similar in configuration to that of FIG. 1 with the exception that the diode members are oppositely polarized with respect to the differential amplifier outputs and the common DC source is positive rather than negative. The operation is similar though in this case the output line assumes the potential of the least algebraically positive or most negative one of the input signals.

With reference to FIG. 2, input signals 26, 27, and 28 are the first inputs to associated differential amplifiers 29, 30, and 31. The outputs of the amplifiers are taken through diode members 32, 33, and 34, respectively, and through feedback lines 35, 36, and 37, respectively, as second inputs to the associated differential amplifiers. The common connection 38 interconnects all of the second inputs of the differential amplifiers. The common line 38 is connected through a common resistive member 39 to a positive DC voltage source 40, the magnitude of which exceeds the operational range of the differential amplifiers, and the output 41 then assumes a potential instantaneously equal to the most negative one of the input signals 26, 27, and 28. In this instance the current flow situation is reversed and hence the diode members 32, 33, and 34 are connected in circuit with reversed polarity as compared to those of FIG. 1. In a fashion similar to the configuration of FIG. 1, any number of inputs may be connected in like manner each sharing the common output line 38.

FIG. 3 illustrates a combination of the circuitries of FIG. 1 and FIG. 2 into a functional system wherein the output is at all times made to correspond in potential to one of the midvalue ones of a plurality of input signals, in this instance four input signals being applied. In accordance with the present invention the input signals 1, 2, 3, and 4 are applied in pairs to signal development means 41 and 42 each of which is configured in accordance with FIG. 1 and thus selects at all times the most algebraically positive one of the input signals. Inputs 1 and 2 are applied to signal development means 41 as respective first inputs to first and second differential amplifiers. The common line 43 connecting the second feedback lines to the differential amplifiers is thus maintained at a potential corresponding to the most positive one of input signals 1 and 2. Likewise, the remaining pair of input signals, inputs 3 and 4, are applied as respective first inputs to a further pair of operational differential amplifiers in a signal development means 42 which functions to apply the most algebraically positive ones of input signals 3 and 4 to a common line 44. The lines 43 and 44 are thus collectively devoid of the most negative one of the input signals 1, 2, 3, and 4. Lines 43 and 44 are connected as respective first inputs to a further pair of differential operational amplifiers employed in a signal development means 45 which operates in accordance with the circuitry of FIG. 2 and selects on a common output line 46 that one of the input signals 43 and 44 which is instantaneously most algebraically negative. The circuitry 45 eliminates the most positive one of the input signals 43 and 44 and the output taken from the common line 46 of circuit 45 is thus devoid of both the most algebraically positive and the least algebraically positive ones of the four input signals 1, 2, 3, and 4. As will be further discussed, four input signals of varying magnitude may be ranked in 24 permutations and the output 46 of FIG. 3 will at all times select a predetermined one of the two midvalue input signals for each of the 24 permutations of algebraic rank. The output thus eliminates the most positive and the most negative one of the input signals and assures that one of the two midvalue signals is applied to the output for subsequent control purposes.

The operation of circuitry of FIG. 3 is seen to include a comparison or election between pairs of the input signals followed by a subsequent comparison or election between the outputs of the first two elections. All four of the input signals are seen to be included in the pairs of input signals for the first election process. The circuitry of FIG. 3 is shown in a more functional sense in FIG. 11 wherein signals 1 and 2 are applied

to the circuitry 41 for selection of the most positive one on line 43 and signals 3 and 4 are applied to circuitry 42 for selection of the most positive one on line 44, with subsequent application of the signals on lines 43 and 44 to a circuitry 45 to select the most negative one of the signals on lines 43 and 44 for application to output line 46.

FIG. 12 illustrates a further embodiment wherein the same signal pairs; that is, 1-2 and 3-4 are applied first to circuitries 45 to select the most negative one of the associated input signals, followed by the application of the most negative one of each of the two comparisons to a circuitry 41 which selects the most positive one for application to the output line 90. It is to be realized that in either of these embodiments, the output is devoid of the most algebraically positive and most algebraically negative ones of the input signals 1, 2, 3, and 4. It may be shown that each of the circuits selects one of the two midvalue signals but each selects a particular permutation of the midvalue signals for each of the 24 possible permutations of algebraic rank defined by the four inputs. Further, although not specifically illustrated, the basic function of midterm selection may be accomplished by other discrete pairs of input signals than the 1-2 and 3-4 pairs described thus far. For example, 1-4 and 2-3 may comprise the signal pairs first compared in each of the embodiments of FIG. 11 and FIG. 12, it being understood that the output remains one of the midvalue signals exclusive of the most algebraically positive and negative ones of the inputs, although again a slightly different selection logic for each of the particular possible algebraic ranks of the input signals is realized.

Therefore, whether input signal pairs are first applied to a "most positive" selecting circuit and the outputs of these circuits applied subsequently to a "most negative" selector, or vice versa, the output is still at all times one of the midvalue input signals. Still further, whether the input pairs comprise one particular combination or another, the circuitry of both the embodiments of FIGS. 11 and 12 functions to provide a midvalue output. In each of the particular permutations of the basic circuitry, a peculiarly different permutation as to the selected one of the two midterm values is realized. In a situation where four inputs may be logically voted on with equal emphasis, it is apparent that the basic embodiments of FIGS. 11 and 12 function equally well, and as to the choice of signal comparisons, the pairs of signals should include all four input signals at least once.

FIG. 4 illustrates a further slightly more involved embodiment employing the above-described principles wherein three particular signal pairs are applied to three circuitries each of which selects the most positive with subsequent selection of the most negative one of the outputs from the first comparisons. With reference to FIG. 4, input signals 1 and 2 are applied to a signal development circuitry 41 (as illustrated in FIG. 3) while the combination of inputs 1 and 4 is applied to a further circuitry 41 and finally a third combination of input signals 3-4 is applied to a third circuitry 41. Output lines 53, 54, and 55 from the three "most positive" selectors are applied as respective inputs to a "most negative" selector 56 to develop an output 57. As in the previously discussed cases, the voted output 57 is again devoid of the most algebraically positive and most algebraically negative ones of the input signals 1, 2, 3, and 4, and one of the two midvalue inputs is applied to the output line 57 for each of the 24 possible permutations of algebraic rank of the input signals.

Reference is made to FIG. 5 wherein a functional diagram of the arrangement of FIG. 4 is shown in more detail. Signals 1 and 2 are applied as first inputs to the differential operational amplifiers associated with a first signal development means 41. Signals 1 and 4 are seen to be applied as respective first inputs to the differential operational amplifiers associated with a further first signal development means 41 and finally input signals 3 and 4 are applied as respective first inputs to the differential operational amplifiers to a third signal development means 41. The output lines 53, 54 and 55 carry the most positive one of the signal pair applied to the particular preceding

circuitries. Output lines 53, 54, 55 are in turn applied as first inputs to a further plurality of differential operational amplifiers which form a "most negative" selecting circuitry to develop output 57 which corresponds to one of the midvalue signals of the input signals 1, 2, 3 and 4.

The election as to midvalue signals realized from the circuitry of FIG. 5 is illustrated graphically in the table of FIG. 6. The 24 possible permutations as to algebraic rank of input signals 1, 2, 3 and 4 are illustrated with the top number of each column representing the most algebraically positive one of the input signals with subsequent inputs in each column representing descending algebraic rank to the least algebraically positive (or most algebraically negative) one on the bottom of each column. The particular signal selected for application to the output line 57 is illustrated in the boxed portions. It is to be realized that the previously discussed embodiments likewise would choose one or the other of the midvalue inputs illustrated in the table of FIG. 6 but not the particular selections as shown in FIG. 6.

The particular embodiment of FIG. 5 is uniquely adaptable to a particular voting requirement wherein inputs 2 and 3 may stem from computations which have a vulnerability to a common failure. FIG. 8 illustrates such a situation with four signals computed in channels 61, 63, 64 and 66, and among the computations of each of the channels may be a gyro input as from gyro 60 to channel 61 and gyro 65 to channel 66. Note, however, that the two midchannels which produce the control signals 2 and 3 include in the computations the output from a shared or common gyro 62. In this instance, should the gyro fail, both channels 63 and 64 and thus control signals 2 and 3 may exhibit simultaneous "hard-over" conditions. For this reason in a system as depicted in FIG. 8, it would not be logically permissible to include in a voting or election process any direct comparison or election between signals 2 and 3. Further, if signals 2 and 3 would ever be the two most positive or the two most negative ones of a particular algebraic rank permutation, it would be inadvisable to select either one of the signals 2 or 3 for ultimate control since the condition may stem from a common failure due to the common gyro 62.

Referring again to table 6, for all 24 permutations of algebraic rank of the input signals 1-4, the selected one of the two midvalue signals is never 2 or 3 when the particular rank places 2 and 3 as the two most positive or the two most negative ones of the four input signals. The election illustrated in FIG. 6, as accomplished by the embodiment of FIG. 5, is thus a logically best election process as concerns a system requirement as illustrated in FIG. 8. Again, should all four channels of computation be completely independent, each could be given an equal "vote" under all circumstances and a lesser complicated embodiment such as previously discussed with respect to FIGS. 3, 11 and 12 could be employed to select an arbitrary combination of midvalue signals.

It can be further shown with reference to FIG. 10 that the same combinations employed in the embodiment of FIG. 5 as to input signal pairs may be applied first to "most negative" selectors followed by a "most positive" election process. In this case, however, the particular selection of midvalue signals would not agree with the selections shown in FIG. 6 but would, in fact, still fit the particular requirement of the FIG. 8 embodiment.

It may further be shown that other permutations of input signal pairs could be applied to the embodiment of FIG. 5 and in each case a peculiarly different permutation of elected ones of the midvalue signals would be effected, each of which would fail in one or more cases to meet the particular requirement of the FIG. 8 configuration. In all cases, however, the input pair must include all of the input signals at least once and, generally speaking, the FIG. 3 or FIG. 12 embodiments represent the simplest ways to elect one or the other of the midvalue signals and further pair comparisons of input signals would lead only to further restrictions on which of the midterms may be selected. The inclusion of three signal comparisons as embodied in FIG. 5 was found to be necessary in

order to meet the special requirements inherent in a system as depicted in FIG. 8.

In accordance with the present invention, the operation of the voting processes is somewhat analogous to the switching of a particular one of a plurality of input signals to a common line. The signals are not actually "switched;" rather, the output line is maintained at a potential in correspondence with a particular one of the input signals. The control of the output signal as it changes from that defined by one or the other of the midvalue signals is always changed at such a time that the newly elected or controlling input signal amplitude is already at the potential of the preceding or previously elected one, such that when "switching" occurs, there can be absolutely no switching transient to detrimentally affect the controlled system.

The electing or voting process of the FIG. 5 embodiment may be defined graphically by reference to FIG. 7 in conjunction with the election table of FIG. 6. FIG. 7 represents arbitrarily varying input signals 1, 2, 3, and 4 as a function of time. While FIG. 7, for purposes of illustration, represents all four signals as having the same polarity, a zero reference line may be drawn anywhere through the signals wherein any one or all of the signals may vary from time to time from positive to negative polarity. Emphasis is made of the fact that the election process in accordance with the present invention is based on comparative algebraic rank and the selection is based on the most algebraically positive and/or negative ones of the input signals.

With reference to FIG. 7, the particular ranks of the input signals 1, 2, 3, and 4 are identified by I through XI. In the first rank the signals are ranked 1-2-3-4 and, according to the election table of FIG. 6, input signal 3 is selected which happens to be the lower one of the two midvalue terms. Note that at point A in FIG. 7, input signals 1 and 2 change in rank while signals 3 and 4 remain in the same relative rank so as to define a rank 2-1-3-4. With reference to FIG. 6, the algebraic rank 2-1-3-4 likewise elects signal 3. At point B the rank changes again as signal 3 rises above signal 1. This defines a rank of 2-3-1-4 which elects input signal 1. At point C a further interchange is made to define a rank of 2-1-3-4 which continues the election of input signal 3. At point D a further change in rank is experienced which reverts the permutation back to rank 1-2-3-4 to continue election of input signal 3. At point E a change to rank 1-3-2-4 is experienced which maintains the election of input signal 3. At F a further change in rank to 1-3-4-2 is experienced which according to the table likewise maintains the election of input signal 3. At point G a change to rank 1-4-3-2 is experienced which causes the election of input signal 4. At point H a change to rank 1-4-3-2 maintains the election of input signal 4. At point I a still further change to rank 1-2-4-3 maintains the selection of input signal 4. At point J a final change in rank back to the original rank 1-2-3-4 again elects input signal 3.

When the election changes from input signal 3 to input signal 1 at point B, the newly elected signal 1 has fallen to a potential equaling that of the previously selected signal 3. The changeover of control thus introduces no transient. A similar situation occurs at each change in rank which effects a different signal selection from that previously selected. The newly selected input signal is always at a potential equaling that of the previously selected one. It is further apparent in FIG. 7 that the output signal from the embodiment of FIG. 5 is always one of the midvalue terms. Further reference shows that during the time period III, where signals 2 and 3 are the two most positive ones of the input signals, signal 3 is a mid-term value but is not elected. Further, in the time period designated by VIII, when signals 2 and 3 are the two most negative ones of the four input signals, signal 3 is not elected.

The discussion thus far has been based on the assumption that all four input signals are "good." A further provision may be made to modify the selection of midterm values to different modes of operation when one or more of the input channels fail. FIG. 8 represents functionally the inclusion of mode

switching means 67 which receives the four input signals and selectively applies the input signals to the Quad Voter in a manner to effect less desirable, but nonetheless operable, operational modes should there be a failure in the input channels. Basically, the mode switching employs a comparator logic which defines one or more channels as being "bad" and eliminates these particular channels from subsequent election processes.

Reference is made to FIG. 9 which illustrates a functional schematic diagram of the mode switching means 67 as it would be connected in circuit between the input signals 1, 2, 3 and 4, and the Quad Voter circuitry such as depicted in FIG. 5.

With reference to FIG. 9 each of the input signals 1, 2, 3 and 4 is selectively applied through a respective switch 67a, 67b, 67c and 67d to the inputs of the Quad Voter in accordance with FIG. 5. In general function each of the input signal pairs which (with reference to FIG. 5) are applied to the first "most positive" elections in the Quad Voter are also applied to a voltage comparator. Signal pair 1-2 is applied to a voltage comparator 68, signal pair 1-4 is applied to a voltage comparator 79, and signal pair 3-4 is applied to a voltage comparator 82. The voltage comparators 68, 79 and 82 produce output signals unless the absolute magnitude difference between the signal pair applied exceeds a predetermined threshold. The outputs from the comparators are applied as first inputs to subsequent AND gates 69, 80 and 83, respectively. Other inputs to the AND gates 70, 81 and 84 might comprise further monitor logic in a given system. The AND gates 69, 80 and 83 develop a positive output signal of predetermined threshold when both the "other monitor logic" inputs 70, 81 and 84, and the associated comparator outputs are both present to indicate "good" conditions.

The switches 67a, 67b, 67c, 67d are illustrated as comprising two single-pole double-throw sections under the control of an energizing solenoid one end of which is connected through a diode to a source 89 of positive DC voltage. The output from each of the AND gates 69, 80 and 83 is applied through a resistive member and a diode member to the other end of one or more of the relay energizing solenoids. The output from AND gate 69 is applied through resistor 73 and diode 74 to the solenoid of switch 67a and through the resistor 73 directly to the solenoid of switch 67b. The output from AND gate 80 is applied through resistor 71 and diode 72 to the energizing solenoid of switch 67a and further through resistor 86 and diode 87 to the energizing solenoid of switch 67d. The output from AND gate 83 is applied through resistor 85 directly to the energizing solenoid of switch 67c and through diode 88 to the energizing solenoid of switch 67d.

The switches in FIG. 9 are depicted in unenergized condition. The output from the AND gates is a positive DC level in excess of the positive DC source 89 and thus, in the presence of an output from the AND gates, the associated switch energizing solenoid or solenoids cause the switches to be energized and closed. Each switch when closed connects the input signal directly to its assigned input terminal of the Quad Voter. Switch 67a when deenergized connects input 1 of the Quad Voter to system ground. The interconnections between switches 67b and 67c are such that when switches 67b and 67c are simultaneously deenergized as pictured, input 2 of the Quad Voter is grounded through switch 67c and input 3 of the Quad Voter is grounded through switch 67b. Under conditions of one or the other of switches 67b and 67c being energized, inputs 2 or 3 are applied to both terminals 2 and 3 of the Quad Voter. For example, if switch 67b is deenergized while switch 67c is energized, input 2 to the Quad Voter receives input signal 3 through an energized position of switch 67c, thus input signal 3 is applied to both inputs 2 and 3 of the Quad Voter. Similarly, when switch 67b is energized and switch 67c is deenergized, input signal 2 is applied to both inputs 2 and 3 of the Quad Voter.

The above-described switching interconnections between the input signals to be voted on and the Quad Voter circuitry

per se are based on a logical selection and substitution process whereby, upon certain voltage comparator "failures," the system may logically be adapted to lesser sophisticated operating modes where the voting is actually done on a midvalue selection basis where three input signals are involved. In some cases three of the four input signals, and in still lesser sophisticated systems, only two of the four input signals together with system ground or other "zero signal" level are used in the election process.

Table I illustrates six operating cases outlining the "good" channels for each of the cases, the particular voting logic that is involved, the permutations of switches actuated for each operating case, and the logical indication of which channel comparators are indicating "good" outputs for each case.

TABLE I

Operating cases	Good channels	Voting logic	Switches actuated	Channel comparators "good"
I.....	1, 2, 3, 4	(Figure 6)	A, B, C, D	1-2, 3-4, 1-4
II.....	1, 2, 4	Mid-value	A, B, D	1-2, 1-4
III.....	1, 3, 4	do.	A, C, D	3-4, 1-4
IV.....	1, 2	Mid-value including zero.	A, B	1-2
V.....	3, 4	do.	C, D	3-4
VI.....	1, 4	do.	A, D	1-4

The "good" channel depicted for each of the operating cases in Table I is based on a logical assumption from the "good" and "bad" particular comparator outputs. Thus, in operating Case 1, which is the case involving all four good channels, all four switches are actuated and all three of the comparators are good, the operation is normal as though the switches were not connected into the circuit and the four inputs were applied directly to the corresponding inputs of the Quad Voter.

Operating Case 2 is based on channel comparators 1-2 and 1-4 being good while 1-3 is bad. This logically leads to the operating case which considers that channel 3 is suspect or bad and thus the voting logic is converted through the switching arrangement to a midvalue selection based on inputs 1, 2 and 4 with switch "c" being deenergized.

Operating Case 3 is based on a good output from comparators 3-4 and 1-4 leading to the logical assumption that channel 2 is suspect or bad and again the voting logic is altered to one of midvalue selection including inputs 1, 3 and 4.

Operating Case 4 is based on a good output from only comparator 1-2. In this case only 1 and 2 of the input signals can be logically considered to be good and due to the introduction of system ground via the switches of FIG. 9, the voting logic converts to a midvalue selection process including system ground, it being realized that the Quad Voter of this invention is algebraic in operation. Thus, in certain cases system ground (or, alternatively "zero signal" level) may be the elected one in operating Case 4 since it could be the midvalue between respective negative and positive input signals on lines 1 and 2.

Similarly, operating Case 5 is based on a good comparator output only from comparator 3-4 wherein only input signals 3 and 4 can logically be considered valid and the voting logic converts to a midvalue selection including system ground or "zero signal" level.

Finally, a sixth operating case is indicated wherein a good output is obtained only from channel comparator 1-4, only input signals 1 and 4 can be considered valid and the system again reverts to a midvalue process including system ground or "zero signal" level.

The present invention is thus seen to provide a novel signal selection circuitry whereby the algebraically extreme ones of a plurality of input signals are excluded from the output and an election process is realized where one of the midvalue ones of the plurality of input signals is selected as an output. The selection is not based on a switching operation, per se, but rather on a common line assuming the potential of predetermined ones of the midvalue terms for each of the algebraic rank permutations defined by the plurality of input signals.

This invention has been described in general terms for operation on a plurality of input signals each carrying equal voting strength and further in terms of a unique particular embodiment for selection of one of the midvalue ones of four input signals where two of the four input signals share some common computation parameter or circuitry such that they are vulnerable to common failure, in which case a system not involving direct comparison of these interdependent channels is described. Additionally lesser sophisticated embodiments are described which are attained automatically by the inclusion of logic switching under the influence of channel comparators whereby input signals logically considered to be unreliable due to the particular permutation of comparator outputs are excluded from the voting process and the voter reverts to an operable but less sophisticated fail-safe system.

Although the present invention has been described with respect to particular embodiments thereof, it is not to be so limited as changes might be made therein which fall within the scope of the invention as defined in the appended claims.

I claim:

1. Signal translating means for selectively applying one of a plurality of input signals to a common output line, comprising a plurality of first signal development means for receiving a predetermined number of pairs of said input signals, said predetermined number of pairs including each of said input signals in at least one pair, each of said first signal development means developing an output corresponding to the instantaneous magnitude of the most algebraically positive one of the signal pair applied thereto, a second signal development means receiving the outputs from said plurality of first signal development means, said second signal development means developing an output corresponding to the instantaneous magnitude of the most algebraically negative one of the signals applied thereto, the output of said second signal development means thereby corresponding to a midvalue one of said input signals exclusive of the most algebraically positive and most algebraically negative ones of said input signals, each of said first signal development means comprises first and second differential operational amplifiers, having first and second input terminals, the signals comprising one of said predetermined pairs of input signals being applied respectively to said first input terminals, the output of each of said differential operational amplifiers being connected to the anode electrode of a unilateral conduction device the cathode electrode of which is connected to the second input terminal of each of said operational amplifier, the second input terminals being connected in common through a common resistive member to a negative direct current voltage source, the aforedefined common interconnection comprising the output from said first signal comparison means, said common interconnection assuming a potential corresponding to the most algebraically positive one of the input signal pair; said second signal development means comprising a further plurality of differential operational amplifiers first inputs to which comprise the respective outputs from said plurality of first signal development means, the output of each of said further differential amplifiers being connected to the cathode electrode of a unilateral conduction device the anode electrode of which is connected as a second input to the associated one of said differential amplifiers, the second inputs of each of said further differential amplifiers being connected in common and through a common resistive member to a positive direct current voltage source, said common interconnection comprising the output from said second signal development means, the output from said second signal development means comprising the least algebraically positive one of the respective input signals thereto.

2. Signal translating means for selectively applying one of a plurality of input signals to a common output line, comprising a plurality of first signal development means for receiving a predetermined number of pairs of said input signals, said predetermined number of pairs including each of said input signals in at least one pair, each of said first signal development means developing an output corresponding to the instan-

aneous magnitude of the most algebraically negative one of the signal pair applied thereto, a second signal development means receiving the outputs from said plurality of first signal development means, said second signal development means developing an output corresponding to the instantaneous magnitude of the most algebraically positive one of the signals applied thereto, the output of said second signal development means thereby corresponding to a midvalue one of said input signals exclusive of the most algebraically positive and most algebraically negative ones of said input signals, each of said first signal development means comprises a pair of differential operational amplifiers each having first and second input terminals, the signals comprising one of said predetermined pairs of input signals being applied respectively to said first input terminals, the output of each of said differential operational amplifiers being connected to the cathode electrode of a unilateral conduction device the anode electrode of which is connected to the second input terminal of said operational amplifier, said second input terminals of each of said differential amplifiers being connected in common and through a common resistive member to a positive direct current voltage source, said common interconnection assuming a potential corresponding to the least algebraically positive one of the input signal pair; said second signal development means comprising a further plurality of differential operational amplifiers first inputs to which comprise the respective outputs from said plurality of first signal development means, the output of each of said further differential operational amplifiers being connected to the anode electrode of a unilateral conduction device the cathode electrode of which is connected as a second input to the associated one of said differential amplifiers, the second input of each of said further operational amplifiers being connected in common and through a common resistive member to a negative direct current voltage source, said common connection comprising the output from said second signal development means and comprising the most algebraically positive one of the respective input signals thereto.

3. Signal translating means for selectively applying one of a plurality of input signals to a common output line, comprising a plurality of first signal development means for receiving a predetermined number of pairs of said input signals, said predetermined number of pairs including each of said input signals in at least one pair, each of said first signal development means developing an output corresponding to the instantaneous magnitude of that one of the signal pair applied exhibiting a first algebraic magnitude extreme, a second signal development means, said second signal development means developing an output corresponding to the instantaneous magnitude of that one of the signals applied thereto exhibiting the opposite algebraic magnitude extreme, the output of said second signal development means thereby corresponding to a midvalue one of said input signals exclusive of the most algebraically positive and most algebraically negative ones of said input signals, said plurality of input signals being four in number and comprising first and second ones of said plurality of first signal development means, the first one of said first signal development means receiving a first pair of said input signals, the second one of said first signal development means receiving a second pair of said input signals, said second signal development means comprising first and second differential amplifiers receiving the outputs from said first and second ones of said first signal development means as respective first inputs thereto.

4. Signal translating means for selectively applying one of a plurality of input signals to a common output line, comprising a plurality of first signal development means for receiving a predetermined number of pairs of said input signals, said predetermined number of pairs including each of said input signals in at least one pair, each of said first signal development means developing an output corresponding to the instantaneous magnitude of that one of the signal pair applied exhibiting a first algebraic magnitude extreme, a second signal

development means receiving the outputs from said plurality of first signal development means, said second signal development means developing an output corresponding to the instantaneous magnitude of that one of the signals applied thereto exhibiting the opposite algebraic magnitude extreme, the output of said second signal development means thereby corresponding to a midvalue one of said input signals exclusive of the most algebraically positive and most algebraically negative ones of said input signals, said plurality of input signals being four in number and comprising first, second, and third ones of said plurality of first signal development means, said first, second, and third ones of said first signal development means receiving as respective inputs three different input signal pairs which pairs collectively include each of said input signals at least once, said second signal development means comprising first, second, and third differential amplifiers receiving the outputs from said first, second, and third ones of first said signal development means as respective first inputs thereto.

5. Translating means as defined in claim 4 where the first one of said first signal development means receives the first and second ones of said input signals, the second one of said first signal development means receives the first and fourth ones of said input signals, and the third one of said first signal development means receives the third and fourth ones of said plurality of input signals.

6. Translating means as defined in claim 4 wherein the predetermined pairs of input signals as applied to said first signal development means are additionally applied to respective voltage comparators, said voltage comparators being adapted to provide an enabling output signal when the respective inputs thereto exhibit an absolute magnitude difference within a predetermined threshold, said first, second, third and fourth input signals being selectively applied to said first signal development means through respective first, second, third and fourth switching means the energization of which is effected by the enabling output signal from selected ones of said voltage comparators, said switching means being normally energized and being deenergized upon the controlling ones of said voltage enabling outputs from said voltage comparators being absent in response to said predetermined threshold being exceeded.

7. In a signal translating means of the type which develops an output signal corresponding to one of the midvalue ones of a plurality of applied input signals exclusive of the most algebraically negative and most algebraically positive ones of said input signals, a plurality of first signal development means each of which develops an output signal corresponding to the most algebraically positive one of at least two of said plurality of input signals applied thereto, each of said first signal development means comprising a plurality of differential operational amplifiers first inputs to which comprise preselected ones of said input signals, the outputs of each said operational amplifier being connected to the anode electrode of a unilateral conduction device the cathode electrode of which is connected to a second input of said differential amplifier, said second inputs being connected in common and through a common resistive member to a negative direct current voltage source, said common interconnection comprising the output of said first signal development means and exhibiting an instantaneous amplitude corresponding to the most algebraically positive one of the input signals applied thereto; second signal development means for developing a signal corresponding to the least algebraically positive one of a plurality of signals applied thereto comprising a further plurality of differential operational amplifiers first inputs to which comprise the respective outputs of said plurality of first signal development means, the outputs of each said further differential operational amplifier being connected to the cathode electrode of a unilateral conduction device the anode electrode of which is connected to a second input of said further differential amplifier, the second inputs of said further operational amplifiers, being connected in common and through a common resistive member to a positive direct current voltage

source, said common interconnection comprising the output of said second signal development means and the signal developed thereon comprising said signal translating means output signal.

8. A signal development means for developing an output signal the amplitude of which corresponds to that of the most algebraically positive one of a plurality of applied input signals, comprising a plurality of differential operational amplifiers receiving said plurality of input signals as respective first inputs thereto, the output of each of said differential operational amplifiers being connected to the anode electrode of a unilateral conduction device the cathode electrode of which is connected to a second input of said differential amplifier, said second inputs being connected in common and through a common resistive member to a negative direct current voltage source, the instantaneous potential of said common interconnection comprising said output signal.

9. A signal development means for developing an output signal the amplitude of which corresponds to that of the least algebraically positive one of a plurality of applied input signals, comprising a plurality of differential operational amplifiers first inputs to which comprise the respective ones of said input signals, the output of each of said differential amplifiers connected to the cathode electrode of a unilateral conduction device the anode electrode of which is connected to a second input of said differential amplifier, said second inputs being connected in common and through a common resistive member to a positive direct current voltage source, the instantaneous potential of said common interconnection comprising said output signal.

10. Signal translating means for selectively applying one of a plurality of input signals to a common output line, comprising a plurality of first signal development means for receiving a predetermined number of pairs of said input signals, said predetermined number of pairs including each of said input signals in at least one pair, each of said first signal development means developing an output corresponding to the instantaneous magnitude of the most algebraically positive one of the signal pair applied thereto, a second signal development means receiving the outputs from said plurality of first signal development means, said second signal development means developing an output corresponding to the instantaneous magnitude of the most algebraically negative one of the signals applied thereto, the output of said second signal development means thereby corresponding to a midvalue one of said input signals exclusive of the most algebraically positive and most algebraically negative ones of said input signals, a first one of said first signal development means receives the first and second ones of said input signals, a second one of said first signal development means receives the first and fourth ones of said input signals, and a third one of said first signal development means receives the third and fourth ones of said plurality of input signals, the predetermined pairs of input signals as applied to said first signal development means are additionally applied to respective voltage comparators, said voltage com-

parators being adapted to provide an enabling output signal when the respective inputs thereto exhibit an absolute magnitude difference within a predetermined threshold, said first, second, third and fourth input signals being selectively applied to said first signal development means through respective first, second, third and fourth switching means the energization of which is effected by the enabling output signal from selected ones of said voltage comparators, said switching means being normally energized and being deenergized upon the controlling ones of said voltage enabling outputs from said voltage comparators being absent in response to said predetermined threshold being exceeded.

11. Translating means as defined in claim 10 wherein a first one of said voltage comparators receives the first and second ones of said input signals and provides an output effective in enabling those of said switching means serially interconnected between said first and second input signals and said first signal development means, a second voltage comparator receiving the first and fourth ones of said input signals and providing an enabling output to those of said switching means effective in controlling the application of said first and fourth input signals to said first signal development means, a third voltage comparator receiving said third and fourth input signals and providing an enabling output to those of said switching means effective in controlling the application of said third and fourth input signals to said first signal development means, said first and fourth switching means when deenergized applying a zero-signal potential to the respective first and fourth input lines to said first signal development means, the second and third ones of said switching means including interconnecting means to connect to said zero-signal potential the associated input terminal to said first signal development means through the other one of said second and third switching means when said second and third switching means are deenergized simultaneously, each of said second and third ones of said switching means additionally including interconnection means to connect the applied second and third input signals when energized through the other unenergized one of said third and second switches, respectively, to the associated first signal development means input line associated with the unenergized one, a first operational mode being effected upon enabling outputs from each of said first, second and third comparators to select as an output from said translating means one of the midvalue input signals exclusive of the most algebraically positive and most algebraically negative ones of said input signals, second and third operational modes being effected upon absence of an enabling output from the third and first comparators, respectively, and converting the signal translating means operational mode to a midvalue selection of three predetermined ones of the plurality of input signals, and fourth, fifth and sixth operational modes being effected upon enabling outputs only from the first, third and second comparators, respectively, to effect operational modes of midvalue selection based on a predetermined pair of said input signals and said zero-signal potential.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,596,107 Dated July 27, 1971
Inventor(s) Richard L. Kittrell

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 11, line 49, after "means" insert -- receiving the outputs from said plurality of first signal development means, --.

Signed and sealed this 18th day of January 1972.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Acting Commissioner of Patents