Dec. 10, 1968 P. C. BROCKETT 3,416,130

TRAFFIC ACTUATED CONTROL SYSTEM

Filed Nov. 1, 1965 3 Sheets-Sheet 1

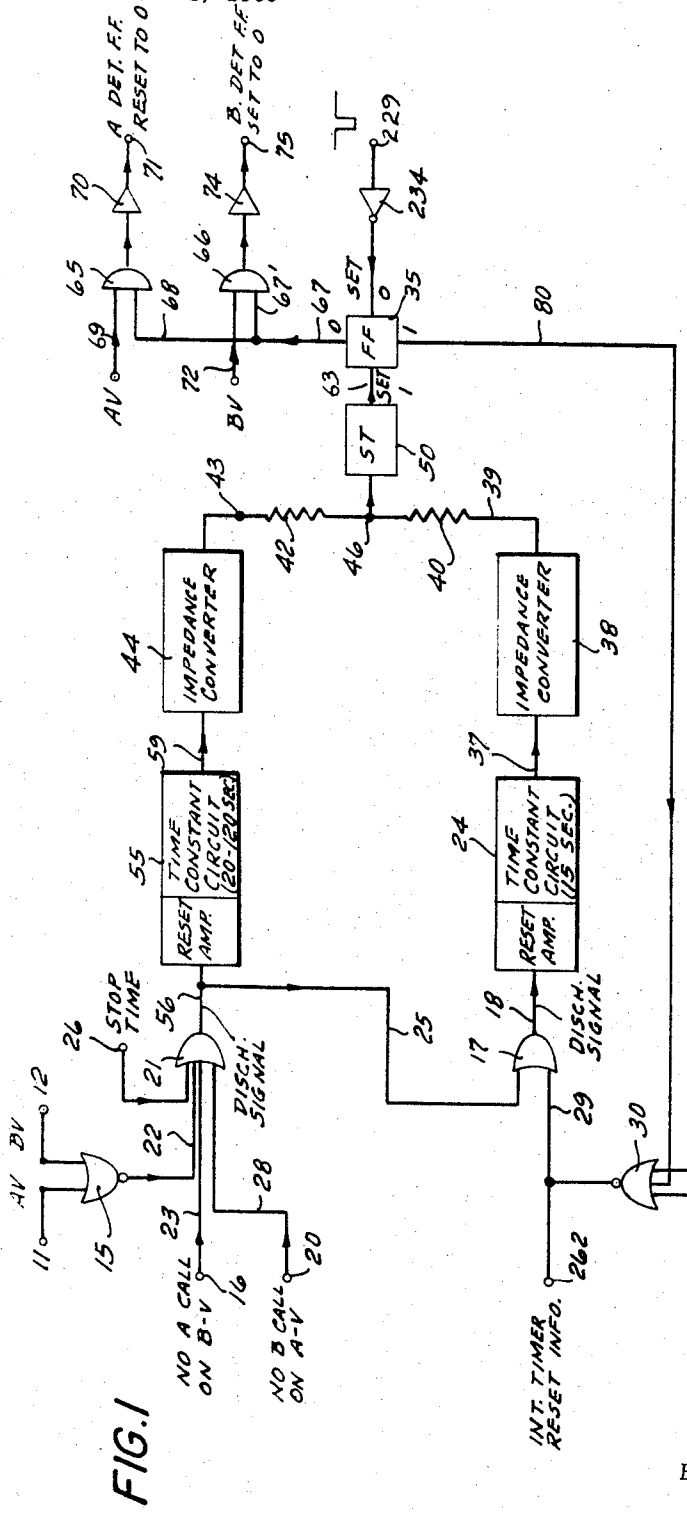


FIG. 1

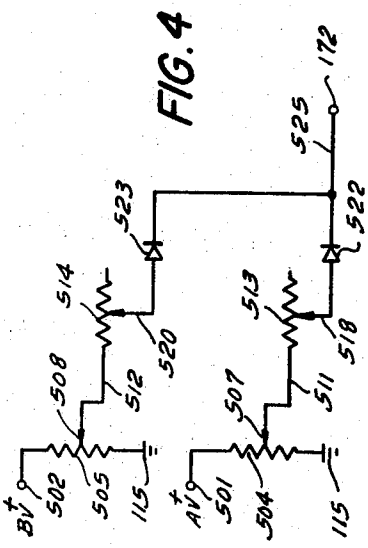


FIG. 4

INVENTOR
PETER C. BROCKETT

BY

Edward H. Eames
ATTORNEY

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TRAFFIC ACTUATED CONTROL SYSTEM

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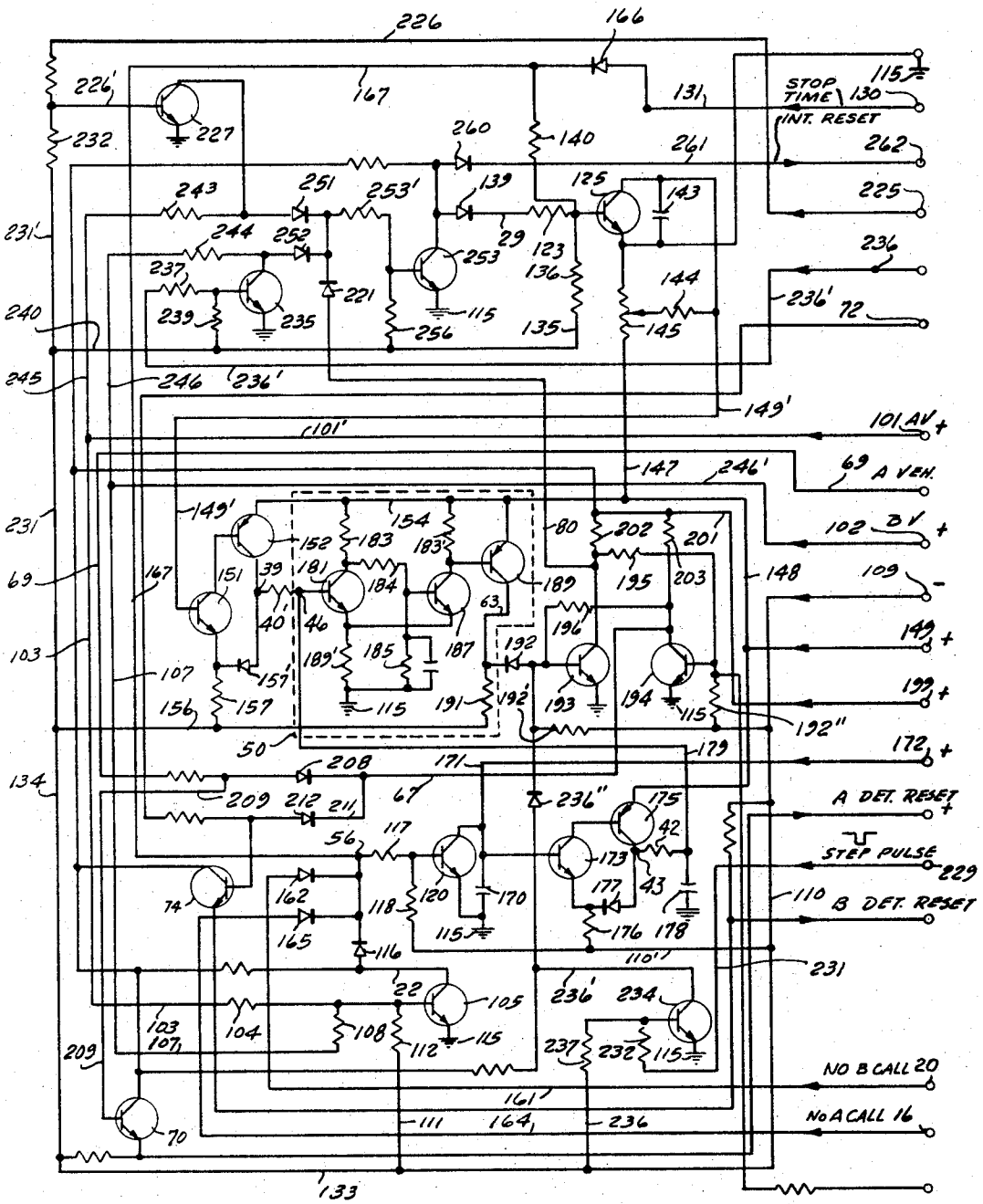


FIG.2

INVENTOR
PETER C. BROCKETT

BY
Edward K. Eames

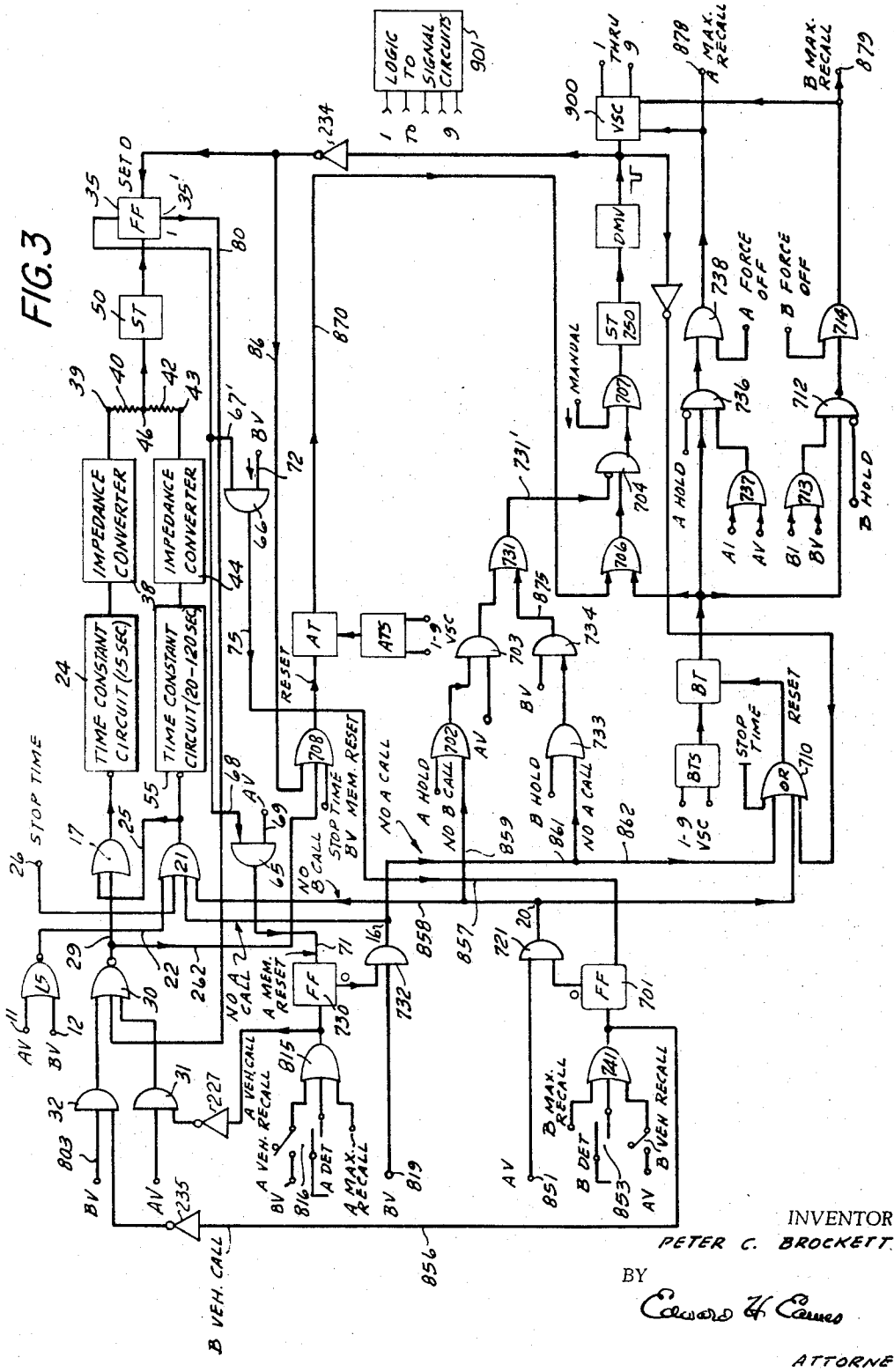
ATTORNEY

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TRAFFIC ACTUATED CONTROL SYSTEM

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FIG. 3



INVENTOR
PETER C. BROCKETT
BY
Edward H. Eames
ATTORNEY

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TRAFFIC ACTUATED CONTROL SYSTEM

Peter Clinton Brockett, Milford, Conn., assignor to Laboratory for Electronics, Inc., Waltham, Mass., a corporation of Delaware

Filed Nov. 1, 1965, Ser. No. 505,874
10 Claims. (Cl. 340—37)

ABSTRACT OF THE DISCLOSURE

An improved traffic actuated control system for the timing of a variable time extension increment or limiting time "gap" between vehicle actuations in prolonging the green or right of way period of a traffic signal cycle. The system employs solid state switching, gating and RC timing circuits. The voltage output from a "gap reduction timer" is additively coupled through a voltage divider circuit to the voltage output from a "gap timer," the gap timer normally having a considerably shorter time constant and being resettable by vehicle actuation on the traffic phase having the right of way, to so extend the right of way period. The relatively slowly increasing voltage of the gap reduction timer progressively reduces the voltage level required to be reached by the progressively increasing voltage of the gap timer between resetting vehicle actuations, for the combined voltage to operate a trigger circuit, thus reducing such limiting time gap. The trigger circuit is coupled to substantially a mid-point on the voltage divider circuit to receive the combined voltage as an average of the respective voltage outputs. High impedance buffer circuits couple the respective voltages of the two timers to the voltage divider circuit.

Gating circuits, controlled by vehicle actuation input circuits for respective traffic phases and by respective steps of a step-by-step switching circuit providing a control cycle corresponding to right of way periods for the respective traffic phases, serve to control initiation of timing of the two timing circuits on the phase having right of way, in response to vehicle actuation on the other phase, and to control reset for such gap time extension by vehicle actuation on the phase having right of way, in selected steps.

Operation of the trigger circuit by the combined voltage reaching a triggering level, initiates transfer of right of way from one phase to another by switching a flip-flop circuit which acts through further gating circuits and a third timing circuit to time a brief continuation of the right-of-way period and thereupon to advance the step switching circuit for transfer of right of way.

This invention is directed to electronic solid state circuitry adapted for multiple-phase traffic control with special emphasis directed to improved time-waiting gap reduction circuitry.

In pending application Ser. No. 338,555, filed by the present applicant jointly with Charles L. Du Vivier on Jan. 2, 1964, now U.S. Patent 3,267,424, an improved form of a full actuated two-phase traffic control circuitry is described in substantial detail. The earlier-filed application, like that here presented, embodies no mechanically

moving parts (other than the switches or relays for the lights). One of the principal advantages obtained is the improvement in right-of-way control provided between cross or conflicting traffic flows on different phases of a pair of intersecting paths.

The control provided by the present invention uses a step-by-step cyclic operation with improved provisions incorporated therewith in the form of solid state components to insure control in accordance with the actual and immediate need or demand of one cross-street or artery with respect to another.

In two-phase traffic control systems, it frequently happens that one of the paths or streets at an intersection is normally busier than the other, or, during certain time periods of the day the traffic flow one way is heavier than the other. The present invention makes provisions whereby a control of the timing of one of the traffic paths or streets relative to the other is regulated automatically in accordance with both the traffic flow in one path or direction and the waiting time in the other or intersecting path or direction.

So considered, the circuitry here to be disclosed contemplates an operation whereby right-of-way ordinarily shall not be given to any street or phase without actuation thereon. In cases of complete absence of traffic on the other street or phase, it is usually preferable that the right-of-way shall remain on the street or phase where last assigned. The foregoing, however, is subject to the exception that recall circuits may be provided to cause the right-of-way to be returned to any selected street despite the absence of traffic thereon, or, in fact, manual control may be used to the exclusion of automatic, where desired.

In its preferred form, the invention is so organized that the longer traffic waits against a red light in one direction, the more closely spaced must be the vehicles moving in the other direction in order to retain the right-of-way. Despite the resultant reduction in "gap" (the time spacing between vehicles or vehicle actuations to retain the right-of-way), the control circuitry allots ample time for the last of the traffic flow in the prevailing direction to be cleared prior to a reassignment of the right-of-way.

Since the invention, in its preferred form, constitutes an improvement of the invention described and claimed in the aforesaid pending application, reference may be made to the pending application for completeness of description and circuit details not herein specifically set forth or outlined in any substantial detail. Suffice it to say that for operational purposes, the circuitry described preferably operates on a signal sequence such that the control cycle may be divided into any selected number of parts or intervals. The invention contemplates that under certain conditions of operation equal time intervals may be allotted to the differene steps of the sequence, although this is not the usual or normal operation. For the purpose of understanding the nature of the invention and for orienting the improvement herein involved to illustrate circuit conditions, it may be assumed for a nine-step control that the control will provide essentially the following signaling sequence (disregarding any pedestrain control which may be added in accordance with the teachings of the copending application, Ser. No. 338,555, for instance).

In those cases where the nine (9) position counter se-

quence switch is used, the time periods and cyclic positions may be considered illustratively as follow:

Street	Time period—cycle position								
	AV 1	AY 2	ARR 3	BI 4	BV 5	BY 6	BRR 7	SKIP 8	AI 9
Street "A"-	G	Y	R	R	R	R	R	S	G
Street "B"-	R	R	R	G	G	Y	R	S	R

In the foregoing pattern, the letters G, Y and R represent respectively, green, yellow and red (or, respectively, go, caution or stop). The letter S represents a "skip" or a cyclic position which is almost instantly passed over and is not displayed or may have the same display as one of the adjacent positions. Further, in the table no pedestrian conditions are included but may be added, as above suggested.

AV represents the vehicle interval for the A phase, AY represents the yellow interval for the A phase, ARR represents the interval when both phases are red and AI represents the initial interval position of the A phase. The B phase is similarly designated BV, BY, BRR and BI. Still further, since the table shows pedestrian conditions omitted, they also will be omitted in the following explanation as being not germane to the substance of the novel features here included.

In some forms of circuitry, as was explained in application Ser. No. 338,555, above identified, instead of operating as a nine-unit code being considered, the operation may be modified to include ten steps through the use of a modified switching circuit.

The operation may also be controlled from an eight-unit code normally accomplished illustratively, with flip-flop types of circuitry where three separate appropriately connected binary units of two components each serve to provide eight distinct operational steps. In the operation, various timing periods may be allotted to the various chosen operational conditions and it is within the contemplation of the invention that prior to a transference of the right-of-way from one traffic phase to the other there shall be substantial freedom in choosing the range in time over which the various conditions may function. Certain of the conditions which are dealt with in the operation involve a choice of the initial time interval, the passage time allotted for a vehicle between the detector and the final stop line, and the time which is permitted to reduce the allowed gap from what might be considered a normal passage time to a minimal time gap. In addition, for some conditions of operation, it is important to consider the caution interval, the use of all-red clearance intervals, the maximum time period over which the operation may be extended while remaining in one phase, and, in addition to this, the wait period. Where pedestrian control is also involved, the walk and the pedestrian clearance intervals must be considered.

The counters or stepping units are controlled from an appropriate type of pulsing circuit, such as a Schmitt trigger. The operation of these units is, in turn, dependent upon the timing control circuits.

The invention in its preferred form from the standpoint of a control of the allowable gap period in the vehicle intervals of the signal cycle will be discussed in connection with the accompanying drawings forming a part of this disclosure and with which reference also may be made to the companion application above identified for circuit details carrying beyond the circuitry to control the gap reduction and the semi-actuated operational status.

The invention has been illustrated in its preferred circuit forms by the accompanying drawings wherein:

FIG. 1 is a schematic and logic diagram of the circuit portion for controlling the gap variance;

FIG. 2 is a circuit diagram of the circuit of FIG. 1; and

FIG. 3 is a logic diagram showing the control circuit of FIG. 1 in combination with a two-phase full-actuated control.

FIG. 4 is a schematic diagram of the charging circuits for the long period timing circuit of FIGS. 1–3.

Referring now to the drawings and first to the logic diagram of FIG. 1, the circuit is directed primarily to an arrangement for controlling the permitted gap-time on one phase with respect to activity on the other phase. For purposes of designation, the phases are represented respectively as A and B, so that designations such as AV and BV indicate the intervals in the traffic signal control cycle which may be extended by detector actuation by vehicles having the right-of-way accorded by the signals, on phase A or phase B, respectively. Illustratively, a situation may first be considered where traffic is present and moving on phase A (signal period AV) but, for the moment, not moving or present on phase B. Later traffic will appear on phase B so that passage on phase A shall be interrupted after an appropriate control and reduction of the allotted gap-time between vehicles. So considered, indication of one time (interval AV) when traffic can move on phase A, for instance, is provided by a voltage signal at terminal **11** derived from a control point (position **1**, for instance of component VSC, indicated as **900** in FIG. 3).

Similarly, indication of one allotted time (interval BV) for traffic on phase B is provided by way of a voltage signal supplied from the same control component VSC at terminal point **12** for the B phase. Each of the input signals at the input terminals **11** or **12** feeds to a NOR gate represented at **15**.

Signal circuits for the signals G, Y and R for the respective phases are controlled by the output of the logic to signal circuits component **901** of FIG. 3.

First of all, the NOR gate **15** supplies an input to OR gate **21**. An input to gate **21** may be connected from a stop-timer source (not shown), at terminal **26**.

Other input signals may be supplied. These are signals indicative of the lack of any B-call (i.e. a stored vehicle actuation of a detector on the B-phase) while the system is in the AV interval. This signal is supplied to the OR gate **21** from terminal **20** through conductor **28**. A similar condition may obtain if the system is in the BV interval. The fact that there is no A-call will be reflected in a signal at terminal **16**. This signal is supplied to the OR gate **21** through conductor **23**. Each of the signals at any of terminals **11**, **26**, **20** and **16** appears in the positive sense. The NOR gate **15** establishes that the signal on conductor **22** be of appropriate polarity at the gate **21**. Thus, any output of OR gate **21** on conductor **56** due to a signal present on any input of **21** will be such as to discharge the capacitor of a time constant circuit **55**, later to be described.

The output on conductor **56** when in a positive sense will maintain the capacitor of the time-constant circuit **55** in a discharged state (see capacitor **170**, FIG. 2). This component is included as a part of the reset amplifier and the time constant circuit conventionally shown at **55** in FIG. 1. The signals at terminals **16** and **20** are positive during the time the system is either in the BV or the AV phase, respectively, as long as there is no A call in the B-phase or B call in the A-phase, as the case may be.

The second OR gate **17** receives input signals from the output of the OR gate **21** through conductor **25**. In addition, it receives a control input from the NOR gate **30** by way of conductor **29**. The NOR gate **30** also supplies the same signal at the terminal **262** which supplies the interval timer (see FIG. 3) with reset information.

The NOR gate **30** is controlled by the outputs of either of two AND gates **31** and **32**. Signals indicative of periods of operation in the AV and the BV intervals are supplied respectively to AND gates **31**, **32**. These are positive signals as are those representing the A-vehicle call and the B-vehicle call which are supplied through the indicated amplifiers with inversion. Thus, there will be no output from the AND gate **31** in the AV position if there is an A-vehicle call. The system is symmetrical so that a similar

condition exists relative to the BV position at the output of AND gate **32**. Accordingly, the NOR gate **30** under such conditions will provide an output voltage on conductor **29** which will provide a discharge signal output from the OR gate **17** available on conductor **18** to maintain a capacitor (see capacitor **143** in FIG. 2) within the reset amplifier and time-constant circuit **24** discharged. The signal polarity on conductor **29** will provide the gap measuring control.

Considering first a condition where vehicles are present in the A phase but are not present in the B phase and the control is in the AV position, the signal input at OR gate **17**, controls the operation of an appropriate time-constant circuit **24** to determine the stored charge acquired by a suitable capacitor element. Normally, the conventionally represented time-constant circuit **24** includes, as above mentioned, a capacitor (see capacitor **143** of FIG. 2) which is charged through an appropriate charging circuit, later to be described. If discharge of the capacitor element does not occur within the assumed and designated fifteen (15) second time period (or occur at the selected period) the capacitor may charge to the assumed critical voltage level with respect to ground or to any fixed potential point suitably determined.

FIG. 2 of the drawings will be referred to later in particular for a further understanding of the general circuitry for controlling the circuit triggering as a result of capacitor charging, but, at this point, suffice it to say that the output from the OR gate **17** controls a discharge path to reduce the charge level on the storage element of the time-constant circiut **24** to a predetermined fixed value, for instance, zero.

The more frequently vehicular traffic appears in phase A, the more frequently the capacitor will be discharged and the lower will be the voltage developed across its output. Operation of the time-constant circuit is thus controlled through the OR circuit **17** for the stated condition. There is also another possible control which will be mentioned later which can occur by signal voltage on conductor **25** or a signal on conductor **80**.

Each time the capacitor of time-constant circuit **24** is charged, it acquires a voltage with respect to ground (or some other fixed reference potential) according to a generally linear charging path. The critical voltage or trigger level reached by the storage element of the time-constant circuit **24** here will be assumed as 6.0 volts. This voltage (or any voltage acquired during the charging time) is applied by way of the conductor **37** through an impedance converter circuit **38** to act in a control capacity along with a second time-constant circuit **55** (to be described) on a triggering circuit **50**, (such as a Schmitt trigger). The impedance converter **38** consists essentially of a pair of transistor components (see FIG. 2) which are directly connected and which, illustratively, are activated in accordance with the charge acquired by the storage element, as above stated. Normally, the impedance converter receives an input activating voltage which corresponds to that to which the storage capacitor of the time-constant circuit is charged. The impedance converter provides a high impedance input for isolating the time-constant circuit so that it is not loaded by the Schmitt trigger **50** or flip-flop circuit **35** which follows it. The impedance converter output connects to one terminal **39** of an output resistor element **40**. Resistor **40** and resistor element **42** of like value (later to be discussed) whose terminal **43** connects to an impedance converter **44**, provide a voltage divider with the potential at point **46** controlling the operation of the conventionally represented Schmitt trigger **50**.

Illustratively, the triggering point is set (assuming resistors **40** and **42** to be of like value) to trigger at a voltage just slightly higher than half the assumed charging level to which the capacitor of the time-constant circuit **24** normally charges. This point actually may be, illustratively, set at 3.01 volts or thereabouts. The Schmitt trigger **50** generates an output signal which triggers a flip-flop circuit **35** of any well known variety, all as will later be mentioned.

The time-constant circuit **55**, which is controlled by the OR gate **21** and the output available on conductor **56**, is of relatively long time duration in contrast to that of the time-constant circuit **24**. For illustration, circuit **55** may have a time-constant adjusted in the time range between 20 and 120 seconds. Like the circuit **24**, the time-constant circuit **55** also has a reset input as schematically indicated. This will be described further in connection with FIG. 2 but at this point, note may be made of capacitor **170** in FIG. 2. The capacitor circuit is usually so selected that in the chosen time cycle, the maximum charge which it can acquire will be to a voltage level somewhat below 6.0 volts for example. Such voltage level to which capacitor **170** can charge must be set at some value such that its charge level never reaches a value which, of itself, could operate the Schmitt trigger **50**, as will later be discussed in more detail.

The RC charging circuit in **24** is operated such that the critical level (for instance, 6 volts) is reached in a period equal to RC or 62% of its charging voltage whereas the charging circuit in **55** is operated such that it charges toward a finite voltage level which is held below the critical level. The time indicated (20–120 seconds) is three times the normal time constant RC or is, in other words, the time required to reach 95% of the charging voltage.

The output from the time-constant circuit **55** is supplied by conductor **59** to an impedance converter **44** of the type substantially like that above discussed for the impedance converter **38**. The output from the impedance converter **44** is supplied at terminal **43** of an output resistor **42** which connects to the resistor **40** at the junction point **46**. The potential effective at the junction point **46** is that which is used to control the triggering of the schematically represented Schmitt trigger **50**.

In the circuit operation as thus described, signals are supplied at either terminal **16** or **20** whenever there is no vehicle in the phase opposing the traffic having right-of-way. Let it be assumed, for instance, that the controller is in the AV position. This provides a signal level at terminal **11**. In this case, the NOR gate **15** provides a polarity reversal and the control signal on line **22** is removed from the OR gate **21**. If, however, the controller is in the AV position and there is no call on the B vehicle path at terminal **20**, an input signal is applied to the OR gate **21** by way of the conductor **28**. When the controller is in the AV position, there can be no signal on the BV phase at the terminal **16**. The result is that the capacitor within the time-constant circuit **55** is prevented from charging and amounts to what may be considered a reset state since the capacitor is held discharged. Likewise, the capacitor in time-constant circuit **24** is held discharged by virtue of connection from OR gate **21** through conductors **56** and **25** to OR gate **17** and line **18**.

Assuming for the moment that no vehicles are awaiting passage on phase B, both of the time-constant circuits **24** and **55** are held in discharged condition by the presence of the signal on terminal **20** resulting from the condition of no B call in AV. The signal on line **20** acts on gate **21** to apply a signal on line **56** to hold the time-constant circuit **55** reset and also from line **56** via line **25** provides a signal through OR gate **17** to hold the timing circuit **24** reset.

Assume now that a vehicle arrives and is awaiting passage on phase B. This new condition removes the signal present at terminal **20** and consequently via the gates **21** and **17**, removes the discharge action on the respective timing circuits **55** and **24**. Consequently, both of these timing circuits **55** and **24** start timing by charging action in their capacitors. As previously indicated, the timing circuit **55** normally charges more slowly than the circuit **24**.

Thus, with a vehicle waiting on phase B, control of the

charging and discharging of the circuit **24** is under control of the gate **17** which in turn is under the control of A vehicle calls via gates **30** and **31**, while in the AV position.

The maximum time permitted for charge accumulation is therefore the time between successive vehicles on phase A. The capacitor in circuit **24** in charging from a predetermined voltage supply (10 volts, for example), supplies a control potential by way of the impedance converter to one end **39** of the voltage divider formed by resistors **40** and **42**.

A more slowly rising voltage from the capacitor in time-constant circuit **55** is applied through impedance converter **44** to the other end **43** of the voltage divider. The voltage at junction **46** will be one-half the sum of the two voltages applied to the ends **39** and **43** of the voltage divider.

Illustratively, if the Schmitt trigger is set so that it will not trigger until a voltage of at least 3.01 volts is reached at the junction point **46**, closely spaced traffic on phase A will prevent operation of the Schmitt trigger circuit **50**. In the AV position, an A vehicle call will be applied through gates **31** and **30** and line **29** to the gate **17** for restoring the capacitor of time-constant circuit **24** to a discharged state. Therefore, vehicle spacing closer than 15 seconds or some progressively lower value as explained below, will prevent operation of the Schmitt trigger.

The effect of the slowly rising voltage at the upper end **43** of the voltage divider is to provide a slowly increasing aiding voltage enabling the voltage at the mid-point **46** to reach the triggering level in a shorter time as the voltage at the lower end **39** rises, or rises and falls in saw-tooth form, as the timing circuit **24** is periodically reset by successive vehicles on A phase in the AV interval. It will be noted that the slowly rising voltage at the upper end **43**, derived from timing circuit **55**, provides at the mid-point **46**, an increasing half-value voltage to which this point returns on each reset to zero of the voltage at the lower end **39**, as the timing circuit **24** is reset (discharged) by each vehicle on the same phase.

As an example, assume that the maximum voltage to which the time-constant circuit **55** can charge in 120 seconds is four volts, that circuit in 30 seconds might charge to 2.0 volts. On the other hand, assuming the circuit **24** had been reset periodically by closely spaced vehicles, this would still provide a full 15 seconds period during which charging to six volts would normally occur. However, because the average of the voltage to which each circuit **24** and **55** charges will exceed the assumed 3.01 volts at which the trigger **50** operates, it is readily apparent that unless vehicles appear considerably more frequently than each 15 seconds on the instantaneously active phase, a triggering will occur. Operation of the Schmitt trigger as will later become more apparent, provides a control of the complete operation and initiates a switching from one phase to another. Then, as the effect of reducing the level to which the short time-constant circuit will charge before triggering occurs, it reduces the gap period progressively below the assumed 15 second period. Bearing in mind that the circuit **55** can never of itself, as above stated, trigger the Schmitt trigger **50**, it is necessary that there be some charge on the capacitor of the time-constant circuit **24** and that this charging must have occurred over some finite period of time (say at least one second to build up a charge) reaching a voltage which would average with that produced by the circuit **55** to develop a potential at point **46** adequate to trigger the Schmitt trigger **50**. The effect consequently would, in the assumed example, reduce the effective time of the circuit **24** from 15 seconds to one second which would consequently reduce the permissible gap between vehicle reset pulses.

Thus, whenever one of the two phases is activated and vehicles appear in the other phase to start it timing, it is essential that in the first phase activated, the maximum time gap between vehicles will be progressively reduced if triggering of the circuit and a transfer of the operation to the opposite phase is to be avoided. Specifically, a progressive reduction will occur in the time within which successive vehicle actuations must occur to prevent such triggering. In any event, the trigger level will be reached when the average of the voltages acquired by the two storage circuits exceeds that of the triggering level.

In the illustration, it may be assumed that the time-constant circuit **55** may be varied between 20 and 120 seconds by appropriate external controls. In any event, the presence of a control signal output from the OR gate **21**, on the conductor **56**, is adequate to prevent charging of the circuit **55**. With the circuit **55** timing, and assuming the charge approaches but does not reach that level which of itself would be sufficient to trigger the Schmitt trigger **50**, the voltage acquired therein is made available at the voltage divider by way of conductor **59** through the impedance converter **44**. This results in the development of a continuously increasing voltage available at the output of the impedance converter **44** which is supplied to the point **43** to raise its potential with respect to its previous state. Under these conditions, the voltages tend to build up at the output of the impedance converter **44** to an extent such as to make necessary only a minimal build-up of voltage at the output of impedance converter **38** to provide across the voltage divider formed by resistors **40** and **42** a voltage which is sufficient to initiate an operation of the Schmitt trigger **50**.

Any operation of the Schmitt trigger **50** changes the potential of the output voltage available on conductor **63** to a state sufficient to reverse the instantaneous operational state of a flip-flop circuit **35** and change the polarity of the output voltage going into the AND circuits **65** and **66** for the A and B channels, respectively, as supplied through conductors **67**, **67'**, and **68**. The flip-flop **35** has been set in the "0" state by the pulse from terminal **229** through amplifier **234**.

The change is in a direction which will interrupt the output from the AND circuit **65** which is feeding the amplifier **70** and change it to what may be assumed to be a "0" condition at its output terminal **71**.

The signal available at the output **71** serves to reset the memeory circuit **730** of the appropriate channel (see FIG. 3).

From terminal **12** to the terminal **75**, it may be assumed that the connections when the circuit is operating in its B phase follow the pattern already explained for operation in phase A. In either case, the circuits **65** and **66** being of the AND type pass an output signal only at the time of control voltages on the active phases A or B as determined by voltage on conductors **69** or **72** and before the FF **35** is set to the "one" condition by operation of the trigger circuit **50**.

As previously explained, terminal **71** controls the memory circuit **730** of phase A and likewise terminal **75** in a similar manner controls the phase B memory circuit **701**.

When flip-flop **35** has been set to the "one" condition by operation of the trigger circuit **50**, conductor **80** passes a signal into NOR gate **30** which prevents any further output appearing on conductor **29** and at terminal or line **262**. This therefore prevents any further resetting of the timing capacitor in **24** and likewise any further reset of the timing capacitor in the interval timer AT in the controller. Thus the interval timer will continue to time and at completion of the remainder of its normal interval cause the controller to move to the next interval, resulting in change of allocation of right-of-way from that phase to the opposing phase.

A complete circuit operating as described by the logic showing of FIG. 1 is embodied in FIG. 2. Referring now to FIG. 2, the AV and the BV inputs at terminals **101** and **102**, like terminals **11** and **12** of FIG. 1, which are positive voltages, as indicated, determine the voltage from the output of NOR gate **105** as supplied through diode **116** of the OR gate **21** and resistor **117** to the base of

transistor 120. The NOR gate 15 output (as represented by the voltage output of diode 116) through conductor 22 is grounded with either AV or BV energized. Therefore, this voltage cannot act to carry transistor 120 to a conductive state.

The stop time control is supplied from terminal 130 via conductor 131, diode 166, conductor 167 and then through resistor 117 to the base of transistor 120. The voltage is positive at terminal 130 and, therefore, provides that capacitor 170 (connected between collector of transistor 120 and ground 115) will be discharged to zero at signal presence. The transistor is biased from the negative source connected at terminal 109, with the voltage applied through conductors 110 and 110' and resistor 118. The emitter is grounded.

The condition of no call on B when in the AV position is supplied to transistor 120 from terminal 20 by way of conductor 161 and diode 162 through resistor 117. The similar condition for no call on A when in the BV position is supplied from terminal 16 through conductor 164 and diode 165 to the same resistor.

Thus, the four inputs shown by the logic diagram of FIG. 1 are available at the base of transistor 120. The nonconducting periods of transistor 120 thus control the time during which capacitor 170 can accumulate a charge. This capacitor has been charged from terminal 172 (see FIG. 4) through conductor 171. The charging and discharging of capacitor 170 correspond to the operation described for the circuit 55 of FIG. 1 and are not here repeated.

The OR gate 17 of FIG. 1 is provided by the FIG. 2 circuit through the combination of inputs from diode 139 and resistors 123 and 140 each of which is connected to the base of transistor 125. This transistor is biased from the negative source (not shown) connected at terminal 109 which leads through conductors 110, 133, 134, 231, 240 and 135 to resistor 136 which connects to the transistor base. The transistor provides the control of the charging and discharging of a capacitor 143 which constitutes the capacitor already discussed in respect to the time-constant circuit 24 of FIG. 1. The capacitor 143 is connected across the collector and emitter of transistor 125. It is charged from a positive source (not shown) connected at terminal 149 and thence through conductors 148 and 147 to charge the capacitor through the lower portion of the potentiometer 145 and resistor 144 so that the plate of the capacitor connected to the collector element charges positive relative to ground. The ground terminal 115 connects to the emitter and the capacitor plate connected thereto.

Conductive periods of transistor 125 are set by the output of the gate 21 (voltage at point 56) so that all of the voltages which control the charge and discharge periods of capacitor 170 also control charge and discharge of capacitor 143. Illustratively, the outputs of all diodes 116, 165, 162 and 166 from the OR gate 21 are supplied to the OR gate 17 and thus determine the conductive periods of transistor 125.

The output of the NOR gate 30 which is provided by the transistor 253 and diode 139 supplies control voltage through resistor 123 to the base of transistor 125. Thus, as explained by FIG. 1, the voltage to which capacitor 143 can charge is determined by the conductive periods of transistor 125.

The input significant of the A vehicle call is here supplied as a positive pulse at terminal 225 and through conductors 226 and 226' to the base of transistor 227. The base is biased through resistor 232 from the negative terminal 109 through conductors 110, 133, 134, 231 and 231'. The AV signal is supplied from terminal 101 through conductors 101' and 245 and resistor 243. The combined signals then feed through diode 251 and resistor 253' to the transistor 253 base. This transistor has its base biased from terminal 109, as did transistor 125 but via resistor 256. The B vehicle call signals are supplied from terminal 236 and conductors 236' and resistor 237 to the base of transistor 235. This transistor is also biased from terminal 109 through resistor 239. The emitter, like that of transistor 227, is grounded. Output is had from the collector and is combined with the BV voltage from terminal 102 supplied through conductors 246' and 246 and resistor 244. The combined voltages are then fed through diode 252 to resistor 253' (along with the output of diode 251) to the base of transistor 253.

With these signals there is combined the output voltage from the flip-flop (see 35 of FIG. 1) which includes transistors 193 and 194. The flip-flop voltage is made available through conductor 80, as well as diode 221, and provides the three separate inputs discussed in FIG. 1 as the inputs to NOR gate 30. The output from the collector of transistor 253 then supplies a control voltage on transistor 125 through diode 139, conductor 29 and resistor 123. Also, as by FIG. 1, the output from transistor 253 supplies to the interval timer AT, the interval reset information to terminal 262 through diode 260 and conductor 261. Each of diodes 260 and 139, as well as the collector of transistor 253 is biased positively from a source (not shown) connected at terminal 199.

Continuing now the analogy between FIGS. 1 and 2, the capacitor 170, which is the storage element of circuit 55 of FIG. 1, charges positively relative to ground from a source (not shown and see FIG. 4) connected at 172 which charges the capacitor through conductor 171. As already mentioned, the emitter of transistor 120 is grounded, as is one terminal of capacitor 170. The other capacitor terminal connects both to the collector of transistor 120 and to the base of transistor 173. The capacitor 170 is charged so that the potential at its upper electrode, and thus the potential at the collector of transistor 120 and the base of transistor 173 is positive relative to ground 115.

Conduction through transistor 120 maintains the capacitor 170 discharged. However, if transistor 120 is nonconducting the capacitor 170 charges and the voltage to which it charges is reflected at the base of transistor 173 which forms with transistor 175, the impedance converter 44.

The control of conductive periods of transistor 120 from each of the voltages available on conductor 167 and the output from diodes 116, 165 and 162 has already been explained. Accordingly, the voltage effective at the base of transistor 173 is thus controlled. This transistor has its emitter biased from terminal 109 through conductors 110 and 110' and resistor 176. The transistor collector is connected directly to the base of transistor 175. This transistor has its emitter bias applied in a positive sense from terminal 149.

Transistor 175 has its output supplied from its collector to one end of resistor 42 which forms a half of the voltage divider which triggers the Schmitt trigger 50. The transistor output also feeds back to the emitter of transistor 173 through diode 177. The remote terminal of resistor 42 connects to point 46 and resistor 40 by way of conductor 179. The connection point is by-passed to ground by a capacitor 178.

Referring now for a moment to the companion part of the circuit the voltage to which capacitor 143 can charge is supplied in a similar manner by conductor 149' to the base of a transistor 151. This transistor also has its emitter bias supplied through resistor 157 from terminal 109. The collector is directly connected to the base of transistor 152 which constitutes the second transistor of impedance converter 38. Transistor 152 also has its emitter bias applied from terminal 149, as did transistor 175. The transistor output available at its collector connects to one end of resistor 40 (the second resistor of the voltage divider) and it feeds back to the emitter of transistor 151 through the diode 157'.

With these components the voltage at point 46, where resistors 40 and 42 connect, is that which is applied as

the voltage developed as above explained to control triggering at a selected level of Schmitt trigger **50**.

The Schmitt trigger **50** is constituted by the transistors **181** and **187** with transistor **189** providing an output relative to ground. Bias is applied from terminal **149** through conductors **148** and **154** and resistors **183**, **184** and **185** forming a voltage divider to set the trigger level. The collector of transistor **181** connects to the junction of resistors **183** and **184** while the base of transistor **187** is biased by the voltage (relative to ground) available at the junction of resistors **184** and **185**. The emitter of each transistor **181** and **187** is biased relative to ground through resistor **189'**. The resistor **183'** applied voltage to the collector of transistor **187** and the base of the output transistor **189** directly connected to the collector of transistor **187**. Voltage is applied to the collector of transistor **187** through resistor **183'** and directly to the emitter of transistor **189** from terminal **149**.

The trigger elements **181** and **187** with associated components function in well known fashion to produce a signal output which is passed through transistor **189** to trip the flip-flop circuit **35** which includes the two transistor elements **193** and **194**. The Schmitt trigger controls the flip-flop by way of a voltage supplied through conductor **63** and diode **192** across resistor **191** to the base element of the first transistor **193**. Each of transistors **193** and **194** is supplied with bias on its base from the source connected at **109** and resistors **192'** and **192''** respectively.

The usual cross-connections are provided by resistors **195** and **196**. Collector voltage is applied from terminal **199** through conductor **201** and resistors **202** and **203** which connect to the collector electrodes.

Output voltages from the flip-flop on conductor **80**, as already discussed, control NOR gate **30** as an input to the base of transistor **253** through resistor **253'**.

The flip-flop is also controlled by the step pulse from terminal **229** which is applied through transistor **234** and then from the collector as the output electrode and conductor **236'** and diode **236''** to provide a positive pulse input on the base of transistor **193**. The input voltage at terminal **229** is positive except during the stepping period, as explained in discussing FIG. 1.

The outputs from flip-flop **35** as available on conductor **67** are supplied through diodes **208** and **212** to provide the input control for transistors **70** and **74** which provide the reset voltages from the memory flip-flops of the A and the B phases respectively.

Reference may now be made to FIG. 3 of the drawings. This figure includes a substantial part of the showing of FIG. 7 of application Ser. 338,555 to which has been added and combined substantially the components shown by the logic form of FIG. 1. The combination shown exemplifies the modified control for establishing a variable and controllable gap time between vehicles to the other remaining components of previous FIG. 7. In the form of showing of FIG. 3, there is a full-actuated two-phase traffic signal control, without any actuated pedestrian intervals. The pedestrian intervals, if desired, may be combined with the circuit components of FIG. 3 in the fashion described in connection with the referenced application. In the showing of the referenced application, numerous two-terminal switches were shown which are capable of being readjusted to provide different types of operation. As the switches were shown in the original application, the circuit was designed for some actuated two-phase traffic signal controls also lacking pedestrian features. In the present application, most of the switches of the type described in the previous application are omitted in that the operation is explained only in connection with one of its possible types. For this reason, the various connections are shown as if switch arms were included with the switch armatures connected to the contact points indicated by the type 3 in connection with the circuitry of the referenced application. Thus, in the present application, some switch arms are not specifically illustrated. Also, in connection with the showing of FIG. 3, certain standard logic components are illustrated, particularly the AND and the OR circuits, as well as the NAND and the NOR circuits. In other instances, other logic components are shown by blocks of well recognized form such as FF for flip-flop and ST for a Schmitt trigger. In other instances, abbreviations have been used to a considerable extent as provided legends for identifying terminals or other components of recognized form. For ease of reference, the drawing shows various abbreviations, the significance of which is noted, but for which reference may also be made to the referenced application.

The timing of timer AT is controlled as to time rate by adjustable resistance elements individually selected for the several positions 1–9 of the cycle by the outputs of VSC, said selectable elements being represented by ATS in FIG. 3.

In considering the circuitry of FIG. 3, the operation may be divided into intervals which may occur in any desired sequential pattern. In the form in which the invention is illustrated, there is a fully actuated two-phase traffic signal control with extendible control periods. In this form of circuit, designations such as inputs A-Hold and B-Hold appear. These provide for the controlling of suitable OR circuits, such as **702**, for the A-Hold and no B call and **733** for the B-Hold with no A call. In the first operation, as was explained in the application Ser. No. 338,555, it may be assumed that a signal is derived from the detector in the A vehicle path. This, then, provides for a signal to be developed through the OR circuit **815** shown which may feed then to each of the flip-flop **730** and to the AND circuit **732**. The flip-flop is also provided with an input for the A channel memory reset which, in turn, is controlled by the output of the AND gate circuit **65**, as activated by the flip-flop **35**. The output signal then derived from the "0" output of flip-flop **730** is supplied as one of the inputs to the AND circuit **732**, which also receives an input signal from the terminal BV, representing the vehicle (extendible) interval of phase B as applied at terminal **819**. If there is an A call, there will be no signal from AND gate **732** at terminal **16**.

Referring generally now to the various components depicted by FIG. 3, the switch components marked A Veh. Recall and B Veh. Recall represent recall switches for the A and B vehicle phases, respectively. These may be closed to provide recall of the respective actuating phase. The recall will be effective only during the BV and AV intervals, respectively. The A max. recall terminal and the B max. recall terminal can be assumed as being connected to the A max. recall output and the B max. recall output, respectively. The input terminals AV and BV are individually provided with input voltage during the phase A vehicle and phase B vehicle intervals, respectively. In the showing, the blocks identified as ST and VSC will be components readily recognized in the art as constituting respectively the Schmitt triggers and the vehicle switching controls the latter being a 9-step switching or counter circuit, for example. A block such as that designated FF is the standard form of flip-flop and serves to provide memory of a call, the indication of a call or the indication of no call. Each is capable of being reset to a no-call condition from a call condition by the application of a signal provided in one or another position of the switching condition during the interval in which the condition occurs. In following through, it has been already stated that the B controls provide control of the right-of-way on one traffic flow. The other phase of the controller designated as the A phase controls the right-of-way to an opposing flow of traffic. The signal developed to provide the control can be regarded as an electrical signal in the form of an applied voltage. Gate controls such as the AND gates may provide an output signal or what is sometimes termed a "pass" signal of a desired character upon application of a predetermined combination of input sig-

nals. Where signal inversion is indicated, this is of the normal form and means a reversal of signal polarity.

The advance of the counter VSC through the several steps of the switching cycle for the respective phases is normally controlled by the normal interval timer AT, which, upon completion of its timing, acts through conductor **870** and gates **706**, **704** and **707** to operate the Schmitt trigger ST**750** and the delay multivibrator DMV to so advance the counter VSC.

This action, however, is subject to the energizing of the inhibiting lead **731'** of gate **704** by a hold signal from the output of the OR gate **731** under certain conditions, for example, in the AV position, via gate **703** if there are no phase B vehicle calls or if an A hold signal is applied, or, correspondingly, via gate **734** in the BV position, and there are no phase A vehicle calls or if a B hold signal is applied.

Reset of the interval timer AT occurs during the AV interval as a result of detector operation by vehicles on phase A, acting through gates **815**, **31**, **30**, conductor **262** and gate **708**. Correspondingly, reset of the timer AT in the BV position would occur by phase B vehicle detector actuations acting through gates **741**, **32**, **30**, conductor **262** and gate **708**.

Since continuous traffic on the phase having right-of-way might possibly continuously reset the interval timer AT, a maximum limit is provided by the maximum limit timer BT acting through gates **706**, **704** and **707** to operate the said Schmitt trigger ST**750** and delay multivibrator DMV and advance the counter, despite such continued reset of timer AT. Timing of the maximum limit interval is controlled by selectable adjustable resistance elements (not shown but indicated by block BTS) individually made effective by inputs from positions 1 through 9 respectively of the counter VSC (**1–9** VSC).

Timing of the maximum limit circuit is under the control of OR gate **710** such that timing does not start during the AV interval, for example, if there are no vehicle calls on phase B. Likewise, it will not start in BV interval if there are no vehicle calls in phase A. Such control is derived from gates **721** and **732** respectively. Receipt of a vehicle call on a phase not having right-of-way during a vehicle interval would remove the signal input to gate **710** and thus allow the maximum limit timer to start timing the maximum interval for that controller position. Thus the maximum timer BT is held reset on one phase by the output of gate **710** until there is a vehicle call on the opposing phase.

The timer BT may also be reset by a further input through gate **710** which occurs during the short advance pulse output of DMV. Output from Max. Timer BT is also supplied into a pair of AND gates **712** and **736**. Into each of these gates the B-hold and the A-hold signals are supplied as inhibit signals while the BV or BI and the AV or AI signals via OR gates **713** and **737** respectively are applied as AND signals. Accordingly lacking the input from the A and B holds, output is available from the gates **712** and **736** during the concurrent presence of input of the maximum timer signal. With the BV or BI signal on gate **712** or the AV or AI signal on gate **736**, an output will be passed to the OR gate **714** or **738** as the case may be. Signals are also supplied to the OR gates from the B force-off contact or to the gate **738** from the A force-off contact by way of the indicative connection. Thus, with the development of output signals from either of the OR gates **714** or **738**, voltages are developed at the B or A maximum recall to provide the maximum B or A recall signals which are supplied into the OR gates **741** or **815** respectively and further, to provide inputs represented as an external signal for driving VSC into the BY interval from phase B or for driving the VSC to the AY interval from phase A and also for a recall of phase B via the B maximum recall or of phase A via the A maximum recall.

It will be noted that in the AV and BV intervals, the timing of timer AT proceeds whether or not there is a vehicle call on the opposing phase, subject to reset by vehicle calls on the same phase, but even if the timer AT were to complete its timing (in absence of such reset) its output signal would be blocked at inhibit gate **704** (on AV interval if there is no vehicle call of phase B or in BV interval if there is no vehicle call on phase A), so that the right-of-way could rest on the particular phase in AV or BV as the case may be.

It will also be appreciated that the time period of the timer AT is normally set for the AV and BV intervals to an intermediate time period as a passage time, such that as the allowable gap time period provided by cooperation of timing circuits **24** and **55** becomes reduced progressively, such allowable gap time period will start at a longer time and be slowly reduced to a shorter time than the passage time.

Thus, assuming a series of vehicle actuations on the same phase resetting both the timer AT and the timer **24**, the progressive reduction of the allowable gap time, as a vehicle waits on the opposing phase, will progressively reduce the allowable time spacing between vehicles required to retain the right-of-way. Consequently, any actual time gap between vehicles which exceeds such reduced allowable gap will cause triggering of ST **50** and, by preventing further vehicle actuated reset of timer AT (as will the gap timer **24**), well as permit timer AT to complete the remainder of its passage time and advance counter VSC to advance the controller to the next interval AY or BY as the case may be, as more fully described above.

It will also be noted that while timer AT is so timing the remainder of its passage time, the applicable memory circuit for storage of vehicle call is reestablished by removal of the "set-to-zero" input to the applicable flip-flop circuit as more fully described above.

Thus, with such restoration of memory, a vehicle arriving too late to reset the gap timer will set its associated detector memory flip-flop to the "one" condition to store a "call" for return of right-of-way at the next opportunity in the traffic cycle, after other traffic has been served.

FIG. 4 is added to exemplify a voltage supply for applying a charging voltage at terminal **172** (see FIG 2) for charging capacitor **170** of circuit **24**. As already mentioned, the voltage is positive at terminal **172**. This voltage is provided from two D.C. sources for the AV and the BV intervals. The sources, as already stated, are also positive at input terminals **501** and **502**.

Considering the voltage on the AV phase the input at terminal **501** is supplied through potentiometer **504** having one end grounded at **115**. The position of slider contact **507** adjustably sets the voltage derived on conductor **511** which connects to a second potentiometer **513**. Again, the slider **581** controls the charging current flowing through diode **522** and conductor **525** to terminal **172** to establish the timing rate desired.

The connections for the BV interval are similar. Input voltage from a D.C. source of suitable value feed through potentiometer **505** to ground **115**. Slider **508** determines the level of voltage in conductor **512** as supplied to potentiometer **514**. A selected current flow is established by the slider **520** position to vary the charging resistance and the charging current supplied at terminal **172** after passing through diode **523** and conductor **525**.

The adjustable potentiometers usually have their sliders adjustable from an external position in the housing for the circuitry thereby to provide a control of the charging of capacitor **170**. The diodes prevent conditions chosen in the AV phase from influencing any selections made for the BV phase, and vice versa.

Suitable values of the voltages to be derived at the slider contactors **507** and **508** of the potentiometers **504** and **505** respectively provide normally less than six

volts. For the major part of the time the settings can be assumed to be of the order or five volts. If the conditions above assumed have a triggering voltage level of 3.01 volts effective at the junction point **46** for triggering the Schmitt trigger **50**, the range throughout which the voltages may be adjusted may be varied as required to any values between say, zero and somewhat less than six volts so that the five volt level assumed above may be considered as generally representative. Other values, of course, can be made as desired and the adjustment of the slider contactors **518** and **520** on the potentiometers **513** and **514** serve to determine and establish the charging current flowing into capacitor **170** from the input terminal **172**.

The operation of the gap timer circuitry of FIG. 3 has been described in some detail in connection with FIGS. 1, 2 and 4. Further illustration of such operation is described below.

Although the timing circuit **24** alone has a time constant of about 15 seconds for example, which would result in its level of charge or voltage rising from the substantially zero reset level to a level of about 6.2 volts in 15 seconds for a charging supply voltage of 10 volts for example, and this voltage level at the end **39** of the resistive voltage divider or load circuit **40**, **42** would provide 3.1 volts at junction **46** for triggering the Schmitt trigger circuit **50** at substantially 15 seconds if the voltage at the other end **43** of the resistance circuit **40**, **42**, from timing circuit **55**, were to remain at zero level, it will be noted, however, that the timing circuit **55** does not remain at zero level but is timing (without traffic actuated reset) concurrently with the timing circuit **24**. The circuit **55** provides a normally more slowly rising voltage from substantially zero reset level to a substantially limiting level of about 5 volts in about 45 seconds for example. This would be to a level of about 3.2 volts in about 15 seconds on the usual exponential charging curve.

Since this voltage from circuit **55** is averaged with the voltage from circuit **24** in the resistance divider circuit **40**, **42** to provide a combined average voltage at junction **46** for input to the trigger circuit **50**, it will be noted that at 15 seconds time (from zero start), in the example mentioned, the combined average voltage at junction **46** would be one half of the sum of 3.2 volts and 6.2 volts or 4.7 volts or well above the assumed triggering level of 3.01 volts.

Thus the aiding effect of the progressively rising voltage from circuit **55** provides a reduced actual time period of the combined timing circuits even in the first timing from zero of both timing circuits, so that if there were no vehicle actuated reset of timing circuit **24**, the first time period before triggering the Schmitt trigger circuit **50**, under the condition assumed would not be 15 seconds but would be about 9 seconds, at which time voltages of about 2.1 volts from circuit **55** and about 4.1 volts from circuit **24** would combine to give an average voltage of about 3.1 volts or substantially triggering level. Thus the resulting time period of the combined timing operation would be about 9 seconds instead of 15 seconds, in the assumed example. It will be understood that other settings of the adjusting potentiometers or adjustable resistors of the charging circuits of FIG. 4 would give other resulting time intervals.

The vehicle switching control VSC may be a 9-step cyclic switching means in the form of two conventional cascaded trinary ring counter stages with a conventional gate matrix to provide nine outputs individually in sequence for the nine steps of a cycle, or may be in the form of a 9-step ring counter for example. Such counter or cyclic switching means would be advanced from each step to the next in its cycle by an output pulse from the DMV as described above.

An alternate form of VSC, without the skip position, may be an 8-step counter circuit of three conventional cascaded binary stages and conventional gate matrix for providing eight outputs individually therefrom in sequence for positions 1–7 and 9 of the cycle indicated above.

A preferred embodiment of the invention and some modifications thereof have been described above, but it will be understood by those skilled in the art that other modifications in the form of equivalent circuits or rearrangement of circuits or substitution of other circuit components may be made without departing from the scope of the invention as claimed.

What is claimed is:

1. A traffic-actuated signal controller for controlling traffic signal circuits for control of right of way for traffic flow on each of two traffic phases comprising

a multi-stage step-by-step electrical switching circuit for controlling said signal circuits in a traffic cycle through accord of right of way to the respective phases in respective selected steps,

a plurality of traffic actuatable input circuits controlled by the presence and absence of one or more vehicles on the associated respective phases,

a pair of time-control circuits to store electrical energy from respective preselected voltage sources to provide respective voltages each progressively varying in voltage level in a selected direction of polarity in timing, one of said timing control circuits having a normally longer time period than the other,

electronic gate circuit means for coupling said time control circuits with said switching circuit in the selected right-of-way allocating steps thereof and with said traffic actuatable input circuits for control of said timing circuits, said gate circuit means including

means for normally precluding energy storage in both time control circuits during the right of way period allotted in the step-by-step control to each one phase in the absence of traffic on another phase not having right of way, and

means to initiate the storage of energy in the time-control circuits in the right of way period allotted in a selected step to the one traffic phase in response to actuation of the input circuit by the presence of a vehicle in said other traffic phase,

a trigger circuit,

means coupling said time control circuits to said trigger circuit to trigger said trigger circuit at a time when the combined average voltage level of the stored energy of the two timing-control circuits reaches a preset level,

further electronic gate circuits means for resetting the timing of the short period time control circuit in said one traffic phase by reinitiating energy storage therein in response to actuation of an input circuit by vehicles in said one traffic phase,

and means responsive to triggering of said trigger circuit for initiating transfer of said switching circuit from said one phase to said other phase.

2. A controller as in claim **1** and said means to trigger said trigger circuit including

a common resistive load circuit coupled to the outputs of the timing control circuits to have the combined stored voltages applied thereacross, and

a connection from the midpoint of the resistive circuit to the triggering circuit for supplying the combined average voltage thereto.

3. A controller as in claim **2** and including

a high input impedance converter coupled between each timing circuit and said resistive load circuit for precluding loading effects upon the energy storage circuits due to the triggering circuit means.

4. A controller as in claim **1** and including

a first impedance converter comprising

a first transistor amplifier having a base input coupled to the output of one of said timing con-

trol circuits, and a bias resistor in the emitter circuit,

a second transistor amplifier of complementary type having its base coupled directly to the collector of said first transistor amplifier and having its collector coupled to the emitter of said first transistor amplifier through a forward biased diode and providing an output from the collector of said second transistor amplifier,

a second impedance converter similar to said first impedance converter and having its base input coupled to the output of said other timing control circuit,

a resistance circuit coupled between the outputs of said first and second impedance converters and having a mid-point on said resistance circuit coupled to said trigger circuit for supplying said combined average voltage thereto.

5. A controller as in claim **1** and in which said timing control circuits include

resistance-capacitance circuits coupled to said supply voltages to so vary the charge on the capacitance progressively for providing such progressively varying voltage level,

and said controller includes a resistive load circuit,

high input impedance converter circuits coupled between the outputs of the respective resistance-capacitance circuits and opposite ends of said resistance load circuit,

and a connection coupling a mid-point of said resistive load circuit to said trigger circuit for supplying thereto the combined average voltage.

6. A controller as in claim **1** and in which said means for initiating transfer includes

a further energy storage timing circuit,

means for coupling said further timing circuit to said traffic actuated input circuit to reset said further timing circuit in one traffic phase in response to actuation by vehicles on the same traffic phase,

said further timing circuit normally having a substantially longer time period than said short period timing circuit,

means coupling said trigger circuit to said resetting means for said further timing circuit to prevent any further such reset thereof in response to triggering of said trigger circuit, thereby permitting said further timing circuit to complete timing of its time period despite further vehicle actuation,

and means for advancing said multi-stage switching circuit from one step to another in its cycle in response to completion by said further timing circuit.

7. A controller as in claim **1** and including

memory flip-flop circuits individual to the respective phases, each said flip-flop circuit being coupled to said input circuit of its associated phase to be set to one of its bistable states in response to vehicle actuation of its associated input circuit,

means for resetting said memory circuit by setting said flip-flop circuit to its other stable state by said multi-stage switching circuit when the latter is in its period alloted to the same traffic phase as its associated memory circuit,

means controlled by triggering of said triggering circuit for inhibiting said resetting operation of said memory circuit to permit said setting of said flip-flop circuit to said first stable state in response to vehicle actuation.

8. A controller as in claim **7** and in which said energy storage precluding means includes

means for each phase coupled to the flip-flop circuit of an opposing phase for so precluding energy storage during the period allotted to one phase when the flip-flop circuit in said opposing phase is in its said other stable state.

9. A controller as in claim **8** and in which said energy storage precluding means includes

clamping circuits for clamping said energy storage timing circuits at an initial storage level from which the timing normally proceeds by variation of energy storage,

and gate circuits coupled between the respective flip-flop circuits for the respective phases and said clamping circuits to control said clamping circuits for so clamping said timing circuits on one phase when said flip-flop circuit for the opposing phase is in its said other state, said gate circuits disabling said clamping circuits to permit operation of said timing circuits by energy storage in response to said flip-flop circuit of said opposing phase being in its said one state.

10. A control circuit for determining the activating time of a step-by-step switching circuit for timing respective right-of-way periods in a pair of separately actuated traffic phases in control of a traffic signal comprising

a pair of electrical storage means,

means to charge each of the storage means toward preselected voltage levels, said charging means including resistive means to cause one of said storage means normally to reach its preselected voltage level at a time longer than that required by the other of said charging means to reach its preselected voltage level,

a trigger circuit adapted to be triggered when voltage applied thereto reaches a predetermined triggering level,

means for coupling said trigger circuit to said storage means to receive the output voltages from said storage means, said output voltages being indicative of the instantaneous charges acquired by the respective storage means with one of the storage circuits providing progressively increasing output voltage acting in effect as a variable height pedestal upon which the voltage of the other is superimposed as the charges accumulate toward a maximum in each storage element,

traffic actuatable input circuits for the associated respective phases,

electronic gate circuit means for coupling said two electrical storage means with said step-by-step circuit in connection with phases thereof activated for timing of right of way and with said traffic actuatable input circuits for control of said electrical storage means,

said gate circuit means including

means normally to prevent the said storage means from charging toward the preselected voltage levels for timing the active traffic phase in absence of actuation of the input circuit of the inactive phase,

means to initiate charging of the said storage means by said charging means for timing in the active phase in response to actuation of the input circuit of the inactive phase,

means operating upon each traffic actuation of the input circuit for the activated traffic phase to reset to substantially a zero datum level momentarily for restart of charging the storage means requiring the shorter time to acquire the selected voltage level so that during the selected timing period the limiting time gap between actuations of the input circuit in the activated traffic phase is progressively reduced while at the same time the period is prolonged between initiation of charge and the time when the combined average of the voltages to which the storage means charge reaches a preset control level,

said trigger circuit coupling means including

further resistive means having a pair of outer terminals of which one is connected to receive a voltage corresponding to that of one storage means and the other of which is connected to receive a voltage corresponding to that of the second storage means,

a connection from substantially the midpoint of the said further resistive means to the trigger circuit to provide a triggering voltage for the triggering circuit representing the average instantaneous voltage acquired by each of the storage means,

and means controlled from the trigger circuit for activating said step circuit for transferring right of way between the phases following activation of the said triggering circuit.

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THOMAS B. HABECKER, *Primary Examiner.*

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