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(54) VERTICAL NANOTUBE SEMICONDUCTOR DEVICE STRUCTURES AND METHODS OF FORMING THE SAME

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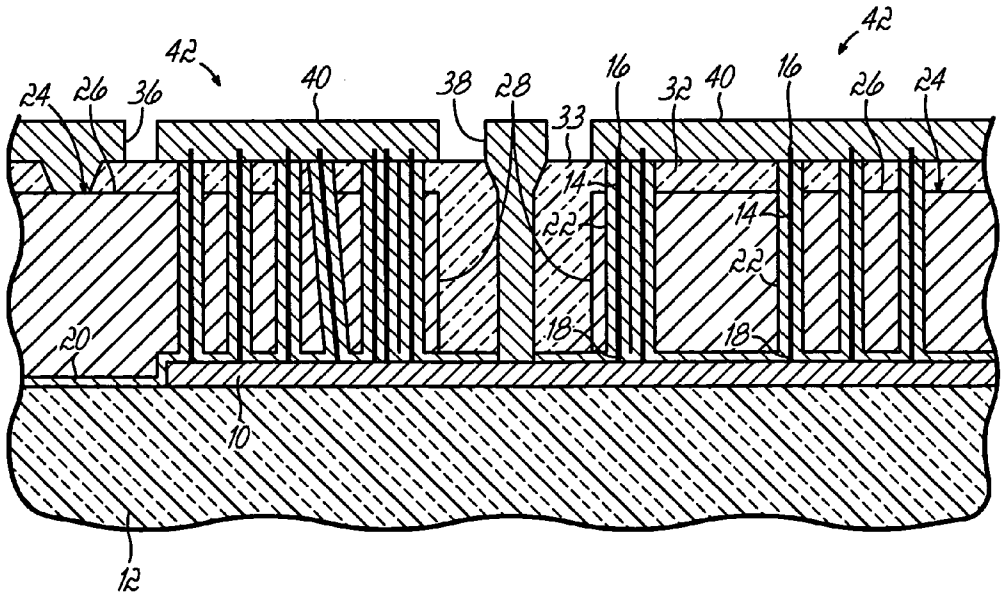
(57) ABSTRACT

Vertical device structures incorporating at least one nanotube and methods for fabricating such device structures by chemical vapor deposition. Each nanotube is grown by chemical vapor deposition catalyzed by a catalyst pad and encased in a coating of a dielectric material. Vertical field effect transistors may be fashioned by forming a gate electrode about the encased nanotubes such that the encased nanotubes extend vertically through the thickness of the gate electrode. Capacitors may be fashioned in which the encased nanotubes and the corresponding catalyst pad bearing the encased nanotubes forms one capacitor plate.



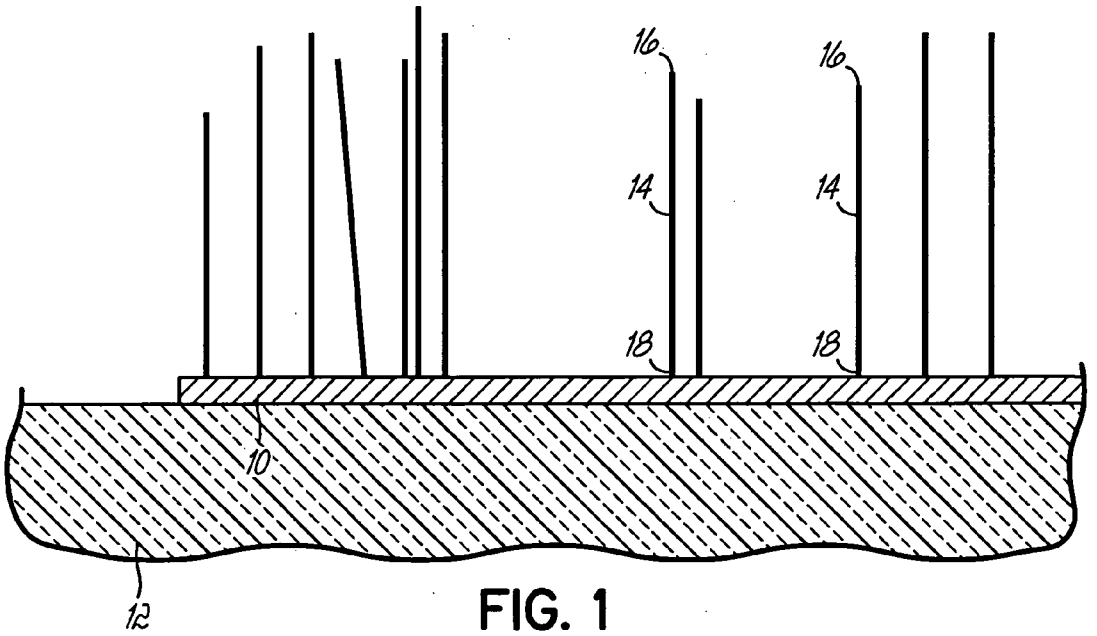


FIG. 1

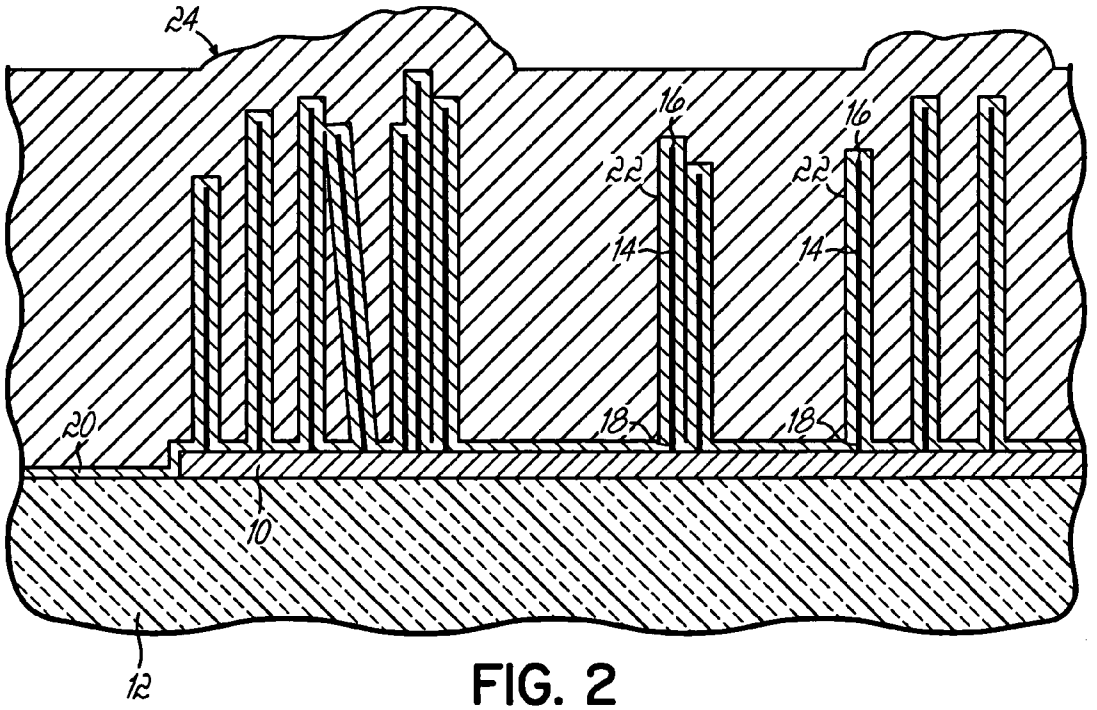


FIG. 2

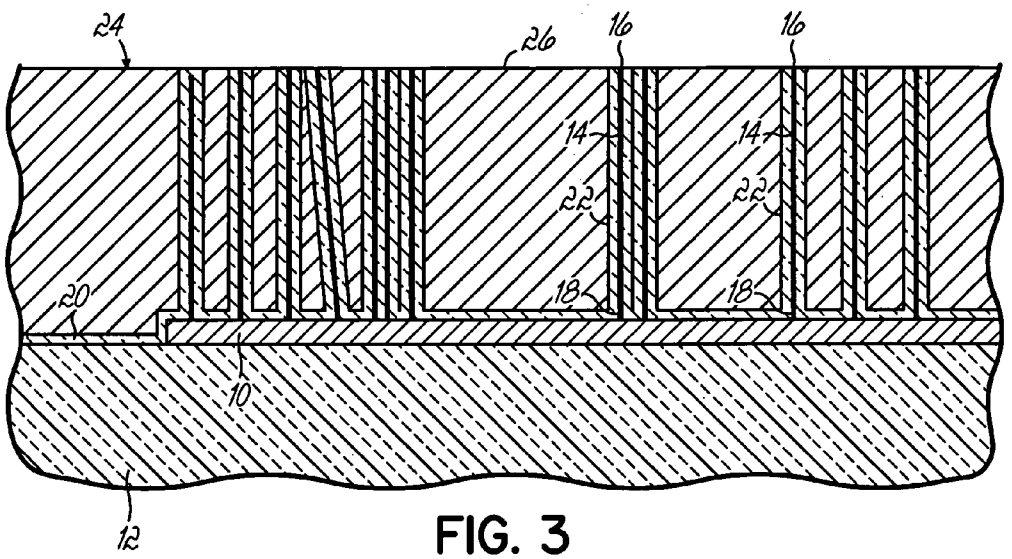

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FIG. 3

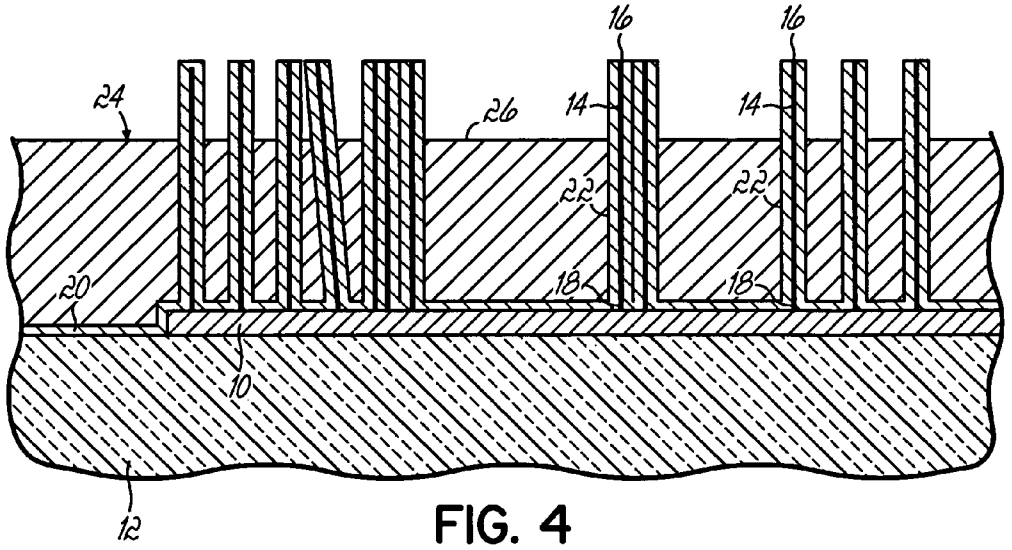
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FIG. 4

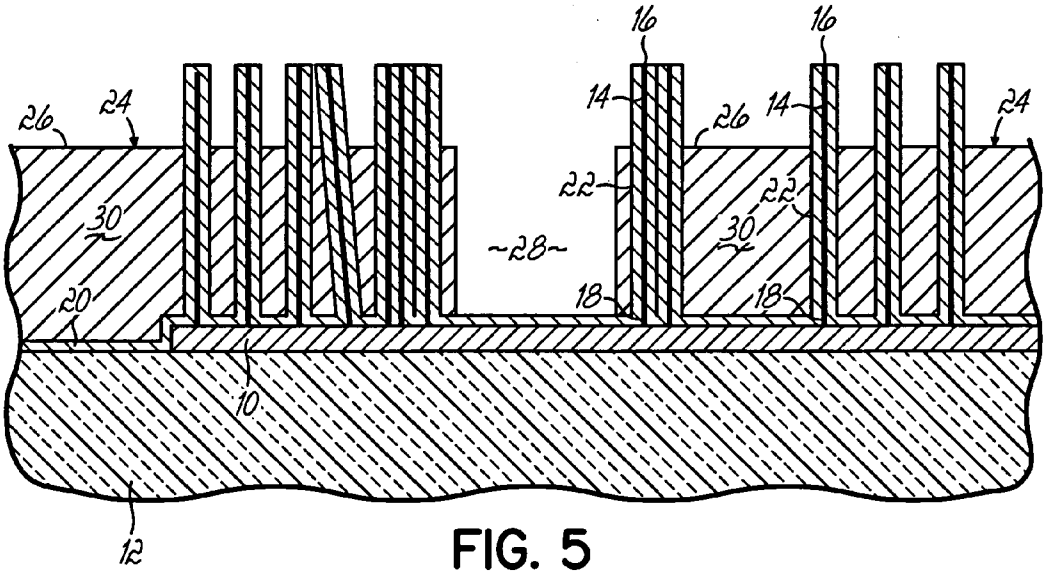
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FIG. 5

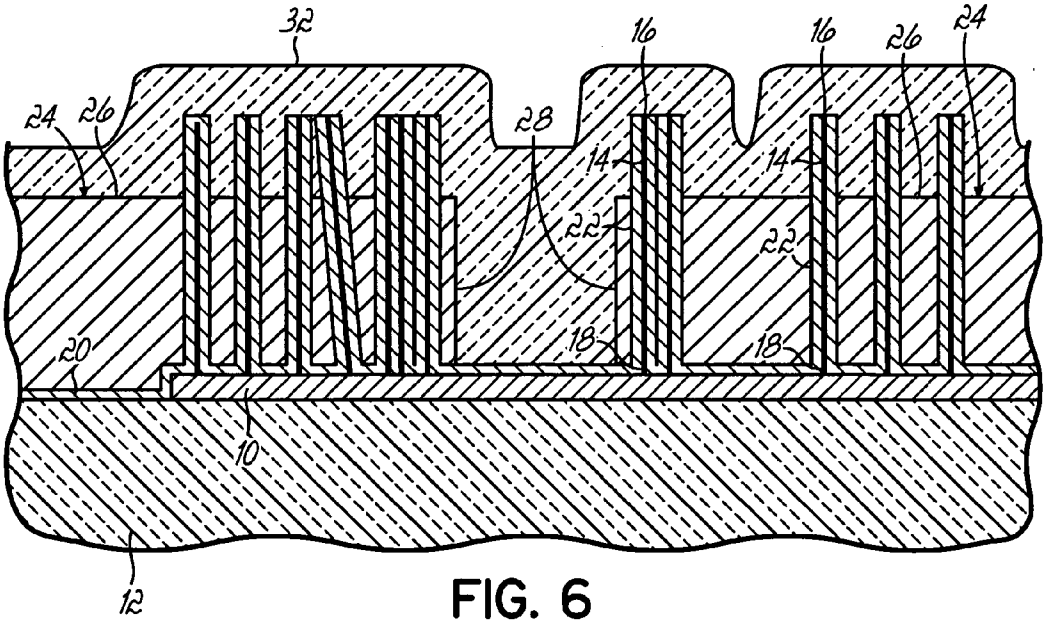
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FIG. 6

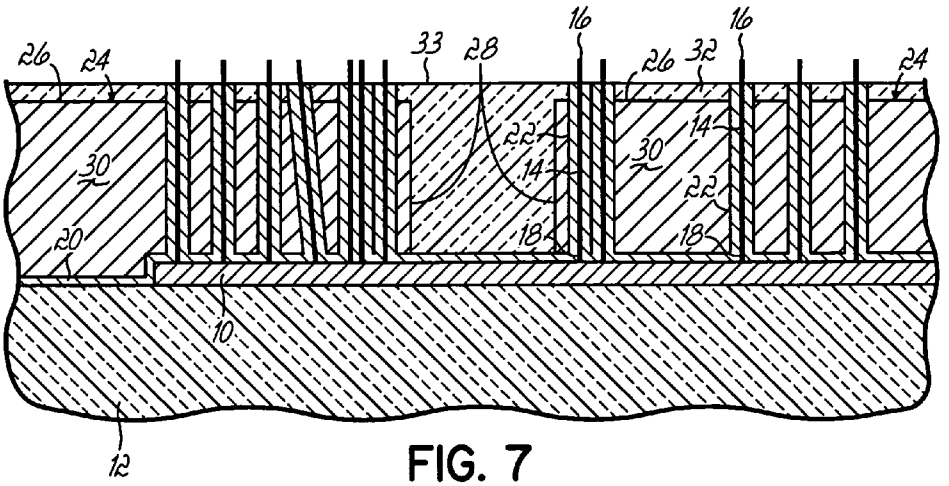
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FIG. 7

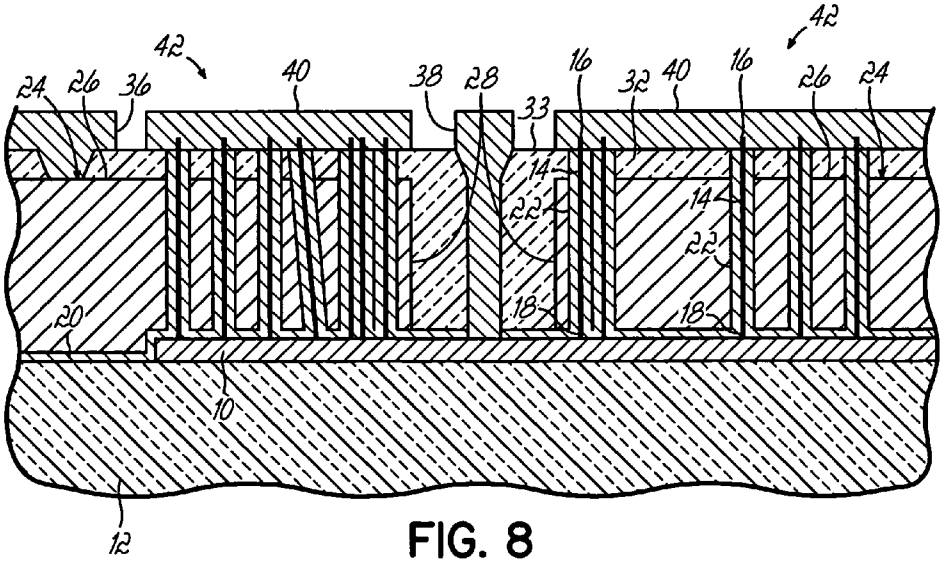
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FIG. 8

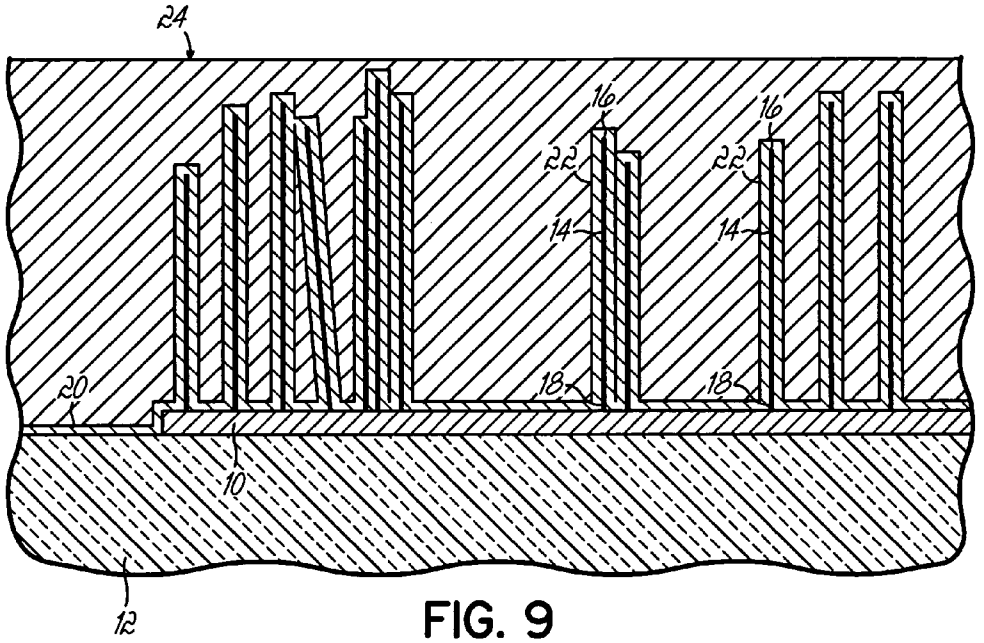
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FIG. 9

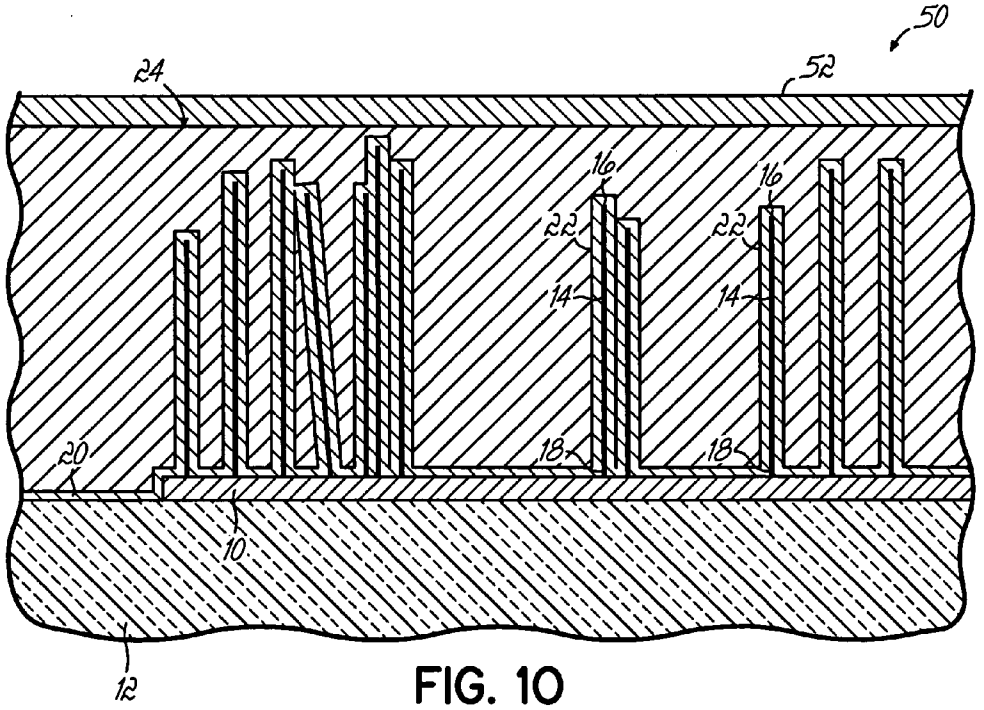
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FIG. 10

VERTICAL NANOTUBE SEMICONDUCTOR DEVICE STRUCTURES AND METHODS OF FORMING THE SAME

FIELD OF THE INVENTION

[0001] The invention relates to semiconductor device fabrication and, more particularly, to vertical semiconductor device structures, such as field effect transistors and capacitors, incorporating nanotubes as a device element and methods of fabricating such vertical semiconductor device structures.

BACKGROUND OF THE INVENTION

[0002] Traditional field effect transistors (FET's) are familiar conventional devices commonly incorporated as a fundamental building block into the intricate circuitry of integrated circuit (IC) chips. A single IC chip may feature many thousands to millions of FET's, along with other passive components such as resistors and capacitors, interconnected by conductive paths. FET's operate by varying the resistivity of a channel in a channel region separating a source and a drain. Carriers flow from the source to the drain through the channel in proportion to the variation in electrical resistivity. Electrons are responsible for channel conduction in n-channel FET's and, in p-channel FET's, holes are responsible for conduction in the channel. The output current of the FET is varied by application of a voltage to an electrostatically-coupled gate electrode located above the channel region between the source and drain. A thin gate dielectric insulates the gate electrode electrically from the channel region. A small change in gate voltage can cause a large variation in the current flowing from the source to the drain.

[0003] FET's can be classified into horizontal architectures and vertical architectures. Horizontal FET's exhibit carrier flow from source to drain in a direction parallel to the horizontal plane of the substrate on which they are formed. Vertical FET's exhibit carrier flow from source to drain in a direction vertical to the horizontal plane of the substrate on which they are formed. Because channel length for vertical FET's does not depend on the smallest feature size resolvable by lithographic equipment and methods, vertical FET's can be made with a shorter channel length than horizontal FET's. Consequently, vertical FET's can switch faster and possess a higher power handling capacity than horizontal FET's.

[0004] Carbon nanotubes are nanoscale high-aspect-ratio cylinders of carbon atoms proposed for use in forming hybrid devices. Carbon nanotubes efficiently conduct in their conducting form and act as a semiconductor in their semiconductor form. Horizontal FET's have been fabricated using a single semiconducting carbon nanotube as a channel region and forming ohmic contacts at opposite ends of the carbon nanotube extending between a gold source electrode and a gold drain electrode situated on the surface of a substrate. A gate electrode is defined in the substrate underlying the carbon nanotube and generally between the source and drain electrodes. An oxidized exposed surface of the substrate defines a gate dielectric between the buried gate electrode and the carbon nanotube. Such horizontal FET's should switch reliably while consuming significantly less power than a comparable silicon-based device structure due to the small dimensions of the carbon nanotube. Horizontal FET's have been successfully formed under laboratory conditions by manipulating single carbon nanotubes using an atomic force microscope or coincidental placement of a single nanotube from a dispersed group of nanotubes. However, these methods of forming such horizontal FET device structures are incompatible with mass production techniques.

[0005] What is needed, therefore, is a vertical FET structure incorporating one or more semiconducting carbon nanotubes as a channel region that is compliant with mass production techniques.

SUMMARY OF THE INVENTION

[0006] In accordance with the principles of the invention, a vertical semiconductor device structure includes a substrate defining a substantially horizontal plane, a gate electrode projecting vertically from the substrate, and at least one semiconducting nanotube extending vertically through the gate electrode between opposite first and second ends. A gate dielectric, which may be disposed on the at least one semiconducting nanotube, electrically insulates the at least one semiconducting nanotube from the gate electrode. A source is electrically coupled with the first end of the at least one semiconducting nanotube and a drain is electrically coupled with the second end of the at least one semiconducting nanotube.

[0007] In another aspect of the invention, a method of forming a semiconductor device structure includes forming a conductive pad on a substrate and then growing at least one semiconducting nanotube extending substantially vertically from the conductive pad between a first end electrically coupled with the conductive pad and a second free end. The method further includes electrically insulating the at least one semiconducting nanotube with a gate dielectric and forming a gate electrode electrically insulated from and overlying the conductive pad, with the at least one semiconductor nanotube extending vertically through the gate electrode. A contact is formed that is electrically coupled with the second end of the at least one semiconducting nanotube and electrically insulated from the gate electrode.

[0008] Each semiconducting nanotube defines a channel region of a field effect transistor having a channel regulated by application of a control voltage to the gate electrode. Consistent with the principles of the invention, the length of the channel region between the source and drain is defined by the vertical dimension or thickness of the gate electrode without the limitations imposed by conventional lithographic processes used in semiconductor device fabrication to form channel regions in conventional field effect transistors.

[0009] In accordance with the principles of the invention, a semiconductor device structure includes a substrate defining a substantially horizontal plane, a conductive first plate disposed on the substrate, and at least one nanotube projecting vertically from the first plate. Each nanotube, which may have a conducting molecular structure or a semiconducting molecular structure, is electrically coupled with the first plate. Positioned vertically above the first plate and the nanotube is a conductive second plate electrically isolated from the first plate and the carbon nanotube by a dielectric layer.

[0010] In another aspect of the invention, a method of forming a semiconductor device structure includes forming a conductive first plate on a substrate and growing at least one nanotube extending substantially vertically from the first plate that is electrically coupled with the first plate. The method further includes encasing each nanotube and covering the first plate with a dielectric layer, and forming a second plate overlying said first plate that is electrically isolated by the dielectric layer from each nanotube and the first plate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with a general description of the invention given above, and the detailed description of the embodiments given below, serve to explain the principles of the invention.

[0012] **FIG. 1** is a cross-sectional view of a portion of a substrate with carbon nanotubes grown vertically on a patterned conductive catalyst pad;

[0013] **FIG. 2** is a cross-sectional view similar to **FIG. 1** at a subsequent fabrication stage;

[0014] **FIG. 3** is a cross-sectional view similar to **FIG. 2** at a subsequent fabrication stage;

[0015] **FIG. 4** is a cross-sectional view similar to **FIG. 3** at a subsequent fabrication stage;

[0016] **FIG. 5** is a cross-sectional view similar to **FIG. 4** at a subsequent fabrication stage;

[0017] **FIG. 6** is a cross-sectional view similar to **FIG. 5** at a subsequent fabrication stage;

[0018] **FIG. 7** is a cross-sectional view similar to **FIG. 6** at a subsequent fabrication stage;

[0019] **FIG. 8** is a cross-sectional view similar to **FIG. 7** at a subsequent fabrication stage;

[0020] **FIG. 9** is a cross-sectional view similar to **FIG. 2** at a subsequent fabrication stage in accordance with an alternative embodiment of the invention; and

[0021] **FIG. 10** is a cross-sectional view similar to **FIG. 9** at a subsequent fabrication stage.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0022] The invention is directed to vertical field effect transistors (FET's) that utilize carbon nanotubes as a semiconducting material for the channel region providing a selective conduction path between a source and a drain when a voltage is applied to an electrostatically-coupled gate electrode. In accordance with the principles of the invention, the length of the channel region between the source and drain is defined by the thickness of the gate electrode, which is substantially equal to the nanotube length, and is not dependent upon a resolution-limited lithographic process. The carbon nanotubes do not have to be individually manipulated for placement between a source and a drain nor does device fabrication depend upon coincidental alignment with the source and drain of one or more nanotubes randomly dispersed on the device surface.

[0023] With reference to **FIG. 1**, a catalyst pad **10** of a catalytic material suitable for supporting the growth of carbon nanotubes **14** is formed as part of a pattern of many pads **10** on a region of an insulating substrate **12**. Carbon nanotubes **14** are oriented to extend substantially vertically upward from the catalyst pad **10**. The insulating substrate **12** may be formed on a wafer (not shown) composed of any suitable semiconductor material, including but not limited to silicon (Si) and gallium arsenide (GaAs), upon which an insulating substrate **12**, such as silicon oxide, may be formed. The catalyst pad **10** may be formed by depositing a blanket layer of the catalytic material on the insulating layer **12** by any conventional deposition technique including, but not limited to, chemical vapor deposition (CVD) using suitable precursors such as metal halides and metal carbonyls, sputtering, and physical vapor deposition (PVD) and then employing a standard lithographic and subtractive etch process to pattern the blanket layer. The catalytic material in catalyst pads **10** is any material capable of nucleating and supporting the growth of carbon nanotubes **14** when exposed to appropriate reactants under chemical reaction conditions suitable to promote nanotube growth. For example, suitable catalytic materials include, but are not limited to, iron, platinum, nickel, cobalt, compounds of each of these metals, and alloys of each of these metals such as metal silicides.

[0024] Carbon nanotubes **14** are grown on the catalytic pad **10** by any suitable growth or deposition technique. In one embodiment of the invention, the carbon nanotubes **14** are grown by chemical vapor deposition (CVD) or plasma-enhanced CVD using any suitable gaseous or vaporized carbonaceous reactant including, but not limited to, carbon monoxide (CO), ethylene (C_2H_4), methane (CH_4), acetylene (C_2H_4), a mixture of acetylene and ammonia (NH_3), a mixture of acetylene and nitrogen (N_2), a mixture of acetylene and hydrogen (H_2), xylene ($C_6H_4(CH_3)_2$), and a mixture of xylene and ferrocene ($Fe(C_5H_5)_2$) under growth conditions suitable for promoting carbon nanotube growth on the catalytic material forming the catalyst pad **10**. The carbonaceous reactant and catalyst pad **10** may be heated to a temperature adequate to promote and/or hasten CVD growth. The reactant chemically reacts with the catalyst material of catalyst pad **10** to nucleate carbon nanotubes **14** and to sustain their growth after nucleation. The catalyst material of the catalyst pad **10** participates in nanotube growth without itself being transformed or consumed by the chemical reaction transpiring at its exposed surface by reducing the activation energy for the reaction forming carbon nanotubes **14** to occur.

[0025] The carbon nanotubes **14** constitute hollow cylindrical tubes composed of precisely arranged groups including hexagonal rings of bonded carbon atoms. The cylindrical tubes have a diameter ranging from about 0.5 nm to about 20 nm and a sidewall thickness of about 0.5 nm to about 3 nm. The carbon nanotubes **14** are expected to have a statistical distribution of heights or lengths each measured between a free end or leading tip **16** and a bonded end or base **18**. The carbon nanotubes **14** extend on average substantially vertically upward from the catalyst pad **10** with a perpendicular or, at the least, approximately perpendicular orientation to the horizontal surface of the catalyst pad **10**. The invention contemplates that one or all of the carbon nanotubes **14** may be inclined slightly from the vertical direction, as defined herein and that the nanotube orientation may be characterized by a statistical distribution that, on

average, is substantially vertical. The nanotube density and spacing between adjacent carbon nanotubes **14** will depend, among other variables, upon the growth conditions. The carbon nanotubes **14** will typically grow at substantially random spatial locations on the exposed surface area of the catalyst pad **10**.

[**0026**] Growth conditions of the CVD or plasma-enhanced CVD process are chosen for preferentially growing carbon nanotubes **14** having a semiconducting electonic structure or molecular structure. Alternatively, carbon nanotubes **14** having a semiconducting molecular structure may be preferentially selected from among a random collection of as-grown nanotubes **14** including both metallic and semiconducting molecular structures by, for example, applying a current sufficiently high to destroy nanotubes **14** having the metallic (e.g., conducting) molecular structure. Post-synthesis destruction of conducting carbon nanotubes is described in commonly-assigned U.S. Pat. No. 6,423,583, which is hereby incorporated by reference herein in its entirety. The invention also contemplates that nanotubes **14** may be composed of a material other than carbon characterized by a band gap and semiconductor properties.

[**0027**] The term "horizontal" as used herein is defined as a plane parallel to the conventional plane or surface of insulating substrate **12** and the underlying wafer, regardless of orientation. The term "vertical" refers to a direction perpendicular to the horizontal, as just defined. Terms, such as "on", "above", "below", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

[**0028**] With reference to **FIG. 2**, a thin dielectric layer **20** is conformally deposited on the catalyst pad **10** and the insulating substrate **12**. Dielectric layer **20** may be constituted by silicon dioxide (SiO_2) deposited by a low pressure chemical vapor deposition (LPCVD) process using tetraethylorthosilicate (TEOS) as the silicon precursor source. The dielectric layer **20** also coats an exterior of each of the carbon nanotubes **14** along their respective height or length. Many other materials may be used instead of TEOS-based oxide, as long as electrical isolation is ensured. The coatings on the carbon nanotubes **14** will define respective gate dielectrics **22** that participate as a feature in the structure of a field effect transistor (FET) device structure, as described below.

[**0029**] A blanket layer **24** of a conducting material deposited on the insulating substrate **12** fills the vacant spaces between adjacent carbon nanotubes **14** and covers the nanotubes **14**, insulating substrate **12**, and catalyst pad **10**. Blanket layer **24** is electrically isolated from the insulating substrate **12** by portions of dielectric layer **20**. Suitable conducting materials for blanket layer **24** include, but are not limited to, doped polycrystalline silicon (polysilicon) and metals such as aluminum (Al), copper (Cu), gold (Au), molybdenum (Mo), tantalum (Ta), titanium (Ti), and tungsten (W). Blanket layer **24** may be deposited by any suitable deposition process such as CVD by thermal decomposition/thermolysis of a metal-containing precursor such as metal halides and metal carbonyls, PVD, or sputtering. The thickness of the blanket layer **24** should completely cover the free ends of the insulator-covered carbon nanotubes **14**. Each gate dielectric **22** electrically isolates the corresponding carbon nanotube **14** from the blanket layer **24**.

[**0030**] With reference to **FIG. 3**, an exposed surface **26** of the blanket layer **24** is polished flat by a chemical-mechanical polishing (CMP) process or any other suitable planarization technique. Generally, CMP processes involve a polishing or mechanical abrasion action aided chemically by a slurry introduced between a polishing pad and blanket layer **24**. The thickness of blanket layer **24** is reduced by removing material to a depth such that the leading tips **16** of a significant number of carbon nanotubes **14** are substantially coplanar with the exposed surface **26** and accessible for subsequent processing.

[**0031**] With reference to **FIG. 4**, the exposed surface **26** of blanket layer **24** is removed selectively to the carbon nanotubes **14** so that the leading tips **16** project above the exposed surface **26**. Techniques for recessing exposed surface **26** include reactive ion etching (RIE) and wet etching with a suitable etchant solution. For example, polysilicon or aluminum constituting blanket layer **24** may be etched by RIE using a chlorine-containing gas, a bromine-containing gas, or a mixture thereof, which is known to be selective to SiO_2. The residual thickness of blanket layer **24** determines the channel length of the FET device structure.

[**0032**] With reference to **FIG. 5**, a recess **28** is formed in the blanket layer **24** that extends vertically from exposed surface **26** to the depth of dielectric layer **20**. The recess **28** is formed by a standard lithographic and etch process that patterns blanket layer **24** to expose unmasked areas in which recess **28** and other similar recesses for other like device structures will be formed and masked areas, and then etched by, for example, a dry etch process using, for example, NH_3 to remove the conductive material in the unmasked areas. Dielectric layer **20** serves as an etch stop layer. The blanket layer **24** is also partitioned or sectioned by a standard lithographic and etch process, which may be the same lithographic and etch process forming recess **28**, into individual gate electrodes **30** that define the future location of individual FET device structures **42** (**FIG. 8**). Any carbon nanotubes **14** that may be present in the unmasked areas of blanket layer **24** are removed by the etch process forming recess **28** or may be eliminated by any other suitable process capable of removing the carbon nanotubes **14** from recess **28**. The invention contemplates that the order of the process steps described with regard to **FIGS. 4 and 5** may be reversed so that the individual gate electrodes **30** are formed before the exposed surface **26** is recessed to expose the leading tips **16** of carbon nanotubes **14**.

[**0033**] With reference to **FIG. 6**, an insulating layer **32** of a dielectric material is conformally provided that fills recess **28** and covers exposed areas of blanket layer **24** to cover the leading tips **16** of carbon nanotubes **14**. The insulating layer **32** may constitute, for example, silicon nitride (Si_3N_4) deposited using LPCVD or plasma-enhanced CVD using NH_3 and silane (SiH_4) as precursor sources or SiO_2, which may be deposited by a CVD process using TEOS as a precursor source. The portion of insulating layer **32** filling recess **28** electrically isolates the adjacent gate electrodes **30** from each other.

[**0034**] With reference to **FIG. 7**, the leading tip **16** of each carbon nanotube **14** is exposed above a planar recessed exposed surface **33** of insulating layer **32** and a length of the associated gate dielectric **22** is removed therefrom. To that end, insulating layer **32** is polished flat by a CMP process or

any other suitable planarization technique to define the exposed surface **33**. The exposed surface **33** is then further recessed relative to the carbon nanotubes **14** using one or more RIE processes that remove insulating layer **32** and gate dielectric **22** to the depth of the recessed exposed surface **33** selective to the carbon nanotubes **14**. Alternatively, a wet etch process using a suitable etchant solution, such as a buffered hydrofluoric acid (HF) solution, may be used. The carbon nanotubes **14** may have a distribution of lengths and although not shown, certain carbon nanotubes **14** may remain buried in the insulating layer **32** and/or the gate electrodes **30** after the exposed surface **33** is recessed.

[**0035**] With reference to **FIG. 8**, gate contacts **36** and source contacts **38** are formed by defining contact openings in insulating layer **32** at appropriate locations with a standard lithographic and etch process and filling the contact openings with a conductive material. The lithographic and etch process also defines areas of conductive material that operate as drain contacts **40**. Each gate contact **36** is electrically coupled, preferably ohmically, with one of the gate electrodes **30** and each source contact **38** is electrically coupled, preferably ohmically, with one of the catalytic pads **10**. Each drain contact **40** is electrically coupled, preferably ohmically, with the leading tips **16** of carbon nanotubes **14** extending through the associated one of the gate electrodes **30**. Contacts **36**, **38** and **40** are electrically isolated from each other and are formed from any suitable conducting materials including, but not limited to, Au, Al, Cu, Mo, Ta, Ti, and W deposited by, for example, CVD, PVD or sputtering. Standard back-end-of-the-line (BEOL) processing is used to fabricate and couple an interconnect structure linking contacts **36**, **38** and **40** with corresponding contacts of adjacent FET's.

[**0036**] The completed device structure **42** forms an FET having a gate or gate region defined by one of the gate electrodes **30**, a source or source region defined by catalyst pad **10** and source contact **38**, a drain or drain region defined by drain contact **40**, a semiconducting channel region defined collectively along the length of the carbon nanotubes **14** extending through the associated gate electrode **30** with a vertical orientation relative to the horizontal plane of the insulating substrate **12**, and a gate dielectric defined by each of the individual gate dielectrics **22** covering the nanotubes **14**. Although only two completed device structures **42** are visible in **FIG. 8**, it is understood that multiple replicas of structure **42** are provided on insulating substrate **12** as detailed herein. Each completed device structure **42** is electrically coupled for device operation with additional circuit components (not shown) supported on adjacent regions of the insulating substrate **12**. Carriers flow selectively from the catalyst pad **10** through the carbon nanotubes **14** to the drain contact **40** when an electrical voltage is either applied via the corresponding gate contact **36** to one of the gate electrodes **30** to create a channel in the carbon nanotubes **14** extending therethrough. The invention contemplates that, in certain embodiments, the catalyst pad **10** and source contact **38** may serve as a drain region and drain contact **40** may act as a source region.

[**0037**] With reference to **FIGS. 9 and 10** in which like reference numerals refer to like features in **FIGS. 1 and 2** and in accordance with an alternative embodiment of the invention, a capacitor device structure **50** (**FIG. 10**) may be formed by a different set of processing steps performed subsequent to the device fabrication stage illustrated in **FIG. 2**. Specifically, the blanket layer **24** of a conducting material is planarized to a depth that is above the dielectric-covered leading tips **16** of the carbon nanotubes **14** and a layer **52** of conducting material is applied to the planarized blanket layer **24**. A contact (not shown) is electrically coupled with the catalyst pad **10** so that the catalyst pad **10** and the carbon nanotubes **14** supply one electrode or plate of the capacitor device structure **50** and the layer **52** supplies the opposite electrode or plate of the capacitor device structure **50**. Dielectric layer **20** electrically isolates the two plates. The presence of the carbon nanotubes **14**, which are covered by the dielectric layer **20**, increases the effective surface area of one of the plates.

[**0038**] As the carbon nanotubes **14** are semiconducting, a superimposed constant bias voltage must be applied to the plates of the capacitor device structure **50** so that the carbon nanotubes **14** conduct current. In an alternative embodiment of the invention, the carbon nanotubes **14** may be grown under growth conditions suitable to provide the conducting molecular structure so that the constant bias voltage is not required.

[**0039**] While the present invention has been illustrated by a description of various embodiments and while these embodiments have been described in considerable detail, it is not the intention of the applicants to restrict or in any way limit the scope of the appended claims to such detail. Additional advantages and modifications will readily appear to those skilled in the art. Thus, the invention in its broader aspects is therefore not limited to the specific details, representative apparatus and method, and illustrative example shown and described. Accordingly, departures may be made from such details without departing from the spirit or scope of applicants' general inventive concept.

1. A vertical semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a gate electrode projecting vertically from said substrate;

at least one semiconducting nanotube extending vertically through said gate electrode between opposite first and second ends;

a gate dielectric electrically insulating said at least one semiconducting nanotube from said gate electrode;

a source electrically coupled with said first end of said at least one semiconducting nanotube; and

a drain electrically coupled with said second end of said at least one semiconducting nanotube.

2. The semiconductor device structure of claim 1 wherein said source is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

3. The semiconducting device structure of claim 1 wherein said drain is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

4. The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode.

5. The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode.

6. The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube is composed of arranged carbon atoms.

7. The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode.

8. The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

9. The semiconducting device structure of claim 1 further comprising:

a plurality of semiconducting nanotubes extending vertically through said gate electrode.

10. The semiconducting device structure of claim 1 wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

11. (canceled)
12. (canceled)
13. (canceled)
14. (canceled)
15. (canceled)
16. (canceled)
17. (canceled)
18. (canceled)
19. (canceled)
20. (canceled)
21. (canceled)
22. (canceled)
23. (canceled)
24. (canceled)

25. A semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a conductive first plate disposed on said substrate,

at least one nanotube projecting vertically from said first plate and electrically coupled with said first plate;

a conductive second plate positioned vertically above said first plate; and

a dielectric layer electrically isolating said second plate from said first plate and said at least one carbon nanotube.

26. The semiconductor device structure of claim 25 wherein said at least one nanotube has a conducting molecular structure.

27. The semiconductor device structure of claim 25 wherein said at least one nanotube has a semiconducting molecular structure.

28. The semiconducting device structure of claim 25 wherein said dielectric layer defines a coating that encases said at least one nanotube.

29. (canceled)
30. (canceled)
31. (canceled)
32. (canceled)

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