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(71) Applicant: **ACM RESEARCH (SHANGHAI) INC.** [CN/CN]; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-Tech Park, Shanghai 201203 (CN).

(72) Inventors: **JIA, Zhaowei**; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-Tech Park, Shanghai 201203 (CN). **WANG, Jian**; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-Tech Park, Shanghai 201203 (CN). **WANG, Hui**; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-Tech Park, Shanghai 201203 (CN).

(74) Agent: **SHANGHAI PATENT & TRADEMARK LAW OFFICE, LLC**; 435 Guiping Road, Shanghai 200233 (CN).

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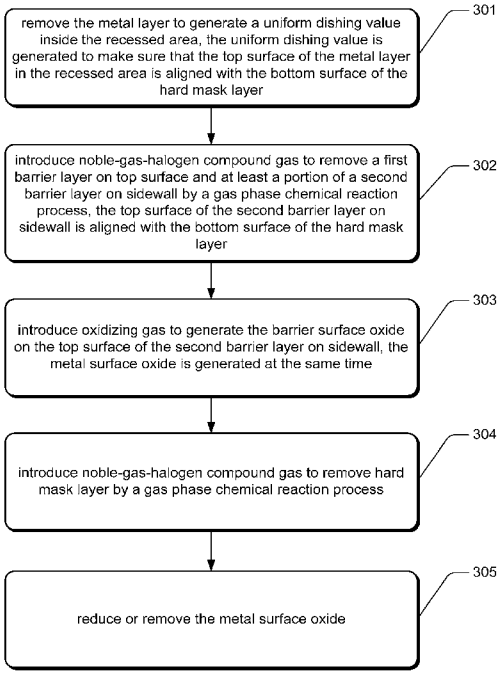

FIG 3

(57) Abstract: A method for processing an interconnection structure for minimizing barrier sidewall recess, comprises the following steps: step 1, remove a metal layer (408) to generate a uniform dishing value inside the recessed area (409), the uniform dishing value is generated to make sure that the top surface of the metal layer (408) in the recessed area (409) is aligned with the bottom surface of the hard mask layer (405), step 2, introduce noble-gas-halogen compound gas to remove a first barrier layer (406) on top surface and at least a portion of a second barrier layer (407) on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer (407) on sidewall is aligned with the bottom surface of the hard mask layer (405), step 3, introduce oxidizing gas to generate a barrier surface oxide (411) on the top surface of the second barrier layer (407) on sidewall, a metal surface oxide (412) is generated at the same time, step 4, introduce noble-gas-halogen compound gas to remove hard mask layer (405) by a gas phase chemical reaction process, step 5, reduce or remove the metal surface oxide (412).

METHOD FOR PROCESSING INTERCONNECTION STRUCTURE FOR MINIMIZING BARRIER SIDEWALL RECESS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to semiconductor manufacture, and more particularly relates to a method for processing an interconnection structure for minimizing barrier sidewall recess.

2. The Related Art

[0002] In semiconductor manufacturing process, along with the advance in IC manufacturing process and improvement in integration degree of chips, copper interconnection has replaced aluminum interconnection as the main tridimensional interconnection in VISI.

[0003] As the density of transistors increases, copper and low k dielectric materials gradually become the mainstream technology of interconnection structures. However, the integration of copper and low k dielectric materials has some technical problems to solve in a practical application, such as barrier sidewall recess problem. FIG.1 shows the cross-sectional view of a typical interconnection structure, the metal layer above the barrier layer has been removed and a uniform dishing value has already generated. Referring to FIG.1, from bottom to top, the interconnection structure includes a substrate 101, an isolation layer 102, a first dielectric layer 103, a second dielectric layer 104, a hard mask layer 105 and a barrier layer. The interconnection structure further comprises a metal layer 108 inside a recessed area 109. The first dielectric layer 103 is a low k dielectric layer，the barrier layer is used for preventing the metal from diffusing into the low k dielectric materials in the interconnection

structure. And the barrier layer could be defined as a first barrier layer 106 on top surface and a second barrier layer 107 on sidewall. The top surface of the metal layer 108 divides the second barrier layer 107 on sidewall into two parts: the upper part and the lower part. Both the first barrier layer 106 on top surface and the upper part of the second barrier layer 107 on sidewall are exposed, but the lower part of the second barrier layer 107 on sidewall is not exposed. The exposed barrier layer of the interconnection structure shall be removed in the next step.

[0004] At present, CMP (chemical mechanical polishing) process is a conventional method for removing the barrier layer. However, the CMP process has several deleterious effects on the underlying structures of the interconnection structures because of the relatively strong mechanical force involved. Especially, when the k value of the dielectric materials increasingly reduces, the mechanical force may cause permanent damage to the dielectric materials. The dielectric materials may be scratched by the CMP process.

[0005] In order to overcome the disadvantages of the CMP process, a more advanced technology, the gas phase etching technology, is used for removing the barrier layer. The gas phase etching technology utilizes chemical gas to react with the barrier layer at a certain temperature and pressure. More about the gas phase etching details can refer to the patent application with the application number PCT/CN2008/072059. Because there is no mechanical stress generated during the whole etching process, so there is no damage to the low k dielectric materials. But with the continuous decrease of the line width, new barrier layer materials, such as cobalt, ruthenium are used instead of conventional barrier layer materials such as Ta, TaN, Ti, TiN, and the thickness of the barrier layer becomes thinner and thinner, both of which increase the difficulty of the gas phase etching. As shown in FIG.2, during the gas phase chemical reaction process, if the end point control is not accurate, the second barrier layer 107 on sidewall may be over etched, and an undesired sidewall recess 110 will be

generated between the dielectric layers and the metal layer 108. Once the second barrier layer 107 on the sidewall is over etched, the metal in the recessed areas 109 diffuses into the low k dielectric layer.

[0006] Referring to the FIG.2, typically, the barrier layer is a layer of Ta and TaN, and the hard mask layer 105 is a layer of TiN. Both the exposed barrier layer and the hard mask layer 105 are removed in one gas phase chemical reaction process at a certain temperature. Since the gas phase chemical reaction process is isotropic, besides the etching rate of TiN is lower than the etching rate of TaN at this operating temperature, the second barrier layer 107 on sidewall will be over etched if the hard mask layer 105 is totally removed. When the gas phase chemical reaction process is over, the result shows that the top surface of the second barrier layer 107 on sidewall is much lower than the top surface of the metal layer 108. So the sidewall recesses 110 are formed, which may cause current leakage issue, and device life time will be shortened.

SUMMARY

[0007] The present invention provides a method for processing an interconnection structure for minimizing barrier sidewall recess. The method comprises the following steps: Step 1,remove a metal layer to generate a uniform dishing value inside the recessed area, the uniform dishing value is generated to make sure that the top surface of the metal layer in the recessed area is aligned with the bottom surface of the hard mask layer. Step 2, introduce noble-gas-halogen compound gas to remove a first barrier layer on top surface and at least a portion of a second barrier layer on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer on sidewall is aligned with the bottom surface of the hard mask layer. Step 3,introduce oxidizing gas to generate a barrier surface oxide on the top surface of the second barrier layer on sidewall, a metal surface oxide is generated at the same time. Step 4,

introduce noble-gas-halogen compound gas to remove hard mask layer by a gas phase chemical reaction process. Step 5, reduce or remove the metal surface oxide.

[0008] As described above, the present invention introduces the oxidizing gas and generates barrier surface oxide on top surface of the second barrier layer on sidewall, to prevent the second barrier layer on sidewall from being over etched, thereby may improve or even overcome the barrier sidewall recess issues.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention will be apparent to those skilled in the art by reading the following description of embodiments thereof, with reference to the attached drawings, in which:

[0010] FIG. 1 is a cross-sectional view illustrating an interconnection structure in prior art.

[0011] FIG. 2 is a cross-sectional view illustrating the barrier layer on sidewall of the interconnection structure shown in FIG.1, which is over etched and the barrier sidewall recess is generated.

[0012] FIG. 3 is a flow chart illustrating the method according to embodiment one of the method for processing an interconnection structure for minimizing barrier sidewall recess.

[0013] FIG. 4 is a cross-sectional view illustrating the interconnection structure according to embodiment one.

[0014] FIG. 5 is a cross-sectional view illustrating the interconnection structure according to embodiment one after the uniform dishing value is generated.

[0015] FIG.6 is a cross-sectional view illustrating the interconnection structure according to embodiment one after the exposed barrier layer is removed.

[0016] FIG.7 is a cross-sectional view illustrating the interconnection structure according to embodiment one after the oxidizing gas is introduced.

[0017] FIG.8 is a cross-sectional view illustrating the interconnection structure according to embodiment one after the hard mask layer is removed.

[0018] FIG.9 is a cross-sectional view illustrating the interconnection structure according to embodiment one after the reducing gas is introduced.

[0019] FIG. 10 is a flow chart illustrating the method according to embodiment two for processing an interconnection structure for minimizing barrier sidewall recess.

[0020] FIG.11 is a cross-sectional view illustrating the interconnection structure according to embodiment two.

[0021] FIG. 12 is a cross-sectional view illustrating the interconnection structure according to embodiment two after the uniform dishing value is generated.

[0022] FIG.13 is a cross-sectional view illustrating the interconnection structure according to embodiment two after the exposed barrier layer is removed.

[0023] FIG.14 is a cross-sectional view illustrating the interconnection structure according to embodiment two after the oxidizing gas is introduced.

[0024] FIG.15 is a cross-sectional view illustrating the interconnection structure according to embodiment two after the hard mask layer is removed.

[0025] FIG.16 is a cross-sectional view illustrating the interconnection structure according to embodiment two after the metal surface oxide is removed.

[0026] FIG.17 is a flow chart illustrating the method for processing an interconnection structure for minimizing barrier sidewall recess.

DETAILED DESCRIPTION OF EMBODIMENTS

[0027] For solving the technical problems in prior art, the present invention provides a method for processing an interconnection structure for minimizing barrier sidewall recess. The method is operated in a processing chamber, and the interconnection structure is located on a wafer surface.

[0028] FIG.3 to FIG.9 show the method and the interconnection structure according to embodiment one of the present invention.

[0029] FIG.3 is a flow chart illustrating the method for processing an interconnection structure for minimizing barrier sidewall recess. The method comprises the following steps:

[0030] Step 301: remove the metal layer 408 to generate a uniform dishing value inside the recessed area 409, the uniform dishing value is generated to make sure that the top surface of the metal layer 408 in the recessed area 409 is aligned with the bottom surface of the hard mask layer 405;

[0031] Step 302: introduce noble-gas-halogen compound gas to remove a first barrier layer 406 on top surface and at least a portion of a second barrier layer 407 on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer 407 on sidewall is aligned with the bottom surface of the hard mask layer 405;

[0032] Step 303: introduce oxidizing gas to generate the barrier surface oxide 411 on the top surface of the second barrier layer 407 on sidewall, the metal surface oxide 412 is generated at the same time;

[0033] Step 304: introduce noble-gas-halogen compound gas to remove hard mask layer 405 by a gas phase chemical reaction process;

[0034] Step 305: reduce the metal surface oxide 412;

[0035] FIG.4 shows the cross-sectional view of the interconnection structure according to embodiment one. Referring to FIG.4, from bottom to top, the interconnection structure includes a substrate 401, an isolation layer 402, a first dielectric layer 403, a second dielectric layer 404, a hard mask layer 405 and a barrier layer. The interconnection structure further comprises a metal layer 408 above the barrier layer and inside a recessed area 409. The first dielectric layer 403 is a low k dielectric layer. The second dielectric layer 404 is a layer of TEOS. And the barrier layer could be defined as a first barrier layer 406 on top surface and a second barrier layer 407 on sidewall. It is known that the barrier layer is used for preventing the metal from diffusing into the low k dielectric materials in the interconnection structure. The first barrier layer 406 on top surface and the second barrier layer 407 on sidewall are layers of Ru. In other embodiments, the material of the barrier layer could be Ta, WN, Co, TaN, etc. The hard mask layer 405 is a layer of TiN. The metal layer 408 above the barrier layer and inside the recessed area is a layer of Cu.

[0036] FIG.5 is a cross-sectional view illustrating the interconnection structure after the uniform dishing value is generated. The metal layer 408 in the recessed area 409 is removed by SFP process in Step 301. SFP process is a stress free polishing process which use electro-polishing to remove Cu, so there is no damage to the low k layer. The metal layer 408 in the recessed area is removed by SFP process, but the barrier layer is not, so a uniform dishing value is generated inside the recessed area 409. This dishing value could be from 0 to 1000Å depending on the thickness of the barrier layer and the hard mask layer. It is preferred that the top surface of the metal layer 408 in the recessed area 409 is aligned with the bottom surface of the hard mask layer 405. In this embodiment, the dishing value in each recessed area 409 is 400Å, and the top surface of the metal layer 408 in the recessed area 409 is aligned to the bottom surface of the hard mask layer 405. In other word, the top surface of the metal layer 408 in the recessed area 409 is aligned to the top surface of the second dielectric layer 404. Since

the uniform dishing is generated, the second barrier layer 407 on sidewall is divided into two parts by the top surface of the rest of the meta layer 408: an upper part and a lower part. The upper part of the second barrier layer 407 on sidewall is exposed after SFP process, and the lower part of the barrier layer 407 on sidewall remains unexposed. So both the exposed barrier layer 406 on top surface and the exposed barrier layer 407 on sidewall need to be removed in the next step.

[0037] FIG.6 shows the exposed barrier layer 407 on sidewall and the exposed barrier layer 406 on top surface are removed by the gas phase chemical reaction process in step 302. In this embodiment, the thickness of the second barrier layer 407 on sidewall is aligned to the thickness of the first barrier layer 406 on top surface. Besides, the gas phase chemical reaction process is isotropic, so after the noble-gas-halogen compound gas is introduced to the processing chamber, the upper part of the second barrier layer 407 on sidewall will be removed, as well as the first barrier layer 406 on top surface. The first barrier layer 406 on top surface is totally removed after the gas phase chemical reaction process, so there is no barrier residual on the top surface of the hard mask layer 405. And the hard mask layer 405 is exposed after the gas phase chemical reaction process. In order to overcome the barrier sidewall recess problem, the gas phase chemical reaction process in Step 302 need to be controlled accurately by an end point control mechanism, so that the exposed second barrier layer 407 on sidewall is removed and the unexposed second barrier layer 407 on sidewall is aligned with the bottom surface of the hard mask layer 405.The end point control mechanism, for example, is to control the gas phase chemical reaction process by the length of time.

[0038] The process conditions of the gas phase chemical reaction process in Step 302 can be set as follows: the operating temperature is from RT (Room temperature) to 400°C, the gas flow rate of the noble-gas-halogen compound gas is from 2sccm to 100sccm, the operating pressure is from 5mTorr to 20Torr. And the noble-gas-halogen compound gas in Step 302 can be one of the following: XeF_2, XeF_4, XeF_6 or KrF_2. An

inert gas, such as Ne or Ar, could also be introduced into the processing chamber with the noble-gas-halogen compound gas as a carrier gas.

[0039] In embodiment one, the process conditions of the gas phase chemical reaction process in Step 302 are as follows: the operating temperature is 110°C, the gas flow rate of the noble-gas-halogen compound gas is 6sccm, the operating pressure is 4Torr. The the noble-gas-halogen compound gas is XeF_2. It takes about 50s to finish the gas phase chemical reaction process in Step 302 at these certain conditions. Since the XeF_2 doesn't react with neither Cu nor low k materials, the low k layer will not be damaged, and the electrical performance and the life time of the IC device will be enhanced.

[0040] Referring to FIG.7. FIG.7 is a cross-sectional view illustrating the interconnection structure after the oxidizing gas is introduced in Step 304. The oxidizing gas is O_2 in this embodiment. In Step 303, after the O_2 is introduced into the processing chamber, the top surface of the second barrier layer 407 on sidewall will be oxidized, as well as the top surface of the rest of the metal layer 408 in the recessed area 409. So the barrier surface oxide 411 is generated on top of the second barrier layer 407 on sidewall, and the metal surface oxide 412 is generated at the same time. Both the barrier surface oxide 411 and the metal surface oxide are very thick. The barrier surface oxide 411 is conductive to prevent the second barrier layer 407 on sidewall from being further etched in the next step, so that the barrier sidewall recess will not be generated. The metal surface oxide 412 is copper surface oxide which is undesired, so it will be processed in subsequent steps.

[0041] In Step 303, the O_2 can be introduced at conditions of the following: the operating temperature is from 150°C to 400°C, the gas flow rate of the O_2 is from 0.1 to 20slm, the operating pressure is from 200Torr to 800Torr. The operating temperature is important, because there will be no obvious oxidization occurring on the barrier layer if the operating temperature is lower than 150°C. What's more, if the

operating temperature is higher than 400°C, the interconnection structure will be damaged by thermo stress. Meanwhile,the oxidization threshold temperature of TiN is 800°C, so the hard mask layer 405 will not be oxidized at current conditions. In this embodiment in Step 303, the O_2 is introduced at conditions of the following: the operating temperature is 180°C, the gas flow rate of the O_2 is 20slm,the operating pressure is 1atm, and the process time is 60s.

[0042] FIG.8 is a cross-sectional view illustrating the interconnection structure in embodiment one after the hard mask layer 405 is removed in Step 304 In Step 304, noble-gas-halogen compound gas is introduced into the processing chamber to remove the hard mask layer 405. The noble-gas-halogen compound gas is XeF_2. Since the top surface of the barrier layer 407 on sidewall is protected by the barrier surface oxide 411, and the hard mask layer 405 of TiN is not oxidized, so in the end of the gas phase chemical reaction process in Step 304, only the hard mask layer 405 will be removed by XeF_2. The second barrier layer 407 on sidewall is not further etched in the gas phase chemical reaction process in Step 304, so that the barrier sidewall recess problem is avoided.

[0043] According to the experimental data, there is a positive correlation between the etching rate of TiN and temperature. Therefore, in order to achieve a better effect and etching efficiency, the processing conditions in the gas phase chemical reaction process in Step 304 are a little different from the gas phase chemical reaction process in Step 302. The processing conditions in the gas phase chemical reaction process in Step 304 are as follows: the operating temperature is from 150°C to 400°C, the gas flow rate of the noble-gas-halogen compound gas is from 2sccm to 100sccm, the operating pressure is from 5mTorr to 20Torr. An inert gas, such as Ne or Ar, could also be introduced into the processing chamber with the noble-gas-halogen compound gas as a carrier gas.

[0044] FIG.9 is a cross-sectional view illustrating the interconnection structure in embodiment one after the reducing gas is introduced in Step 305. The top surface of the metal layer 408 should be Cu instead of copper surface oxide, so the metal surface oxide 412 need to process. In Step 305, a reducing gas is introduced to the processing chamber to reduce the metal surface oxide 412. The reducing gas is a mixed gas of N_2 and H_2, and the ratio of H_2 is below 4% for safety. After the reducing gas is introduced to the processing chamber, the metal surface oxide 412 is reduced to Cu. The barrier surface oxide 411 still exists on top of the barrier layer 407 on sidewall after the reducing gas is introduced, but it has little impact on follow-up processes.

[0045] FIG.10 to FIG.16 show the method and the interconnection structure according to embodiment two of the present invention.

[0046] FIG.10 is a flow chart illustrating the method for processing an interconnection structure for minimizing barrier sidewall recess. The method comprises the following steps:

[0047] Step 501: remove the metal layer 608 to generate a uniform dishing value inside the recessed area 609, the uniform dishing value is generated to make sure that the top surface of the metal layer 608 in the recessed area 609 is aligned with the bottom surface of the hard mask layer 605;

[0048] Step 502: introduce noble-gas-halogen compound gas to remove a first barrier layer 606 on top surface and at least a portion of a second barrier 607 layer on sidewall by a gas phase chemical reaction process, the top surface of the second barrier 607 layer on sidewall is aligned with the bottom surface of the hard mask layer 605;

[0049] Step 503: introduce oxidizing gas to generate the barrier surface oxide 611 on the top surface of the second barrier layer 607 on sidewall, the metal surface oxide 612 is generated at the same time;

[0050] Step 504: introduce noble-gas-halogen compound gas to remove hard mask layer 605 by a gas phase chemical reaction process;

[0051] Step 505: remove the metal surface oxide 612.

[0052] FIG.11 shows the cross-sectional view of the interconnection structure in embodiment two. Referring to FIG.11, from bottom to top, the interconnection structure includes a substrate 601, an isolation layer 602, a first dielectric layer 603, a second dielectric layer 604, a hard mask layer 605 and a barrier layer. The interconnection structure further comprises a metal layer 608 above the barrier layer and inside a recessed area 609.The first dielectric layer 603 is a low k dielectric layer. The second dielectric layer 604 is a layer of TEOS. And the barrier layer could be defined as the first barrier layer 606 on top surface and the second barrier layer 607 on sidewall. It is known that the barrier layer is used for preventing the metal from diffusing into the low k dielectric materials in the interconnection structure. The first barrier layer 606 on top surface , as well as the second barrier layer 607 on sidewall are two layers of Ta and TaN. In other embodiments, the material of the barrier layer could be Ru, Co, etc. The hard mask layer 605 is a layer of TiN. The metal layer 608 above the barrier layer and inside the recessed area is a layer of Cu.

[0053] FIG.12 is a cross-sectional view illustrating the interconnection structure after the uniform dishing value is generated. Since the dishing value in this embodiment is not very large, the metal layer 608 in the recessed area 609 is also removed by CMP process in Step 501.The metal layer 608 in the recessed area is removed by CMP process, but the barrier layer is not, so a uniform dishing value is generated inside the recessed area 609.This dishing value could be from 0 to 100Å depending on the thickness of the barrier layer and the hard mask layer. It is preferred that the top surface of the metal layer 608 in the recessed area 609 is aligned with the bottom surface of the hard mask layer 605. In this embodiment, the dishing value in each

recessed area 609 is 100Å, and the top surface of the metal layer 608 in the recessed area 609 is aligned to the bottom surface of hard mask layer 605. In other words, the top surface of the metal layer 608 in the recessed area 609 is aligned to the top surface of the second dielectric layer 604.Since the uniform dishing is generated, the second barrier layer 607 on sidewall is divided into two parts by the top surface of the rest of the meta layer 608:the upper part and the lower part. The upper part of the second barrier layer 607 on sidewall is exposed after CMP process, and the lower part of the second barrier layer 607 on sidewall remains non-exposed. So both the exposed barrier layer 606 on top surface and the exposed barrier layer 607 on sidewall need to be removed in the next step.

[0054] FIG.13 shows the exposed barrier layer 607 on sidewall and the exposed barrier layer 606 on top surface are removed by the gas phase chemical reaction process in step 502. In this embodiment, the thickness of the second barrier layer 607 on sidewall is thicker than the thickness of the first barrier layer 606 on top surface. Besides, the gas phase chemical reaction process is isotropic, so after the noble-gas-halogen compound gas is introduced to the processing chamber, the upper part of the second barrier layer 607 on sidewall will be removed, but only a portion of the first barrier layer 606 on top surface will be removed. The barrier layer 606 on top surface is not totally removed, so there is some barrier residual on the top surface of the hard mask layer 605.Therefore, not the top surface but the side part of the hard mask layer 605 is exposed. In order to overcome the barrier sidewall recess problem, the gas phase chemical reaction process in Step 502 need to be controlled accurately by an end point control mechanism, so that the exposed barrier layer 607 on sidewall is removed and the non-exposed barrier layer 607 on sidewall is aligned with the bottom surface of the hard mask layer 605.The end point control mechanism, for example, is to control the gas phase chemical reaction process by detecting the variation of reflection rate .

[0055] The process conditions of the gas phase chemical reaction process in Step 502 can be set as follows: the operating temperature is from RT(Room temperature) to 400°C, the gas flow rate of the noble-gas-halogen compound gas is from 2sccm to 100sccm, the operating pressure is from 5mTorr to 10Torr. And the noble-gas-halogen compound gas in Step 502 can be a mixture of at least two of the following: XeF_2, XeF_4, XeF_6 or KrF_2.An inert gas, such as Ne or Ar, could also be introduced into the processing chamber with the noble-gas-halogen compound gas as a carrier gas.

[0056] In embodiment two, the process conditions of the gas phase chemical reaction process in Step 502 are as follows: the operating temperature is 400°C, the gas flow rate of the noble-gas-halogen compound gas is 100sccm, the operating pressure is 20Torr.The the noble-gas-halogen compound gas is XeF_2 and KrF_2.It takes about 40s to finish the gas phase chemical reaction process in Step 502 at these certain conditions. Since the XeF_2 and KrF_2 don't react with neither Cu nor low k materials, the low k layer will not be damaged, and the electrical performance and the life time of the IC device will be enhanced.

[0057] Referring to FIG.14.FIG.14 is a cross-sectional view illustrating the interconnection structure after the oxidizing gas is introduced in Step 503. The oxidizing gas is O_3 in this embodiment. In Step 503, after the O_3 is introduced into the processing chamber, the top surface of the second barrier layer 607 on sidewall will be oxidized, as well as the top surface of the rest of the metal layer 608 in the recessed area 609.Moreover, the barrier residual on the top surface of the hard mask layer 605 is also oxidized. The barrier surface oxide 611 is generated on top of the second barrier layer 607 on sidewall, and the metal surface oxide 612 is generated at the same time. Both the barrier surface oxide 611 and the metal surface oxide are very thick. The barrier surface oxide 611 is conductive to prevent the second barrier layer 607 on sidewall from being further etched in the next step, so that the barrier sidewall recess

will not be generated. The metal surface oxide 612 is copper surface oxide which is undesired, so it will be processed in subsequent steps.

[0058] In Step 503, the O_3 can be introduced at conditions of the following: the operating temperature is from 150°C to 400°C, the gas flow rate of the O_3 is from 0 to 20slm, the operating pressure is from 200Torr to 800Torr.The operating temperature is important, because there will be no obvious oxidization occurring on the barrier layer if the operating temperature is lower than 150°C.What's more, if the operating temperature is higher than 400°C, the interconnection structure will be damaged by thermo stress. Meanwhile, the oxidization threshold temperature of TiN is 800°C, so the hard mask layer 605 will not be oxidized at current conditions. In this embodiment in Step 504, the O_3 is introduced at conditions of the following: the operating temperature is 150°C, the gas flow rate of the O_2 is 10slm, the operating pressure is 200Torr.

[0059] FIG.15 is a cross-sectional view illustrating the interconnection structure in embodiment two after the hard mask layer 605 is removed in Step 504. In Step 504 noble-gas-halogen compound gas is introduced into the processing chamber to remove the hard mask layer 605. The noble-gas-halogen compound gas is a mixture of at least two of the following: XeF_2, XeF_4, XeF_6 or KrF_2.An inert gas, such as Ne or Ar, could also be introduced into the processing chamber with the noble-gas-halogen compound gas as a carrier gas. Since the top surface of the second barrier layer 607 on sidewall is protected by the barrier surface oxide 611, and the hard mask layer 605 of TiN is not oxidized, so in the end of the gas phase chemical reaction process in Step 504, the hard mask layer 605 will be removed from the side part with the oxided barrier residual by the noble-gas-halogen compound gas. the second barrier layer 607 is not further etched in the gas phase chemical reaction process in Step 504 so that the barrier sidewall recess problem is avoided.

[0060] According to the experimental data, there is a positive correlation between the etching rate of TiN and temperature. Therefore, in order to achieve a better effect and etching efficiency, the processing conditions in the gas phase chemical reaction process in Step 504 are a little different from the gas phase chemical reaction process in Step 502.The processing conditions in the gas phase chemical reaction process in Step 504 are as follows: the operating temperature is from 150°C to 400°C, the gas flow rate of the noble-gas-halogen compound gas is from 2sccm to 100sccm, the operating pressure is from 5mTorr to 20Torr.

[0061] FIG.16 is a cross-sectional view illustrating the interconnection structure in embodiment two after the metal surface oxide 612 is removed in Step 505. The top surface of the metal layer 608 should be Cu instead of copper surface oxide, so the metal surface oxide 612 need to be further processed. In Step 505, the metal surface oxide 612 is removed by the means of citric acid solution cleaning. The citric acid is diluted with DIW, and the concentration of the citric acid solution is from 1% to 2%. After the citric acid solution cleaning, the metal surface oxide 612 is removed. The barrier surface oxide 611 still exists on top of the second barrier layer 607 on sidewall after the reducing gas is introduced, but it has little impact on follow-up processes.

[0062] Given the above, a method for processing an interconnection structure for minimizing barrier sidewall recess is disclosed in the present invention. As shown in FIG.17,the method comprises:

Step 1, remove a metal layer to generate a uniform dishing value inside the recessed area, the uniform dishing value is generated to make sure that the top surface of the metal layer in the recessed area is aligned with the bottom surface of the hard mask layer ;

Step 2, introduce noble-gas-halogen compound gas to remove a first barrier layer on top surface and at least a portion of a second barrier layer on sidewall by a

gas phase chemical reaction process, the top surface of the second barrier layer on sidewall is aligned with the bottom surface of the hard mask layer;

Step 3, introduce oxidizing gas to generate a barrier surface oxide on the top surface of the second barrier layer on sidewall, a metal surface oxide is generated at the same time;

Step 4, introduce noble-gas-halogen compound gas to remove hard mask layer by a gas phase chemical reaction process;

Step 5, reduce or remove the metal surface oxide.

[0063] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. Such modifications and variations that may be apparent to those skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

CLAIMS

1. A method for processing an interconnection structure for minimizing barrier sidewall recess, comprising:

step 1, removing a metal layer to generate a uniform dishing value inside the recessed area, the uniform dishing value is generated to make sure that the top surface of the metal layer in the recessed area is aligned with the bottom surface of the hard mask layer;

step 2, introducing noble-gas-halogen compound gas to remove a first barrier layer on top surface and at least a portion of a second barrier layer on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer on sidewall is aligned with the bottom surface of the hard mask layer;

step 3, introducing oxidizing gas to generate a barrier surface oxide on the top surface of the second barrier layer on sidewall, a metal surface oxide is generated at the same time;

step 4, introducing noble-gas-halogen compound gas to remove hard mask layer by a gas phase chemical reaction process;

step 5, reducing or removing the metal surface oxide.

2. The method of claim 1, wherein the oxidizing gas is O_2 or O_3.

3.The method of claim 1, wherein the noble-gas-halogen compound gas is one of the following: XeF_2, XeF_4, XeF_6 or KrF_2.

4. The method of claim 1, wherein the noble-gas-halogen compound gas is a mixture of at least two of the following: XeF_2, XeF_4, XeF_6 or KrF_2.

5. The method of claim 1, wherein the material of the barrier layer is a layer of Ta, TaN, Ru, Co, W, WN, Hf; or a combination of two different layers of the above.

6. The method of claim 1, wherein the material of the hard mask layer is a layer of TiN.

7. The method of claim 1, wherein the gas phase chemical reaction process is controlled by an end point control mechanism.

8. The method of claim 1, wherein the dishing value is within a range of 0Å to 1000Å.

9. The method of claim 2, wherein in step 3,the O_2 or O_3 is introduced at conditions of the following: the operating temperature is from 150°C to 400°C,the gas flow rate of the O_2 is from 0 to 20slm,the operating pressure is from 200Torr to 800Torr.

10. The method of claim 1, wherein in step 2,the process conditions of the gas phase chemical reaction process are as follows: the operating temperature is from RT to 400°C,the gas flow rate of the noble-gas-halogen compound gas is from 2sccm to 100sccm,the operating pressure is from 5mTorr to 20Torr.

11. The method of claim 1, wherein in step 4,the process conditions of the gas phase chemical reaction process are as follows: the operating temperature is from 150°C to 400°C,the gas flow rate of the noble-gas-halogen compound gas is from 2sccm to 100sccm,the operating pressure is from 5mTorr to 20Torr.

12. The method of claim 1, wherein in step 5, the metal surface oxide is reduced by a reducing gas.

13. The method of claim 1, wherein in step 5, the metal surface oxide is removed by the means of citric acid solution cleaning.

14. The method of claim 13,wherein in step 6,the citric acid is diluted with DIW, and the concentration of the citric acid solution is from 1% to 2%.

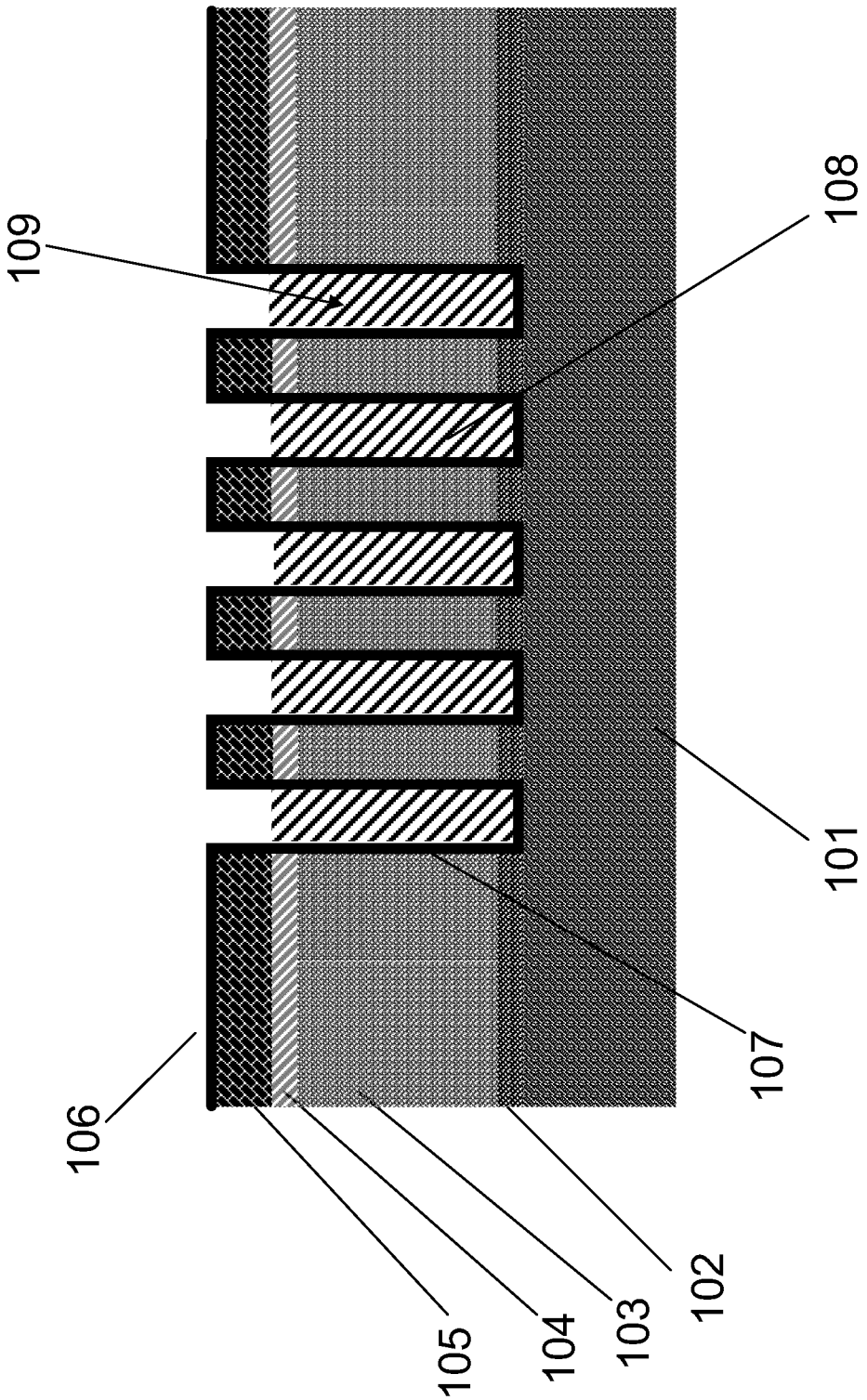

FIG 1

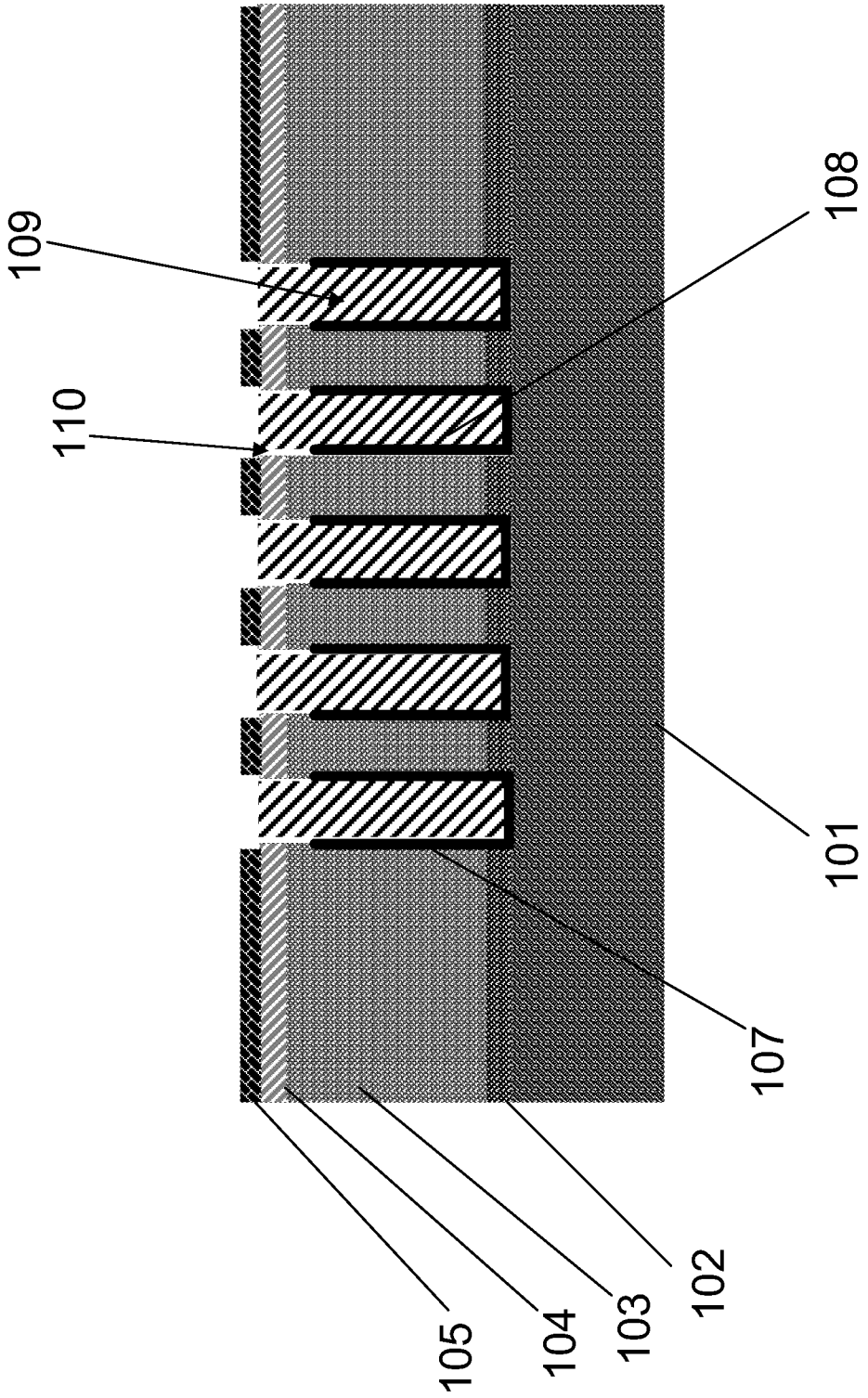

FIG 2

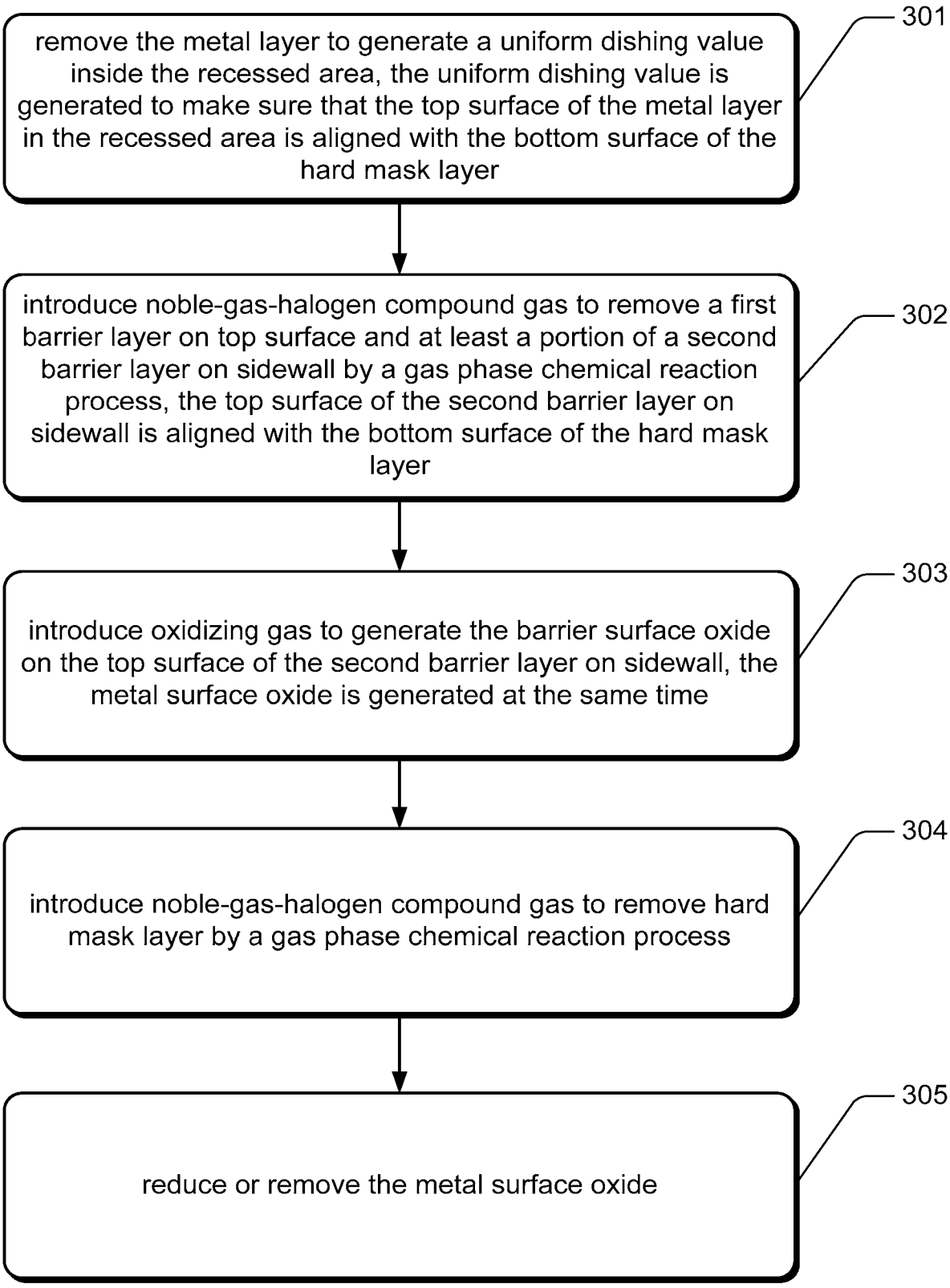
remove the metal layer to generate a uniform dishing value inside the recessed area, the uniform dishing value is generated to make sure that the top surface of the metal layer in the recessed area is aligned with the bottom surface of the hard mask layer
301
introduce noble-gas-halogen compound gas to remove a first barrier layer on top surface and at least a portion of a second barrier layer on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer on sidewall is aligned with the bottom surface of the hard mask layer
302
introduce oxidizing gas to generate the barrier surface oxide on the top surface of the second barrier layer on sidewall, the metal surface oxide is generated at the same time
303
introduce noble-gas-halogen compound gas to remove hard mask layer by a gas phase chemical reaction process
304
reduce or remove the metal surface oxide
305

FIG 3

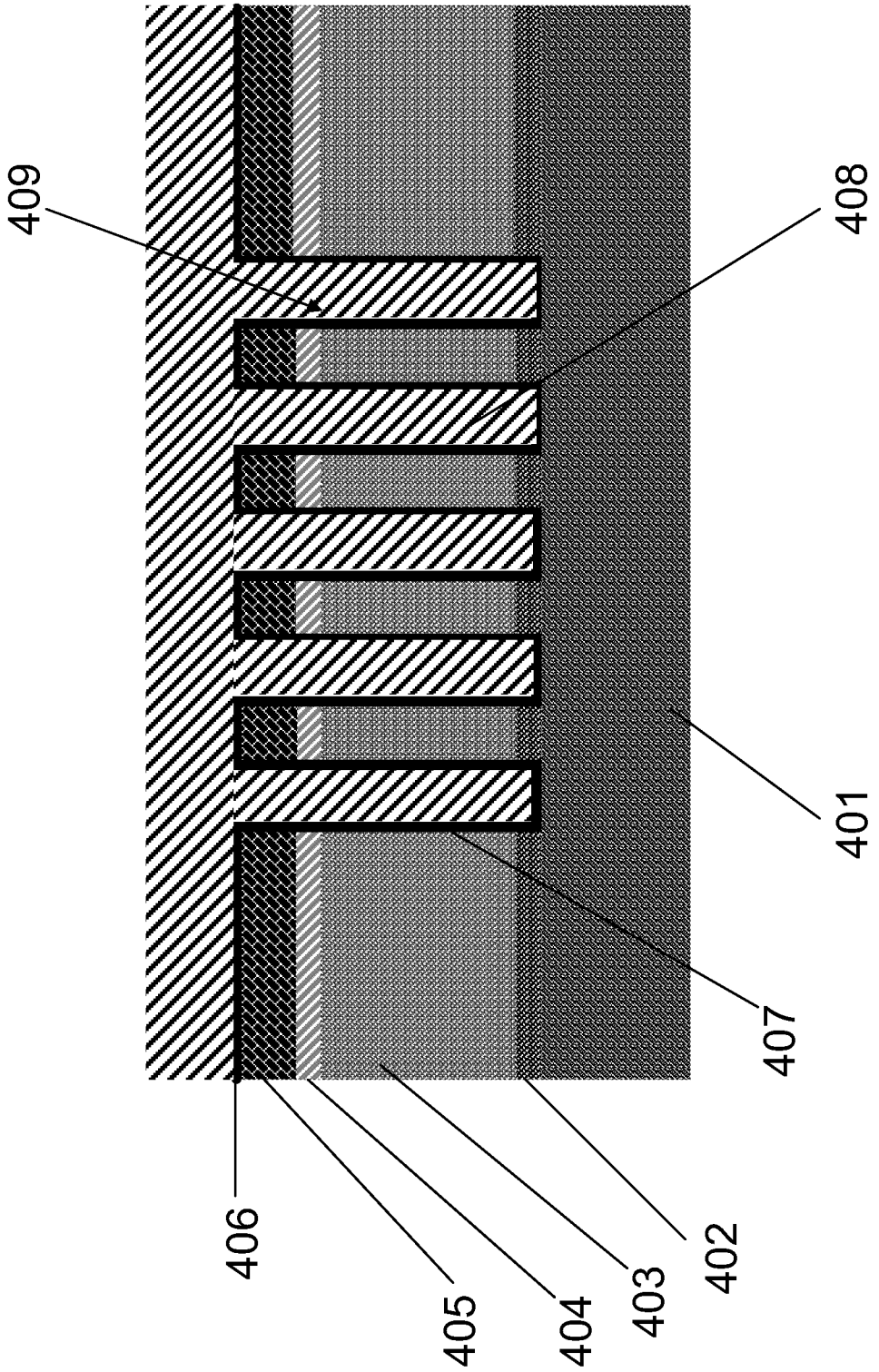

FIG 4

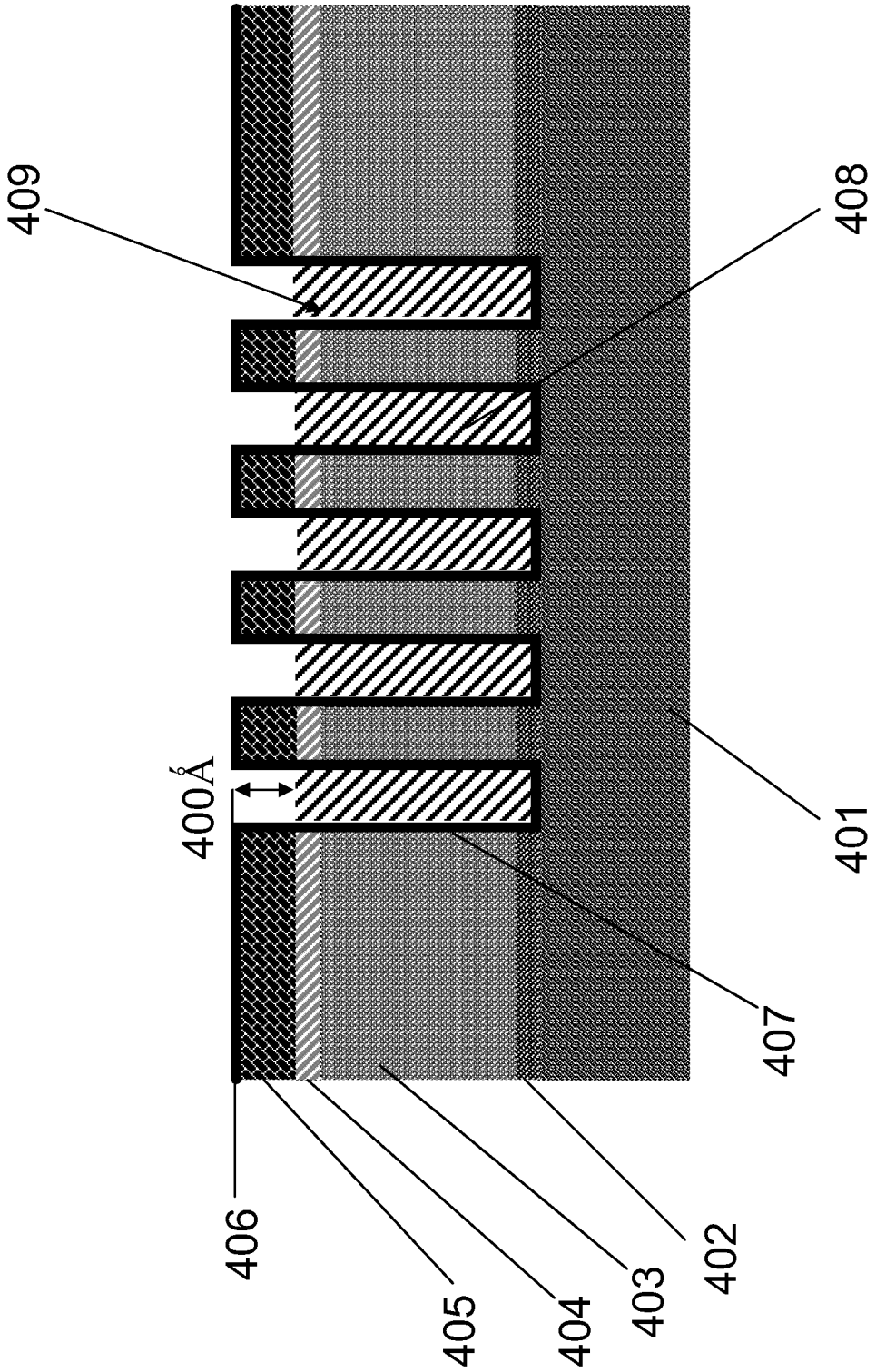

FIG 5

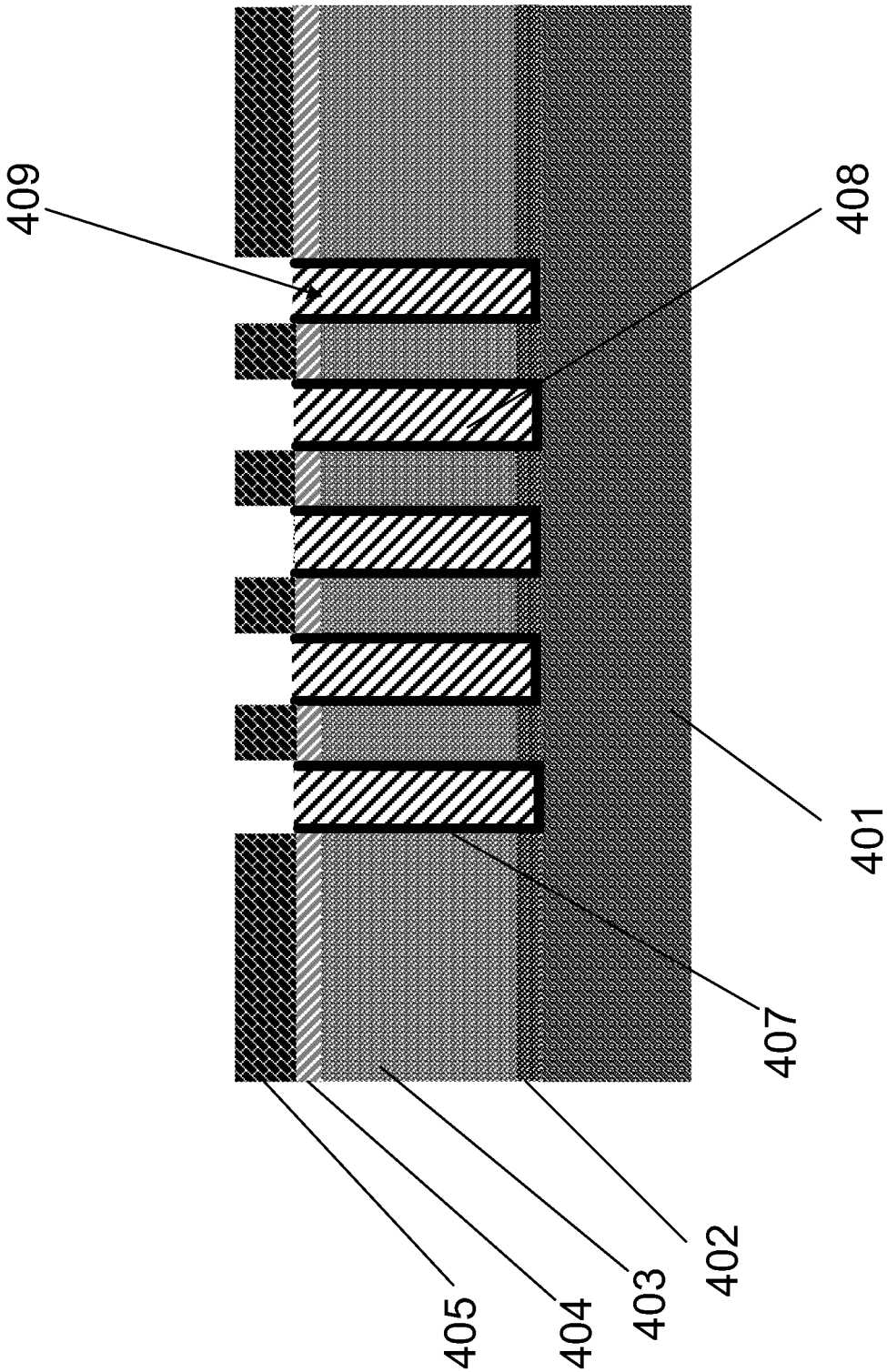

FIG 6

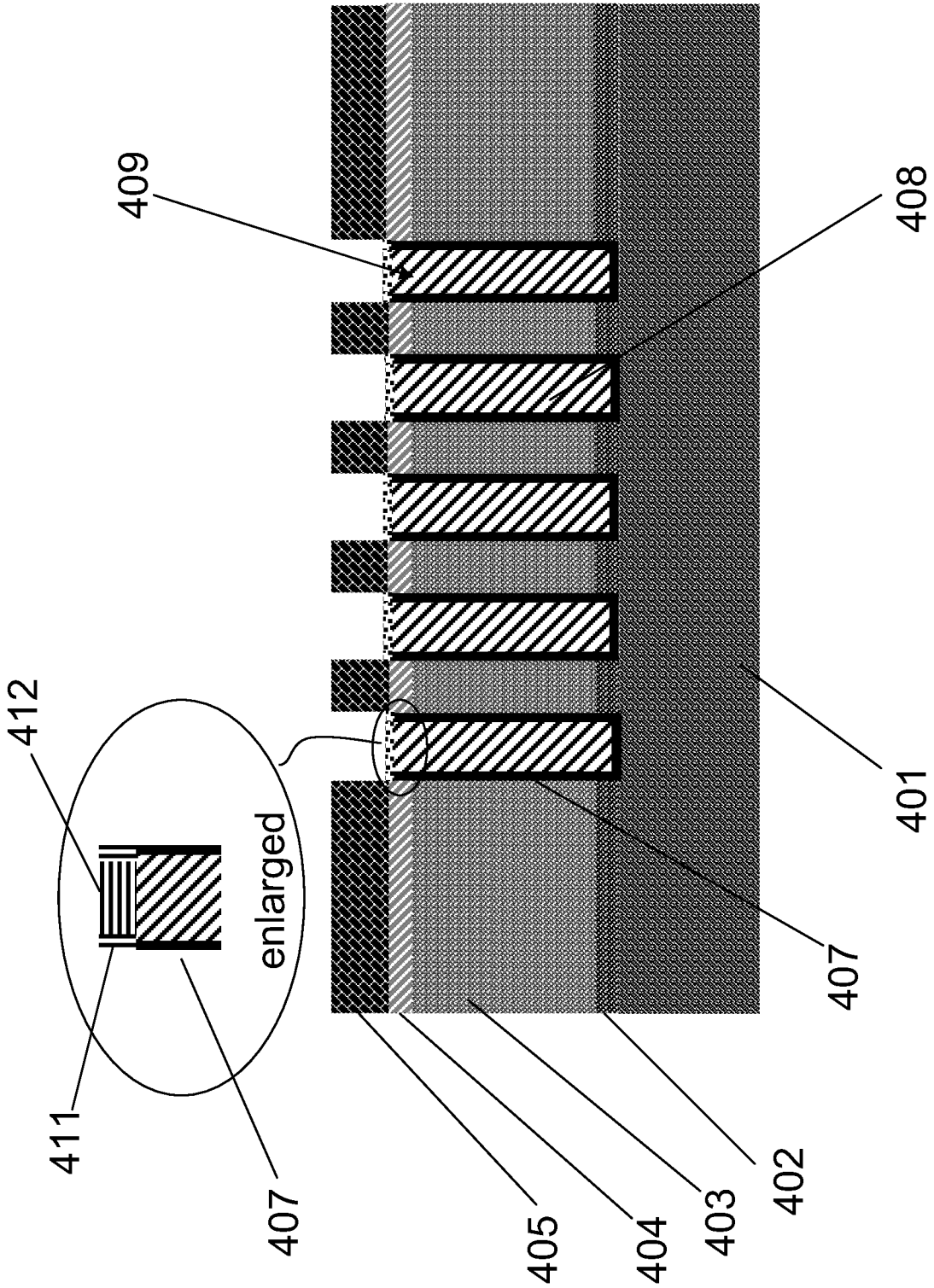

FIG 7

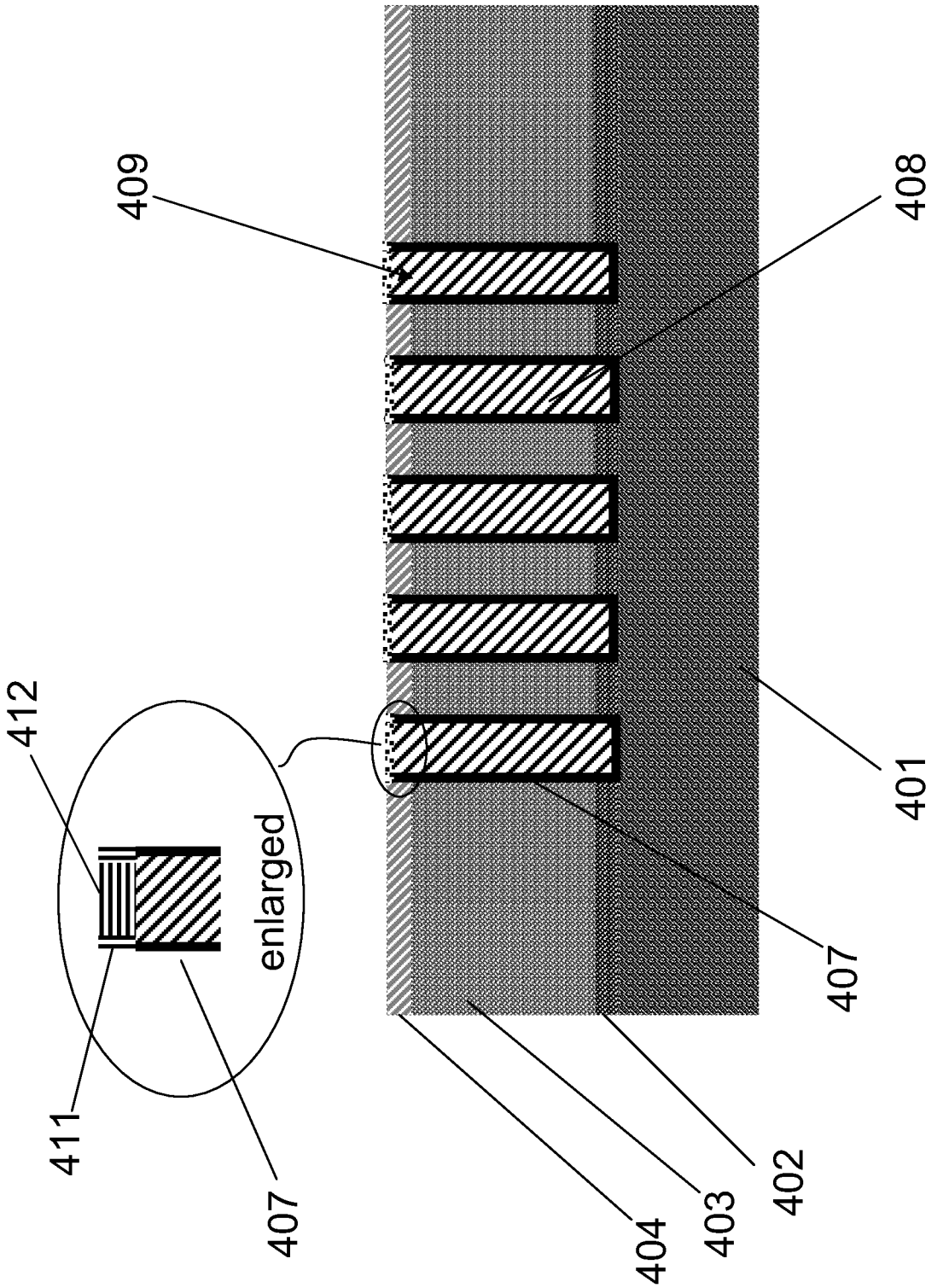

FIG 8

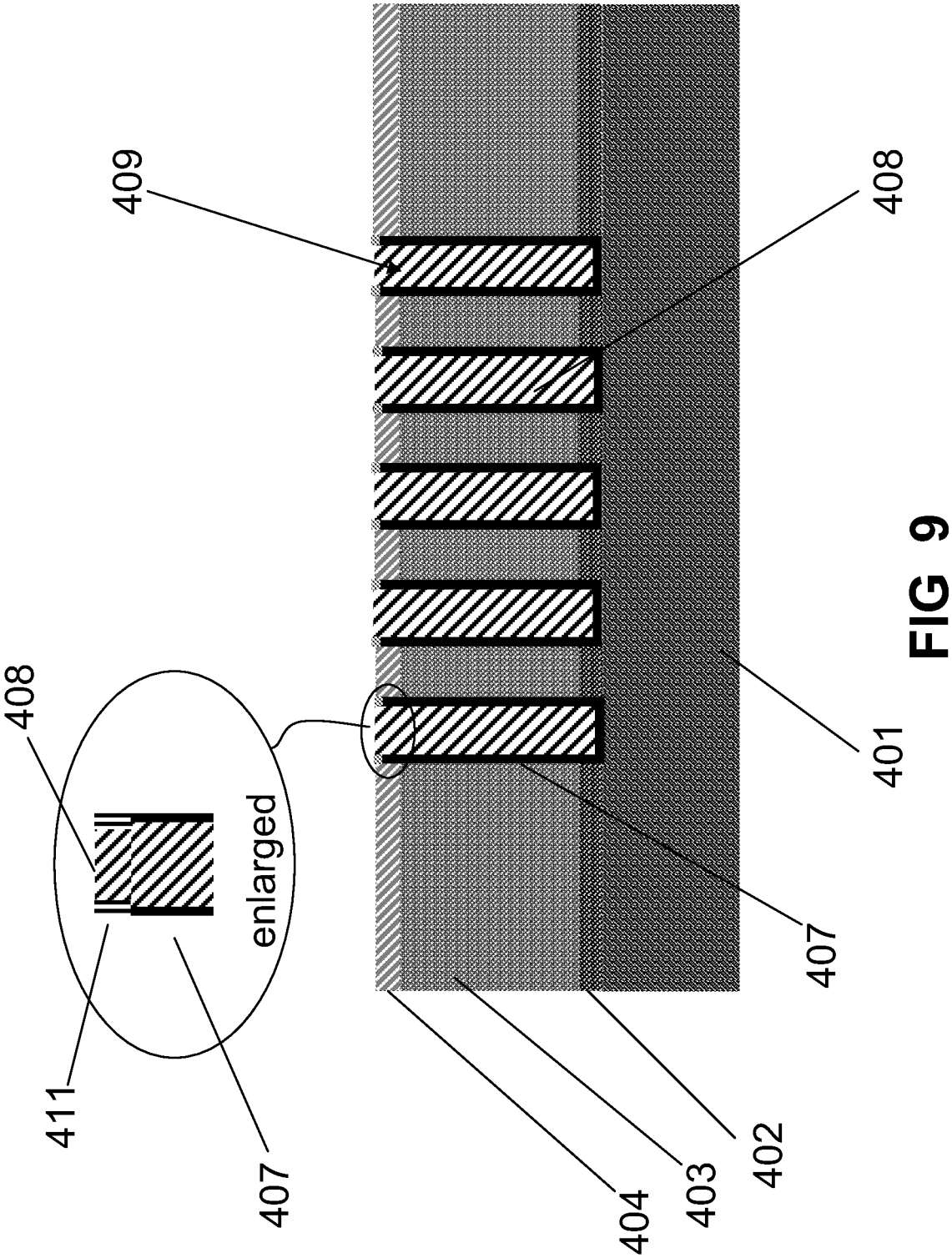

FIG 9

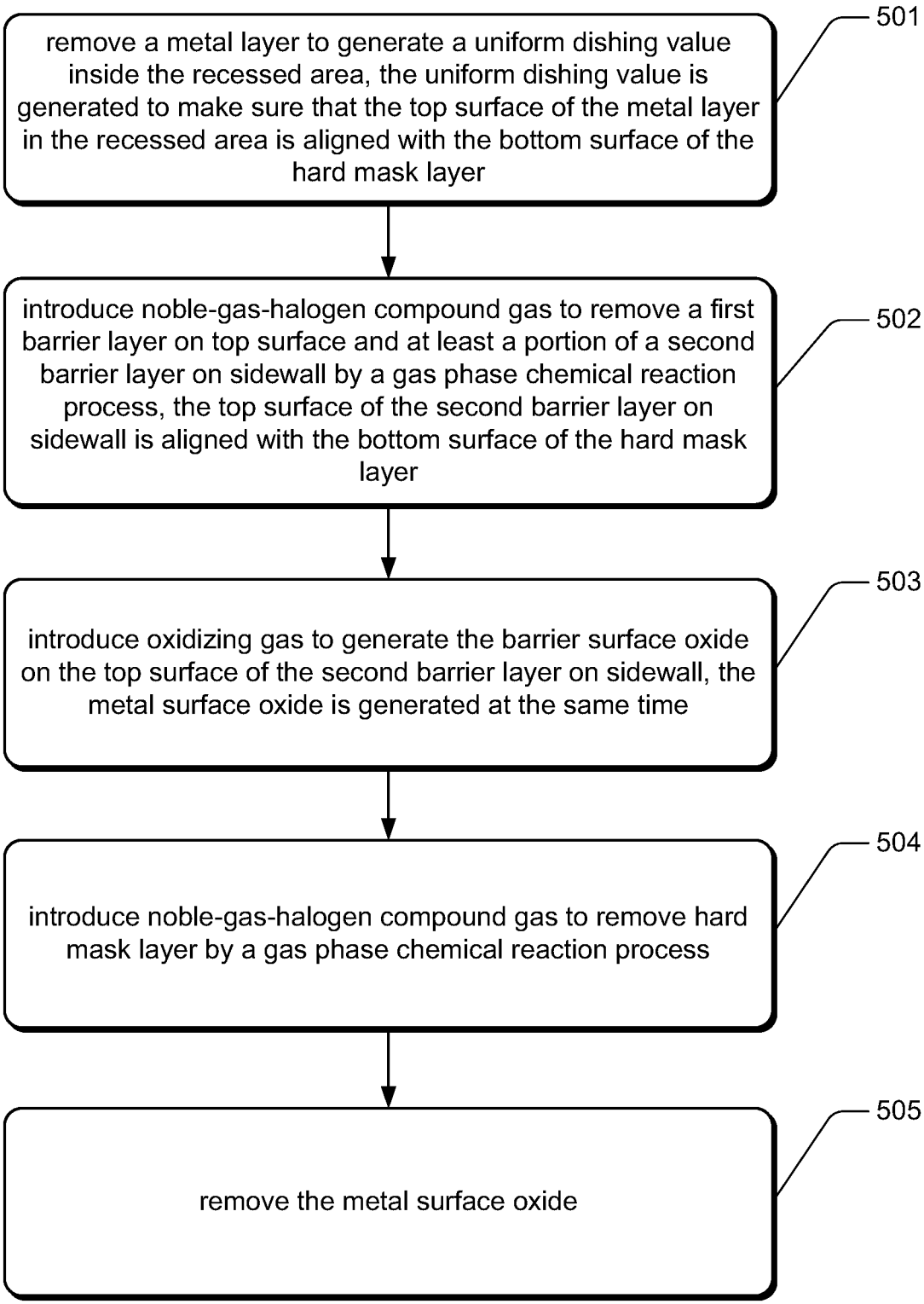
remove a metal layer to generate a uniform dishing value inside the recessed area, the uniform dishing value is generated to make sure that the top surface of the metal layer in the recessed area is aligned with the bottom surface of the hard mask layer
501
introduce noble-gas-halogen compound gas to remove a first barrier layer on top surface and at least a portion of a second barrier layer on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer on sidewall is aligned with the bottom surface of the hard mask layer
502
introduce oxidizing gas to generate the barrier surface oxide on the top surface of the second barrier layer on sidewall, the metal surface oxide is generated at the same time
503
introduce noble-gas-halogen compound gas to remove hard mask layer by a gas phase chemical reaction process
504
remove the metal surface oxide
505

FIG 10

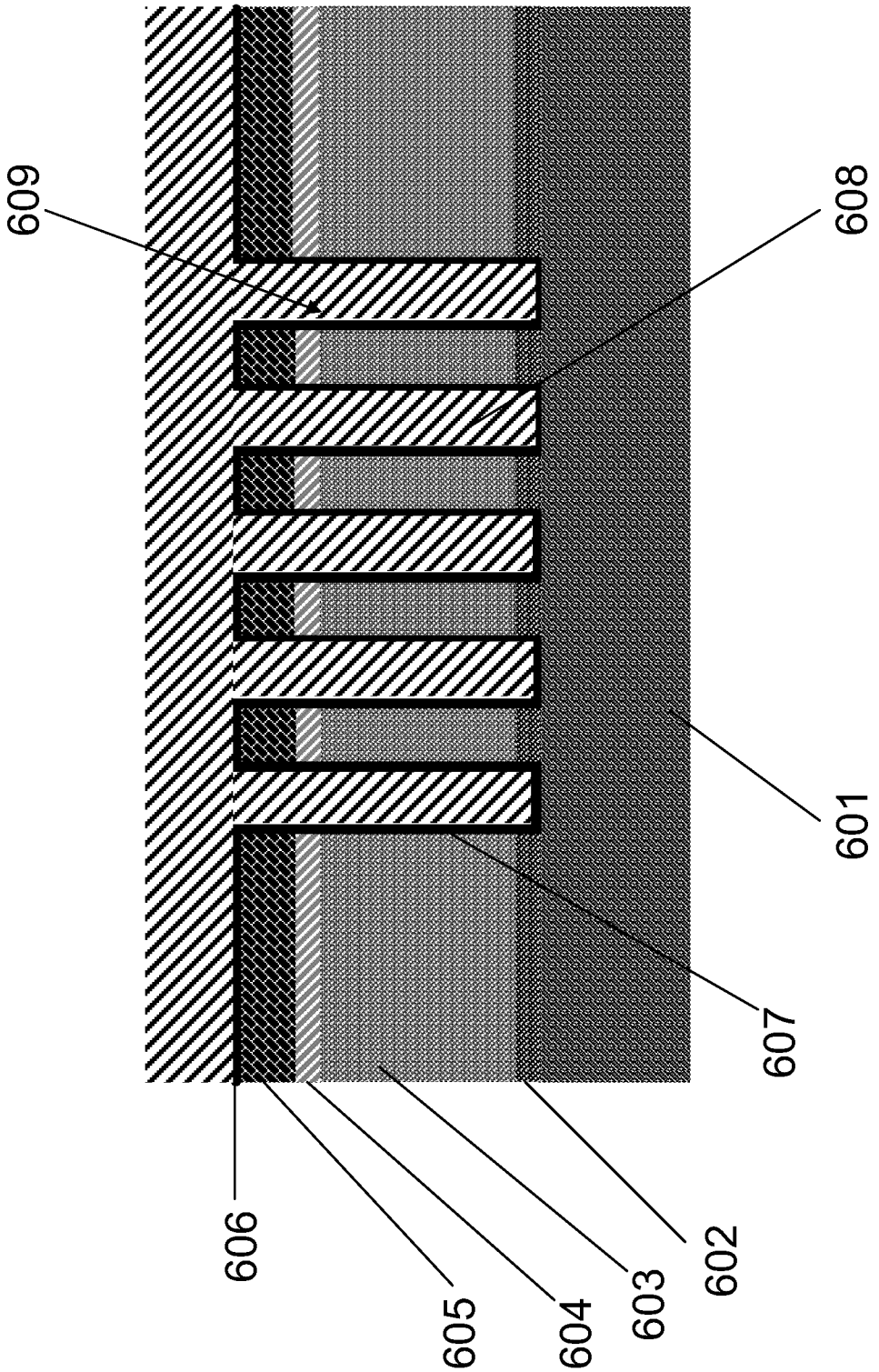

FIG 11

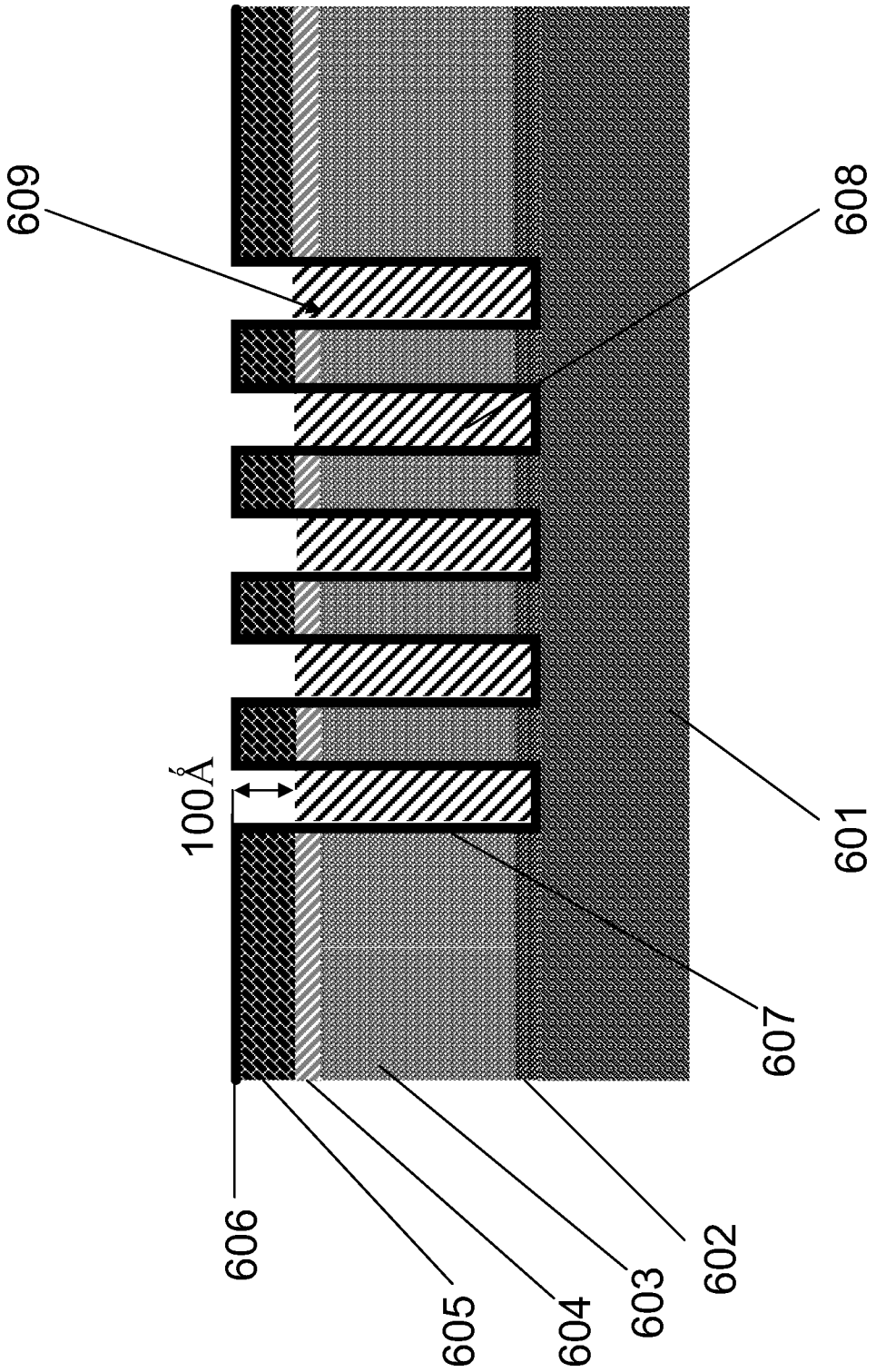

FIG 12

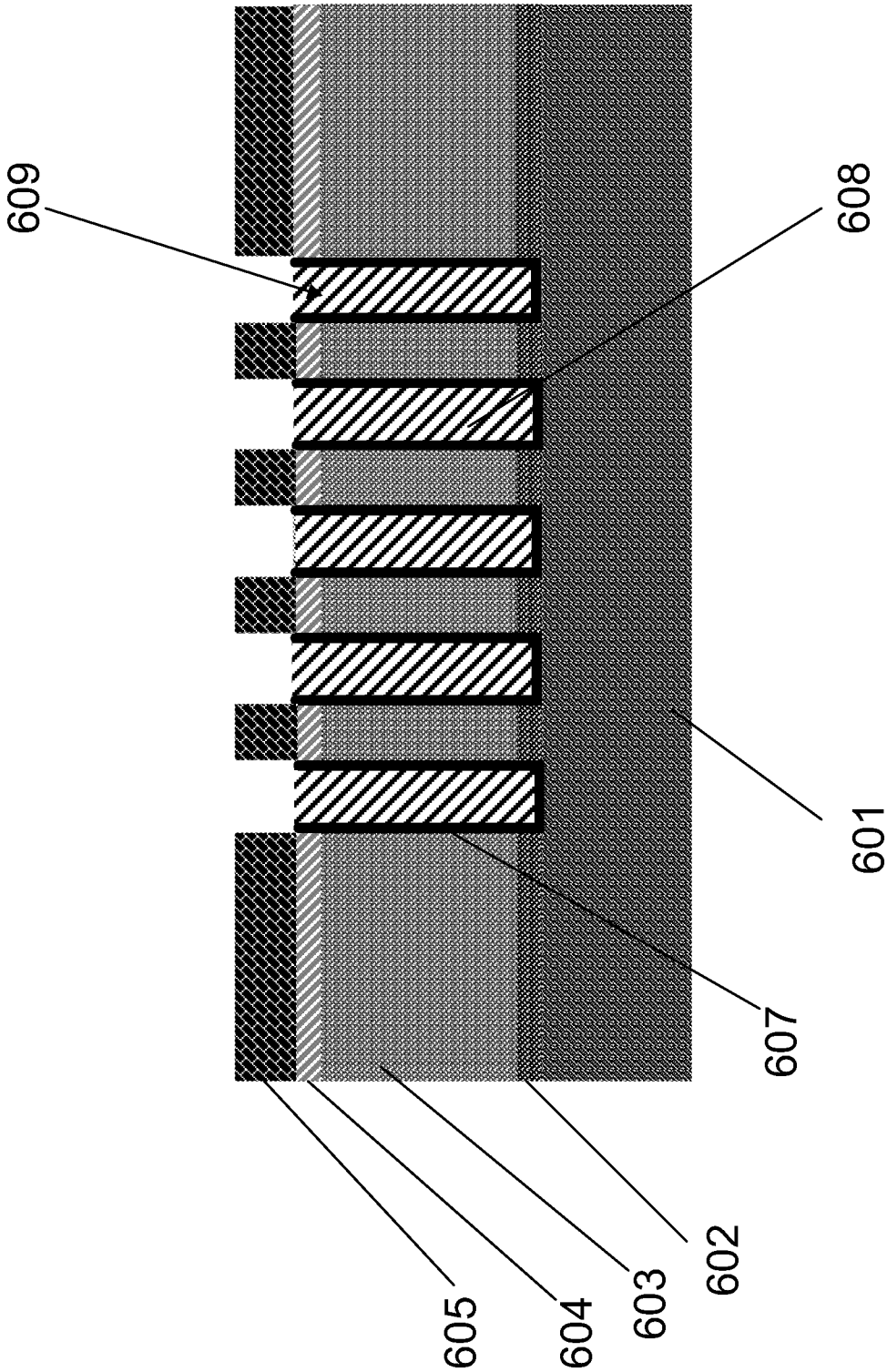

FIG 13

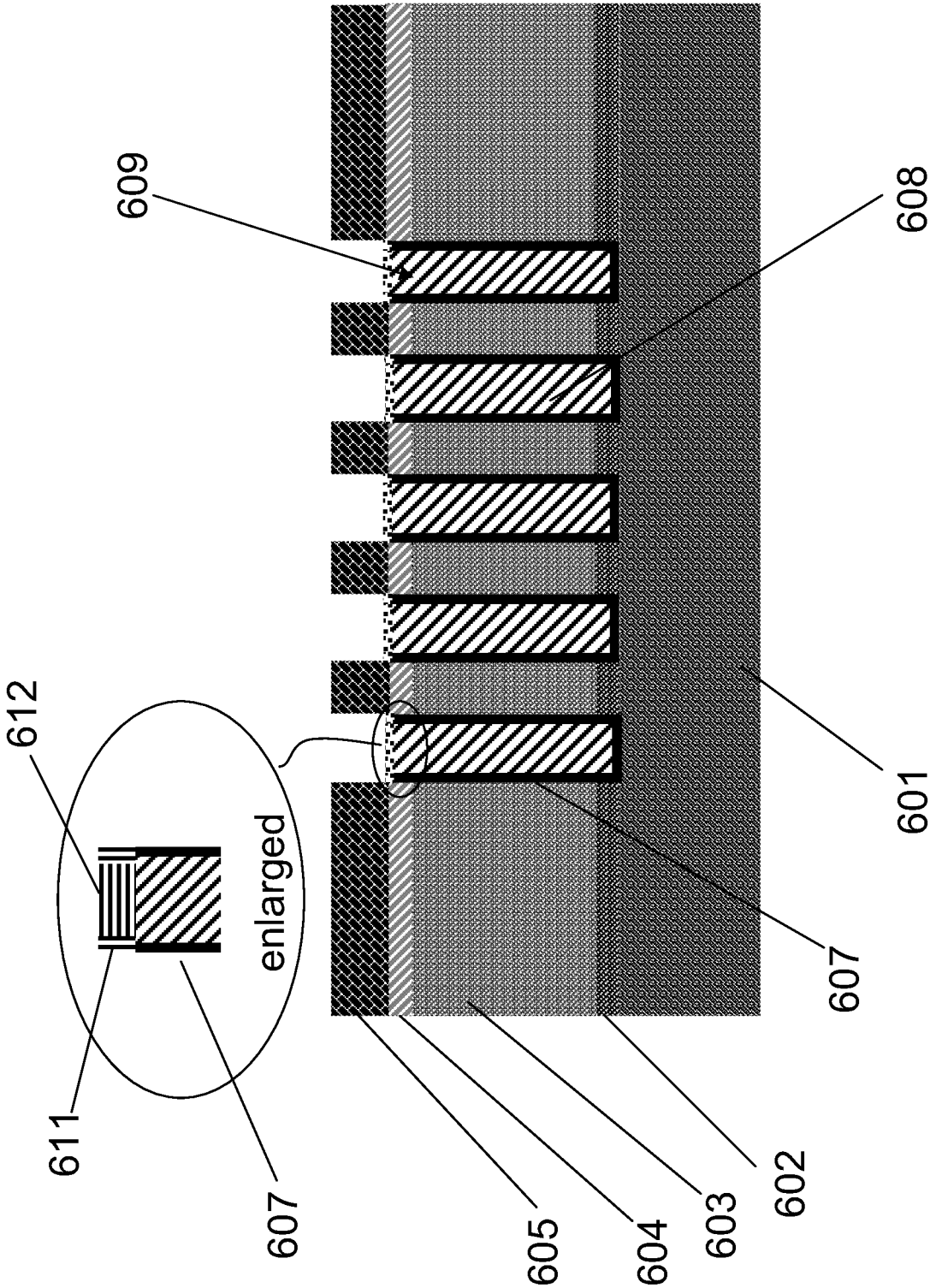

FIG 14

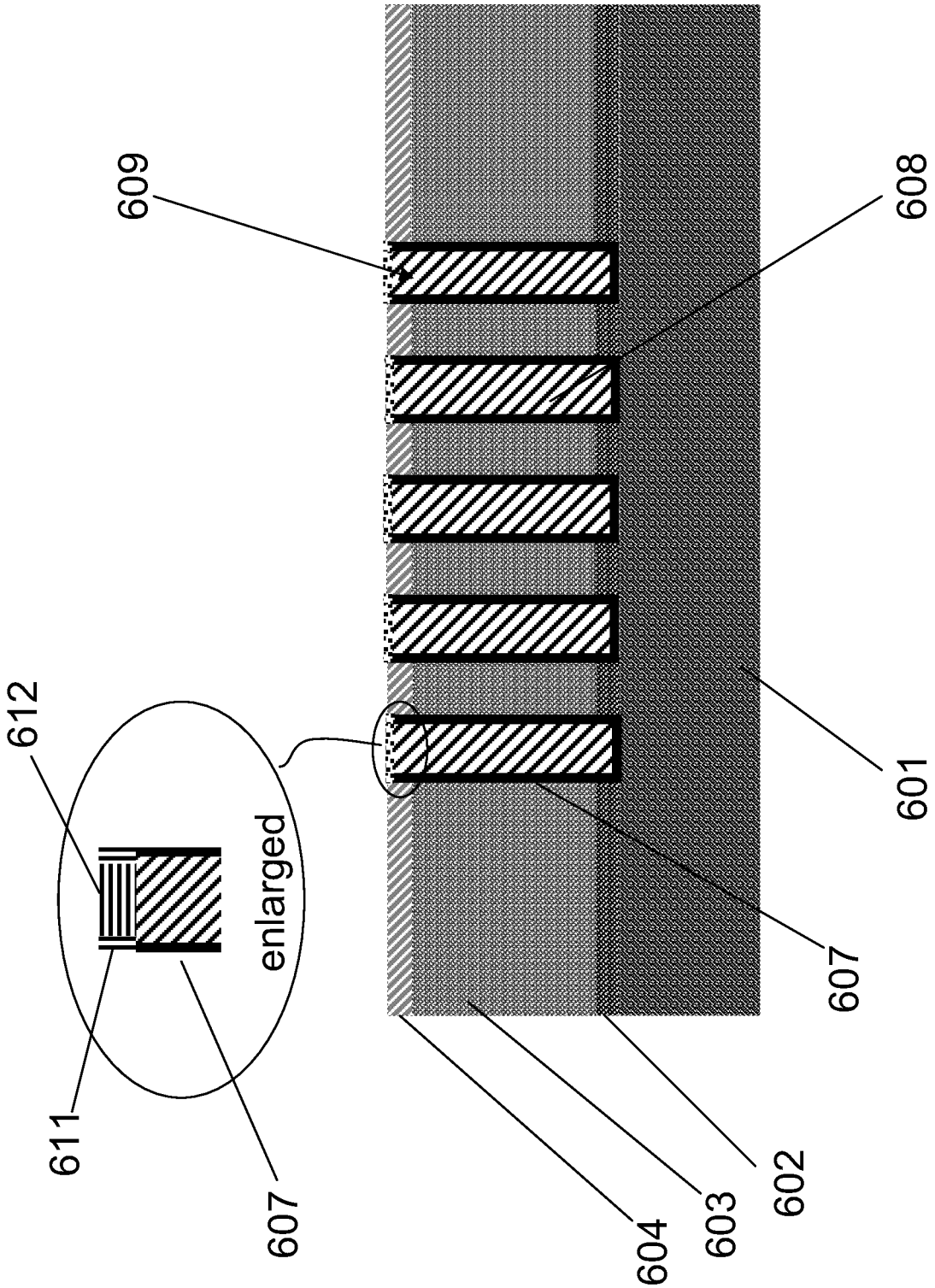

FIG 15

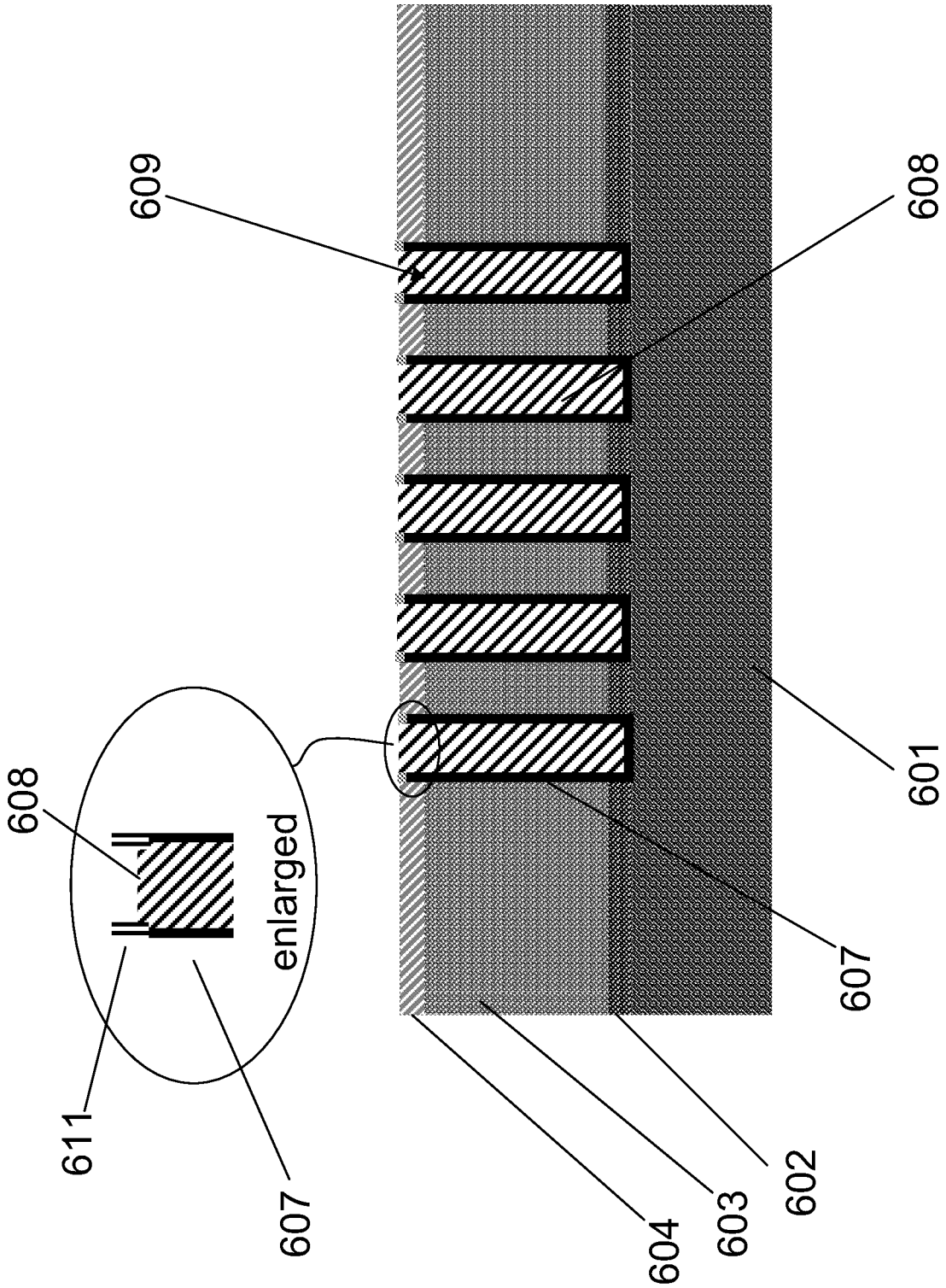

FIG 16

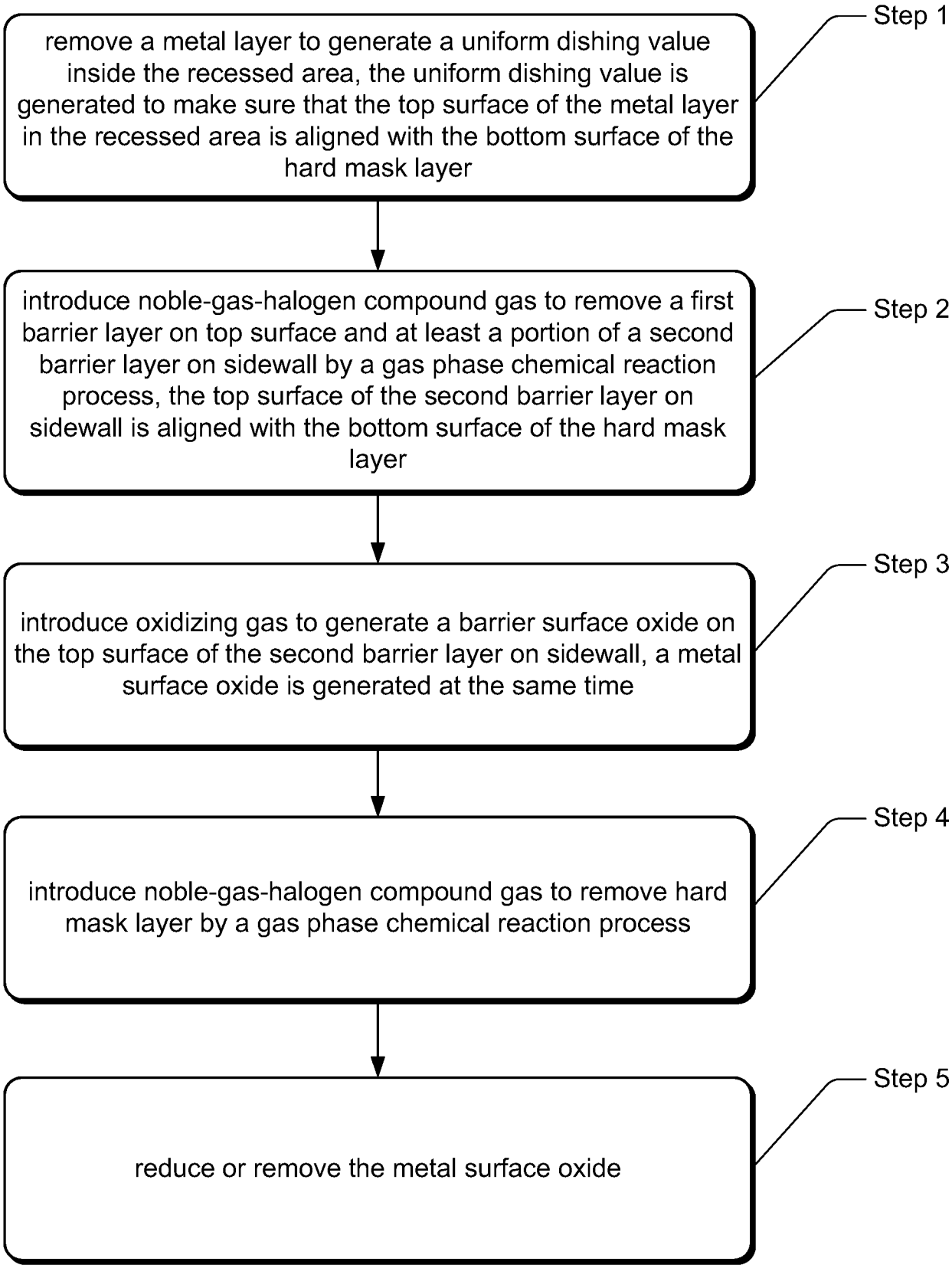
remove a metal layer to generate a uniform dishing value inside the recessed area, the uniform dishing value is generated to make sure that the top surface of the metal layer in the recessed area is aligned with the bottom surface of the hard mask layer
Step 1
introduce noble-gas-halogen compound gas to remove a first barrier layer on top surface and at least a portion of a second barrier layer on sidewall by a gas phase chemical reaction process, the top surface of the second barrier layer on sidewall is aligned with the bottom surface of the hard mask layer
Step 2
introduce oxidizing gas to generate a barrier surface oxide on the top surface of the second barrier layer on sidewall, a metal surface oxide is generated at the same time
Step 3
introduce noble-gas-halogen compound gas to remove hard mask layer by a gas phase chemical reaction process
Step 4
reduce or remove the metal surface oxide
Step 5

FIG 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/086725

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,WPI,EPODOC: ACM, interconnection, barrier, sidewall, recess, noble, gas, phase, chemical, oxidizing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 103839876 A (ACM RESEARCH SHANGHAI INC.) 04 June 2014 (2014-06-04) description, paragraphs [0014]-[0030] and figures 1A-1I	1-14
A	CN 102005407 A (SEMICONDUCTOR MANUFACTURING INTERNATIONAL SHANGHAI CORPORATION) 06 April 2011 (2011-04-06) the whole document	1-14
A	CN 103081066 A (MICRON TECHNOLOGY, INC.) 01 May 2013 (2013-05-01) the whole document	1-14
A	CN 103700615 A (ACM RESEARCH SHANGHAI INC.) 02 April 2014 (2014-04-02) the whole document	1-14
A	US 2004231795 A1 (APPLIED MATERIALS, INC.) 25 November 2004 (2004-11-25) the whole document	1-14
A	US 2009087981 A1 (TOKYO ELECTRON LIMITED) 02 April 2009 (2009-04-02) the whole document	1-14
A	US 2010227473 A1 (MATSUDA, TSUKASA ET AL.) 09 September 2010 (2010-09-09) the whole document	1-14

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 April 2016	**28 April 2016**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	**SHI,Wenqing**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)010-62413411**

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2014082197 A1 (ACM RESEARCH SHANGHAI INC.) 05 June 2014 (2014-06-05) the whole document	1-14

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2015/086725

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	103839876	A	04 June 2014	None			
CN	102005407	A	06 April 2011	CN	102005407	B	19 December 2012
CN	103081066	A	01 May 2013	US	9177917	B2	03 November 2015
				SG	188236	A1	30 April 2013
				US	2016056073	A1	25 February 2016
				WO	2012024056	A2	23 February 2012
				TW	201216410	A	16 April 2012
				KR	20130044354	A	02 May 2013
				TW	I443775	B	01 July 2014
				US	2012043658	A1	23 February 2012
				JP	2013534370	A	02 September 2013
CN	103700615	A	02 April 2014	None			
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				US	8258058	B2	04 September 2012
				KR	20100099575	A	13 September 2010
				US	8148261	B2	03 April 2012
				US	2012164826	A1	28 June 2012
WO	2014082197	A1	05 June 2014	KR	20150088801	A	03 August 2015
				CN	105144363	A	09 December 2015
				US	2015318205	A1	05 November 2015