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(54) **STRUCTURE AND METHOD OF MAKING A SEMICONDUCTOR INTEGRATED CIRCUIT TOLERANT OF MIS-ALIGNMENT OF A METAL CONTACT PATTERN**

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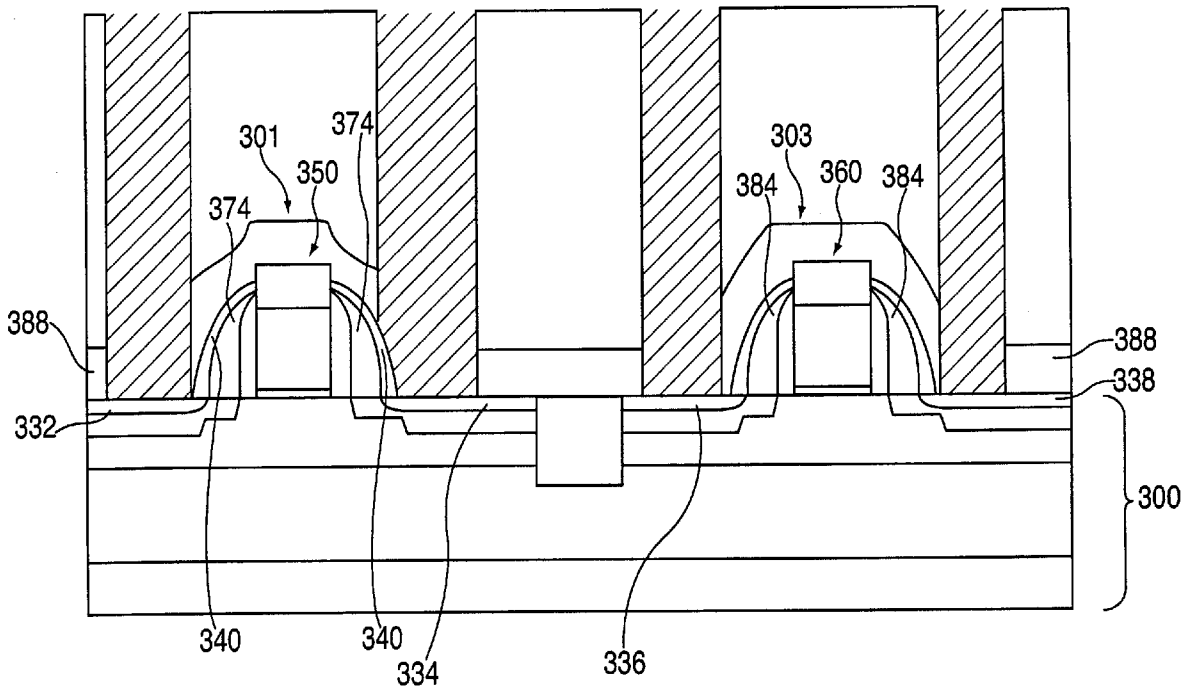
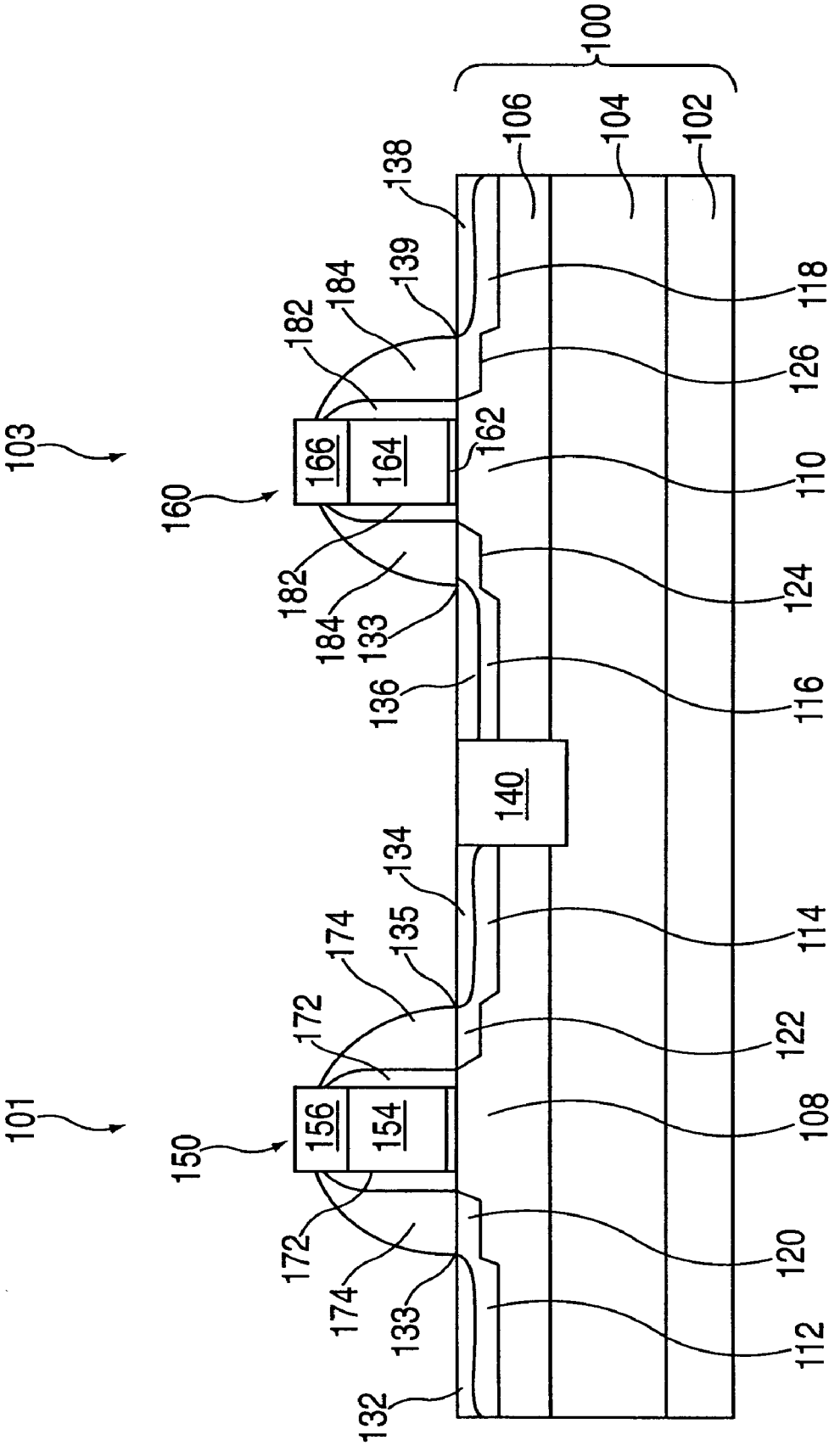
(57) **ABSTRACT**

Disclosed is a method of fabricating a field effect transistor. In the method, a gate stack on a top surface of a semiconductor substrate is formed, and then a first spacer is formed on a sidewall of the gate stack. Next, a silicide self-aligned to the first spacer is deposited in/or on the semiconductor substrate. Subsequently a second spacer covering the surface of the first spacer, and a contact liner over at least the gate stack, the second spacer and the silicide, are formed. Then an interlayer dielectric over the contact liner is deposited. Next, a metal contact opening is formed to expose the contact liner over the silicide. Finally, the opening is extended through the contact liner to expose the silicide without exposing the substrate.




100
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104
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136
116
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112

FIG. 1

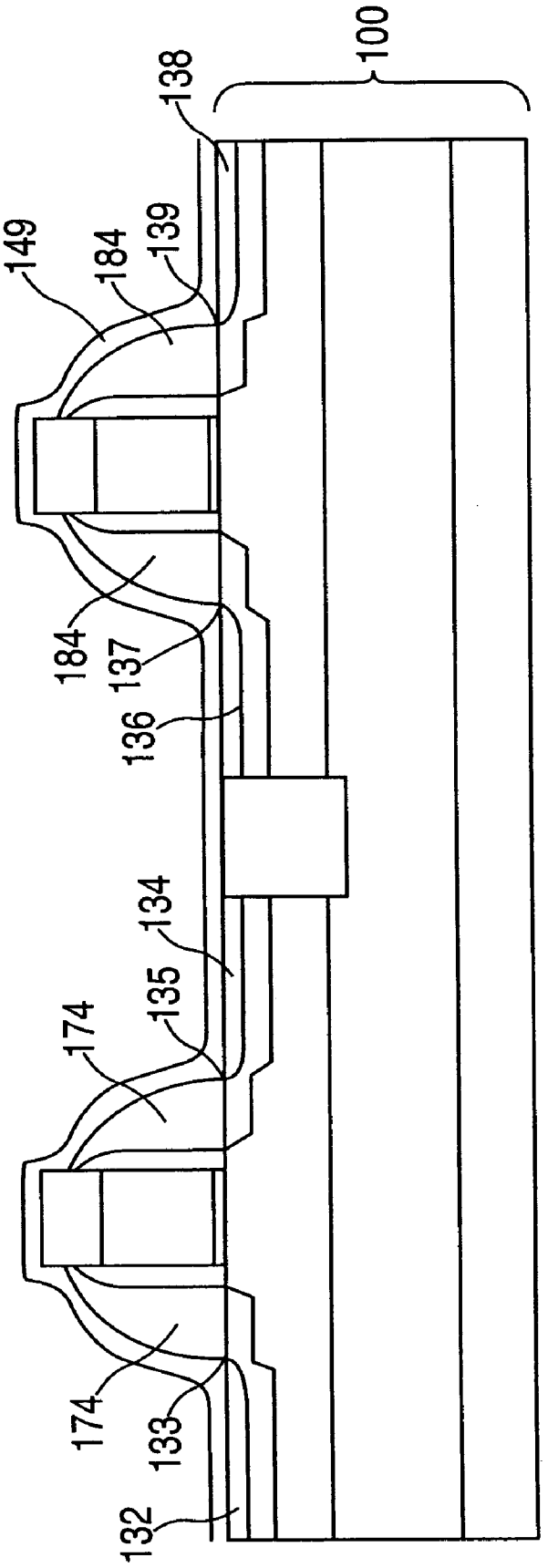

FIG. 2

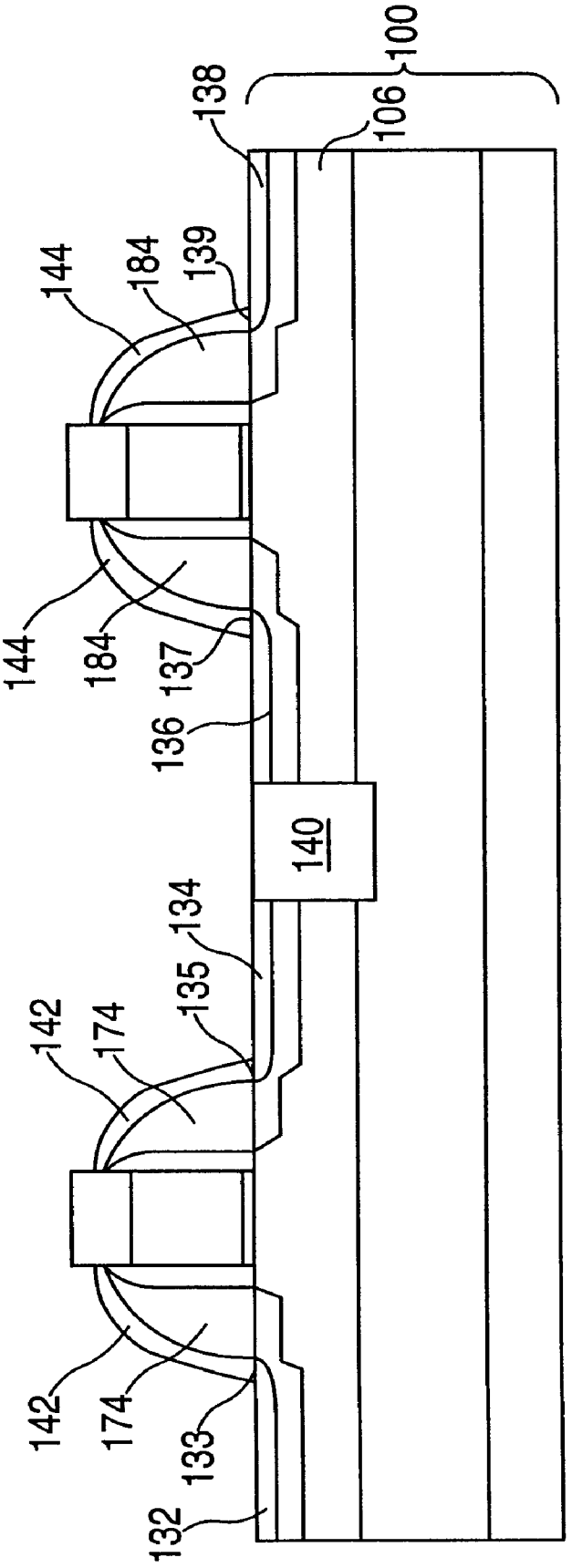

FIG. 3

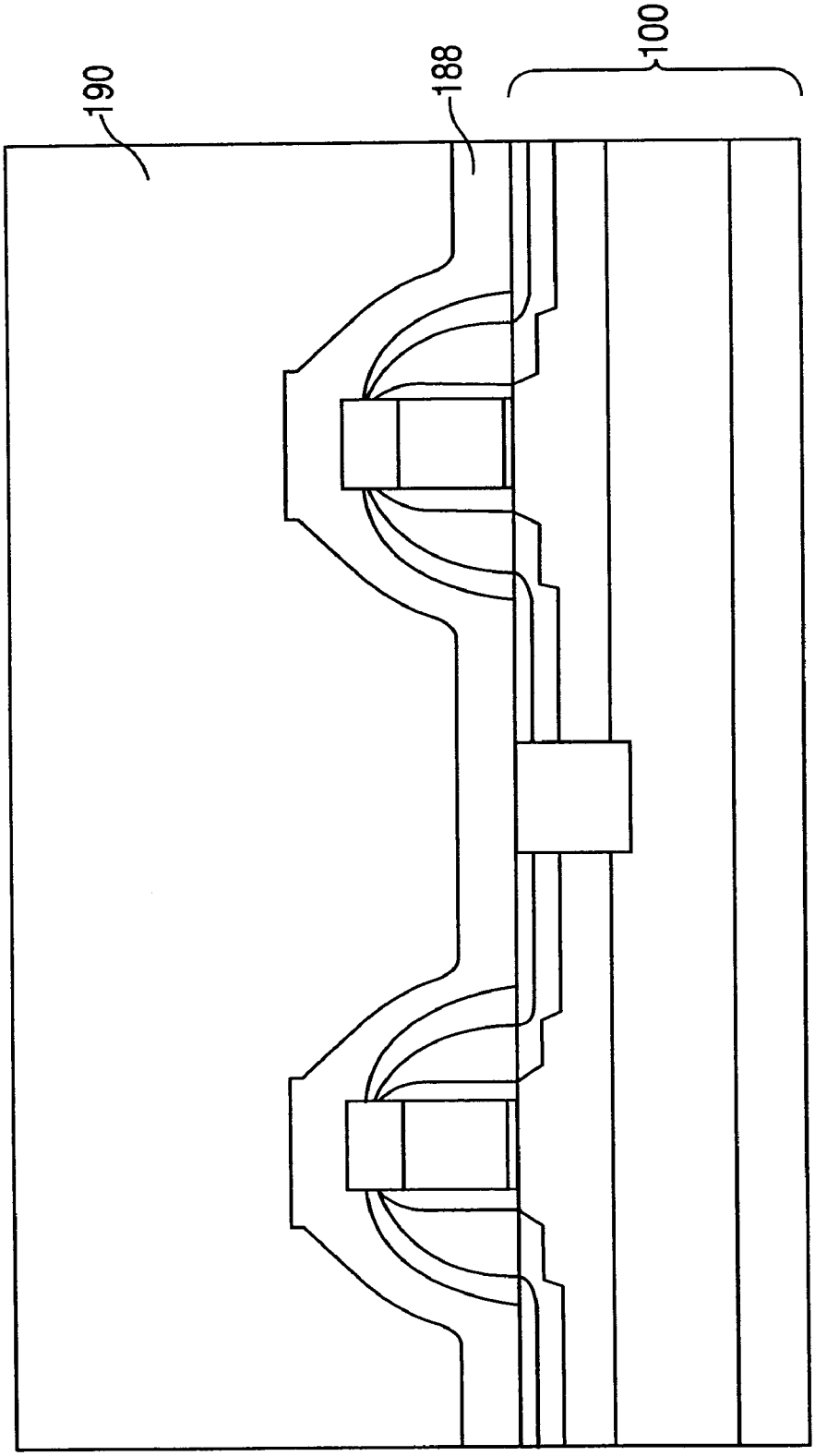

FIG. 4

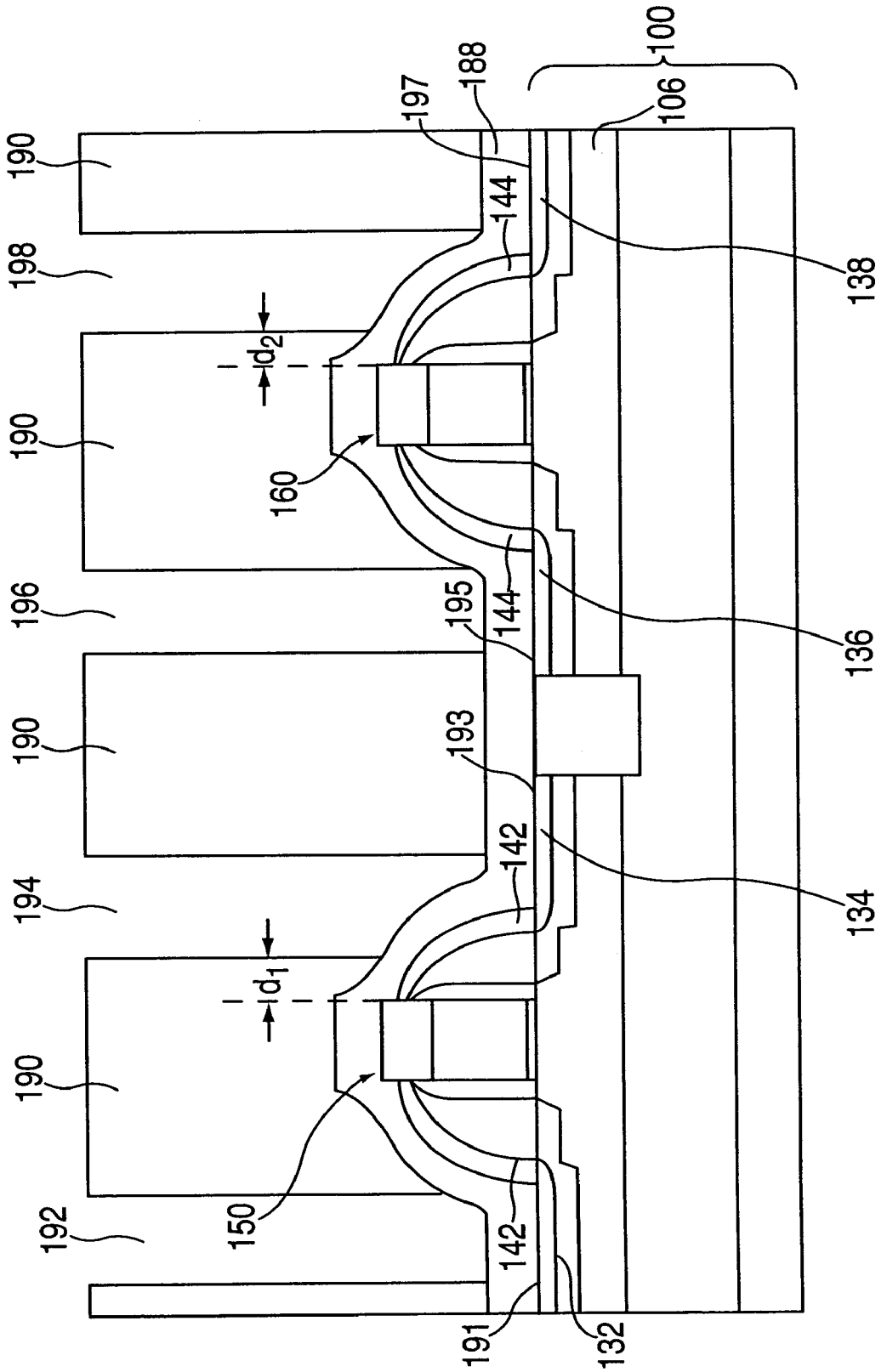
100
188
197
106
190
144
138
198
d_2
190
160
196
195
144
136
190
193
142
194
134
d_1
190
150
192
142
191
132

FIG. 5

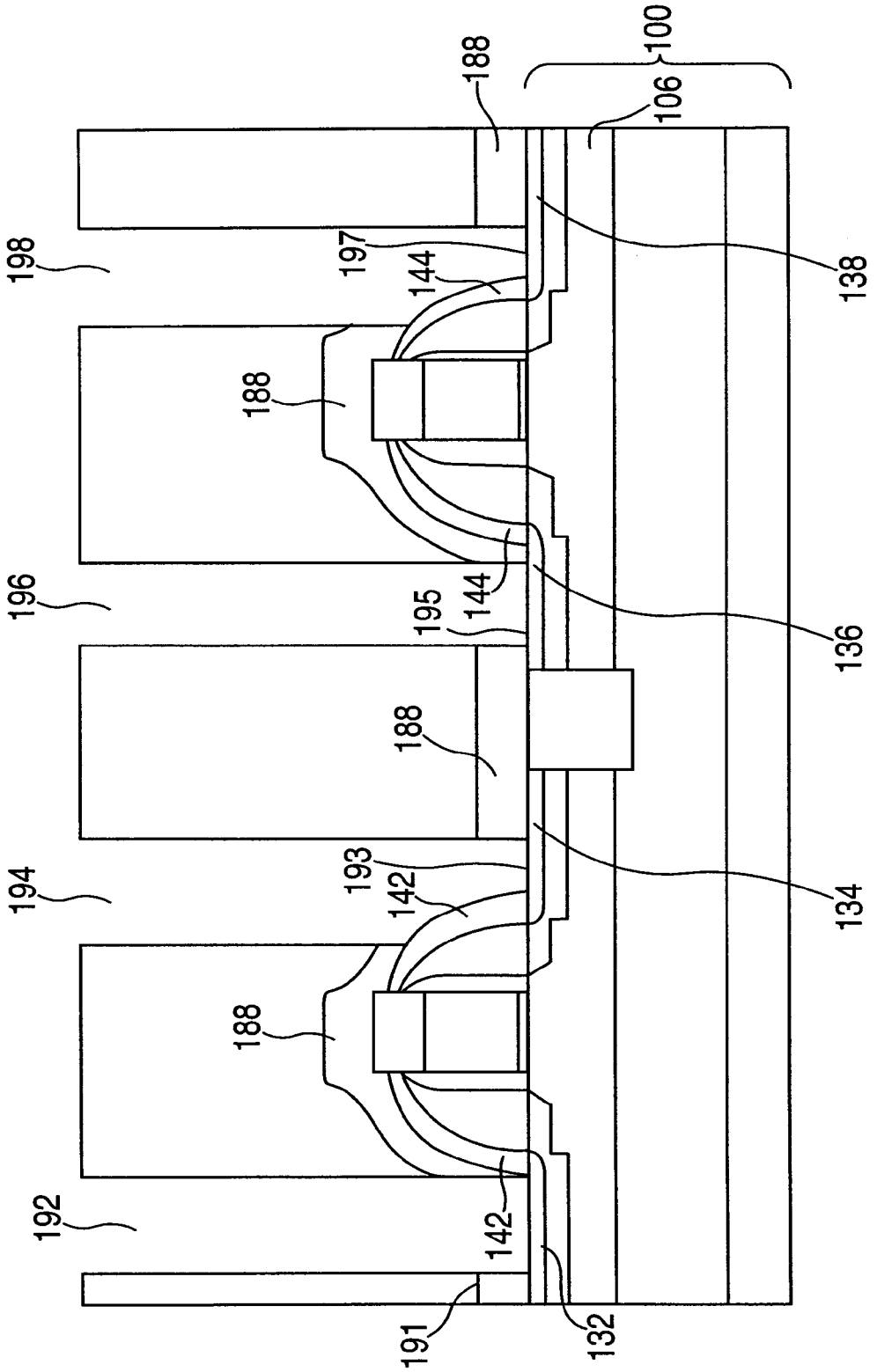
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FIG. 6

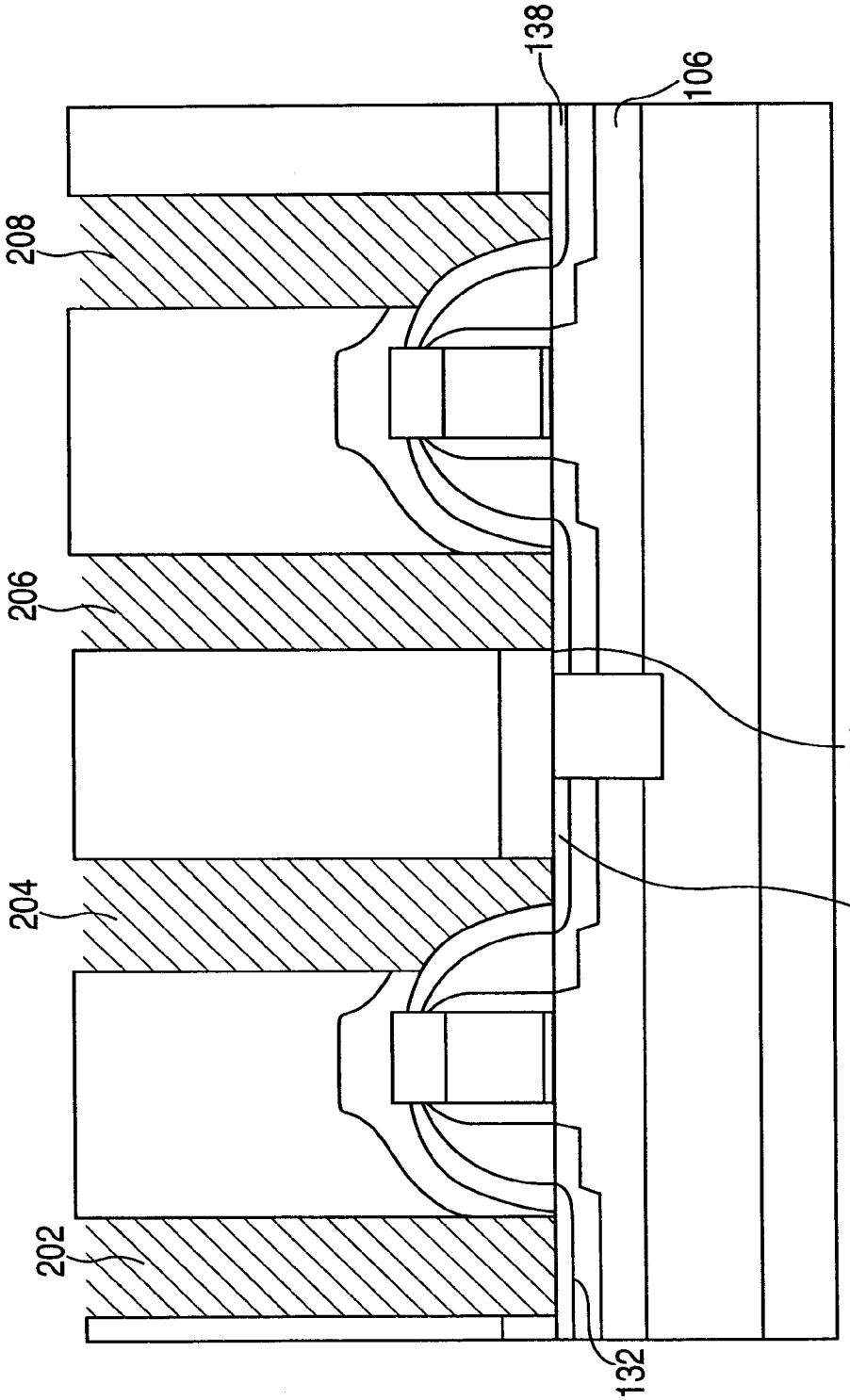

FIG. 7

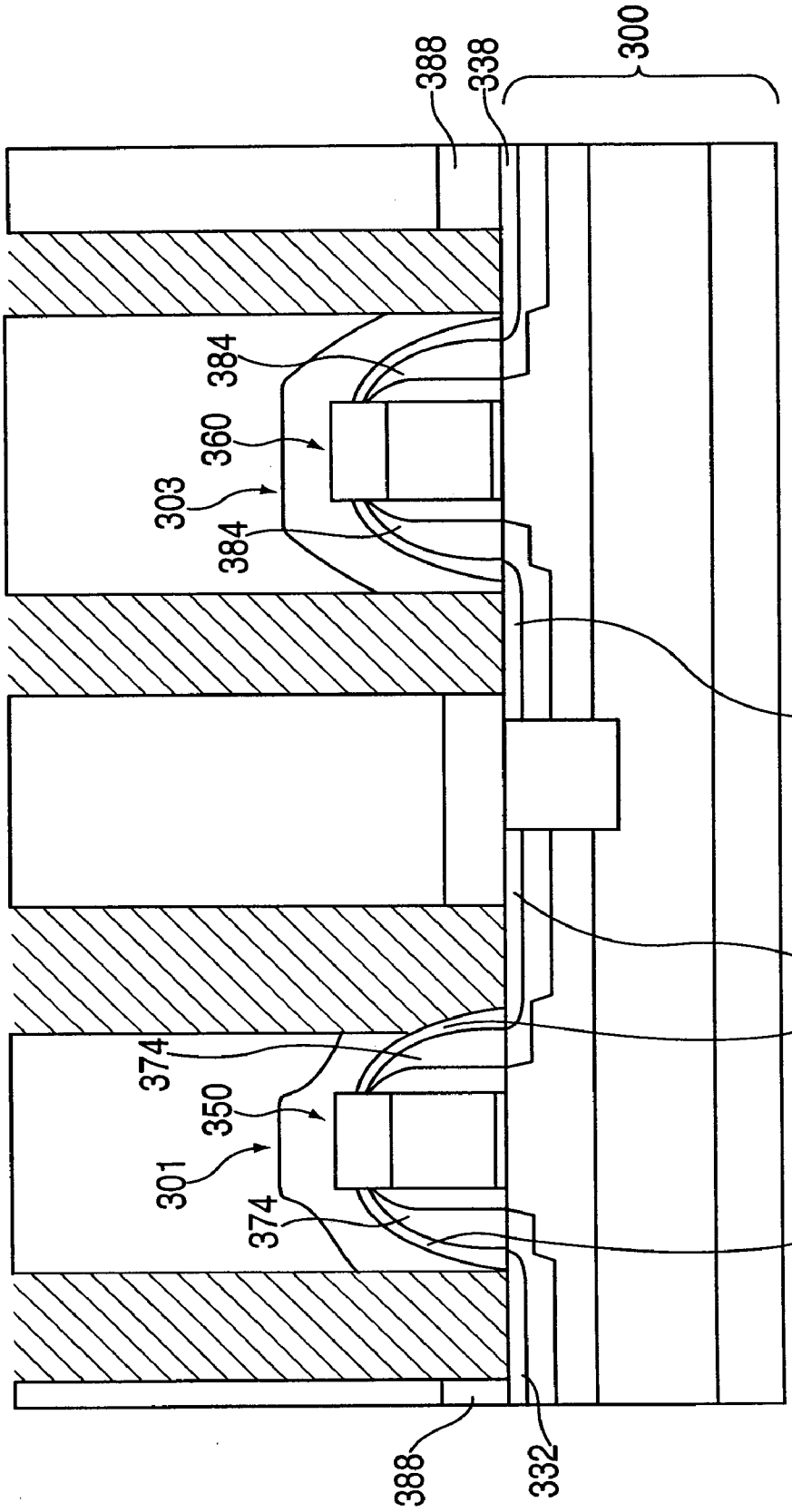
388
338
300
384
360
303
384
336
334
340
374
350
301
374
340
388
332

FIG. 8

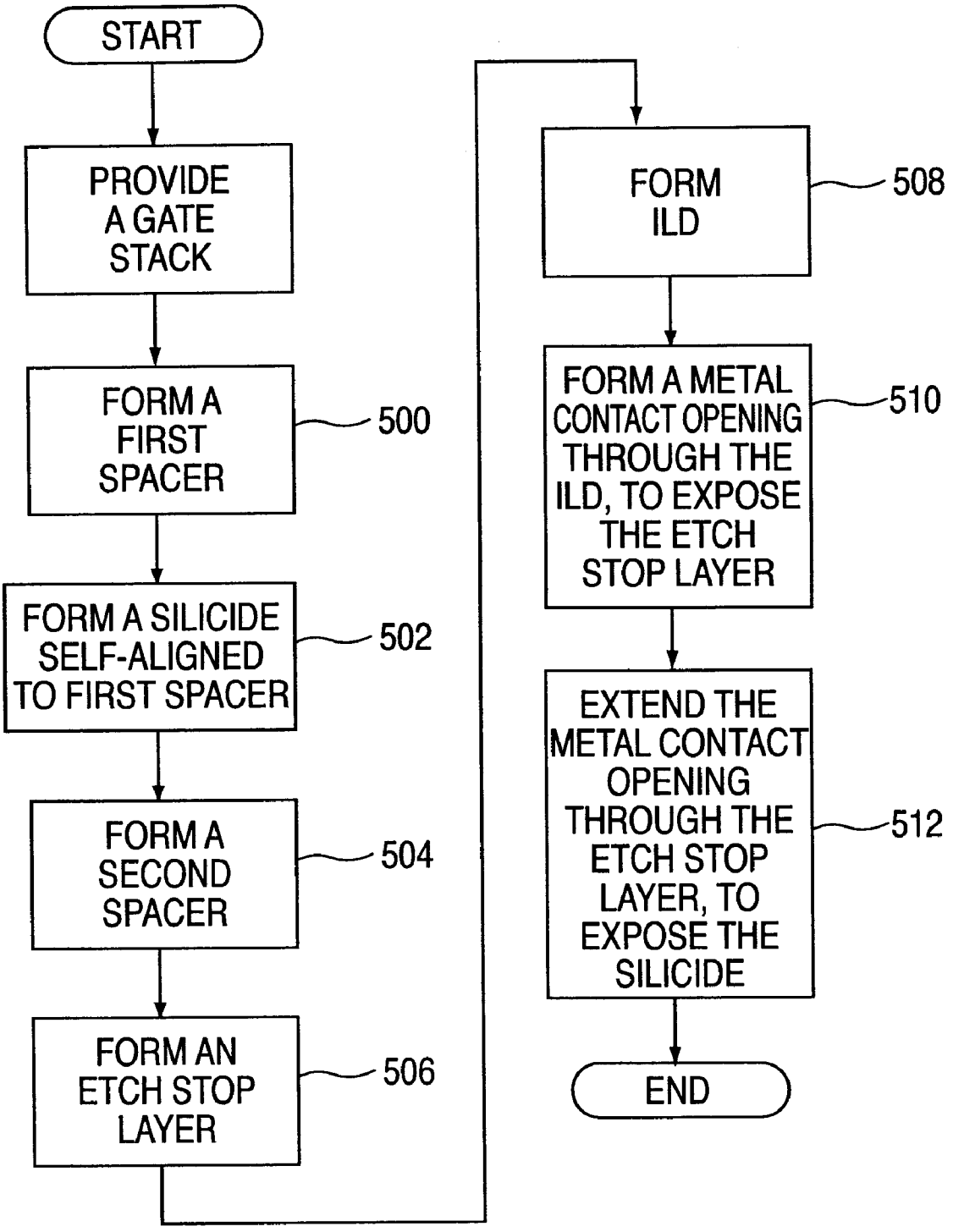
START
PROVIDE A GATE STACK
FORM A FIRST SPACER
500
FORM A SILICIDE SELF-ALIGNED TO FIRST SPACER
502
FORM A SECOND SPACER
504
FORM AN ETCH STOP LAYER
506
FORM ILD
508
FORM A METAL CONTACT OPENING THROUGH THE ILD, TO EXPOSE THE ETCH STOP LAYER
510
EXTEND THE METAL CONTACT OPENING THROUGH THE ETCH STOP LAYER, TO EXPOSE THE SILICIDE
512
END

FIG. 9

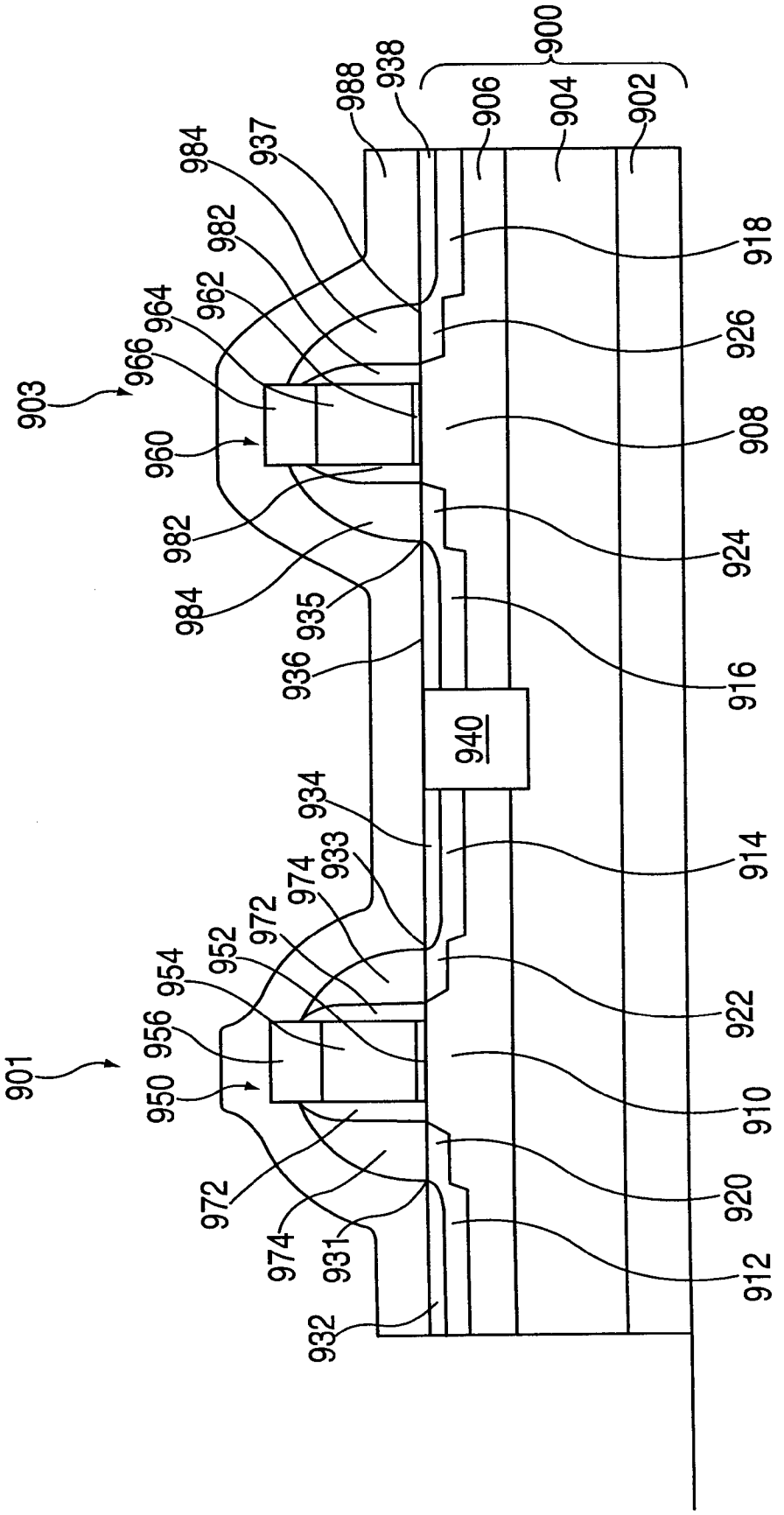

FIG. 10
(PRIOR ART)

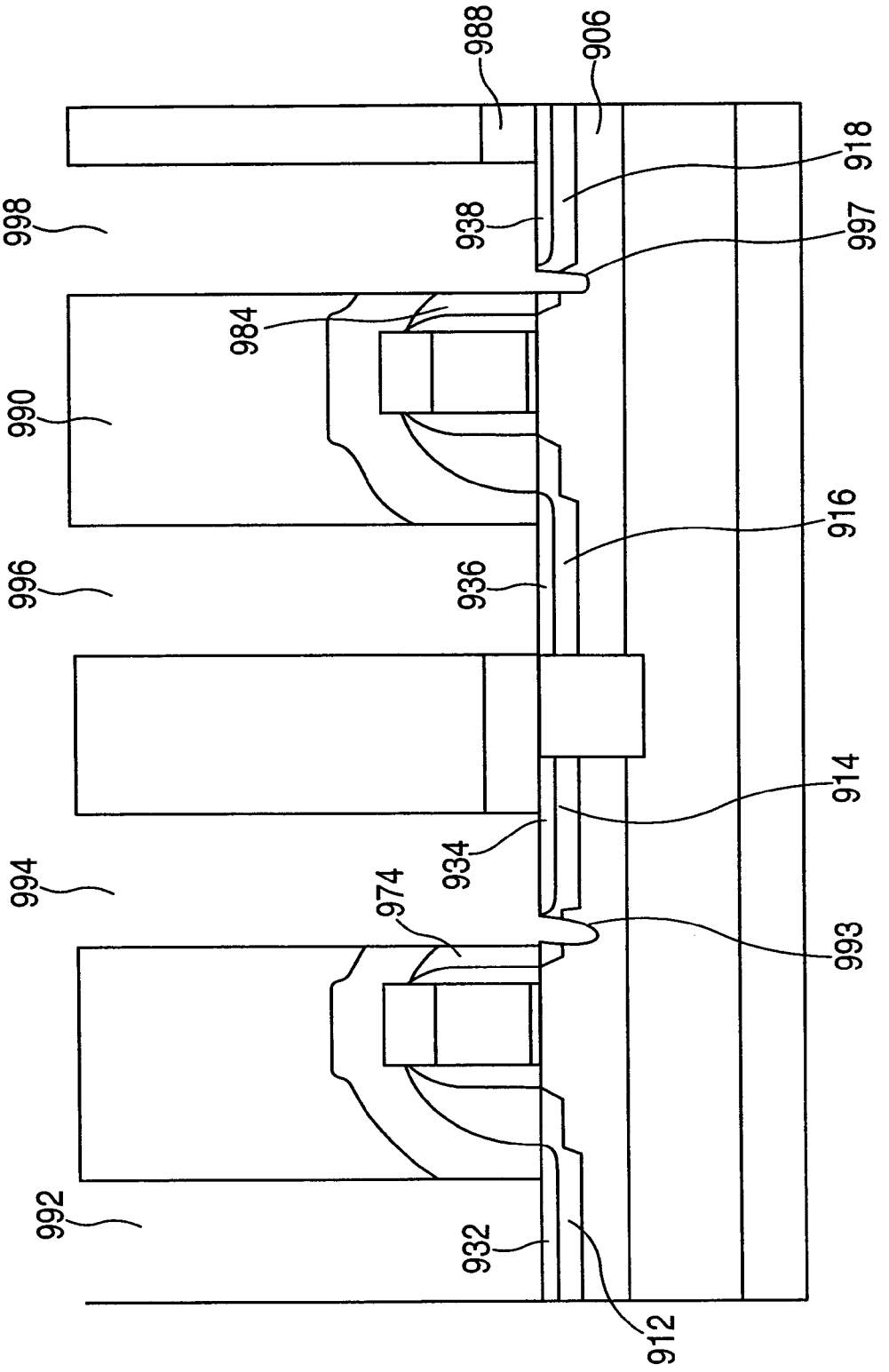

FIG. 11
(PRIOR ART)

STRUCTURE AND METHOD OF MAKING A SEMICONDUCTOR INTEGRATED CIRCUIT TOLERANT OF MIS-ALIGNMENT OF A METAL CONTACT PATTERN

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

[0001] This Patent application is a Continuation patent application of U.S. patent application Ser. No. 11/328,609 filed on Jan. 10, 2006, which is a Divisional patent application of U.S. patent application Ser. No. 10/904,330 filed on Nov. 4, 2004, now U.S. Pat. No. 7,217,647.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to the fabrication of semiconductor integrated circuits, and more specifically to a structure and method of making a semiconductor integrated circuit which is tolerant of mis-alignment of the metal contact pattern to the gate pattern.

[0003] In a semiconductor integrated circuit, a metal contact such as tungsten is used to connect the transistor gate, source/drain, and body to backend wiring. A conventional method for forming a metal contact will be briefly explained.

[0004] FIGS. **10** and **11** illustrate stages in conventional fabrication of a semiconductor integrated circuit.

[0005] Referring to FIG. **10**, a conventional method of forming a metal contact in a semiconductor integrated circuit includes a step of forming a gate stack **950** of a positive field effect transistor (PFET) **901** and a gate stack **960** of a negative field effect transistor (NFET) **903**, on a substrate **900** which includes a silicon substrate **902**, a buried oxide (BOX) layer **904** and a semiconductor layer **906**. Then oxide spacers **972**, **982** are formed on side walls of the gate stacks **950**, **960** followed by formation of source drain (S/D) extensions **920**, **922**, **924**, **926** in a semiconductor layer **906**. Next, nitride spacers **974**, **984** are formed on the oxide spacers **972**, **982** respectively. Subsequently, S/D regions **912**, **914**, **916**, **918** are formed. Further, using the nitride side walls **974**, **984** as masks, metal silicide regions **932**, **934**, **936**, **938** are formed on the S/D regions **912**, **914**, **916**, **918**, respectively. Next, a contact liner **988**, commonly Si_3N_4, is deposited over the substrate **900**, followed by deposition of an interlayer dielectric layer (IDL) **990** and planerization. Thereafter, photolithographic and etching techniques are used to pattern the IDL **990**, forming contact openings **992**, **994**, **996**, **998** that expose the silicide on the S/D regions as illustrated in FIG. **11**. The process typically proceeds by a first anisotropic etch process to form openings in the interlayer dielectric **990** stopping on the contact liner **988**, followed by a second anisotropic etch through the contact liner **988**, using the silicide **932**, **934**, **936**, **938** as an etching stop.

[0006] In the photolithography, the pattern for the contact openings is inevitably slightly mis-aligned to the gate pattern. Thus, at least a portion of a contact opening may be misaligned over the side walls **974**, **984**. However, the etch process designed to etch away the contact liner **988**, typically nitride, has no selectivity to the spacer **974**, **984**, which is also typically nitride. Therefore, at least a part of the spacers **974**, **978** may be etched through, exposing the underlying semiconductor layer **906**. Since the silicide **932**, **934**, **936**, **938** on the S/D regions **912**, **914**, **916**, **918** are formed by using the side walls **974**, **984**, as masks, no silicide is deposited beneath the spacers **974**, **984** in the semiconductor layer **906**. Accordingly, the exposed portion of the substrate may be etched, causing problems such as a short **993**, **997** between a metal contact and the substrate, and causing unexpected parasitic capacitance.

[0007] Further occasionally the semiconductor layer **906** is exposed between the bottom of the spacers **974**, **984** and the edges **931**, **933**, **935**, **937** of the silicide **932**, **934**, **936**, **938** even though the spacers **974**, **984** are used as masks in forming silicide **932**, **934**, **936**, **938**, increasing the possibility of causing a short between a metal contact and the substrate.

[0008] Accordingly, there is a need for a structure and method of forming a metal contact that is tolerant of misalignment of the contact pattern to the gate pattern and avoids shorts between the contact and substrate.

SUMMARY OF THE INVENTION

[0009] According to an aspect of the invention, a method of fabricating a field effect transistor is provided. The method includes steps of forming a gate stack on a top surface of a semiconductor substrate and a first spacer formed on a sidewall of the gate stack; forming, in or on the semiconductor substrate, a silicide adjacent to the first spacer; forming a second spacer covering the surface of the first spacer; forming a contact liner over at least the gate stack, the second spacer and the silicide; forming an interlayer dielectric over the contact liner; forming an opening to expose the contact liner over the silicide; and extending the opening through the contact liner to expose the silicide without exposing the substrate.

[0010] In another aspect of the invention, the second spacer further covers at least a portion of the silicide so that the semiconductor layer is not exposed even if a gap between the second spacer and the silicide exists.

[0011] These, and other aspects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings, which are not necessarily drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGS. **1** through **7** illustrate stages in fabrication of a PFET and an NFET according to an embodiment of the invention.

[0013] FIG. **8** illustrates a stage in fabrication of a PFET and an NFET according to another embodiment of the invention.

[0014] FIG. **9** shows a flow of method for fabricating a semiconductor circuit according to an embodiment of the invention.

[0015] FIGS. **10** and **11** illustrate conventional stages in fabrication of a PFET and an NFET.

DETAILED DESCRIPTION

[0016] FIGS. **1** through **7** illustrate stages in processing to form a PFET **101** and an NFET **103** according to an embodiment of the invention.

[0017] Firstly, as shown in FIG. **1**, a PFET **101** and an NFET **103** are formed on a substrate **100**. The substrate **100** preferably includes a silicon substrate **102**, buried oxide (BOX) layer **104**, a semiconductor layer **106** and a trench isolation region **140**. Alternatively, the substrate **100** may be a bulk semiconductor substrate such as silicon. However, the invention is not limited to silicon substrates but other types of semiconductors such as III-V compound semiconductor materials, e.g. gallium arsenide (GaAs), may be used.

[0018] The PFET **101** and NFET **103** include gate stacks **150**, **160**, channel regions **108**, **110**, source drain extensions **120**, **122**, **124**, **126**, S/D regions **112**, **114**, **116**, **118**, silicide S/D regions (hereinafter "silicide") **132**, **134**, **136**, **138** in the S/D regions respectively. The silicide may include, for example, titanium (Ti), cobalt (Co), Nickel (Ni), tungsten (W) or platinum (Pt). The gate stacks **150**, **160** may further include gate dielectric layers **152**, **162** on the channel regions **108**, **110**, and gate conductor portions **154**, **164**, such as polysilicon. Metal lower resistance portions **156**, **166** may also be included in some embodiment.

[0019] Adjacent the side walls of the gate stacks **150**, **160**, multiple spacers **172**, **174**, **182**, **184** are preferably formed. Alternatively, a single spacer may be deposited on the side walls of each gate stack **150**, **160**. The spacers **174**, **184** preferably include silicon nitride (Si_3N_4). The spacers **174**, **184** are used as masks in the formation of the silicide **132**, **134**, **136**, **138** in the S/D regions **112**, **114**, **116**, **118**.

[0020] The S/D regions **112**, **114**, **116**, **118** may be raised S/D regions, which may be formed by selective epitaxial growth.

[0021] The silicide **132**, **134**, **136**, **138** may be formed by a method such as chemical vapor deposition (CVD) of silicide, or metal sputtering followed by an anneal.

[0022] For example, using CVD, layers of silicide are formed on the S/D regions **112**, **114**, **116**, **118**. At the portions of the silicide adjacent to the gate stacks **150**, **160**, the layers of silicide preferably grow in contact with the outer surfaces of the spacers **174**, **184** so that semiconductor layer **106** is not exposed.

[0023] Alternatively, the silicide may be formed by metal sputtering which preferably includes the steps of (1) sputtering metal into the S/D regions **112**, **114**, **116**, **118**, using the spacers **174**, **184** as masks, (2) performing a first annealing at about 200 to 500° C., (3) removing non-reacted metal, and (4) performing a second annealing at about 400 to 750° C. Since the spacers **174**, **184** are used as masks, silicide **132**, **134**, **136**, **138** are preferably formed in contact with the bottom of the spacers **174**, **184** so that the semiconductor layer **106** is not exposed.

[0024] However, in both methods, a gap between the silicide **132**, **134**, **136**, **138** and the corresponding spacers **174**, **184** may be formed. That is, the semiconductor layer **106** may exposed between the bottom portion of the spacers **174**, **184** and the edges **133**, **135**, **137**, **139** of the silicide **132**, **134**, **136**, **138**.

[0025] Next, as shown in FIG. **2**, another dielectric layer **149**, is formed over the top surface of the substrate **100**. The dielectric material **149** is different than the mask spacers **174**, **184**; for example if mask spacers **174**, **184** are nitride, the dielectric layer **149** is preferably oxide. In the case of an oxide, the formation of the layer **149** preferably includes (1) applying a precursor, such as tetra ethyl ortho silicate (TEOS), SiH_4, $SiCl_2H_2$, over the substrate **100**, and (2) applying heat to grow the oxide layer **149**.

[0026] Heat in step (2) is preferably applied at a temperature so as not to oxidize the silicide **132**, **134**, **136**, **138**. For example, when the silicide includes Ni, the oxide layer **149** is preferably be grown at a temperature in the range about 300° C. to 400° C. The preferable temperature is about 700° C. or less when the silicide includes Co. The thickness of the oxide layer **149** is preferably about 100 Å to 400 Å, most preferably about 160 Å to 200 Å.

[0027] The thickness of the oxide layer **149** is preferably thinner than the nitride spacers **174**, **184**, but sufficient thick so as to overlap the edges **133**, **135**, **137**, **139** of the silicide **132**, **134**, **136**, **138** so as to cover any gap between the edges **133**, **135**, **137**, **139** of the silicide and the nitride spacers **174**, **184**.

[0028] Accordingly, the spacers **174**, **184**, gate stacks **150**, **160**, silicide **132**, **134**, **136**, **138** are covered by the oxide layer **149**.

[0029] Instead of an oxide layer, a layer **149** including silicon carbide (SiC) may be deposited. The layer **149** may be formed by SiH4 and CH4 reaction in a CVD chamber. Preferable reaction temperature is about 400° C. Thickness of the formed SiC layer **149** is preferably about 500 to 1000 Å.

[0030] Next, as shown in FIG. **3**, the oxide layer **149** is etched back by an anisotropic etch, preferably reactive ion etching (RIE), to form spacers **142**, **144**. The spacers **142**, **144** cover the surface of the spacers **174**, **184** respectively. Simultaneously, the spacers **142**, **144** overlap the inner edges of the silicide **132**, **134**, **136**, **138** at portions **133**, **135**, **137**, **139** respectively so that junctions between silicide **132**, **134**, **136**, **138** and spacers **174**, **184** are covered by the spacers **142**, **144**. Accordingly, even if a gap exists between the silicide and the spacers **174**, **184**, the oxide layers **142**, **144** cover the gap so that the semiconductor layer **106** is not exposed.

[0031] Thereafter, as shown in FIG. **4**, a contact liner **188** is applied over the substrate **100**. The contact liner preferably is a different material than the spacers **142**, **144**, and in the case of oxide spacers, **142**, **144**, preferably includes silicon nitride, for example Si_3N_4. The thickness of the contact liner **188** is preferably about 300 to 1500 Å.

[0032] Then, an interlayer dielectric (ILD) **190**, which may include a low-k dielectric material, a dielectric such as borophosphosilicate glass (BPSG) or high density plasma (HDP) oxide, is deposited and planerized. The thickness of the ILD **190** is preferably about 3000 to 5000 Å.

[0033] A two-step selective etch process is used to form the contact openings.

[0034] As shown in FIG. **5**, photolithographic and anisotropic etching techniques, such as RIE, is used to pattern the interlayer dielectric **190**, to form contact openings **192**, **194**, **196**, **198** that expose the contact liner **188**. In the first step, the etching is preferably selective to the contact liner **188** so that the etching is stopped on the contact liner **188**. One skilled in the art would be able to arrange conditions for the etching to achieve the desired selectivity.

[0035] FIG. **5** shows an example where the contact opening pattern is mis-aligned to the gate pattern. Specifically, the contact openings **194**, **198** are formed with unintended short distances d1, d2 from the gate stacks **150**, **160** respectively.

[0036] Next, a second etch step uses process conditions where the etching is selective to the spacers **142**, **144** and also selective to the silicide **132**, **134**, **136**, **138**, so that the contact liner **188** is etched back to the surfaces **191**, **193**, **195**, **197** of the silicide. Thus, as shown in FIG. **6**, spacers **142**, **144**, are not etched back by the second etch process, so that the substrate **100**, specifically the semiconductor layer **106**, is not exposed at the bottom of the contact openings **192**, **194**, **196**, **198**.

[0037] Finally, metal, such as Ti, TiN, W, is filled into the contact holes to form contacts **202**, **204**, **206**, **208** by for example sputtering or chemical vapor deposition (CVD), followed by chemical mechanical polishing (CMP).

[0038] The final structure is illustrated in FIG. **7**.

[0039] According to the invention, the contacts **202**, **204**, **206**, **208** are in direct contact with the silicide **132**, **134**, **136**, **138** and are not in contact with the semiconductor layer **106**, in the case of mis-alignment.

[0040] FIG. **8** illustrates a PFET **301** and an NFET **303** according to another embodiment of the invention.

[0041] Spacers **374** adjacent the PFET **301** are preferably thicker than spacers **384** adjacent the NFET **303**. It is preferable to make the contact pitch constant for ease of connectivity with upper layers, and not too large to minimize the size of the resulting semiconductor integrated circuit. Therefore, PFET **301** tends to be more prone to mis-alignment of the metal contact to the gate pattern.

[0042] Therefore, significant improvement in yield can be achieved even if an additional spacer **340**, such as an oxide layer or a SiC layer, according to the present invention is deposited over only a PFET **301**.

[0043] In the embodiment illustrated in FIG. **8**, a second spacer **340**, preferably including silicon oxide or SiC, is formed only over spacers **374** on the side walls of a gate stack of the PFET **301**. For example, on a PFET **301**, the spacer **374** preferably has about 750 Å maximum thickness, and more preferably the thickness of the spacer **374** is about 100 to 300 Å. It would be readily understood by a skilled person that the spacer **340** may be formed by arranging the method as illustrated in FIGS. **1** through **7** to mask an NFET during the formation of the spacer **374** on a gate stack **350** of the PFET **301**. For instance, the gate stack **350** of the PFET **301**, the gate stack **360** of the NFET **303**, silicide **332**, **334**, **336**, **338** and spacers **374**, **384** may be formed on the substrate **300**. Then, a contact liner **388**, such as silicon nitride, may be formed to first cover only the NFET **303**, while masking the PFET region. The mask is removed from the PFET region. Next, the NFET region is masked and the outer spacer **340** may be formed only on the spacer **374** adjacent the PFET by means of RIE, for example, followed by a formation of a contact liner **388** only on the PFET **301**.

[0044] Subsequently, the mask over the NFET is removed, and the ILD and contact openings are formed as in FIGS. **4-7** described above.

[0045] FIG. **9** shows a flow of method for fabricating a semiconductor circuit according to an embodiment of the invention.

[0046] In the method, a gate stack on a top surface of a semiconductor substrate is formed, and then a first spacer is formed on a sidewall of the gate stack (Step **500**).

[0047] The first spacer may include multiple spacers, where the outer portion of the first spacer is preferably silicon nitride. Next, a silicide self-aligned to the first spacer is deposited in/or on the semiconductor substrate (Step **502**).

[0048] Subsequently a second spacer covering the surface of the first spacer (Step **504**), and a contact liner formed over at least the gate stack, the second spacer and the silicide (Step **506**). In accordance with the invention, the contact liner is a different material than the second spacer. For example, if the second spacer is silicon oxide, the contact liner is preferably silicon nitride. The contact liner is used as an etch stop layer in a subsequent first RIE, discussed below.

[0049] Then an interlayer dielectric, such as a low-k material, BPSG or HDP oxide, over the contact liner is deposited (Step **508**). The ILD is preferably different than the contact liner.

[0050] Next, a metal contact opening through the ILD is formed to expose the contact liner over the silicide (Step **510**). A first RIE of the ILD selective to the contact liner is preferably used. Here, the contact liner is used as an etch stop for the first RIE step. Finally, the contact opening is extended through the contact liner to expose the silicide without exposing the substrate (Step **512**). The extension is preferably performed by a second RIE selective to the second spacer and the silicide. Since the first spacer is covered by the second spacer, the first spacer is not etched through to expose the semiconductor substrate when extending the opening. Therefore, a short between a contact and the semiconductor substrate is prevented.

[0051] While the invention has been described with reference to certain preferred embodiments thereof, those skilled in the art will understand the many modifications and enhancements which can be made without departing from the true scope and spirit of the invention, which is limited only by the appended claims.

What is claimed is:

1. An integrated circuit comprising;

a PFET and an NFET formed on a semiconductor substrate;

the PFET comprising:

a PFET gate stack on a top surface of the semiconductor substrate;

a first PFET spacer formed on a sidewall of the PFET gate stack, said first PFET spacer having an outer edge opposite from said sidewall of said PFET gate stack;

a PFET source/drain region having an edge aligned to said outer edge of said first PFET spacer;

a second PFET spacer covering a surface of said first PFET spacer and said second PFET spacer having an outer edge opposite from said surface of said first PFET spacer; and

a PFET silicide, in or on the semiconductor substrate, having an edge aligned to said outer edge of said second PFET spacer;

the NFET comprising:

an NFET gate stack on a top surface of the semiconductor substrate;

a first NFET spacer formed on a sidewall of the NFET gate stack, said first NFET spacer having an outer edge opposite from said sidewall of said NFET gate stack;

a NFET source/drain region having an edge aligned to said outer edge of said first NFET spacer;

a second NFET spacer covering a surface of said first NFET spacer and said second NFET spacer having an outer edge opposite from said surface of said first NFET spacer; and

a NFET silicide, in or on the semiconductor substrate, having an edge aligned to said outer edge of said second NFET spacer;

wherein said second PFET spacer has a thickness greater than a corresponding thickness of said second NFET spacer.

2. The integrated circuit of claim **1**, wherein said PFET further comprises a third PFET spacer covering the surface of said second PFET spacer and at least the edge of the PFET silicide aligned to said outer edge of said second PFET spacer so that the semiconductor substrate is not exposed between the second PFET spacer and the PFET silicide.

3. The integrated circuit of claim **2**, further comprising a contact liner formed over said PFET and said NFET, said

contact liner in contact with said third PFET spacer, said PFET silicide, said second NFET spacer and said NFET silicide.

4. The integrated circuit of claim **3**, further comprising an interlayer dielectric formed in contact with an upper surface of said contact liner.

5. The integrated circuit of claim **4**, wherein said interlayer dielectric consists of a material that may be etched selectively to said contact liner, and said contact liner consists of a material that may be etched selectively to said third PFET spacer.

6. The integrated circuit of claim **4**, further comprising a PFET contact extending through said interlayer dielectric and said contact liner and in contact with said third PFET spacer and with said PFET silicide without being in contact with said semiconductor substrate.

7. The integrated circuit of claim **6**, further comprising an NFET contact extending through said interlayer dielectric and said contact liner and in contact with said NFET silicide without being in contact with said second NFET spacer or with said semiconductor substrate.

8. The integrated circuit of claim **7**, wherein said PFET and NFET contacts comprise a plurality of contacts having a constant pitch.

* * * * *