



(51) International Patent Classification:

H01L 27/06 (2006.01) H01L 49/02 (2006.01)

H01L 29/94 (2006.01)

(21) International Application Number:

PCT/US2019/043437

(22) International Filing Date:

25 July 2019 (25.07.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/049,256 30 July 2018 (30.07.2018) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US 16/049,256 (CON)
Filed on 30 July 2018 (30.07.2018)

(71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant (for JP only): TEXAS INSTRUMENTS JAPAN LIMITED [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).

(72) Inventors: STEWART, Elizabeth Costner; 6809 Southridge Drive, Dallas, TX 75214 (US). WEST, Jeffrey A.; 8130 Forest Hills Blvd., Dallas, TX 75218 (US).

(74) Agent: ABRAHAM, Ebby et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(54) Title: CRACK SUPPRESSION STRUCTURE FOR HV ISOLATION COMPONENT

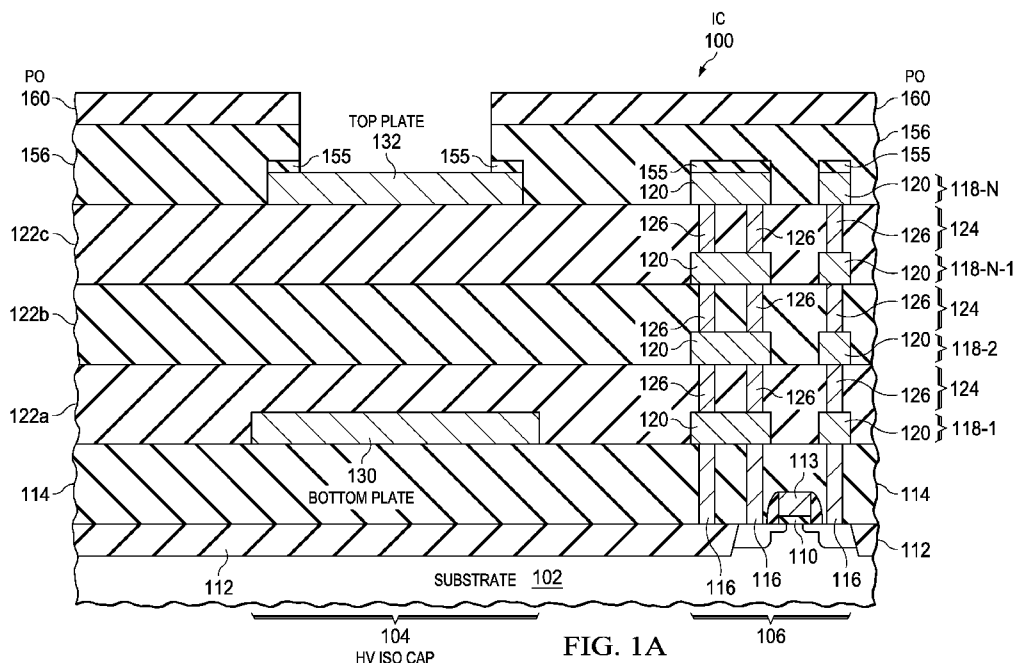


FIG. 1A

(57) Abstract: An integrated circuit (IC) (100) includes a substrate (102) having functional circuitry (106) for realizing at least one circuit function configured together with at least one high voltage isolation component including a top metal feature (132) above the substrate (102). A crack suppressing dielectric structure (155) including at least a crack resistant dielectric layer is on at least a top of the top metal feature (132). At least one dielectric passivation overcoat (PO) layer (160) is on an outer portion of the top metal feature (132).

(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

CRACK SUPPRESSION STRUCTURE FOR HV ISOLATION COMPONENT

[0001] This Disclosure generally relates to the fabrication of integrated circuit (IC) devices having high voltage components such as capacitors or transformers that include crack suppression structures.

BACKGROUND

[0002] Some ICs include high voltage (HV) isolation components such as capacitors or transformers which generally include a first spiral inductor and a second spiral inductor where the first spiral inductor acts to magnetically excite the second spiral inductor. The HV isolation components are positioned above the semiconductor surface within the metal stack, generally having a top metal feature at the top metal layer directly under the passivation layer(s).

[0003] Chemical mechanical polishing/planarization (CMP) is a widely used process of smoothing surfaces with the combination of chemical and mechanical forces. The CMP process uses an abrasive and corrosive chemical slurry together with a polishing pad and retaining ring, typically of a greater diameter than the wafer. The pad and wafer are pressed together by a dynamic polishing head and held in place by a retaining ring. The dynamic polishing head is rotated with different axes of rotation which removes material from the surface of the wafer and tends to even out any irregular topography, making the wafer planar.

[0004] CMP can create cracks in dielectric layers that are polished, such as when CMP is used to planarize a passivation layer stack that generally comprises silicon oxide, such as silicon oxynitride on silicon oxide. The CMP is generally performed on the silicon oxide, then the silicon oxynitride portion of the passivation stack is deposited. The CMP process conditions may be changed to try to reduce the occurrence of such silicon oxide layer cracks.

SUMMARY

[0005] This Summary is provided to introduce a brief selection of disclosed concepts in a simplified form that are further described below in the Detailed Description including the drawings provided. This Summary is not intended to limit the claimed subject matter's scope.

[0006] Disclosed aspects include an IC that comprises a substrate having functional circuitry for realizing at least one circuit function with at least one high voltage isolation component

including a top metal feature above the substrate. A crack suppressing dielectric structure that includes at least a crack resistant dielectric layer is on at least a top of the top metal feature. At least one dielectric passivation overcoat (PO) layer is on an outer portion of the top metal feature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, wherein:

[0008] FIG. 1A depicts a cross-sectional view of a portion of an example IC having a HV isolation capacitor (HV ISO capacitor) including a disclosed dielectric crack suppression structure on top of the top plate of the HV ISO capacitor.

[0009] FIG. 1B depicts a cross-sectional view of a portion of an example IC having a HV ISO capacitor including a disclosed dielectric crack suppression structure on top of the top plate and along the sidewalls of the HV ISO capacitor.

[0010] FIG. 1C shows an example 3 layer crack suppression structure.

[0011] FIGs. 2A-2F are cross-sectional diagrams showing processing progression for an example method of forming an IC having a HV ISO capacitor, according to an example aspect.

[0012] FIG. 2G is a cross-sectional diagram showing a step in the process progression corresponding to FIG. 2F for the HV ISO capacitor for an example method of forming an IC having a HV transformer, according to an example aspect.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] Example aspects are described with reference to the drawings, wherein like reference numerals are used to designate similar or equivalent elements. Illustrated ordering of acts or events should not be considered as limiting, as some acts or events may occur in different order and/or concurrently with other acts or events. Furthermore, some illustrated acts or events may not be required to implement a methodology in accordance with this disclosure.

[0014] Also, the terms "coupled to" or "couples with" (and the like) as used herein without further qualification are intended to describe either an indirect or direct electrical connection. Thus, if a first device "couples" to a second device, that connection can be through a direct electrical connection where there are only parasitics in the pathway, or through an indirect electrical connection via intervening items including other devices and connections. For indirect coupling, the intervening item generally does not modify the information of a signal but may adjust its current level, voltage level, and/or power level.

[0015] While somewhat effective, it is recognized that CMP processing solutions intended to reduce dielectric cracking do not largely eliminate the cracking due to the CMP process. This Disclosure also recognizes dielectric cracks generated during CMP can extend to and terminate on an underlying metal layer, which can result in device failure or degradation in performance. One example of device failure occurs when post-CMP dilute hydrofluoric acid (HF) cleans penetrate through a dielectric crack in the passivation layer to attack the underlying top metal, creating a void in the top metal. Such voids can lead to device failures including failures in the field as a reliability failures, or degradation in IC performance.

[0016] This Disclosure adds a dielectric crack suppression structure comprising a crack resistant dielectric layer between the passivation layer(s) and the top metal layer of the HV isolation component to be crack protected which significantly reduces the incidence of dielectric cracks reaching the top metal that can cause an IC failure or a performance degradation. The HV isolation component is generally designed to withstand a voltage across of at least 100 volts. For example, the crack resistant dielectric layer can comprise a silicon nitride (SiN) layer that can be deposited on top of the top metal before forming the passivation layer(s), which functions as a crack-stop layer to protect the top metal of the HV isolation component from chemical attack when cracks form during CMP of the passivation layer(s).

[0017] FIG. 1A depicts a cross-sectional view of a portion of an example IC 100 having a HV ISO capacitor 104 including a disclosed dielectric crack suppression structure 155 shown by example as a single crack resistant dielectric layer on the outer portion on top of the top plate 132 of the HV ISO capacitor 104. The dielectric crack suppression structure 155 is not shown in the inner window opened through the dielectric passivation overcoat (PO) layer 160 as it is removed during the etch of the PO layer 160.

[0018] The dielectric crack resistant dielectric layer generally comprises SiN, such as 300 to 500Å thick with 100 to 200 MPa of compressive stress. The crack resistant dielectric layer can also comprise other crack resistant materials, such as SiC. The dielectric crack suppression structure 155 can also comprise 2 or more layers, such as the 3 layer crack suppression structure shown in FIG. 1C described below with the crack resistant dielectric layer shown as 155b positioned in between a top layer 155c and a bottom layer 155a. The top plate 132 can comprise TiN, aluminum (Al), or TaN. The bottom plate of the HV ISO capacitor 104 is shown as reference 130. The bottom plate 130 can comprise for example, Al or copper, or alloys thereof.

[0019] The IC 100 may be provided as part of an IC or as a system-on-chip (SOC), and the like. Other configurations for the IC 100 such as a hybrid circuit, are within the scope of the instant example. The IC 100 is formed on a substrate 102 such as a silicon wafer. The HV ISO capacitor 104 is configured for providing galvanic isolation between two voltage domains of an IC or a system having different voltage levels. By way of illustration, a low voltage component which may operate at approximately 24 volts or less, depicted as a metal oxide semiconductor (MOS) transistor 106 with a gate dielectric layer 110 that is generally less than 70 nanometers thick has a gate electrode 113 thereon. MOS transistor 106 is part of functional circuitry that comprises circuit elements (including transistors, and generally diodes, resistors, capacitors, etc.) formed in the substrate 102 configured together with the HV ISO capacitor 104 for realizing at least one circuit function such as analog (e.g., an amplifier, power converter or power field effect transistor (FET)), RF, digital, or a memory function.

[0020] A field oxide (FOX) layer or region 112 may be formed in the substrate 102 (e.g., near or adjacent to a top surface of the substrate) to laterally electrically isolate elements of the IC 100. A pre-metal dielectric (PMD) layer 114 is formed over the substrate 102 including any FOX layer or regions prior to the deposition of subsequent metal layers (e.g., metal levels 118-1 to 118-N). Filled vias 116 may be disposed through the PMD layer 114 to provide electrical connections for the low voltage components such as MOS transistor 106, as well as other components or circuit portions (not specifically shown in FIG. 1A) of the microelectronic device 100A.

[0021] A plurality of metal levels 118-1 (bottom or “first” metal level) to 118-N (top metal level) are disposed over the PMD layer 114 that may include metal interconnects 120 connected to the MOS transistor 106, as well as any additional components, devices, or circuit portions. Inter-level dielectric (ILD) layers 122a, b, c (e.g., dielectric materials or compositions comprised of silicon dioxide-based materials and the like) are disposed between the metal interconnects 120 in each metal level. Respective via levels 124 are disposed between the metal levels 118-1 to 118-N, wherein the example via levels 124 may include metal vias 126 connecting the metal interconnects 120. In one arrangement, the various dielectric layers may be formed in a similar process flow using similar materials. It should be understood that other dielectric materials for the ILD layers 122a, 122b, 122c, such as low dielectric constant (κ) materials, are within the scope of the instant example, for instance, FSG (Fluorinated Silicate Glass with $\kappa = 3.6$), OSG

(Organo-silicate Glass with $\kappa = 2.9$) and ULK (Ultra-low κ Dielectric material, with $\kappa = 2.5$). The ILD layers can include capping layers and etch stop layers of different dielectric materials, such as SiN.

[0022] The bottom plate 130 of the HV ISO capacitor 104 is disposed in one of the metal levels, for example the first metal level 118-1 as depicted in FIG. 1A. The top electrode 132 of the HV ISO capacitor 104 formed from the top metal level 118-N is under a PO layer 160 such as a PO silicon oxynitride layer on another PO layer 156 such as a PO silicon oxide layer, which is depicted over ILD layer 122c.

[0023] The PO layer 156 thickness following CMP is generally 1.0 to 2.0 μm , such as being 1.5 μm measured over the top metal layer 118-N. The PO layer 160 is generally 2.5 μm to 3.0 μm , such as being about 2.8 μm and comprising silicon oxynitride. As single PO layer may also be possible, but a PO only comprising silicon oxide does not provide a moisture barrier, and a PO only comprising silicon nitride may provide too much stress when the top metal level 118-N comprises aluminum.

[0024] The bottom plate 130 and top plate 132 of the HV ISO capacitor 104 are arranged together vertically to operate as a HV capacitor for providing suitable galvanic isolation having desirable breakdown properties in an example implementation of the IC 100, for example, having typical single capacitor surge capability of up to 10kV peak and series capacitor (reinforced isolation) surge capability of up to 17 to 24kV peak, according to certain embodiments.

[0025] The dielectric of the HV ISO capacitor 104 comprising ILD layers 122a, 122b, and 122c may be formed to have a total thickness at least 2 microns (μm) and may be determined by a desired operating voltage of the HV ISO capacitor 104 between its plates 130, 132 and possibly also the substrate 102. For example, an embodiment of the HV ISO capacitor 104 in which the top plate 132 is designed to operate at 750 volts may have a capacitor dielectric with a thickness of 8 μm to 14 μm .

[0026] FIG. 1B depicts a cross-sectional view of a portion of an example IC 150 having a HV ISO capacitor 104' including a disclosed dielectric crack suppression structure 155' on top of the top plate 132 and along the sidewalls of the HV ISO capacitor 104'. As with HV ISO capacitor 104 in FIG. 1A, the dielectric crack suppression structure 155' is not present in the inner window opened through the PO layer 160 as it is removed during the etch of the PO layer 160. The

dielectric crack suppression structure can be deposited on the top metal feature (top plate 132 in FIG. 1B) prior to the patterning and the etching of the top metal feature. In this case, a single mask can be used, and the crack resistant dielectric layer (e.g., SiN) and top metal etches will generally use different chemistries, and the crack suppression structure 155' will only be on top of the top metal feature (as shown in FIG. 1A). The crack suppressing dielectric structure can also be deposited after the patterning and etching of the top metal feature. In this case, the crack suppressing dielectric structure is also positioned on top and on the sidewalls of the top metal features and over layer 122c between metal features.

[0027] FIG. 1C shows an example 3 layer crack suppression structure, shown as a top layer 155c on crack resistant dielectric layer 155b on a bottom layer 155a. The 3 layer crack suppression structure can include a silicon oxide layer as layer 155a for adhesion, a SiN as crack resistant dielectric layer 155b for the crack suppression dielectric layer, and layer 155c comprising a capping oxide to provide a hydrophilic surface for metal patterning. One particular example 3 layer dielectric crack suppression structure stack comprises layer 155a as a 50A silicon oxide layer, crack resistant dielectric layer 155b as a 300 to 500A SiN layer, and layer 155c as a 50 A silicon oxide layer.

[0028] FIG. 2A illustrates in a cross-section view the structure of an in-process HV ISO capacitor on an IC shown at the beginning of the formation of the bottom plate 130. Depicted in FIG. 2A is a semiconductor substrate 102, and the processing layers 212 thereon that represent multiple layers formed during front end processing in prior performed conventional semiconductor processing steps, PMD layer 114 on the processing layer and metal level 118-1 on the PMD layer 114. Filled vias 116 are formed through the PMD layer 114. Metal level 118-1 will be patterned become a bottom plate 130 in the final HV ISO capacitor. In the processing layers 212, the prior processing steps such as lithography, etch, ion implantation and diffusion to form various devices (not shown for simplicity) in the substrate 102 and may interconnect them, such as transistors including MOS transistors, bipolar transistors, or FETs other than MOS, diodes, resistors, inductors, capacitors and the like.

[0029] Metal level 118-1 can be, for example, Al or copper or alloys thereof, the metal being the one used in the particular semiconductor fabrication process. Single and dual damascene copper or copper alloy materials can be used to form metal level 118-1. However, FIGs. 2B-2G show use of non-damascene metal layer processing made possible by aluminum metal layers

which unlike copper can be directly etched.

[0030] FIG. 2B shows the in-process HV ISO capacitor on an IC after patterning of metal level 118-1 including to form the bottom plate 130 of the HV ISO capacitor, followed by the deposition and subsequent planarization of ILD layer 122a. FIG. 2C shows the in-process HV ISO capacitor on an IC after forming several more metal interconnect levels shown as 118-2, 118-3 separated by ILDs 122a, 122b, 122c comprising forming filled vias 116 in the ILD layers, followed by forming patterned metal thereon, etc. In the region over the bottom plate 130 to form the HV ISO capacitor there is only dielectric, shown as ILD layers 122a, 122b, and 122c. The metal level providing the bottom plate 130 is shown as 118-1.

[0031] FIG. 2D shows the in-process HV ISO capacitor on the IC after forming and patterning the top metal level 118-4 including a top plate 132. FIG. 2E shows the in-process HV ISO capacitor on the IC after forming a dielectric crack suppression structure shown as crack resistant dielectric layer 155b on top of the top plate 132 and along the sidewalls of the HV ISO capacitor. The dielectric layer(s) for the dielectric crack suppression structure can be deposited by a low-pressure chemical vapor deposition (LPCVD) process, such as plasma enhanced CVD (PECVD), or high-pressure deposition (HPD). FIG. 2F shows the HV ISO capacitor as 104'' on the IC after forming a PO layer 160 included over the crack resistant dielectric layer 155b followed by planarization with chemical mechanical planarization (CMP).

[0032] A crack 291 is shown emanating from the surface of the PO layer 160 (that can be due to CMP processing) stopping at the crack resistant dielectric layer 155b. As described above, the crack resistant dielectric layer 155b or the respective layers of a dielectric crack suppression structure when comprising two or more layers is generally removed in the inner window opened through the PO layer 160 during the etch of the PO layer 160. Not shown is etching an aperture through the PO layer 160 over a portion of the top plate 132 to enabling bonding a bond wire thereto. Although no contact is shown to the bottom plate 130, contact is generally made by an extension of metal interconnects 120 from the bottom plate over to a nearby circuit element such as a digital converter or modulator. The connection to bottom plate 130 can be either an input or an output node, depending on if the HV ISO capacitor is in a transmitter channel or a receiver channel.

[0033] FIG. 2G is a cross-sectional diagram showing a step in the process progression corresponding to FIG. 2F for the HV ISO capacitor for an example method of forming an IC

having a HV transformer 250, according to an example aspect. The HV transformer 250 includes a top electrode 132a, a top inductance coil 133, and a bottom electrode 130a and bottom inductance coil 133'. In the case of magnetic sensors, only one inductance coil is needed on the top.

[0034] Disclosed aspects can be used to form semiconductor die that may be integrated into a variety of assembly flows to form a variety of different devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, Insulated Gate Bipolar Transistor (IGBT), CMOS, BiCMOS and MEMS.

[0035] Those skilled in the art to which this Disclosure relates will appreciate that many other aspects are possible within the scope of the claimed invention, and further additions, deletions, substitutions and modifications may be made to the described aspects without departing from the scope of this Disclosure.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit (IC), comprising:
 - providing a substrate having functional circuitry for realizing at least one circuit function with at least one high voltage isolation component including a top metal feature above the substrate;
 - depositing a crack suppressing dielectric structure comprising at least one crack resistant dielectric layer on the top metal feature;
 - patterning and etching at least the top metal feature;
 - depositing at least one dielectric passivation overcoat (PO) layer on at least a top of the top metal feature, and
 - planarizing the dielectric PO layer.
2. The method of claim 1, wherein the crack suppressing dielectric structure is deposited on the top metal feature prior to the patterning and the etching of the top metal feature.
3. The method of claim 1, wherein the crack suppressing dielectric structure is deposited after the patterning and the etching of the top metal feature so that so that the crack suppressing dielectric structure is also positioned on sidewalls of the top metal feature.
4. The method of claim 1, wherein the crack suppressing dielectric layer comprises a silicon nitride (SiN) layer or a silicon carbide (SiC) layer.
5. The method of claim 4, wherein the SiN layer or the SiC layer is 200 to 800A thick and has a 50 to 500 megapascal (Mpa) compressive stress.
6. The method of claim 1, wherein the crack suppressing dielectric layer comprises a silicon nitride (SiN) layer that is deposited by a plasma enhanced chemical vapor deposition process.
7. The method of claim 6, wherein the depositing the crack suppressing dielectric structure further comprises depositing a bottom silicon oxide layer before the depositing of the SiN layer and depositing a top silicon oxide layer after the depositing of the SiN layer.
8. The method of claim 1, wherein the planarizing the dielectric PO layer comprises chemical mechanical polishing (CMP).
9. The method of claim 1, wherein the high voltage isolation component comprises a high voltage capacitor.
10. The method of claim 1, wherein the high voltage isolation component comprises a

transformer, and wherein the top metal feature comprises a top electrode inductively coupled to an outer positioned inductance coil.

11. The method of claim 1, further comprising etching an opening through the dielectric PO layer and through the crack suppressing dielectric structure to reach the top metal feature.

12. An integrated circuit (IC), comprising:

a substrate having functional circuitry for realizing at least one circuit function with at least one high voltage isolation component including a top metal feature above the substrate;

a crack suppressing dielectric structure comprising at least a crack resistant dielectric layer on at least a top of the top metal feature, and

at least one dielectric passivation overcoat (PO) layer on an outer portion of the top metal feature.

13. The IC of claim 12, wherein the crack suppressing dielectric structure is also positioned on sidewalls of the top metal feature.

14. The IC of claim 12, wherein the crack resistant dielectric layer comprises silicon nitride (SiN) layer or a silicon carbide (SiC) layer.

15. The IC of claim 14, wherein the SiN layer or the SiC layer is 200-800Å thick and has a 50 to 500 megapascal (Mpa) compressive stress.

16. The IC of claim 12, wherein the crack suppressing dielectric layer comprises a silicon nitride (SiN) layer that is between a top silicon oxide layer and a bottom silicon oxide layer.

17. The IC of claim 12, wherein the high voltage isolation component comprises a high voltage capacitor.

18. The IC of claim 12, wherein the high voltage isolation component comprises a transformer, and wherein the top metal feature comprises a top electrode inductively coupled to an outer positioned inductance coil.

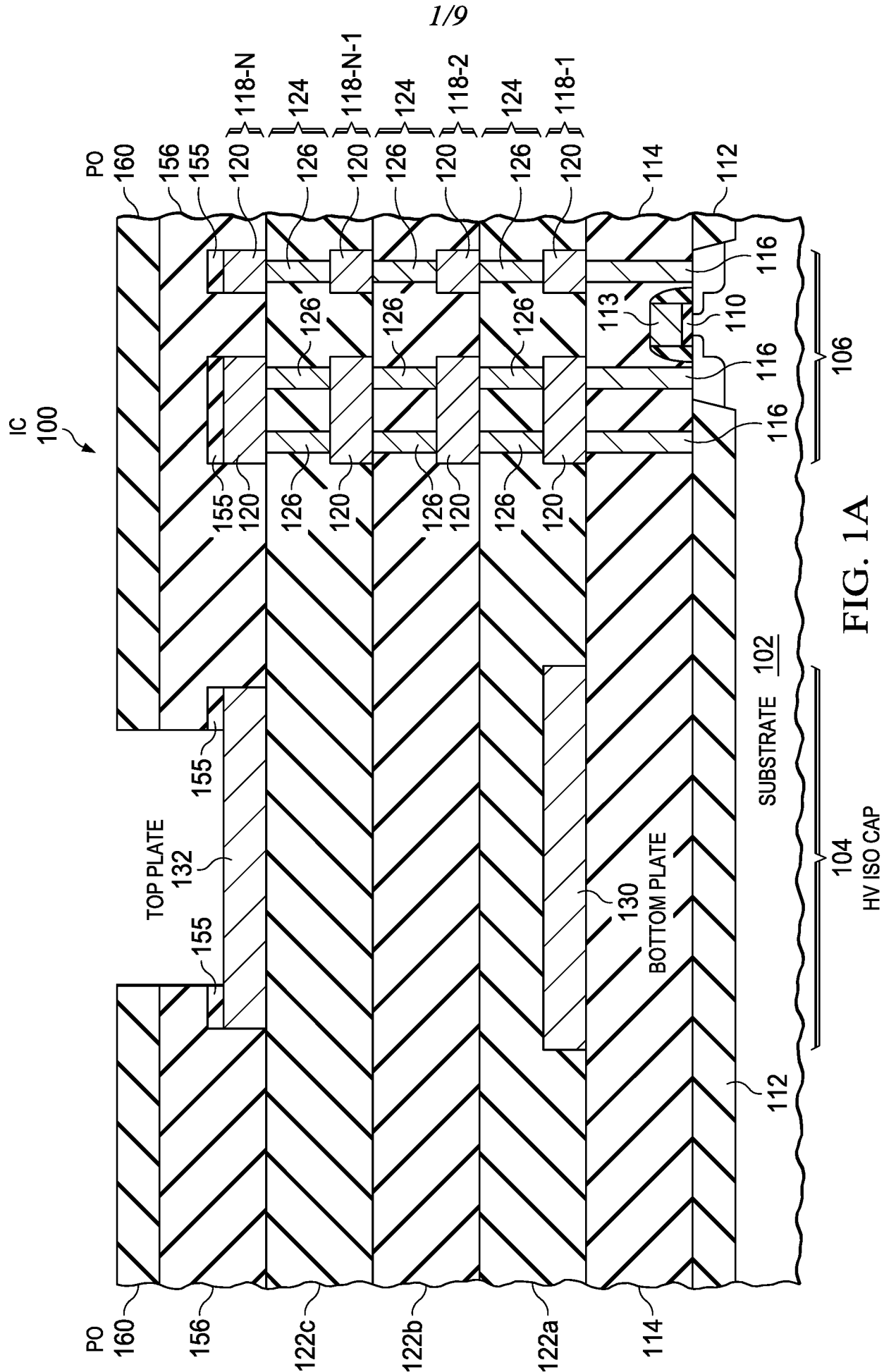
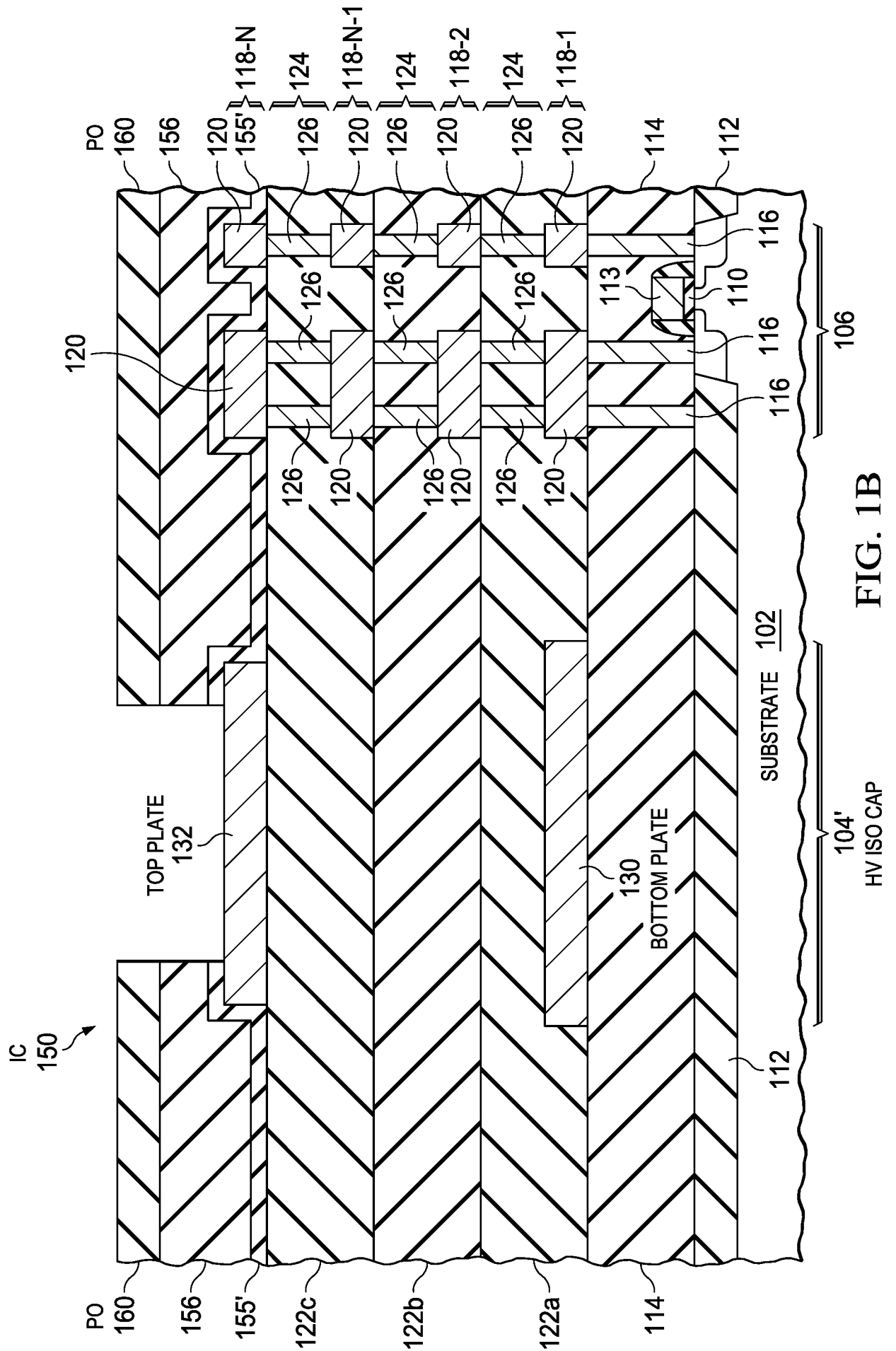


FIG. 1A



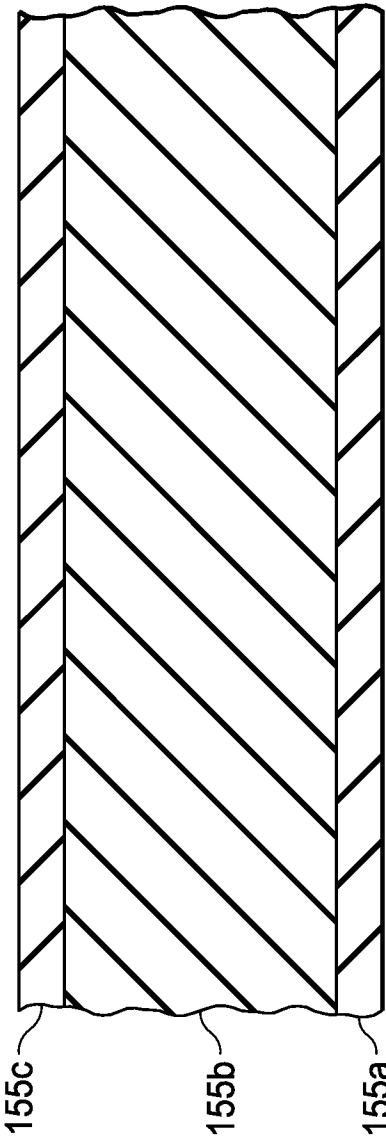


FIG. 1C

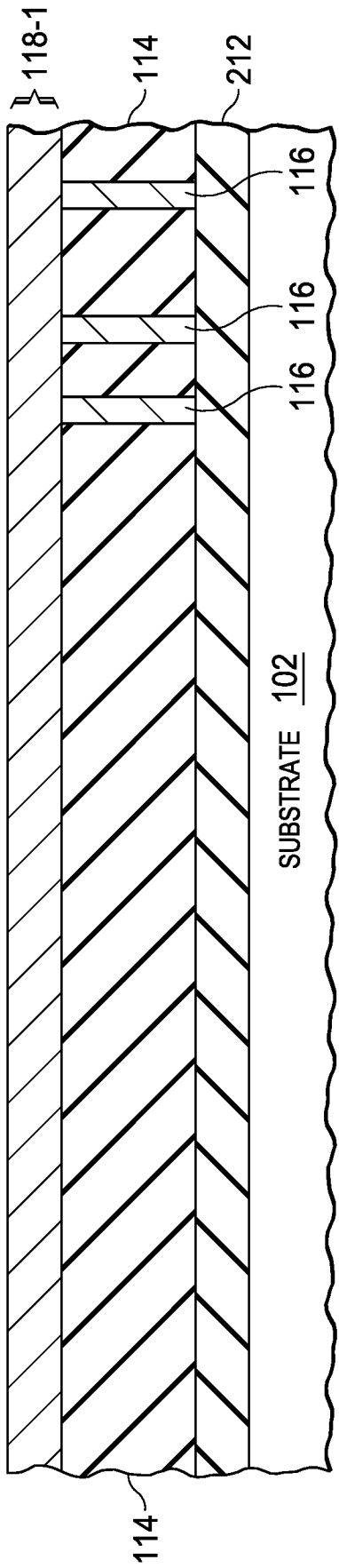


FIG. 2A

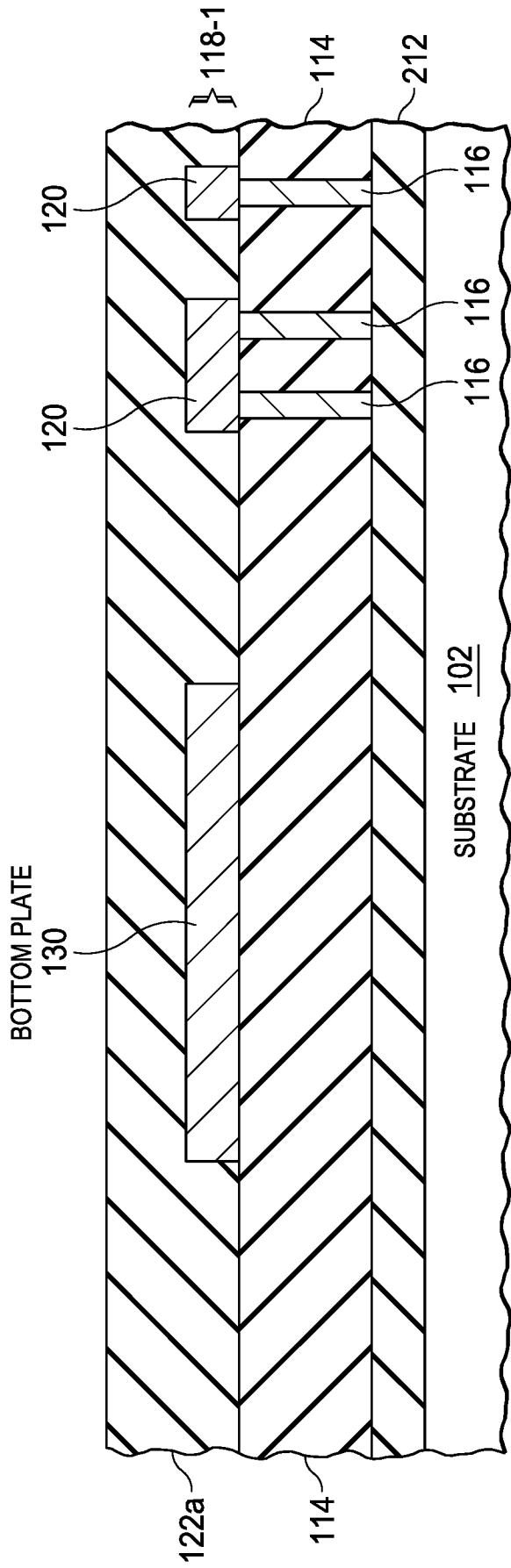


FIG. 2B

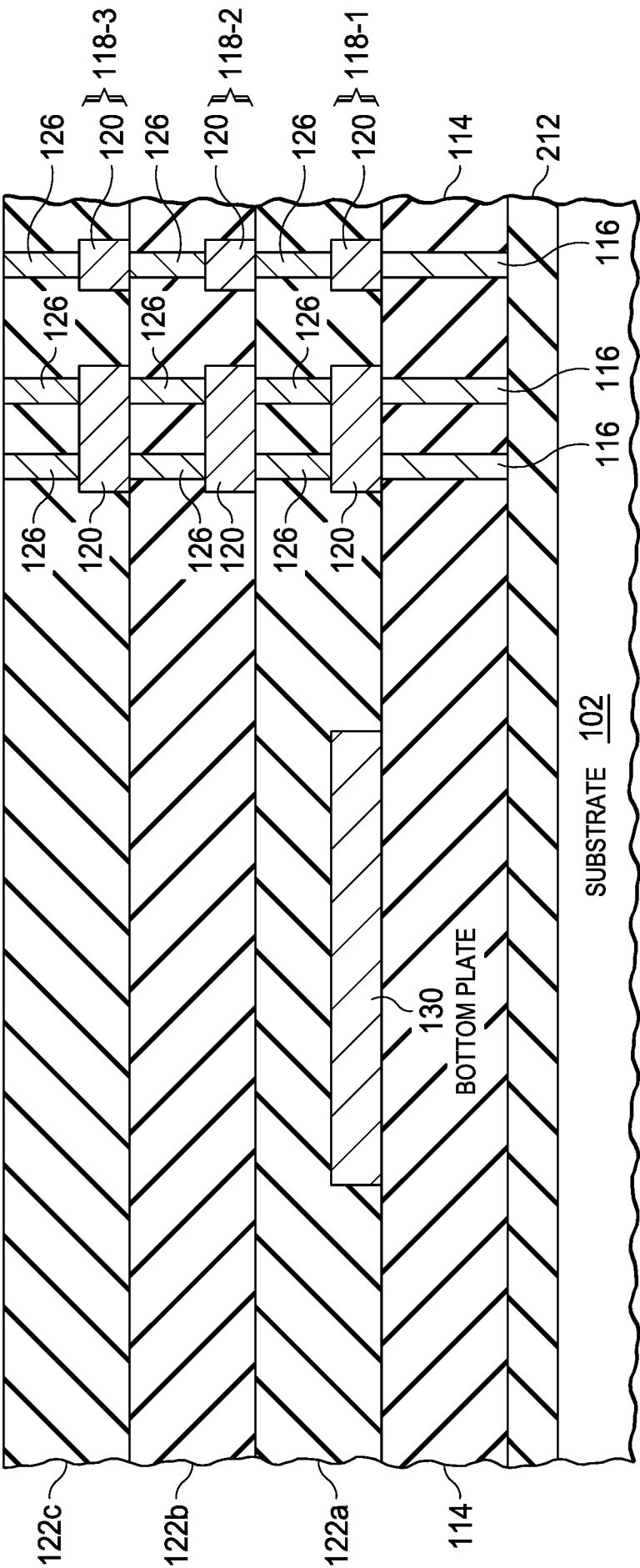


FIG. 2C

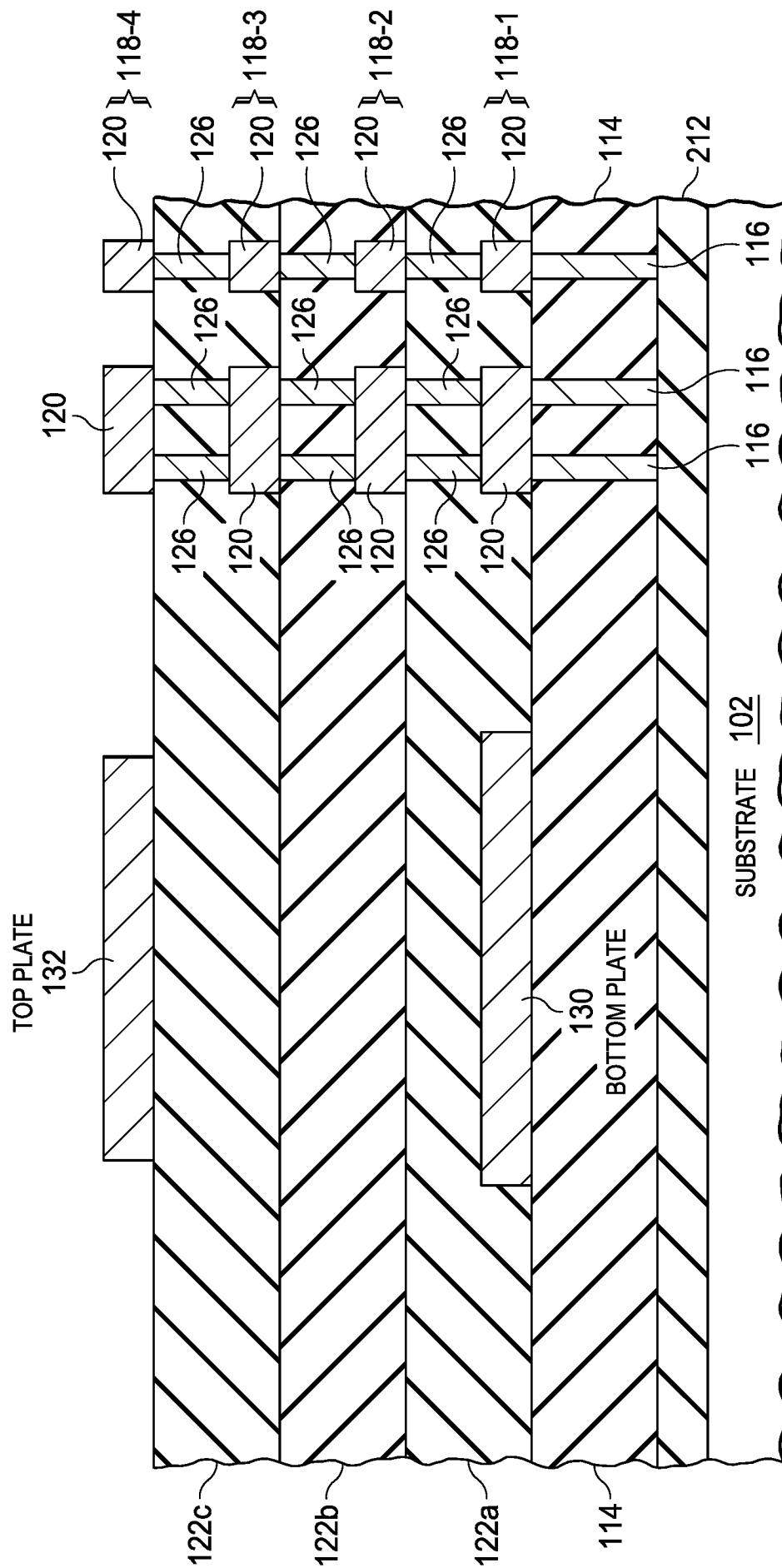


FIG. 2D

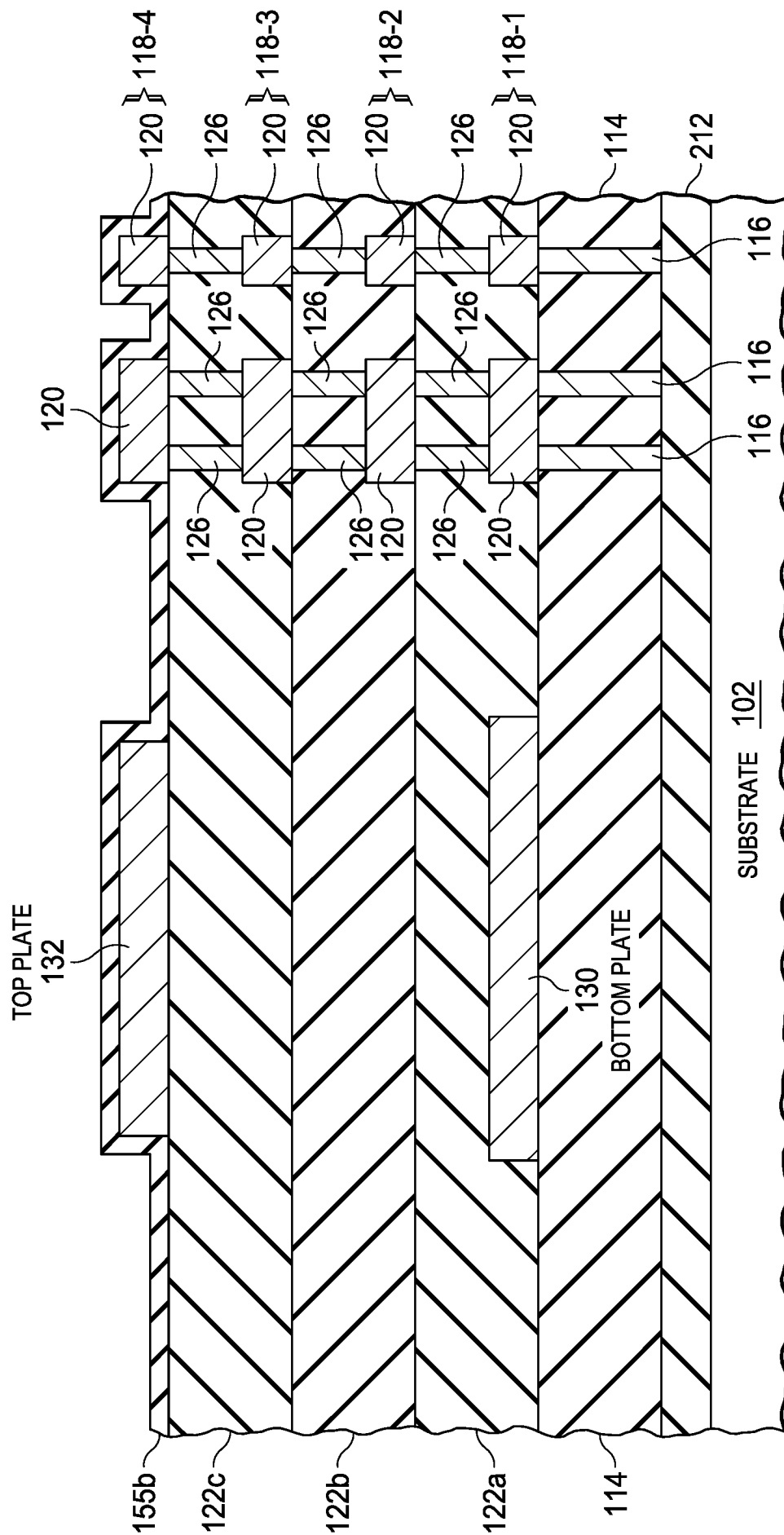


FIG. 2E

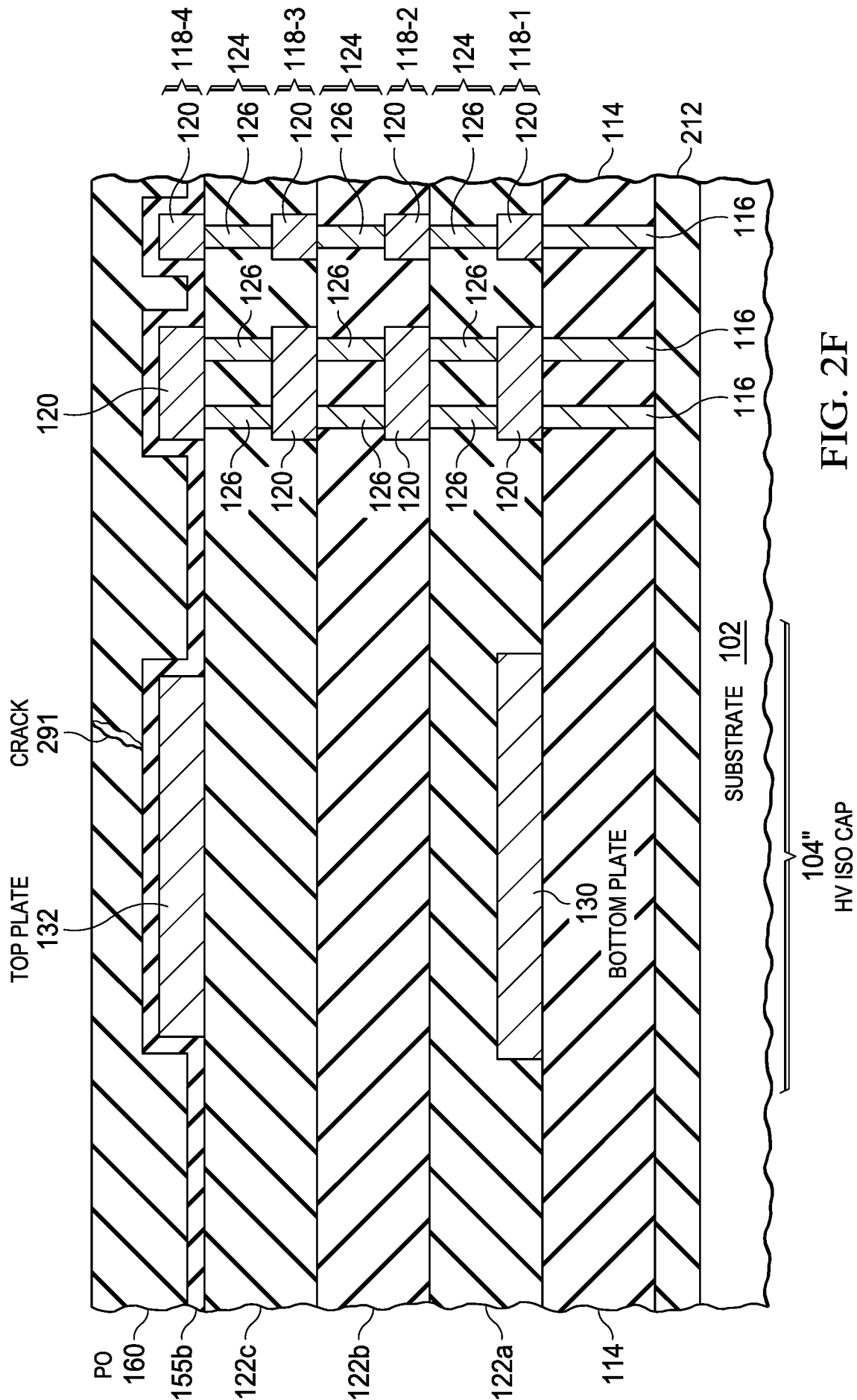
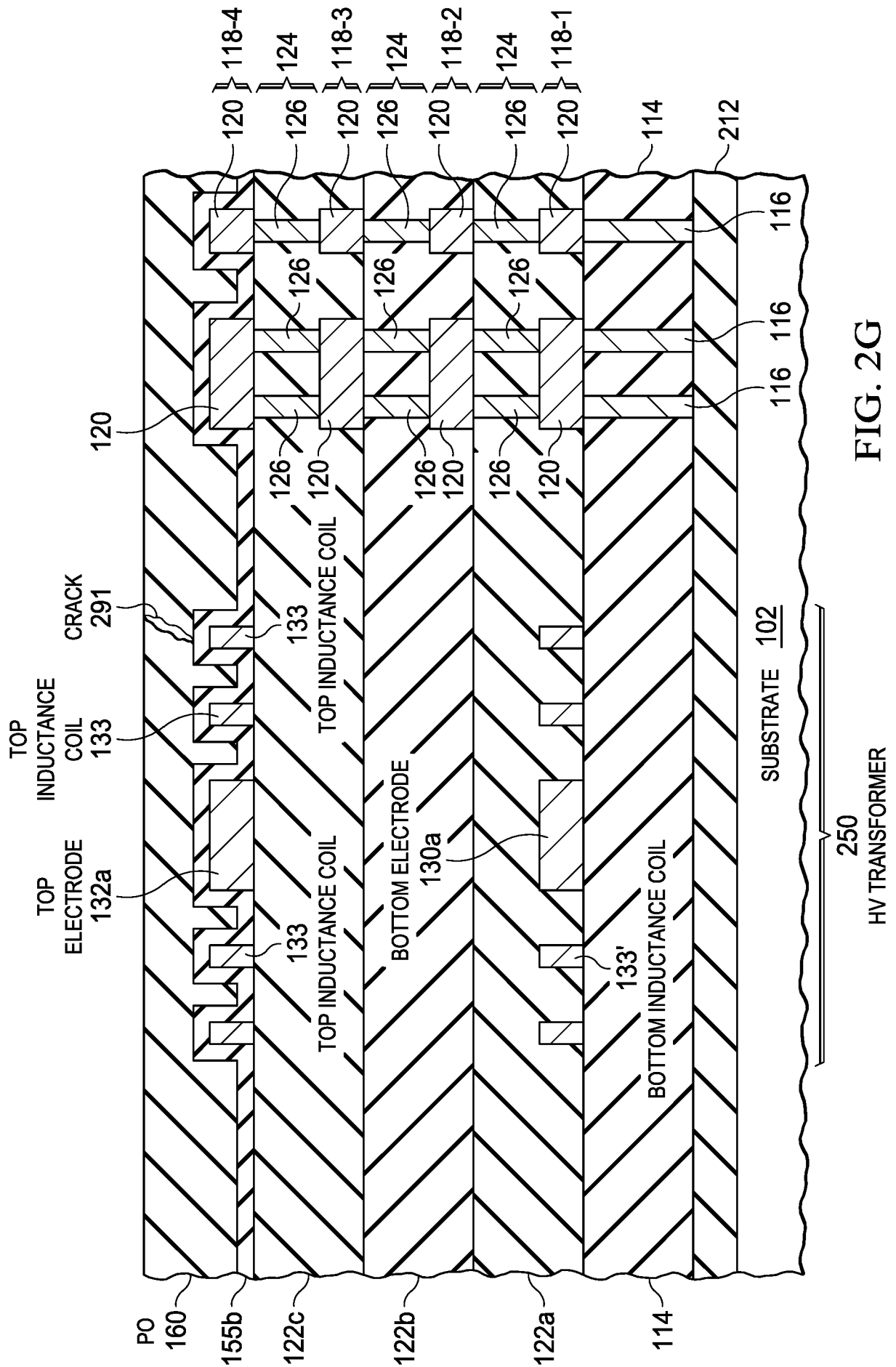


FIG. 2F



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/043437

A. CLASSIFICATION OF SUBJECT MATTER												
H01L 27/06 (2006.01) H01L 29/94 (2006.01) H01L 49/02 (2006.01)												
According to International Patent Classification (IPC) or to both national classification and IPC												
B. FIELDS SEARCHED												
Minimum documentation searched (classification system followed by classification symbols)												
H01L 21/00, 21/28, 21/285, 21/321, 21/3213, 21/762, 21/768, H01L 27/00, 27/06, H01L 29/00, 29/94, H01L 49/00, 49/02												
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched												
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)												
EAPATIS, ESP@CE, ESP@CENET, Google, KIPRIS, PAJ, PatSearch, RUABRU, RUABU1, RUPAT, RUPAT OLD, RUPTO, USPTO, USPTO DB, WIPO, elibrary.ru												
C. DOCUMENTS CONSIDERED TO BE RELEVANT												
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.										
A	US 2016/0163785 A1 (TEXAS INSTRUMENTS INCORPORATED) 09.06.2016	1-18										
A	WO 2016/073960 A1 (TEXAS INSTRUMENTS INCORPORATED) 12.05.2016	1-18										
A	US 2015/0187598 A1 (TEXAS INSTRUMENTS INCORPORATED) 02.07.2015	1-18										
A	US 2016/0155737 A1 (GLOBALFOUNDRIES SINGAPORE PTE. LTD.) 02.06.2016	1-18										
A	US 5618749 A (YAMAHA CORPORATION) 08.04.1997	1-18										
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.												
* Special categories of cited documents: <table border="0"> <tr> <td>“A” document defining the general state of the art which is not considered to be of particular relevance</td> <td>“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>“E” earlier document but published on or after the international filing date</td> <td>“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>“O” document referring to an oral disclosure, use, exhibition or other means</td> <td>“&” document member of the same patent family</td> </tr> <tr> <td>“P” document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			“A” document defining the general state of the art which is not considered to be of particular relevance	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	“E” earlier document but published on or after the international filing date	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	“O” document referring to an oral disclosure, use, exhibition or other means	“&” document member of the same patent family	“P” document published prior to the international filing date but later than the priority date claimed	
“A” document defining the general state of the art which is not considered to be of particular relevance	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention											
“E” earlier document but published on or after the international filing date	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone											
“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art											
“O” document referring to an oral disclosure, use, exhibition or other means	“&” document member of the same patent family											
“P” document published prior to the international filing date but later than the priority date claimed												
Date of the actual completion of the international search		Date of mailing of the international search report										
18 November 2019 (18.11.2019)		21 November 2019 (21.11.2019)										
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer M. Adireeva Telephone No. 499-240-60-15										