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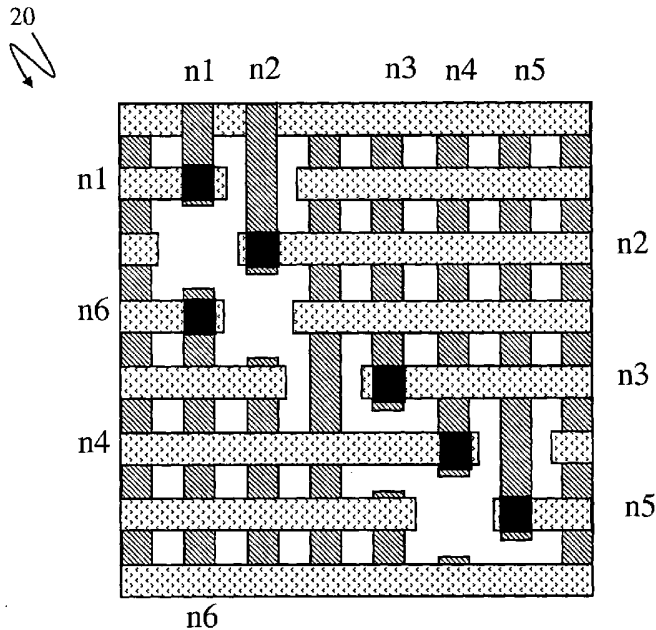
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(54) Title: LITHOGRAPHY AND ASSOCIATED METHODS, DEVICES, AND SYSTEMS



(57) Abstract: An integrated circuit, comprising a plurality of interconnect lines each having a spacing and width, wherein the interconnect lines are formed with a mask (72), at least one of a contact and via connected to at least one of the interconnect lines, wherein the at least one contact and via has the same spacing and width as the interconnect lines, and wherein the contact or via is formed with the mask (72) used to form the interconnect lines. Also disclosed are methods for forming integrated circuits.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G03F H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 5 343 271 A (MORISHIGE ET AL) 30 August 1994 (1994-08-30) the whole document -----	1-26
Y	EP 0 347 332 A (FUJITSU LIMITED) 20 December 1989 (1989-12-20) the whole document -----	1-26
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A	US 2002/106588 A1 (LAI CHIEN-WEN ET AL) 8 August 2002 (2002-08-08) ----- -/--	

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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