



(43) International Publication Date
18 October 2012 (18.10.2012)

- (51) International Patent Classification:
H01L 21/02 (2006.01) *H01L 21/265* (2006.01)
H01L 21/20 (2006.01)
- (21) International Application Number:
PCT/US2012/032727
- (22) International Filing Date:
9 April 2012 (09.04.2012)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
61/473,984 11 April 2011 (11.04.2011) US
13/440,616 5 April 2012 (05.04.2012) US
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD,

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(54) Title: METHOD FOR EPITAXIAL LAYER OVERGROWTH

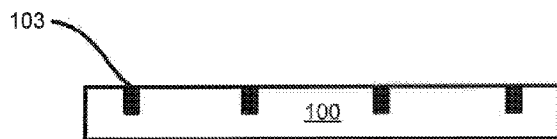


FIG. 2A

(57) Abstract: Oxygen, silicon, germanium, carbon, or nitrogen is selectively implanted into a workpiece. The workpiece is annealed to incorporate the ions into the workpiece. A compound semiconductor is then formed on the workpiece. For example, gallium nitride may be formed on a silicon, silicon carbide, or sapphire workpiece. The width of the implanted regions can be configured to compensate for any shrinkage during annealing.

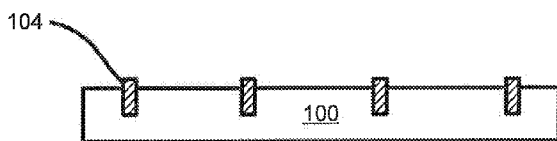


FIG. 2B

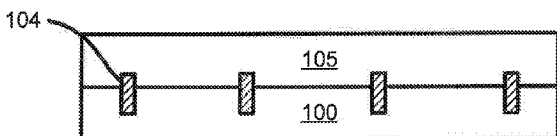


FIG. 2C



SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD,
RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ,

DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT,
LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS,
SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

METHOD FOR EPITAXIAL LAYER OVERGROWTH

FIELD

This invention relates to epitaxial layer overgrowth (ELOG) and, more particularly, to ELOG using ion implantation.

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BACKGROUND

Ion implantation is a standard technique for introducing conductivity-altering impurities into a workpiece. A desired impurity material is ionized in an ion source, the ions are accelerated to form an ion beam of prescribed energy, and the ion beam is directed at the surface of the workpiece. The energetic ions in the beam penetrate into the bulk of the workpiece material and are embedded into the crystalline lattice of the workpiece material to form a region of desired conductivity.

In order for light-emitting diodes (LEDs) to gain more of the lighting market, improvements in efficiency and manufacturing cost may be required. LEDs, laser diodes, or other devices may be fabricated on compound semiconductors, such as GaN. One method of improving the efficiency of compound semiconductor devices is ELOG. ELOG uses a periodic mask structure to block the growth of GaN in some areas. Then some GaN will grow more laterally when it joins neighboring areas. This may result in a higher quality solid layer of GaN. Previous methods used a photoresist (PR) mask to block a portion of the implanted ions, but this adds cost and complexity. Accordingly, there is a need in the art for improved methods of ELOG.

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SUMMARY

According to a first aspect of the invention, a method of workpiece processing is provided. The method comprises selectively implanting ions into a plurality of implanted regions in a workpiece. The ions comprise oxygen, silicon, germanium, carbon, or nitrogen. The workpiece is annealed such that the ions are incorporated into the implanted regions. A compound semiconductor is formed on the workpiece.

According to a second aspect of the invention, a method of workpiece processing is provided. The method comprises determining a width of an implanted region to compensate for shrinkage of the width during annealing. Oxygen ions are selectively implanted into a plurality of the implanted regions in a workpiece. Each of the implanted regions has a box profile beginning at a surface of the workpiece and has the width. The workpiece comprises silicon. The workpiece is annealed to form silicon oxide on the implanted regions. A compound semiconductor is formed on the workpiece.

According to a third aspect of the invention, a method of workpiece processing is provided. The method comprises determining a width of an implanted region to compensate for shrinkage of the

width during annealing. Nitrogen ions are selectively implanted into a plurality of implanted regions in a workpiece. Each of the implanted regions has a box profile beginning at a surface of the workpiece and has the width. The workpiece comprises silicon. The workpiece is annealed to form silicon nitride on the implanted regions. A compound semiconductor is formed on the workpiece.

5

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present disclosure, reference is made to the accompanying drawings, which are incorporated herein by reference and in which:

FIG. 1 is a block diagram of a plasma processing apparatus having a plasma sheath modifier;

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FIGs. 2A-2C are cross-sectional side views of a first embodiment of ELOG using implantation;

FIG. 3 is a side view of an embodiment of selective ion implantation; and

FIG. 4 is a cross-sectional side view illustrating shrinkage of the implanted areas.

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DETAILED DESCRIPTION

The embodiments are described herein in connection with formation of a compound semiconductor such as GaN, but these embodiments also may be used with other III/V compound semiconductors, II/VI compound semiconductors, or other materials known to a person skilled in the art. While one specific type of implanter is disclosed, other ion implantation systems known to those skilled in the art that can focus an ion beam or that can implant particular regions of a workpiece without a mask on the workpiece may be used in the embodiments described herein. For example, this may involve a stencil or shadow mask disposed a distance from the workpiece in an alternate embodiment. Beamline implanters, plasma doping implanters, flood implanters, or focused ion beam implanters may be used. Thus, the invention is not limited to the specific embodiments described below.

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FIG. 1 is a block diagram of a plasma processing apparatus. The plasma 140 is generated as is known in the art. This plasma 140 is generally a quasi-neutral collection of ions and electrons. The ions typically have a positive charge while the electrons have a negative charge. The plasma 140 may have an electric field of, for example, approximately 0 V/cm in the bulk of the plasma 140. In a system containing the plasma 140, ions 102 from the plasma 140 are attracted toward a workpiece 100. These ions 102 may be attracted with sufficient energy to be implanted into the workpiece 100. The plasma 140 is bounded by a region proximate the workpiece 100 referred to as a plasma sheath 242. The plasma sheath 242 is a region that has fewer electrons than the plasma 140. Hence, the differences between the negative and positive charges cause a sheath potential in the plasma sheath 242. The light emission from this plasma sheath 242 is less intense than the plasma 140 because

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fewer electrons are present and, hence, fewer excitation-relaxation collisions occur. Thus, the plasma sheath 242 is sometimes referred to as "dark space."

The sheath modifier 101 is configured to modify an electric field within the plasma sheath 242 to control a shape of a boundary 241 between the plasma 140 and the plasma sheath 242.

5 Accordingly, ions 102 that are attracted from the plasma 140 across the plasma sheath 242 may strike the workpiece 100 at a large range of incident angles. This sheath modifier 101 also may be referred to as, for example, a focusing plate or sheath engineering plate and may be a semiconductor, insulator, or conductor.

10 In the embodiment of FIG. 1, the sheath modifier 101 includes a pair of panels 212 and 214 defining an aperture therebetween having a horizontal spacing (G). In other embodiments, the sheath modifier 101 may include only one panel or more than two panels. The panels 212 and 214 may be a pair of sheets having a thin, flat shape. In other embodiments, the panels 212 and 214 may be other shapes such as tube-shaped, wedge-shaped, and/or have a beveled edge proximate the aperture. The panels 212 and 214 also may be positioned a vertical spacing (Z) above the plane 151 defined by the
15 front surface of the workpiece 100. In one embodiment, the vertical spacing (Z) may be about 1.0 to 10.0 mm.

Ions 102 may be attracted from the plasma 140 across the plasma sheath 242 by different mechanisms. In one instance, the workpiece 100 is biased to attract ions 102 from the plasma 140 across the plasma sheath 242. In another instance, a plasma source that generates the plasma 140 and
20 walls surrounding the plasma 140 are biased positively and the workpiece 100 may be grounded. The biasing may be pulsed in one particular embodiment. In yet another instance, electric or magnetic fields are used to attract ions 102 from the plasma 140 toward the workpiece 100.

Advantageously, the sheath modifier 101 modifies the electric field within the plasma sheath 242 to control a shape of the boundary 241 between the plasma 140 and the plasma sheath 242. The
25 boundary 241 between the plasma 140 and the plasma sheath 242 may have a convex shape relative to the plane 151 or another shape not parallel to the plane 151. When the workpiece 100 is biased, for example, the ions 102 are attracted across the plasma sheath 242 through the aperture between the panels 212 and 214 at a large range of incident angles. For instance, ions 102 following trajectory path 271 may strike the workpiece 100 at an angle of $+0^\circ$ relative to the plane 151. Ions 102
30 following trajectory path 270 may strike the workpiece 100 at about an angle of 0° relative to the same plane 151. Ions 102 following trajectory path 269 may strike the workpiece 100 an angle of -0° relative to the plane 151. Accordingly, the range of incident angles may be between $+0^\circ$ and -0° centered about 0° . In addition, some ion trajectories paths such as paths 269 and 271 may cross each other. Depending on a number of factors including, but not limited to, the horizontal spacing (G)
35 between the panels 212 and 214, the vertical spacing (Z) of the panels 212 and 214 above the plane

151, the dielectric constant of the panels 212 and 214, or other process parameters of the plasma 140, the range of incident angles (θ) may be between $+60^\circ$ and -60° centered about 0° , though other ranges of θ are possible. In another embodiment, the panels 212 and 214 may each have different vertical spacing (Z) relative to the workpiece 100, which may allow the ions 102 to primarily follow

5 trajectories at an angle relative to the plane 151.

In one embodiment, the process disclosed herein is used to grow GaN on a workpiece. FIGs. 2A-2C are cross-sectional side views of a first embodiment of ELOG using implantation. In FIG. 2A, the workpiece 100, which may be silicon, sapphire, or another material, is selectively implanted with oxygen to form implanted regions 103. Four implanted regions 103 are illustrated in FIG. 2A, but
10 more or fewer are possible. Each implanted region 103 may be between, for example, a few μm to a few mm in dimension and may be a line across the surface of the workpiece 100. The implanted regions 103 may be formed using the plasma sheath modifier 101 of FIG. 1 in one instance. The workpiece 100 or plasma sheath modifier 101 may be translated or scanned to form the multiple implanted regions 103. The biasing may be timed with this translation or scanning to form the
15 implanted regions 103. The embodiment illustrated in FIG. 2A does not require a mask on the surface of the workpiece 100 to form the implanted regions 103.

In one particular embodiment, the implanted regions 103 have a box profile beginning at the surface of the workpiece 100. Thus, the implanted regions 103 may have a surface peak. The implanted regions 103 may be doped to a depth of greater than approximately 100 nm in one instance.

20 In an alternate embodiment, the implanted regions 103 have a curved profile.

In FIG. 2B, the workpiece 100 is annealed. This incorporates the implanted species into the workpiece. SiO_2 regions 104 are created using some or all of the implanted regions 103. These SiO_2 regions 104 are then used for ELOG. Then in FIG. 2C a GaN layer 105 is formed on the workpiece 100 using ELOG. The GaN layer 105 may not grow in a blanket pattern. Instead, the GaN layer 105
25 may begin growing between the SiO_2 regions 104 and eventually grow together over the SiO_2 regions 104. This growth pattern may decrease the number of dislocations that occur within the GaN layer 105. The use of ELOG will result in a GaN layer 105 of higher quality.

In an alternate embodiment, the workpiece 100 is sapphire or SiC and silicon is implanted to form the implanted regions 103. During an anneal in an oxygen atmosphere the SiO_2 regions 104 are
30 formed. A GaN layer 105 is then formed on the workpiece 100 using ELOG.

In yet another alternate embodiment, nitrogen is used to form the implanted regions 103 in a workpiece 100. SiN regions are formed during the anneal instead of SiO_2 regions 104. A GaN layer 105 is then formed on the workpiece 100 using ELOG.

Germanium also may be used to form the implanted regions 103 in the workpiece 100. SiGe
35 regions are formed during the anneal instead of SiO_2 regions 104. A GaN layer 105 is then formed on

the workpiece 100 using ELOG. The presence of SiGe may cause some strain in the workpiece 100, which may benefit the growth of the GaN layer 105 during ELOG. For example, the GaN layer 105 may grow above the implanted regions 103 at a different rate than the non-implanted regions.

Carbon also may be used to form the implanted regions 103 in the workpiece 100.

5 Amorphous regions containing carbon are formed during implantation or anneal instead of the of SiO₂ regions 104. A GaN layer 105 is then formed on the workpiece 100 using ELOG. The carbon or crystal structure of the implanted regions 103 may prevent or reduce growth of the GaN layer 105 over the implanted regions 103. These implanted regions 103 may not shrink during an anneal.

10 In another embodiment, a mixture of ions may be implanted into the workpiece. For example, nitrogen and oxygen may be used to form the implanted regions 103. Other combinations of species disclosed herein or combinations of species disclosed herein with other species are possible.

FIG. 3 is a side view of an embodiment of selective ion implantation. Implanted regions 103 are formed in the workpiece 100 using the ions 102. The workpiece 100 is scanned with respect to the sheath modifier 101 or ions 102, as illustrated by the arrow 106. This may involve moving the
15 sheath modifier 101, workpiece 100, or both. The scanning may be in one dimension or two dimensions. In one particular embodiment, the workpiece 100 is biased when the ions 102 implant the implanted regions 103. The bias scheme is adjusted to produce the desired pattern of implanted regions 103. Thus, the workpiece 100 is not biased when the ions 102 would implant between the implanted regions 103. This eliminates or reduces ions 102 from impacting between the implanted
20 regions 103. In this manner, the implanted regions 103 may be formed without a mask or photoresist layer on the workpiece 100. Alignment, lithography, or photoresist removal steps may be eliminated.

The location of the implanted regions 103 may be carefully controlled because spacing of the implanted regions 103 may affect growth of the GaN layer 105 during ELOG. This spacing may be optimized for the best GaN layer 105 growth.

25 The dose rate and focus of the ions 102 can be varied to form the implanted regions 103. If the workpiece 100 is scanned, then the ions 102 may be switched on and off to form the implanted regions 103, the dose of the ion 102 may be adjusted to reduce implantation between the implanted regions 103, or the ions 102 may be focused when implanting the implanted regions 103. If the ions 102 are focused when implanting the implanted regions 103, the ions 102 may be less focused over
30 other parts of the workpiece 100, which reduces implantation between the implanted regions 103.

FIG. 4 is a cross-sectional side view illustrating shrinkage of the implanted areas. Here, the implanted regions 103 are illustrated as shaded black with a width 107. The SiO₂ regions 104 are illustrated in cross-hatch with a width 108, though this also may be used for SiN regions or for other species disclosed herein. The width 108 is less than the width 107. This is due to the annealing step,
35 which leads to shrinkage. For example, some of the oxygen (or nitrogen) may diffuse from the

workpiece 100 during the anneal. In one particular embodiment, a width 107 of an implanted region 103 is determined in order to compensate for shrinkage of the width 107 during annealing to the width 108. Thus, the width 108 is configured to the desired dimension for ELOG during growth of the GaN layer. In one instance, the width 108 is approximately 30% to 70% less than the width 107 and the width 107 is configured to be larger to compensate for this shrinkage. In one instance, a width 107 of 10 μm shrank to a width 108 3 μm during anneal.

The anneal conditions also may be varied to improve the later ELOG step. These anneal conditions affect the sharpness of the implanted regions 103.

In another alternate embodiment, the implanted regions 103 are doped after formation or after anneal. This may change the conductivity of the implanted regions 103. In another instance, the implanted regions 103 are subsequently doped with silicon after an anneal. For example, silicon may be implanted into the SiO_2 of the implanted regions 103 to improve ELOG. In another example, an ion species such as germanium is implanted into the implanted regions 103 to cause stress in the lattice of the workpiece 100.

The implants disclosed herein may be performed into a heated workpiece 100. This workpiece 100 may be at a temperature elevated above room temperature, such as up to about 400°C or other elevated temperatures. This may affect the incorporation of ion species into the workpiece 100 or affect the required anneal.

The embodiments disclosed herein can be applied to other compound semiconductors besides GaN, such as other II-VI or III-V compound semiconductors. Other workpiece materials, ions, or annealing environments also may be used. This technique enables a higher quality thin film. Patterned or textured workpieces also can be used, which was difficult using previous methods. An angular distribution of ions may be used to treat all the sidewalls of the patterned or textured workpiece. In another instance, multiple implants at different angles may be used to treat all the sidewalls of the patterned or textured workpiece.

The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. These other embodiments and modifications are intended to fall within the scope of the present disclosure. Furthermore, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

What is claimed is:

1. A method of workpiece processing comprising:
selectively implanting ions into a plurality of implanted regions in a workpiece, wherein
5 said ions comprise oxygen, silicon, germanium, carbon, or nitrogen;
annealing said workpiece such that said ions are incorporated into said implanted regions;
and
forming a compound semiconductor on said workpiece.
- 10 2. The method of claim 1, wherein said workpiece is silicon and said ions comprise oxygen or nitrogen.
3. The method of claim 1, wherein said workpiece is one of sapphire or silicon carbide and said ions comprise silicon.
- 15 4. The method of claim 1, wherein said compound semiconductor is one of a II-VI semiconductor or a III-V semiconductor.
5. The method of claim 1, wherein said selectively implanting comprises scanning said
20 workpiece with respect to said ions and increasing a bias to said workpiece to form said implanted regions.
6. The method of claim 1, wherein said workpiece has a non-planar surface.
- 25 7. The method of claim 1, wherein said ions are implanted in a box profile beginning at a surface of said workpiece.
8. The method of claim 7, wherein said ions are implanted to a depth of at least 100 nm.
- 30 9. The method of claim 1, wherein each of said implanted regions has a width and further comprising determining said width to compensate for shrinkage of said width during said annealing.
10. A method of workpiece processing comprising:

determining a width of an implanted region to compensate for shrinkage of said width during annealing;
selectively implanting oxygen ions into a plurality of said implanted regions in a workpiece, each of said implanted regions having a box profile beginning at a surface of said workpiece and each of said implanted regions having said width, said workpiece comprising silicon;
annealing said workpiece to form silicon oxide on said implanted regions; and forming a compound semiconductor on said workpiece.

11. The method of claim 10, wherein said selectively implanting comprises scanning said workpiece with respect to said oxygen ions and increasing a bias to said workpiece to form said implanted regions.

12. The method of claim 10, wherein said compound semiconductor is one of a II-VI semiconductor or a III-V semiconductor.

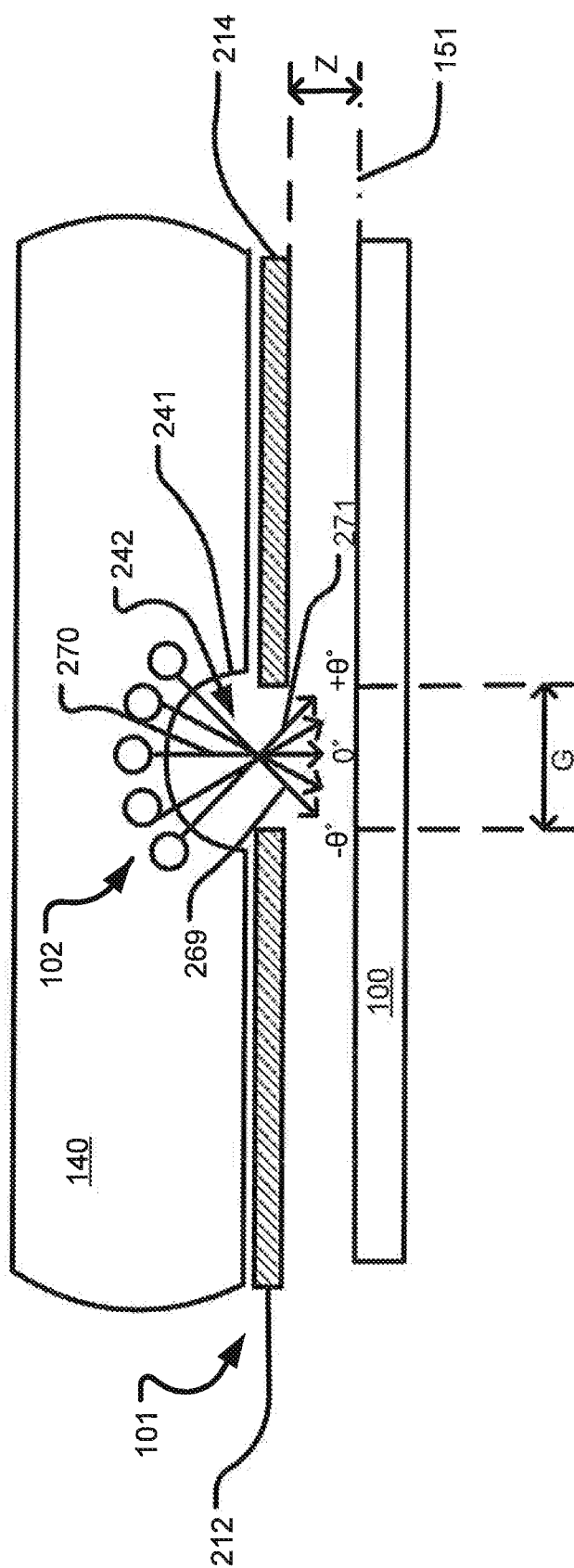
13. The method of claim 12, wherein said compound semiconductor is GaN.

14. The method of claim 10, wherein said workpiece has a non-planar surface.

15. The method of claim 10, wherein said oxygen ions are implanted to a depth of at least 100 nm.

16. A method of workpiece processing comprising:
determining a width of an implanted region to compensate for shrinkage of said width during annealing;
selectively implanting nitrogen ions into a plurality of implanted regions in a workpiece, each of said implanted regions having a box profile beginning at a surface of said workpiece and each of said implanted regions having said width, said workpiece comprising silicon;
annealing said workpiece to form silicon nitride on said implanted regions; and forming a compound semiconductor on said workpiece.

17. The method of claim 16, wherein said selectively implanting comprises scanning said workpiece with respect to said nitrogen ions and increasing a bias to said workpiece to form said implanted regions.
- 5 18. The method of claim 16, wherein said compound semiconductor is one of a II-VI semiconductor or a III-V semiconductor.
19. The method of claim 16, wherein said compound semiconductor is GaN.
- 10 20. The method of claim 16, wherein said workpiece has a non-planar surface.



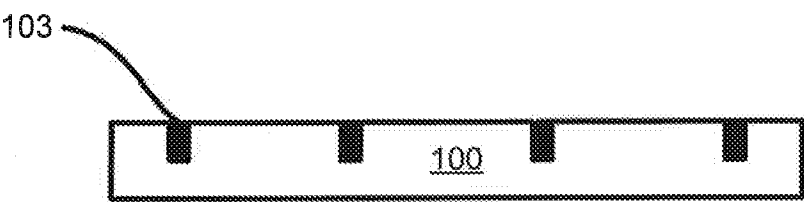


FIG. 2A

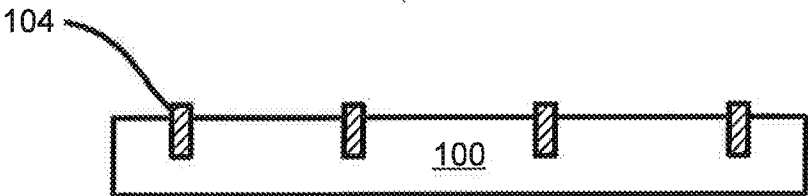


FIG. 2B

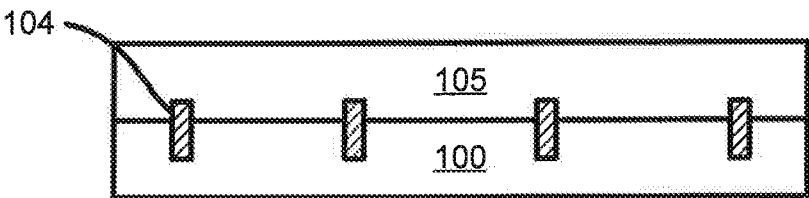


FIG. 2C

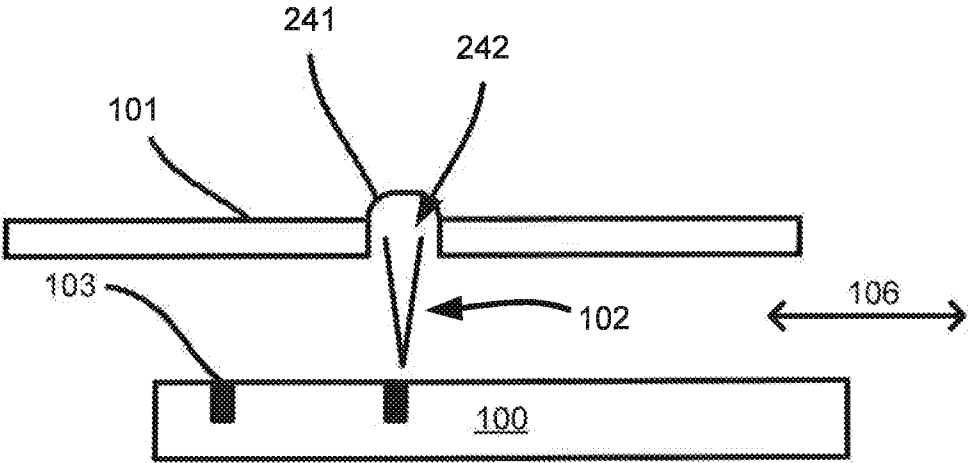


FIG. 3

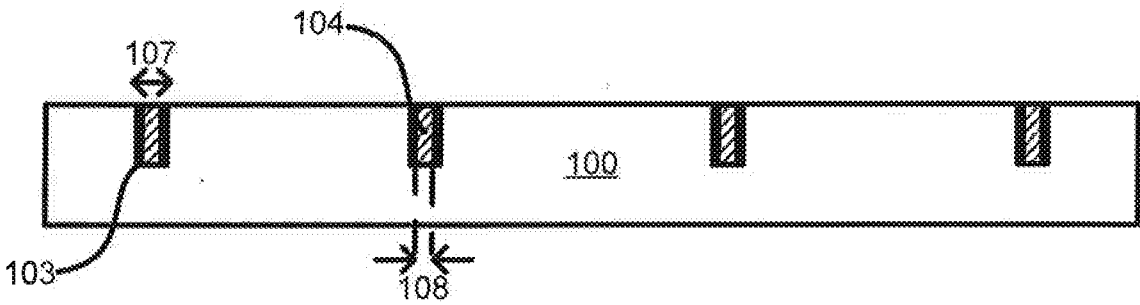


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/032727

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/02 H01L21/20 H01L21/265
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	BUMJOON KIM ET AL: "Epitaxial Lateral Overgrowth of GaN on Si (111) Substrates Using High-dose, N<+> Ion Implantation", CHEMICAL VAPOR DEPOSITION WILEY-VCH GERMANY, vol. 16, no. 1-3, 1 January 2010 (2010-01-01), pages 80-84, XP002678344, ISSN: 0948-1907, DOI: DOI:10.1002/CVDE.200906807 *Section "2. Results and Discussion", "3. Conclusions", "4. Experimental" * ----- -/--	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

2 July 2012

Date of mailing of the international search report

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Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2012/032727

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SASAKI T ET AL: "Surface smoothing effect in patterned SOI fabrication with SIMOX technology", 2003 IEEE INTERNATIONAL SOI CONFERENCE. PROCEEDINGS 29 SEPT.-2 OCT. 2003 NEWPORT BEACH, CA, USA, 1 January 2003 (2003-01-01), pages 48-49, XP002678345, 2003 IEEE International SOI Conference. Proceedings (Cat. No.03CH37443) IEEE Piscataway, NJ, USA ISBN: 0-7803-7815-6 *Section "Introduction", "Patterned SOI fabrication" ; figures 1, 2, 3 * -----	1-20
A	US 2010/323508 A1 (ADIBI BABAK [US] ET AL) 23 December 2010 (2010-12-23) the whole document -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2012/032727

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