



- (51) **International Patent Classification:**
H01L 23/48 (2006.01) H01L 21/60 (2006.01)
- (21) **International Application Number:**
PCT/US2015/062031
- (22) **International Filing Date:**
21 November 2015 (21.11.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant:** INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054-1549 (US).
- (72) **Inventors:** GRIGGIO, Flavio; 937 NW Glisan, Unit 735, Portland, Oregon 97209 (US). INDUKURI, Tejaswi K.; 10564 NW La Cassel Crest Lane, Portland, Oregon 97229 (US).
- (74) **Agent:** HARTMANN, Natalya; Patent Capital Group, c/o CPA Global, 900 Second Avenue South, Suite 600, Minneapolis, MN 55402 (US).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,

BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

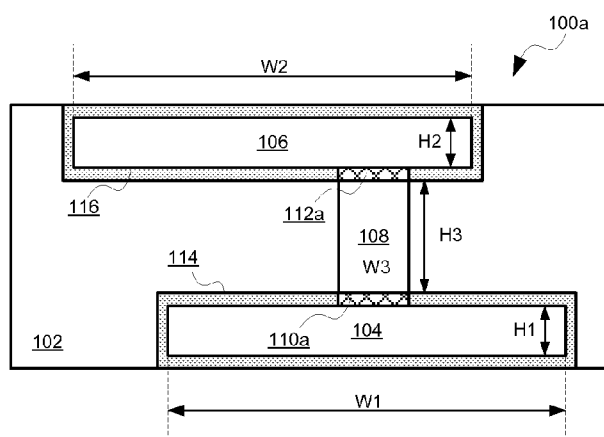
Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

- (54) **Title:** METALLIZATION STACKS WITH ENCLOSED VIAS

**FIG. 1a**

(57) **Abstract:** Described herein are systems and methods for providing a metallization stack to be used in an integrated circuit (IC) package. The metallization stack includes a via for providing electrical interconnection between a first interconnect and a second interconnect. The via is isolated from each of the first and the second interconnects by a respective barrier layer of an electrically conductive material. Enclosing the via from the interconnects using barrier layers reduces electromigration due to interdiffusion of the materials filling each of the interconnects and the material filling the via. Furthermore, such decoupling the via from the interconnects may allow the use of scaled thin conformal barriers for the interconnects and via, thus improving interconnect resistance, via resistance, and/or RC performance of the interconnect.

METALLIZATION STACKS WITH ENCLOSED VIAS

Technical Field

[0001] This disclosure relates generally to the field of integrated circuits, and more specifically, to metallization stacks with interconnects and vias.

Background

[0002] As integrated circuit features are scaled down and density increases, material properties such as resistivity, which influences observed resistance, exhibit relatively more pronounced effects. In addition, reliability of integrated circuits is affected by a number of stresses that increase as feature size drops and density increases. These stresses include electrical, thermal, environmental, and mechanical stresses. Electromigration is an important reliability concern in modern metallization stacks.

[0003] Electromigration is an example of phenomena that reduce semiconductor reliability, lead to interconnection failure, and become relatively more prominent as feature size decreases, particularly below 50 nanometers (nm), and as power density increases. Electromigration is understood as the transport of material due to movement of ions in a conductor. Electromigration can occur through surface, interface, grain-boundary and lattice diffusion, with strongest contributions from interface and surface diffusion. Electromigration may result in the formation of hillocks or voids within the vias and interconnects, and eventually lead to its failure.

[0004] Various approaches have been implemented in order to reduce electromigration and other stress induced failures. Current technologies attempt to fix dual damascene trench interconnect electromigration fails by thickening barrier, adding dopants such as aluminum (Al), manganese (Mn), or cobalt (Co), or by adding selective metal depositions such as electro-less Co doped with W, P, B to various structures in the dual damascene metallization stack. All these attempts increase interconnect and via resistance.

[0005] Therefore, as feature sizes continue to decrease, room remains for the improvement in the design of metallization stacks, in particular, for the improvement with respect to

reducing electromigration while maintaining adequate electrical conductivity and resistive-capacitance (RC) performance of metallization stacks.

Brief Description of the Drawings

[0006] FIGS. 1a-1e provide schematic illustrations of a metallization stack with an enclosed via, according to different embodiments of the present disclosure.

[0007] FIG. 2 provides a schematic illustration of possible adhesion layers for the first barrier layer enclosing the via, according to some embodiments of the present disclosure.

[0008] FIG. 3 provides a schematic illustration of possible adhesion layers for the second barrier layer enclosing the via, according to some embodiments of the present disclosure.

[0009] FIG. 4 provides a schematic illustration of a third barrier layer enclosing the via and possible adhesion layers for the third barrier layer, according to some embodiments of the present disclosure.

[0010] FIG. 5 provides a schematic illustration of an adhesion layer at an interface between the via and the interconnect support layer, according to some embodiments of the present disclosure.

[0011] FIG. 6 provides a flow chart of a method for forming a metallization stack with an enclosed via, according to some embodiments of the present disclosure.

[0012] FIG. 7 provides a flow chart of a method for forming a metallization stack with an enclosed via as shown in FIG. 1e, according to some embodiments of the present disclosure.

[0013] FIGs. 8a-8i provide schematic illustrations of a metallization stack as the method of FIG. 7 progresses, according to some embodiments of the present disclosure.

[0014] FIGs. 9a-9c provide schematic illustrations of forming a fully enclosed metal line, according to some embodiments of the present disclosure.

[0015] FIG. 10 is an interposer implementing one or more embodiments of the disclosure.

[0016] FIGs. 11a and 11b provide schematic illustrations 1100a and 1100b of cross-sections of a metallization stack, according to some embodiments of the present disclosure.

[0017] FIG. 12 is a computing device built in accordance with an embodiment of the disclosure.

Detailed Description

[0018] Described herein are systems and methods for providing a metallization stack to be used in an integrated circuit (IC) package.

[0019] In the present disclosure, differentiation is made between interconnects and vias of metallization stacks. As is known in the art, the term “interconnect” (also sometimes referred to as a trench, a metal interconnect, a line, a metal line, an interconnect trench, or a trench interconnect) is used to describe an electrically conductive line isolated by a support layer typically comprising an interlayer low-k dielectric that is provided within the plane of an IC chip. Such a support layer is typically referred to as an “interconnect support layer.” Such interconnect trenches are typically stacked into several levels. As is also known in the art, the term “via” is used to describe an electrically conductive element that electrically interconnects two or more metal trenches of different levels. To that end, vias are provided substantially perpendicularly to the plane of an IC chip. A via may interconnect two metal trenches in adjacent levels or two metal trenches in levels that are not adjacent to one another. In the following, the terms “interconnect” and “trench” are sometimes used interchangeably.

[0020] In one aspect of the present disclosure, a disclosed metallization stack includes a via for providing electrical interconnection between a first interconnect and a second interconnect. The via is isolated from each of the first and the second interconnects by a respective barrier layer of an electrically conductive material. Enclosing the via from the metal interconnects using barrier layers reduces electromigration due to interdiffusion of the materials filling each of the interconnects and the material filling the via. Furthermore, such decoupling the via from the interconnects may allow the use of scaled thin conformal barriers for the interconnects and via, thus improving trench resistance, via resistance, and/or RC performance of the metallization stack.

[0021] Barrier layers described herein are intended to prevent or at least reduce interdiffusion of materials on the opposite sides of each barrier layer. Such diffusion barriers are understood to typically occupy a small fraction of the cross-sectional area of the metallization stack.

[0022] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0023] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0024] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0025] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be

a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0026] In various embodiments, the metallization stacks as described herein may be used to connect various components associated with an integrated circuit. Components include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an integrated circuit may include those that are mounted on an integrated circuit or those connected to an integrated circuit. The integrated circuit may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a computer.

[0027] In the embodiments where at least some of the components associated with an integrated circuit are transistors, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

[0028] Each MOS transistor includes a gate stack formed of at least two layers, a gate interconnect support layer and a gate electrode layer. The gate interconnect support layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate interconnect support layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate interconnect support layer to improve its quality when a high-k material is used.

[0029] The gate electrode layer is formed on the gate interconnect support layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0030] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0031] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0032] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0033] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in

situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0034] One or more interlayer dielectrics (ILD) may be deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0035] Each of FIGS. 1a-1e illustrates a cross-sectional view of an embodiment of a metallization layer including a metallization stack 100, indicated as a metallization stack 100a for the embodiment shown in FIG. 1a, as a metallization stack 100b for the embodiment shown in FIG. 1b, as a metallization stack 100c for the embodiment shown in FIG. 1c, as a metallization stack 100d for the embodiment shown in FIG. 1d, and as a metallization stack 100e for the embodiment shown in FIG. 1e. For each metallization stack 100 shown in FIGS. 1a-1e, the stack includes a first interconnect or trench 104, a second interconnect or trench 106, and a via 108 supported by an interconnect support layer 102. In other words, the first trench 104, the second trench 106, and the via 108 are formed in the interconnect support layer 102. Furthermore, each metallization stack 100 includes a first barrier layer 110 provided at an interface between the first trench 104 and the via 108, and a second barrier layer 112 provided at an interface between the second trench 106 and the via 108. In this manner, the via 108 is enclosed by the first and second barrier layers 110, 112 with respect to the first and second interconnects, respectively.

[0036] In various embodiments, the interconnect support layer 102 may be an interlayer dielectric. Two or more layers of the interlayer dielectric may be stacked to form an integrated circuit. In some embodiments, the interconnect support layer may include one

or more sacrificial layers deposited over a dielectric substrate. The interconnect support layer typically includes one or more dielectric materials, which are understood to be materials that are insulators but are polarized upon application of an electric field. In embodiments, the dielectric may include a low-k dielectric material, that is, a material with a dielectric constant that is lower than 3.9, i.e., the dielectric constant of silicon dioxide, including all values and ranges from 1.1 to 3.8, such as 1.7, 1.9, 2.1, 2.8, 2.7, etc. Non-limiting examples from which the dielectric materials may be selected include fluorine-doped silicon dioxide, carbon doped oxide (i.e., carbon-doped silicon dioxide), organo silicate glass, silicon oxycarbide, hydrogenated silicon oxycarbide, porous silicon dioxide, and organic polymer dielectrics such as polyimide, polytetrafluoroethylene, polynorbornenes, benzocyclobutene, hydrogen silsesquioxane and methylsilsesquioxane. The interconnect support layer may have a thickness in the range of 10 nm to 1000 nm, including all values and ranges therein, such as e.g. 100 nm to 300 nm, 100 nm to 200 nm, etc.

[0037] As illustrated in the figures provided herein, for simplicity, various parts of the metallization stacks 100 are rectangular in cross-section. However, in various embodiments, other geometries may be assumed for the cross-section as well as for a top-view of different parts of the metallization stack (the top-view not shown in the figures) such as square, oblong, elliptical or variations thereof. In fact, in practice, fabricated metallization stacks rarely have perfectly rectangular cross-sections, as e.g. is illustrated in FIG. 11 with a schematic illustration of a transmission electron microscopy (TEM) image of a cross-section of an exemplary metallization stack.

[0038] As illustrated only in FIG. 1a but applicable to all metallization stacks described herein, in the cross-section shown in FIG. 1a, the first trench 104 may have a width W_1 and height H_1 , excluding any additional barrier layers. Similarly, the second trench 106 may have a width W_2 and height H_2 , excluding any additional barrier layers, also shown in FIG. 1a. The third dimension, typically referred to as a “length” of a trench is not shown in the FIGS provided herein because that dimension would have to be shown in a top-view of a metallization stack (i.e. the dimension of the interconnects in the direction perpendicular to the plane of the cross-sections shown in the FIGS). Typically, in embodiments, lengths of

the interconnects exhibit the largest dimensions of a metallization stack. In various embodiments, interconnects of a metallization stack may have a length L in the range of a few nm to several microns, including all values and ranges therein, a width W in the range of 0.020 micron to 0.100 micron including all values and ranges therein, and a height H in a range that provides aspect ratios (H/W) of 0.5 to 2.0 including all values and ranges therein.

[0039] As illustrated only in FIG. 1a but applicable to all metallization stacks described herein, in the cross-section shown in FIG. 1a, the via 108 may have a width W_3 and height H_3 , excluding any additional barrier layers. The length L_3 of the via 108 is not shown in FIG. 1a because that dimension would have to be shown in a top-view of the metallization stack 100. In various embodiments, a via of a metallization stack may have a length L in the range of a 1/100 of a micron to 5000 microns, including all values and ranges therein, a width W in the range of 1/100 micron to 5000 microns including all values and ranges therein, and a height H in a range that provides aspect ratios (H/W) of 0.25 to 100.0 including all values and ranges therein.

[0040] Various parts of the metallization stacks 100 may be filled with materials having a wide range of resistivity ρ , such as in the range of 0.1 $\mu\Omega\cdot\text{cm}$ to 400 $\mu\Omega\cdot\text{cm}$. The resistivity of the film could be higher as long as the thickness is scaled down to meet the resistivity requirements of the circuit.

[0041] In various embodiments, the first trench 104, the second trench 106, and the via 108 may be filled with same or different materials. For example, the first trench 104 and/or the second trench 106 of the metallization stacks 100 may include, consist of, or consist essentially of copper (Cu). The via 108 may include, consist of, or consist essentially of one or more bulk materials comprising aluminum (Al), copper (Cu), tungsten (W), cobalt (Co), ruthenium (Ru), nickel (Ni), iron (Fe), and molybdenum (Mo) and/or one or more alloys comprising aluminum (Al), copper (Cu), tungsten (W), cobalt (Co), ruthenium (Ru), manganese (Mn), magnesium (Mg), boron (B), phosphorus (P), nitrogen (N), carbon (C), and sulfur (S).

[0042] Embodiments illustrated in FIGS. 1a-1d differ in how the first barrier layer 110 and the second barrier layer 112 are provided, which would depend on a particular method for

forming a metallization stack being used. Therefore, the first and second barrier layers are shown in FIGS. 1a-1d with different letters following their numerals 110 and 112, i.e. as first barrier layer 110a-110d and second barrier layer 112a-112d in FIGS. 1a-1d. Embodiment illustrated in FIG. 1e also differs in that a barrier layer on the side walls of the via 108 is provided, thus completely enclosing the via.

[0043] As illustrated in the exemplary embodiment of FIG. 1a with the first barrier layer 110a, that barrier layer may be part of a barrier layer 114 enclosing at least the top, but possibly all sides, of the first trench. When used on all sides of the trench, as shown in FIG. 1a, the barrier layer 114 may be used to provide a diffusion barrier for preventing diffusion of the material filling the first trench 104 out of the trench. Preferably, the first barrier layer 110a is formed of the same material and substantially at the same time, or as a part of, forming the barrier layer 114. However, in other embodiments, the first barrier layer 110a may be formed from a different material and/or at a different time as the barrier layer 114.

[0044] As illustrated in the exemplary embodiment of FIG. 1a with the second barrier layer 112a, that barrier layer may be part of a barrier layer 116 enclosing at least the bottom, but possibly all sides, of the second trench. When used on all sides of the trench, as shown in FIG. 1a, the barrier layer 116 may be used to provide a diffusion barrier for preventing diffusion of the material filling the second trench 106 out of the trench. Preferably, the second barrier layer 112a is formed of the same material and substantially at the same time, or as a part of, forming the barrier layer 116. However, in other embodiments, the second barrier layer 112a may be formed from a different material and/or at a different time as the barrier layer 116.

[0045] In various embodiments, each of the first and second barrier layers 110 and 112 may be formed from the same or different materials. For example, the first barrier layer 110 and/or the second barrier 112 layer may include, consist of, or consist essentially of one or more tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), ruthenium (Ru), and cobalt (Co). Because the first and second barrier layers are provided in the area of a metallization stack that has to provide electrical conductivity, choice of materials used for these barrier layers should reflect that. To that end, materials selected for the first and/or second barrier layers 110, 112 include materials having a wide range of resistivities, such as

in the range of 0.1 $\mu\Omega\cdot\text{cm}$ to 400 $\mu\Omega\cdot\text{cm}$, including all values and ranges therein. More specifically than resistivity, in some implementations, choice of materials for the first and/or second barrier layers 110, 112 may be made so that the resistance of the electrical connection satisfies appropriate requirements of the particular electrical circuit being implemented. Therefore, in some embodiments, high resistivity material(s) may still be used at an appropriately low thickness such that the net resistance satisfies circuit requirements.

[0046] In various embodiments, each of the first and second barrier layers 110 and 112 may have the same or different thicknesses as measured in the vertical dimension for the cross-sections shown in the FIGS, i.e. in the dimension in which the height H is indicated for the interconnects and the via in FIG. 1a. In some embodiments, a thickness of each of the first and second barrier layers 110, 112 may be between 0.2 nm and 20 microns, including all values and ranges therein.

[0047] As illustrated in the exemplary embodiment of FIG. 1b with the first barrier layer 110b, in contrast to the barrier layer 110a, the first barrier layer 110b may be provided on the bottom of the via 108. The first barrier layer 110b may be provided e.g. by creating an opening for the via 108 and the second trench 106 after the first trench 104 has been formed and filled with a suitable material for the first trench 104, and then depositing the first barrier layer into the opening, after which the via 108 is filled with a suitable via material.

[0048] As illustrated in the exemplary embodiment of FIG. 1b with the second barrier layer 112b, in contrast to the barrier layer 112a, the second barrier layer 112b may be provided on the top surface of the material filling the via 108. The second barrier layer 112b may be provided following fill of the via 108 with a suitable via material by recessing the upper surface of the via below the surface of the second trench 106 and then filling the recess with a suitable barrier layer material for forming the second barrier layer 112b.

[0049] In various embodiments not shown in the FIGs, the first barrier layer 110b may be provided in addition to the barrier layer surrounding the first trench 104 at least on some sides, e.g. in addition to the barrier layer 114 as shown in FIG. 1a, and/or the second barrier

layer 112b may be provided in addition to the barrier layer surrounding the second trench 106 at least on some sides, e.g. in addition to the barrier layer 116 as shown in FIG. 1a.

[0050] The exemplary embodiment of FIG. 1c illustrates using the first barrier layer 110a as illustrated in FIG. 1a and using the second barrier layer 112b as illustrated in FIG. 1b. All of the descriptions provided above for the first barrier layer 110a and the second barrier layer 112b are applicable to the embodiment of FIG. 1c and, therefore, in the interest of brevity, are not repeated.

[0051] The exemplary embodiment of FIG. 1d illustrates using the first barrier layer 110b as illustrated in FIG. 1b and using the second barrier layer 112a as illustrated in FIG. 1a. All of the descriptions provided above for the first barrier layer 110b and the second barrier layer 112a are applicable to the embodiment of FIG. 1d and, therefore, in the interest of brevity, are not repeated.

[0052] The exemplary embodiment of FIG. 1e illustrates using the first barrier layer 110a and the second barrier layer 112a as illustrated in FIG. 1a. All of the descriptions provided above for the first barrier layer 110a and the second barrier layer 112a are applicable to the embodiment of FIG. 1e and, therefore, in the interest of brevity, are not repeated. The metallization stack 100e of FIG. 1e further illustrates using a third barrier layer 118 on the side walls of the via 108, thus completely enclosing the via on all sides. Considerations in using a third barrier layer are described with reference to FIG. 4.

[0053] In various further embodiments of the exemplary embodiment shown in FIG. 1e, top part 120 of the barrier 114 enclosing the first trench 104 and top part 122 of the barrier 116 enclosing the second trench 106 may or may not be of the same materials as the barriers 114 and 116, respectively. Thus, in various embodiments, any combination of barrier layers 114, 120, 116, and 122 may be made of the same or different materials.

[0054] Each of the first barrier layer 110 and the second barrier layer 112 may be provided with one or more adhesion layers.

[0055] FIG. 2 provides a schematic illustration of possible adhesion layers for the first barrier layer 110 enclosing the via 108 from the first trench 104, according to some

embodiments of the present disclosure. As shown in FIG. 2, the first barrier layer 110 may be surrounded by a first barrier-trench adhesion layer 202 disposed between the first barrier layer 110 and the first trench 104 and/or a first barrier-via adhesion layer 204 disposed between the first barrier layer 110 and the via 108.

[0056] The first barrier-trench adhesion layer 202 is chosen from the materials that promote adhesion between the material of the first barrier layer 110 and the material filling the first trench 104. Examples of such materials include but are not limited to, tantalum, titanium, titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, and the like. In case the first barrier layer 110 is provided on top of another barrier layer surrounding the first trench, such as e.g. the barrier layer 114 shown in FIG. 1a, then the first barrier-trench adhesion layer 202 is chosen from the materials that promote adhesion between the material of the first barrier layer 110 and the material of the trench barrier layer 114.

[0057] The first barrier-via adhesion layer 204 is chosen from the materials that promote adhesion between the material of the first barrier layer 110 and the material filling the via 108. Examples of such materials include but are not limited to, tantalum, titanium, titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, and the like.

[0058] Because the first barrier-trench adhesion layer 202 and the first barrier-via adhesion layer 204 are provided in the area of a metallization stack that has to provide electrical conductivity, choice of materials used for these adhesion layers should reflect that, i.e. both of these adhesion layers should be electrically conductive.

[0059] In various embodiments, the adhesion layers illustrated in FIG. 2 may be used in combination with any of the embodiments shown in FIGs. 1a-1d.

[0060] FIG. 3 provides a schematic illustration of possible adhesion layers for the second barrier layer 112 enclosing the via 108 from the second trench 106, according to some embodiments of the present disclosure. As shown in FIG. 3, the second barrier layer 112 may be surrounded by a second barrier-trench adhesion layer 302 disposed between the second barrier layer 112 and the second trench 106 and/or a second barrier-via adhesion layer 304 disposed between the second barrier layer 112 and the via 108.

[0061] The second barrier-trench adhesion layer 302 may be chosen from the materials that promote adhesion between the material of the second barrier layer 112 and the material filling the second trench 106. Examples of such materials include but are not limited to, tantalum, titanium, titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, and the like. In case another barrier layer surrounding the second trench, such as e.g. the barrier layer 116 shown in FIG. 1a is provided on top of the second barrier layer 112, then the second barrier-trench adhesion layer 302 is chosen from the materials that promote adhesion between the material of the second barrier layer 112 and the material of the second trench barrier layer 116.

[0062] The second barrier-via adhesion layer 304 may be chosen from the materials that promote adhesion between the material of the second barrier layer 112 and the material filling the via 108. Examples of such materials include but are not limited to, tantalum, titanium, titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, and the like.

[0063] Because the second barrier-trench adhesion layer 302 and the second barrier-via adhesion layer 304 are provided in the area of a metallization stack that has to provide electrical conductivity, choice of materials used for these adhesion layers should reflect that, i.e. both of these adhesion layers should be electrically conductive.

[0064] In various embodiments, the adhesion layers illustrated in FIG. 3 may be used in combination with any of the embodiments shown in FIGs. 1a-1d and 2.

[0065] FIG. 4 provides a schematic illustration of a third barrier layer 402 enclosing the via 108 and possible adhesion layers 404 and 406 for the third barrier layer, according to some embodiments of the present disclosure. The third barrier layer 402 may, optionally, be provided at an interface between the via 108 and the interconnect support layer 102 in order to prevent interdiffusion of material filling the via 108 with the material(s) of the interconnect support layer 102. When such third barrier layer is used together with the first barrier layer 110 and the second barrier layer 112, material filling the via 108 is fully enclosed within the via 108 and the via may be referred to as a “fully clad via.” In various embodiments, the third barrier layer 402 may be electrically conductive, semiconducting, or

dielectric. Examples of materials that could be used for the third barrier layer include one or more of tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), ruthenium (Ru), and cobalt (Co). In addition, since a conductive liner is not used, additional materials may serve as a replacement such as, but not limited to, silicon nitride, silicon carbide, silicon dioxide, aluminum oxide and the like.

[0066] Similar to the first barrier layer 110 and the second barrier layer 112, the third barrier layer 402 may be provided with one or more adhesion layers illustrated in FIG. 4 as a third barrier-dielectric adhesion layer 404 and a third barrier-via adhesion layer 406.

[0067] The third barrier-dielectric adhesion layer 404 may be disposed between the third barrier layer 402 and the interconnect support layer 102. The third barrier-dielectric adhesion layer 404 may be chosen from the materials that promote adhesion between the material of the third barrier layer 402 and the material(s) of the interconnect support layer 102. Examples of such materials include but are not limited to, tantalum, titanium, titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, and the like.

[0068] The third barrier-via adhesion layer 406 may be disposed between the third barrier layer 402 and an electrically conductive material filling the via 108. The third barrier-via adhesion layer 406 may be chosen from the materials that promote adhesion between the material of the third barrier layer 402 and the material filling the via 108. Examples of such materials include but are not limited to, tantalum, titanium, titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, and the like.

[0069] In various embodiments, each of the third barrier-dielectric adhesion layer 404 and the third barrier-via adhesion layer 406 may be electrically conductive, semiconducting, or dielectric.

[0070] In various embodiments, the third barrier layer and/or the adhesion layers illustrated in FIG. 4 may be used in combination with any of the embodiments shown in FIGs. 1a-1d, 2 and 3.

[0071] FIG. 5 provides a schematic illustration of a via-dielectric adhesion layer 502 at an interface between the via 108 and the interconnect support layer 102, according to some

embodiments of the present disclosure. Such an adhesion layer may be provided in order to promote adhesion between the material filling the via 108 and the interconnect support layer 102 in case no third barrier layer as shown in FIG. 4 is involved. Examples of materials that could be used for the adhesion layer 502 include but are not limited to, metals, such as cobalt, ruthenium, platinum, palladium, rhenium, iridium, molybdenum, nickel, silicon, tungsten, silver, and alloys or components thereof, as well as their borides, carbides, silicides, and nitrides; as well as silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), silicon carbide (SiC), tantalum, tantalum nitride, titanium, titanium nitride. In various embodiments, the via-dielectric adhesion layer 502 may be electrically conductive, semiconducting, or dielectric.

[0072] In various embodiments, the adhesion layer illustrated in FIG. 5 may be used in combination with any of the embodiments shown in FIGs. 1a-1d, 2 and 3.

[0073] In various embodiments, the adhesion layers 202, 204, 302, 304, 404, 406, and 502 may each have a thickness in the range of 1 nm to 300 nm, including all values and ranges therein.

[0074] One embodiment of a method of forming a metallization stack in a metallization layer with an enclosed via is illustrated in FIG. 6 as a method 600. The method 600 may include providing the first trench 104 (box 602), providing the second trench (box 604), providing the via 108 enabling electrical interconnection between the first trench and the second trench (box 606), providing the first barrier layer 110 between the via and the first trench (box 608), and providing the second barrier layer 112 between the via and the second trench (box 610). Optionally and not shown in FIG. 6, the method 600 may also include providing the third barrier layer and/or one or more of the adhesion layers 202, 204, 302, 304, 404, 406, and 502 as described herein.

[0075] A person of ordinary skill in the art would recognize that the actions described with reference to FIG. 6 are not necessarily performed in order shown in or described with reference to FIG. 6. A person of ordinary skill in the art would further recognize various methods and means for achieving each one of these actions, all of which methods and means, therefore, being within the scope of the present disclosure. In addition, description

below provides illustration for some of the approaches that could be used to accomplish the actions shown in FIG. 6.

[0076] One embodiment of a method of forming a metallization stack in a metallization layer with an enclosed via as shown in FIG. 1e is illustrated in FIG. 7 as a method 700. FIGs. 8a through 8i illustrate the configuration of the metallization layer as the method of forming the interconnect with an enclosed via as shown in FIG. 1e progresses. Some of the elements of the metallization stack 100 are indicated in some but not all of the FIGs. 8a-8i in order to not clutter the drawings. Since FIGs. 8a-8i illustrate results of sequential actions performed on the same structure, a lot of the elements shown in these FIGs are common between the FIGs, thus eliminating the need to indicate each element on each FIG. The same applies to the illustration of FIGs. 9a-9c.

[0077] In the embodiment shown in FIG. 7, the method 700 may begin with forming a fully enclosed (clad) first trench 104 (box 702 in FIG. 7). One way of forming a fully enclosed trench is illustrated in FIGs. 9a-c and described in greater detail below.

[0078] Turning back to the method 700, once a fully enclosed first trench has been formed, openings for the via and for the next layer, second, trench may be formed (box 704 in FIG. 7). To that end, any kind of patterning techniques for patterning the interconnect support layer may be used. In an embodiment, patterning includes depositing a photoresist over the interconnect support layer. The photoresist may be a positive or negative resist and may include for example, poly(methyl methacrylate), poly(methyl glutarimide), DNQ/novolac, or SU-8 (an epoxy based negative resist). The photoresist may be deposited by a casting process such as, for example, spin-coating. Spin coating may be performed at 1 to 10,000 rpm, including all values and ranges therein, for a time period in the range of 1 second to 10 seconds, including all values and ranges therein. The photoresist may then be patterned by optically projecting an image of a desired pattern onto the photoresist using photolithography, such as optical photolithography, immersion photolithography, deep UV lithography, extreme UV lithography, or other techniques, wherein the wavelength of projected light may be up to 436 nm, including all values and ranges from 157 nm to 436 nm, such as 157 nm, 193 nm, 248 nm, etc. A developer, such as tetramethylammonium hydroxide TMAH (with or without surfactant) at a concentration of in the range of 0.1 N to

0.3 N, may be applied to the photoresist, such as by spin-coating, and portions of the photoresist are removed to expose regions of the underlying interconnect support layer correlating to the desired pattern.

[0079] In some embodiments, baking of the interconnect support layer may occur before or after any of the above actions. For example, the interconnect support layer may be prebaked to remove surface water. In some embodiments, prebaking may be performed at a temperature in the range of 200° C to 400° C, including all values and ranges therein, for a time of 30 to 60 minutes, including all values and ranges therein. After application of the photoresist, a post application bake may occur, wherein at least a portion of the solvents in the photoresist are driven off. A post application bake is, for example, performed at temperatures in the range of 70° C to 140° C, including all values and ranges therein, for a time period in the range of 60 seconds to 240 seconds, including all values and ranges therein. After patterning, the resist may be hard baked at a temperature in the range of 100° C to 300° C, including all values and ranges therein, for a time period of 1 minute to 10 minutes, including all values and ranges therein.

[0080] The exposed portions of the interconnect support layer are then chemically etched, wherein the exposed portions of the surface are removed until a desired depth is achieved, forming openings in the interconnect support layer. The remaining photoresist is optionally removed via a process such as ashing, wherein the photoresist is exposed to oxygen or fluorine, which combines with the photoresist to form ash. FIG. 8a illustrates an embodiment of a patterned interconnect support layer 102 including an opening 802 for the via and an opening 804 for the second trench. The interconnect support layer at least partially surrounds the openings, isolating them from other openings that may be formed (not shown in FIG. 8a) both physically and electrically.

[0081] Referring again to FIG. 7, after patterning the interconnect support layer, the first diffusion barrier is deposited into the openings (box 706 in FIG. 7).

[0082] In some embodiments, deposition of the first diffusion barrier may be performed using a conformal coating process, wherein the diffusion barrier is deposited on any exposed surface of the interconnect support layer, including on the sidewalls and bottom of

any opening formed in the interconnect support layer. A conformal coating may, therefore, be understood as a coating that is applied to exposed surfaces of the interconnect support layer, and not, for example, just to horizontal surfaces. In some embodiments, the coating may exhibit a variation in thickness of less than 35%, including all values and ranges from 1% to 35%, such as 10% or less, 15% or less, 20% or less, 25% or less, etc. The conformal coating process may be selected from processes such as chemical vapor deposition or atomic layer deposition. Other processes that may be used include physical vapor deposition such as, magnetron sputtering, evaporative deposition or e-beam deposition.

[0083] In chemical vapor deposition, for example, one or more reactive gases are provided in a chamber including the interconnect support layer at a flow rate of 5 sccm to 500 sccm, including all values and ranges therein. In some examples, the reactive gas may be selected from one or more of the following: pentakis(dimethylamino)tantalum, tris(diethylamido)(tert-butylimido)tantalum(V), tris(ethylmethyldamido)(tert-butylimido)tantalum(V), or titanium tetrachloride and ammonia provided at a 1:1 stoichiometric ratio. The reactive gas may be provided with a carrier gas, such as an inert gas, which may include, for example, argon.

[0084] In some embodiments, the chamber may be maintained at a pressure in the range of 1 mTorr to 100 mTorr, including all values and ranges therein, and a temperature in the range of 100° C to 500° C, including all values and ranges therein. In some embodiments, the process may be plasma assisted where electrodes are provided within the process chamber and are used to ionize the gases. Alternatively, plasma may be formed outside of the chamber and then supplied into the chamber. In the chamber, a layer of the metal is deposited on the surface of the interconnect support layer due to reaction of the gas.

[0085] In physical vapor deposition a workpiece (the dielectric) is placed in a process chamber. A reactive gas, such nitrogen, is supplied to the process chamber at a flow rate in the range of 10 sccm to 100 sccm, including all values and ranges therein such as 40 sccm to 50 sccm or 45 sccm. An inert gas, such as argon, may optionally be supplied into the process chamber as well. Prior to supplying the reactive gas, the base pressure of the process chamber may be in the range of 10^{-8} torr and held at a pressure in the range of 10^{-7} to 10^{-1} torr during sputtering, such as in the range of 1 millitorr to 10 millitorr, or 2.5 millitorr. The

process chamber may be maintained at a temperature in the range of 10° C to 100° C, including all values and ranges therein, such as in the range of 10° C to 20° C or 17° C.

[0086] A metal target may be positioned in the process chamber and formed of a metal such as titanium or tantalum. The metal target may be biased by a DC sources rated in the range of –50 V to –1000 V, including all values and ranges therein. The workpiece, or worktable, may also be biased by an AC source rated in the range of –50 V to –100 V including all values and ranges therein, such as –70 to –80 V.

[0087] During deposition, a plasma forms and is localized around the target due to magnets positioned proximal to or behind the target. The plasma bombards the target sputtering away the metal atoms as a vapor, which is then deposited on the workpiece. The process may continue for a time period in the range of 1 second to 100 seconds.

[0088] FIG. 8b illustrates an embodiment showing a conformal coating 806 of the first diffusion barrier material over the surfaces of the openings for the via and the second trench in the interconnect support layer 102, including the diffusion barrier material being deposited on the walls and bottom of the openings that were formed in box 704.

[0089] After depositing the first diffusion barrier layer, optionally, an adhesion layer may be deposited in order to provide an adhesion layer as described with reference to FIGs. 2-5. In some embodiments, an adhesion layer may deposited using any of the above conformal coating processes. Here, the adhesion layer may be deposited on any exposed surface of the first diffusion barrier layer, including on the sidewalls and bottom of the openings. In examples, the reactive gas may be selected from tantalum(V)chloride, i.e., bis(tert-butylcyclopentadienyl)titanium(IV) dichloride, which is delivered with hydrogen at a 1:1 stoichiometric ratio. Again, the reactive gas may be delivered with an inert gas, such as argon. Physical vapor deposition of the adhesion layer may proceed as described above with respect to the barrier layer, with a few exceptions. For example, during deposition of the diffusion barrier, a reactive gas, such as nitrogen gas, is not fed into the process chamber. Otherwise, the processes remain similar. A similar process may be used to deposit an adhesion layer prior to depositing the barrier layer, e.g. prior to depositing the barrier layer 806.

[0090] Referring again to FIG. 7, the via material may then be deposited into the openings lined with the first diffusion barrier layer (box 708 in FIG. 7). To that end, a vapor deposition method may be used, such as e.g. chemical vapor deposition or physical vapor deposition. The via material may be deposited over various surfaces of the dielectric.

[0091] Physical vapor deposition processes for depositing the via materials again include, for example, magnetron sputtering, evaporative deposition or e-beam deposition. An example of physical vapor deposition includes supplying an inert gas, such as argon, at a flow rate in the range of 5 sccm to 100 sccm, including all values and ranges therein, into a process chamber, which is held at a pressure in the range of 1×10^{-1} torr to 10^{-7} torr, including all values and ranges therein. The process chamber may include a workpiece, i.e., the dielectric, and a metal source, called a target, formed of copper or aluminum. The metal source may be biased by a DC source rated in the range of 0.1 kW to 50 kW, including all values and ranges therein. The workpiece, or worktable upon which the workpiece is positioned, may also be biased by an AC source rated in the range of 0.1 kW to 1.5 kW, including all values and ranges therein. A plasma forms and is localized around the target due to magnets positioned proximal to or behind the target. The plasma bombards the target sputtering away the metal atoms as a vapor, which is then deposited on the workpiece. The process may continue for a time period in the range of 1 second to 100 seconds to allow growth of a layer of the via interconnect material.

[0092] In alternative embodiments, chemical vapor deposition may be performed to fill the via by the processes described above. The reactive gas may be selected from, for example, Cu(II)bis-hexafluoroacetylacetonate, 1,5-cyclooctadiene-Cu(I)-hexafluoroacetylacetonate.

[0093] In some embodiments, first, a seed layer of the interconnect material (such as copper), in the range of 400 Angstroms to 600 Angstroms, such as 500 Angstroms, is formed by the physical vapor deposition process described above, followed by the electroplating of copper, during which the interconnect support layer is placed to a solution of copper sulfate and sulfuric acid. A current density in the range of 25 mA/cm² to 75 mA/cm², such as 50 mA/cm², may be applied for a time period of 30 seconds to 120 seconds, such as 60 seconds.

[0094] FIG. 8b illustrates via material 808 filling the openings of FIG. 8a lined with the first diffusion barrier 806.

[0095] Referring again to FIG. 7, planarization is then performed (box 710 of FIG. 7) to expose the surfaces 810 of the interconnect support layer. Planarization may be performed using either wet or dry planarization processes. In one embodiment, planarization is performed using chemical mechanical planarization (CMP), which may be understood as a process that utilizes a polishing surface, an abrasive and a slurry to remove the overburden and planarize the surface of the interconnect support layer 102 and the metallization stack. FIG. 8c illustrated the planarized surface 810 of the interconnect support layer 102 and the planarized surface 812 of the via material 808 filling the second trench.

[0096] After the planarization, selective metal recess is carried out (box 712 of FIG. 7). This may be carried out e.g. by wet etching the material, composed of the metal fill and the barrier-adhesion layer in the opening 804 using a single solution of mineral or an organic acid and a peroxide, or is performed using two solutions in a two-step process. FIG. 8d illustrated the via material being eliminated from the opening 804 for the second trench as a result of performing selective metal recess of box 712.

[0097] After the via material has been eliminated from the opening 804 for the second trench, the second diffusion barrier is deposited into the opening 804 (box 714 in FIG. 7). Any of the processes described above for depositing the first barrier layer (box 706) could be used for depositing the second barrier layer as well.

[0098] After depositing the second diffusion barrier layer, optionally, an adhesion layer may be deposited in order to provide an adhesion layer as described with reference to FIGs. 2-5. In some embodiments, an adhesion layer may deposited using any of the above conformal coating processes. Here, the adhesion layer may be deposited on any exposed surface of the second diffusion barrier layer, including on the sidewalls and bottom of the openings.

[0099] Next, the second interconnect material may be deposited (box 716 in FIG. 7). In some embodiments, second interconnect material may be deposited in a manner similar to that described above for depositing a via material with reference to box 708. FIG. 8e illustrates material 814 for the second trench filling the opening 804 and covering the

surface 810. FIG. 8e also illustrates an embodiment showing a conformal coating 815 of the second diffusion barrier material over the surfaces of the opening 804 for the second trench in the interconnect support layer 102 (deposited in box 714).

[00100] Referring again to FIG. 7, planarization is then performed (box 718 of FIG. 7) to expose the surfaces 810 of the interconnect support layer, which may be done in a manner described above with reference to box 710. FIG. 8f illustrated the planarized surface 810 of the interconnect support layer 102 and the planarized surface 816 of the material 814 filling the second trench.

[00101] Next, partial selective metal recess is carried out (box 720 of FIG. 7). This may be carried out in a manner similar to that described with reference to box 712, but providing a smaller recess. For example, the upper surface of the material 814 filling the second trench may be recessed from the upper surface 810 of the interconnect support layer 102 at a depth in the range of 1 nm to 20 nm, including all values and ranges therein, such as 1 nm to 5 nm. FIG. 8g illustrated a recess 818 formed as a result.

[00102] Referring again to FIG. 7, after the partial selective metal recess, next diffusion barrier may be deposited (box 722 of FIG. 7), shown with material 820 in FIG. 8h. This may be accomplished in a manner similar to that described above with reference to depositing the first diffusion barrier in box 706.

[00103] Next, planarization is performed again (box 724 of FIG. 7) to expose the surfaces 810 of the interconnect support layer, which may be done in a manner described above with reference to box 710. FIG. 8i illustrated the planarized surface 810 of the interconnect support layer 102 and the planarized surface 822 of the diffusion barrier material 820 enclosing the top surface of the second trench 106.

[00104] Referring back to FIGs. 9a-9c, in order to form a fully enclosed first trench some of the method described above may be used. First, an opening for the first trench may be formed, which could be done in a manner similar to that described above with reference to box 704. Then, the opening in the interconnect support layer may be lined with a diffusion barrier layer, which could be done in a manner similar to that described above with reference to box 706. Next, the opening lines with the diffusion barrier is filled

with an electrically conductive material for the trench, e.g. Cu, which could be done in a manner similar to that described above with reference to box 708.

[00105] The material filling the trench may be recessed within the trench, as shown in FIG. 9a. This may be done in a manner similar to that described above with reference to box 720. The upper surface of the material filling the first trench may be recessed from the upper surfaces of the interconnect support layer 102 at a depth in the range of 1 nm to 20 nm, including all values and ranges therein, such as 1 nm to 5 nm.

[00106] Next, a top barrier layer is deposited, which could e.g. comprise TNT or TaN, as shown in FIG. 9b. This may be done in a manner similar to that described above with reference to box 722. Then the top surface is then polished to provide a flat surface as shown in FIG. 9c. This may be done in a manner similar to that described above with reference to box 722.

[00107] Enclosing the vias according to the embodiments described herein may allow achieving one or more of the following advantages: improved trench and via resistance, elimination of defects due to spurious nucleation, use of scaled thin conformal barriers for trench and via, thus improving trench and via resistance and RC performance, lesser interdiffusion between the materials filling the via and the interconnects. In addition, enclosure of via by barriers above and below is likely to improve electromigration reliability by short line effect. The addition of diffusion barriers above first and second interconnects improves electromigration of the interconnects.

[00108] While embodiments described above are described with reference to a via provided between the first and second interconnects, where the first diffusion barrier is provided between a bottom of the via and the first trench and the second diffusion barrier is provided between a top of the via and the second trench, descriptions provided herein are equally applicable to a via provided between two other vias (as e.g. illustrated in FIG. 10 showing three vias 1010 stacked on top of one another), or a via provided between a trench and a via (as e.g. illustrated in FIG. 10 showing two vias 1010 stacked on top of one another and further having a trench 1008 on top and/or on the bottom of the two-via stack). In such configurations of stacked vias, one or more vias may be isolated from each of the

neighbouring other components, be it a trench or another via, by a respective barrier layer of an electrically conductive material, in a manner analogous to that described above for via and two interconnects. Enclosing the via from either adjacent vias or the interconnects using barrier layers reduces electromigration due to interdiffusion of the materials filling each of the interconnect elements.

[00109] In accordance with embodiments of the disclosure, metallization stacks disclosed herein and processes for forming such metallization stacks may be used in the fabrication of an interposer, such as e.g. the one shown in FIG. 10.

[00110] FIG. 10 illustrates an interposer 1000 that includes one or more embodiments of the disclosure. The interposer 1000 is an intervening substrate used to bridge a first substrate 1002 to a second substrate 1004. The first substrate 1002 may be, for instance, an integrated circuit die. The second substrate 1004 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1000 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1000 may couple an integrated circuit die to a ball grid array (BGA) 1006 that can subsequently be coupled to the second substrate 1004. In some embodiments, the first and second substrates 1002/1004 may be attached to opposing sides of the interposer 1000. In other embodiments, the first and second substrates 1002/1004 may be attached to the same side of the interposer 1000. In further embodiments, three or more substrates may be interconnected by way of the interposer 1000.

[00111] The interposer 1000 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[00112] The interposer may include metal interconnect trenches 1008 and vias 1010, including but not limited to through-silicon vias (TSVs) 1012. The vias 1010 may be enclosed by first and second diffusion barrier layers as described herein. The interposer 1000 may

further include embedded devices 1014, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1000.

[00113] FIGs. 11a and 11b provide schematic illustrations 1100a and 1100b of cross-sections of a metallization stack, according to some embodiments of the present disclosure. As can be seen, FIGs. 11a and 11b are drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines. As shown, FIG. 11a represents a cross-section view parallel to the bottom metallization layer 1102. The schematic is an example of the 100e type metallization stack with a via 1104 and a second interconnect 1106. The interconnect 1102 and 1106 are isolated by an interconnect support layer 1112 and possible processing defects are illustrated, such as via necking 1110, via bottom metal pull-back 1114, seam voids 1116, via bulging 1118 and side wall voids 1120. In Fig. 11a and 11b, 1108, 1122 and 1124 correspond, respectively, to 114, 120 and 116 of Fig. 1e.

[00114] Figure 12 illustrates a computing device 1200 in accordance with one embodiment of the disclosure. The computing device 1200 may include a number of components. In one embodiment, these components may be attached to one or more motherboards. In an alternate embodiment, some or all of these components may be fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 1200 include, but are not limited to, an integrated circuit die 1202 and at least one communications logic unit 1208. In some implementations the communications logic unit 1208 may be fabricated within the integrated circuit die 1202 while in other implementations the communications logic unit 1208 may be fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that may be shared with or electronically coupled to the integrated circuit die 1202. The integrated circuit die 1202 may include a CPU 1204 as well as on-die memory 1206, often used as cache

memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[00115] Computing device 1200 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1210 (e.g., DRAM), non-volatile memory 1212 (e.g., ROM or flash memory), a graphics processing unit 1214 (GPU), a digital signal processor 1216, a crypto processor 1242 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 1220, an antenna 1222, a display or a touchscreen display 1224, a touchscreen controller 1226, a battery 1228 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 1228, a compass 1230, a motion coprocessor or sensors 1232 (that may include an accelerometer, a gyroscope, and a compass), a speaker 1234, a camera 1236, user input devices 1238 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1240 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[00116] The communications logic unit 1208 enables wireless communications for the transfer of data to and from the computing device 1200. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 1208 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1200 may include a plurality of communications logic units 1208. For instance, a first communications logic unit 1208 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 1208

may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[00117] The processor 1204 of the computing device 1200 may include one or more interconnects that are formed in accordance with embodiments of the present disclosure. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[00118] The communications logic unit 1208 may also include one or more interconnects that are formed in accordance with embodiments of the present disclosure.

[00119] In further embodiments, another component housed within the computing device 1200 may contain one or more metallization stacks that are formed in accordance with embodiments of the present disclosure.

[00120] In various embodiments, the computing device 1200 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1200 may be any other electronic device that processes data.

[00121] Some Examples in accordance with various embodiments of the present disclosure are now described.

[00122] Example 1 provides a metallization stack for providing electrical connectivity. The metallization stack includes a first trench interconnect; a second trench interconnect; a via providing electrical interconnection between the first interconnect and the second interconnect; a first barrier layer provided between the via and the first interconnect; and a second barrier layer provided between the via and the second interconnect.

[00123] Example 2 provides the metallization stack according to example 1, where the via is filled with an electrically conductive material including one or more bulk materials

including aluminum, copper, tungsten, cobalt, ruthenium, nickel, iron, and molybdenum and/or one or more alloys including aluminum, copper, tungsten, cobalt, ruthenium, manganese, magnesium, boron, phosphorus, nitrogen, carbon, and sulfur.

[00124] Example 3 provides the metallization stack according to any one of the preceding examples, where the first interconnect and/or the second interconnect is filled with Cu.

[00125] Example 4 provides the metallization stack according to any one of the preceding examples, where the via is filled with an electrically conductive material different from an electrically conductive material of the first interconnect and/or of the second interconnect.

[00126] Example 5 provides the metallization stack according to any one of the preceding examples, where the first barrier layer and/or the second barrier layer includes one or more of tantalum, titanium, ruthenium, cobalt, tantalum boride, titanium boride, ruthenium boride, cobalt boride, tantalum carbide, titanium carbide, ruthenium carbide, cobalt carbide, tantalum silicide, titanium silicide, ruthenium silicide, cobalt silicide, tantalum nitride, titanium nitride, ruthenium nitride, and cobalt nitride.

[00127] Example 6 provides the metallization stack according to any one of the preceding examples, further including a first barrier-interconnect adhesion layer provided between the first barrier layer and an electrically conductive material filling the first interconnect.

[00128] Example 7 provides the metallization stack according to example 6, where the first barrier-interconnect adhesion layer includes an electrically conductive material.

[00129] Example 8 provides the metallization stack according to any one of the preceding examples, further including a first barrier-via adhesion layer provided between the first barrier layer and an electrically conductive material filling the via.

[00130] Example 9 provides the metallization stack according to example 8, where the first barrier-via adhesion layer includes an electrically conductive material.

[00131] Example 10 provides the metallization stack according to any one of the preceding examples, further including a second barrier-interconnect adhesion layer provided between the second barrier layer and an electrically conductive material filling the second interconnect.

[00132] Example 11 provides the metallization stack according to example 10, where the second barrier-interconnect adhesion layer includes an electrically conductive material.

[00133] Example 12 provides the metallization stack according to any one of the preceding examples, further including a second barrier-via adhesion layer provided between the second barrier layer and an electrically conductive material filling the via.

[00134] Example 13 provides the metallization stack according to example 12, where the second barrier-via adhesion layer includes an electrically conductive material.

[00135] Example 14 provides the metallization stack according to any one of the preceding examples, where the first interconnect, the second interconnect, and the via are provided in a metallization stack support layer.

[00136] Example 15 provides the metallization stack according to example 14, further including a third barrier layer provided between the via and the metallization stack support layer.

[00137] Example 16 provides the metallization stack according to example 15, where the third barrier layer includes one or more of tantalum, titanium, ruthenium, cobalt, tantalum boride, titanium boride, ruthenium boride, cobalt boride, tantalum carbide, titanium carbide, ruthenium carbide, cobalt carbide, tantalum silicide, titanium silicide, ruthenium silicide, cobalt silicide, tantalum nitride, titanium nitride, ruthenium nitride, and cobalt nitride.

[00138] Example 17 provides the metallization stack according to examples 15 or 16, further including a third barrier-dielectric adhesion layer provided between the third barrier layer and the metallization stack support layer.

[00139] Example 18 provides the metallization stack according to example 17, where the third barrier-dielectric adhesion layer includes an electrically conductive material.

[00140] Example 19 provides the metallization stack according to example 17, where the third barrier-dielectric adhesion layer includes a dielectric material.

[00141] Example 20 provides the metallization stack according to any one of examples 15-19, further including a third barrier-via adhesion layer provided between the third barrier layer and an electrically conductive material filling the via.

[00142] Example 21 provides the metallization stack according to example 20, where the third barrier-via adhesion layer includes an electrically conductive material.

[00143] Example 22 provides the metallization stack according to example 20, where the third barrier-via adhesion layer includes a dielectric material.

[00144] Example 23 provides the metallization stack according to any one of examples 14-22, further including a via-dielectric adhesion layer provided between the via and the metallization stack support layer.

[00145] Example 24 provides the metallization stack according to example 23, where the via-dielectric adhesion layer includes an electrically conductive material.

[00146] Example 25 provides the metallization stack according to example 23, where the via-dielectric adhesion layer includes a dielectric material.

[00147] Example 26 provides the metallization stack according to any one of examples 14-25, where the metallization stack support layer includes a bulk dielectric or/and a combination of dielectric materials.

[00148] Example 27 provides the metallization stack according to any one of examples 14-26, where the metallization stack support layer includes one or more air gaps.

[00149] Example 28 provides the metallization stack according to any one of the preceding examples, where a thickness of the first barrier layer is between 0.2 nanometers and 20 micrometers.

[00150] Example 29 provides the metallization stack according to any one of the preceding examples, where a thickness of the second barrier layer is between 0.2 nanometers and 20 micrometers.

[00151] Example 30 provides an integrated circuit package, including a component and a metallization stack for providing electrical connectivity to the component, the metallization stack including a first interconnect; a second interconnect; a via providing electrical interconnection between the first interconnect and the second interconnect; a first barrier layer provided between the via and the first interconnect; and a second barrier layer provided between the via and the second interconnect.

[00152] Example 31 provides the integrated circuit package according to example 30, where the component includes a transistor, a die, a sensor, a processing device, or a memory device.

[00153] Example 32 provides the integrated circuit package according to examples 30 or 31, where the metallization stack includes the metallization stack according to any one of examples 2-29.

[00154] Example 33 provides a method of forming a metallization stack for providing electrical connectivity. The method includes providing a first interconnect; providing a second interconnect; providing a via providing electrical interconnection between the first interconnect and the second interconnect; providing a first barrier layer between the via and the first interconnect; and providing a second barrier layer between the via and the second interconnect.

[00155] Example 34 provides the method according to example 33, where providing the first interconnect includes forming a fully enclosed first interconnect in an ILD layer.

[00156] Example 35 provides the method according to example 33, where providing the first barrier layer between the via and the first interconnect includes forming openings for the via and the second interconnect in an ILD layer, and depositing the first barrier layer in at least parts of the openings for the via and the second interconnect.

[00157] Example 36 provides the method according to example 35, where providing the via providing electrical interconnection between the first interconnect and the second interconnect includes depositing a via material in the openings for the via and the second interconnect lined with the first barrier layer.

[00158] Example 37 provides the method according to example 36, where providing the via further includes planarizing the via material to expose surfaces of the ILD layer.

[00159] Example 38 provides the method according to example 33, where providing the via providing electrical interconnection between the first interconnect and the second interconnect includes forming openings for the via and the second interconnect in an ILD layer, and depositing a via material in the openings for the via and the second interconnect.

[00160] Example 39 provides the method according to example 38, where providing the via further includes planarizing the via material to expose surfaces of the ILD layer.

[00161] Example 40 provides the method according to example 33, where providing the second barrier layer between the via and the second interconnect includes forming an opening for the second interconnect in an ILD layer, and depositing the second barrier layer in at least parts of the opening for the second interconnect.

[00162] Example 41 provides the method according to example 40, where providing the second interconnect includes depositing a second interconnect material in the opening for the second interconnect lined with the second barrier layer.

[00163] Example 42 provides the method according to example 33, where providing the second interconnect includes forming an opening for the second interconnect in an ILD layer, and depositing a second interconnect material in the opening for the second interconnect.

[00164] Example 43 provides a method for forming a metallization stack for providing electrical connectivity. The method includes forming a fully enclosed first interconnect in an ILD layer; forming openings for a via and a second interconnect in the ILD layer; depositing a first barrier layer in at least parts of the openings for the via and the second interconnect; depositing a via material in the openings for the via and the second interconnect lined with

the first barrier layer; planarizing the via material to expose surfaces of the ILD layer; removing the via material and the first barrier layer from the opening for the second interconnect; depositing a second barrier layer in at least parts of the opening for the second interconnect; and depositing a second interconnect material in the opening for the second interconnect lined with the second barrier layer.

[00165] Example 44 provides the method according to example 443, further including planarizing the second interconnect material to expose the surfaces of the ILD layer; removing a portion of the second interconnect material to form a recess in the second interconnect material; and depositing a top barrier layer in the recess in the second interconnect material.

[00166] Example 45 provides the method according to example 44, further including planarizing the top barrier layer to expose the surfaces of the ILD layer.

[00167] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[00168] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims:

1. A metallization stack for providing electrical connectivity comprising:
 - a first interconnect;
 - a second interconnect;
 - a via providing electrical interconnection between the first interconnect and the second interconnect;
 - a first barrier layer provided between the via and the first interconnect; and
 - a second barrier layer provided between the via and the second interconnect.
2. The metallization stack according to claim 1, wherein the via is filled with an electrically conductive material different from an electrically conductive material of the first interconnect and/or of the second interconnect.
3. The metallization stack according to any one of claims 1 or 2, wherein the via is filled with an electrically conductive material comprising one or more bulk materials comprising aluminum, copper, tungsten, cobalt, ruthenium, nickel, iron, and molybdenum and/or one or more alloys comprising aluminum, copper, tungsten, cobalt, ruthenium, manganese, magnesium, boron, phosphorus, nitrogen, carbon, and sulfur.
4. The metallization stack according to any one of claims 1 or 2, wherein the first barrier layer and/or the second barrier layer comprises one or more of tantalum, titanium, ruthenium, cobalt, tantalum boride, titanium boride, ruthenium boride, cobalt boride, tantalum carbide, titanium carbide, ruthenium carbide, cobalt carbide, tantalum silicide, titanium silicide, ruthenium silicide, cobalt silicide, tantalum nitride, titanium nitride, ruthenium nitride, and cobalt nitride.
5. The metallization stack according to any one of claims 1 or 2, wherein the first interconnect, the second interconnect, and the via are provided in an interconnect

support layer, the metallization stack further comprising a third barrier layer provided between the via and the interconnect support layer.

6. The metallization stack according to claim 5, wherein the third barrier layer comprises one or more of tantalum, titanium, ruthenium, cobalt, tantalum boride, titanium boride, ruthenium boride, cobalt boride, tantalum carbide, titanium carbide, ruthenium carbide, cobalt carbide, tantalum silicide, titanium silicide, ruthenium silicide, cobalt silicide, tantalum nitride, titanium nitride, ruthenium nitride, and cobalt nitride.

7. The metallization stack according to claim 5, wherein the interconnect support layer comprises a bulk dielectric or/and a combination of dielectric materials.

8. The metallization stack according to any one of claims 1 or 2, wherein a thickness of the first barrier layer is between 0.2 nanometers and 20 micrometers.

9. The metallization stack according to any one of claims 1 or 2, wherein a thickness of the second barrier layer is between 0.2 nanometers and 20 micrometers.

10. An integrated circuit package, comprising:

a component, and

an metallization stack for providing electrical connectivity to the component, the metallization stack comprising:

a first interconnect;

a second interconnect;

a via providing electrical interconnection between the first interconnect and the second interconnect;

a first barrier layer provided between the via and the first interconnect; and

a second barrier layer provided between the via and the second interconnect.

11. The integrated circuit package according to claim 10, wherein the component comprises a transistor, a die, a sensor, a processing device, or a memory device.

12. The integrated circuit package according to claims 10 or 11, wherein the via is filled with an electrically conductive material different from an electrically conductive material of the first interconnect and/or of the second interconnect.

13. The integrated circuit package according to claims 10 or 11, wherein the first barrier layer and/or the second barrier layer comprises one or more of tantalum, titanium, ruthenium, cobalt, tantalum boride, titanium boride, ruthenium boride, cobalt boride, tantalum carbide, titanium carbide, ruthenium carbide, cobalt carbide, tantalum silicide, titanium silicide, ruthenium silicide, cobalt silicide, tantalum nitride, titanium nitride, ruthenium nitride, and cobalt nitride.

14. The integrated circuit package according to claims 10 or 11, wherein the first interconnect, the second interconnect, and the via are provided in an interconnect support layer, the metallization stack further comprising a third barrier layer provided between the via and the interconnect support layer.

15. A method of forming a metallization stack for providing electrical connectivity, the method comprising:

providing a first interconnect;

providing a second interconnect;

providing a via providing electrical interconnection between the first interconnect and the second interconnect;

providing a first barrier layer between the via and the first interconnect; and

providing a second barrier layer between the via and the second interconnect.

16. The method according to claim 15, wherein providing the first interconnect comprises forming a fully enclosed first interconnect in an interlayer dielectric (ILD) layer.

17. The method according to claim 15, wherein providing the first barrier layer between the via and the first interconnect comprises:

forming openings for the via and the second interconnect in an interlayer dielectric (ILD) layer, and

depositing the first barrier layer in at least parts of the openings for the via and the second interconnect.

18. The method according to claim 17, wherein providing the via providing electrical interconnection between the first interconnect and the second interconnect comprises:

depositing a via material in the openings for the via and the second interconnect lined with the first barrier layer.

19. The method according to claim 18, wherein providing the via further comprises planarizing the via material to expose surfaces of the ILD layer.

20. The method according to claim 15, wherein providing the via providing electrical interconnection between the first interconnect and the second interconnect comprises:

forming openings for the via and the second interconnect in an interlayer dielectric (ILD) layer, and

depositing a via material in the openings for the via and the second interconnect.

21. The method according to claim 15, wherein providing the second barrier layer between the via and the second interconnect comprises:

forming an opening for the second interconnect in an interlayer dielectric (ILD) layer, and

depositing the second barrier layer in at least parts of the opening for the second interconnect.

22. The method according to claim 21, wherein providing the second interconnect comprises:

depositing a second interconnect material in the opening for the second interconnect lined with the second barrier layer.

23. The method according to claim 15, wherein providing the second interconnect comprises:

forming an opening for the second interconnect in an interlayer dielectric (ILD) layer, and

depositing a second interconnect material in the opening for the second interconnect.

24. A method of forming a metallization stack for providing electrical connectivity, the method comprising:

forming a fully enclosed first interconnect in an interlayer dielectric (ILD) layer;

forming openings for a via and a second interconnect in the ILD layer;

depositing a first barrier layer in at least parts of the openings for the via and the second interconnect;

depositing a via material in the openings for the via and the second interconnect lined with the first barrier layer;

planarizing the via material to expose surfaces of the ILD layer;

removing the via material and the first barrier layer from the opening for the second interconnect;

depositing a second barrier layer in at least parts of the opening for the second interconnect; and

depositing a second interconnect material in the opening for the second interconnect lined with the second barrier layer.

25. The method according to claim 24, further comprising:

planarizing the second interconnect material to expose the surfaces of the ILD layer;

removing a portion of the second interconnect material to form a recess in the second interconnect material; and

depositing a top barrier layer in the recess in the second interconnect material.

1/10

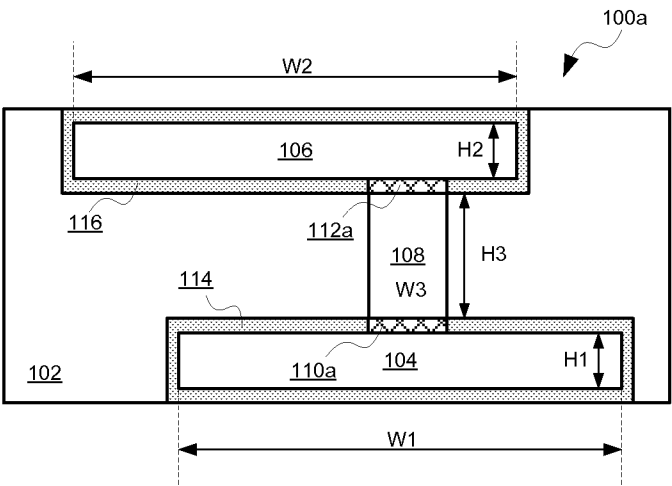


FIG. 1a

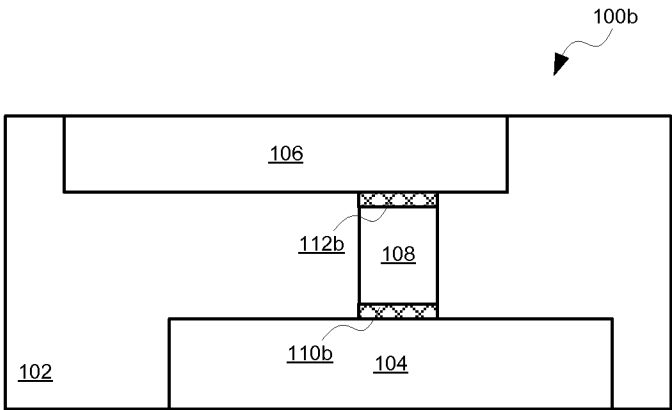


FIG. 1b

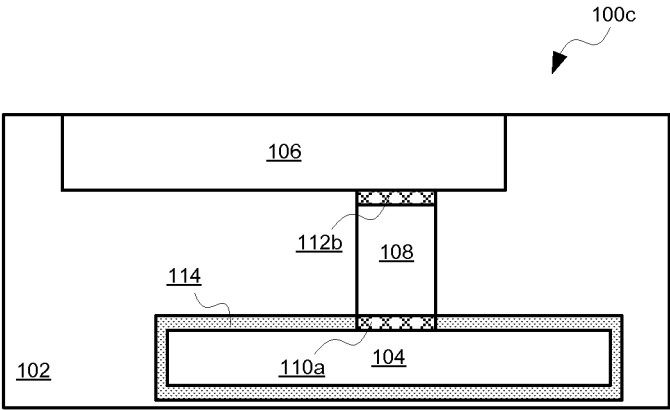


FIG. 1c

2/10

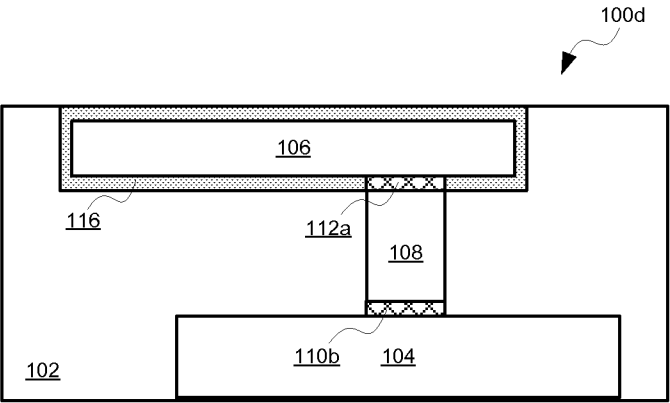


FIG. 1d

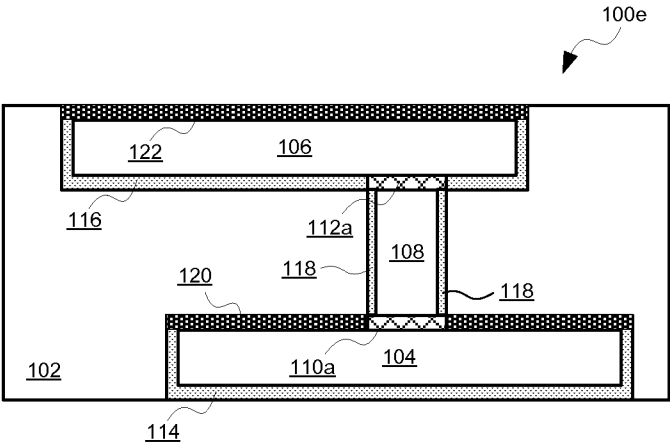


FIG. 1e

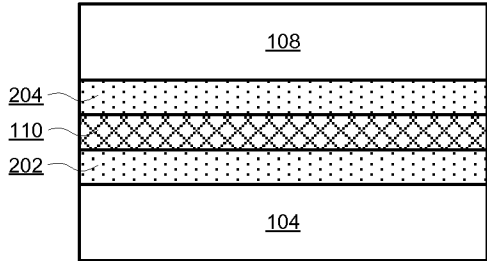


FIG. 2

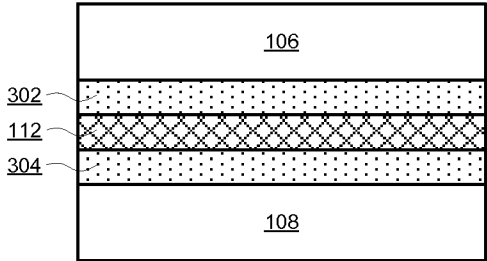


FIG. 3

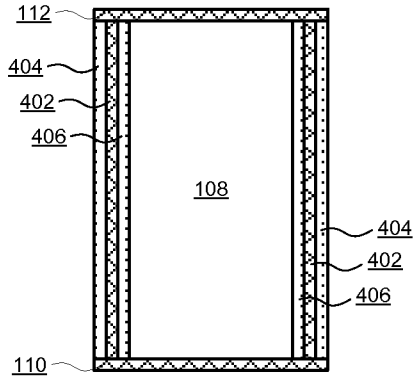


FIG. 4

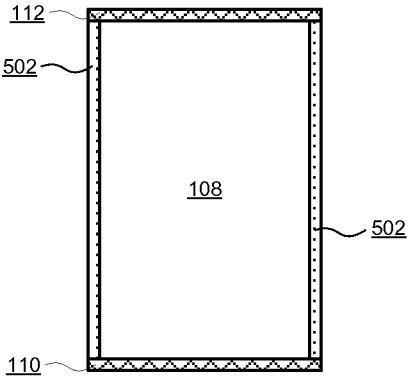


FIG. 5

4/10

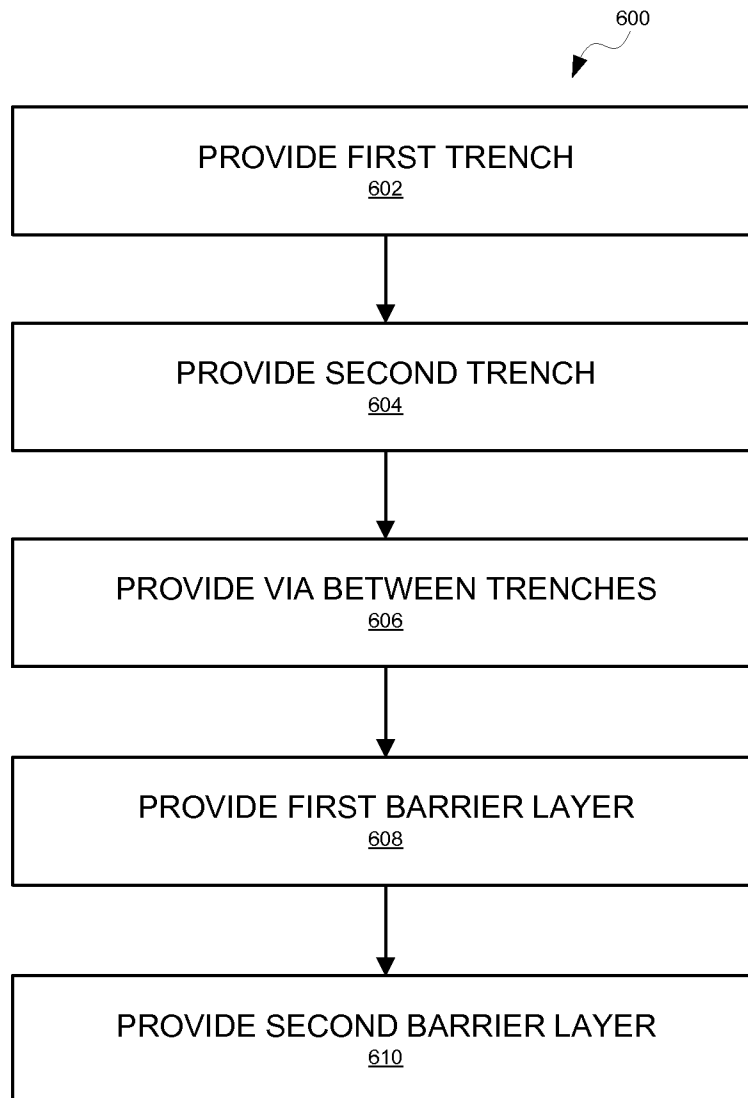


FIG. 6

5/10

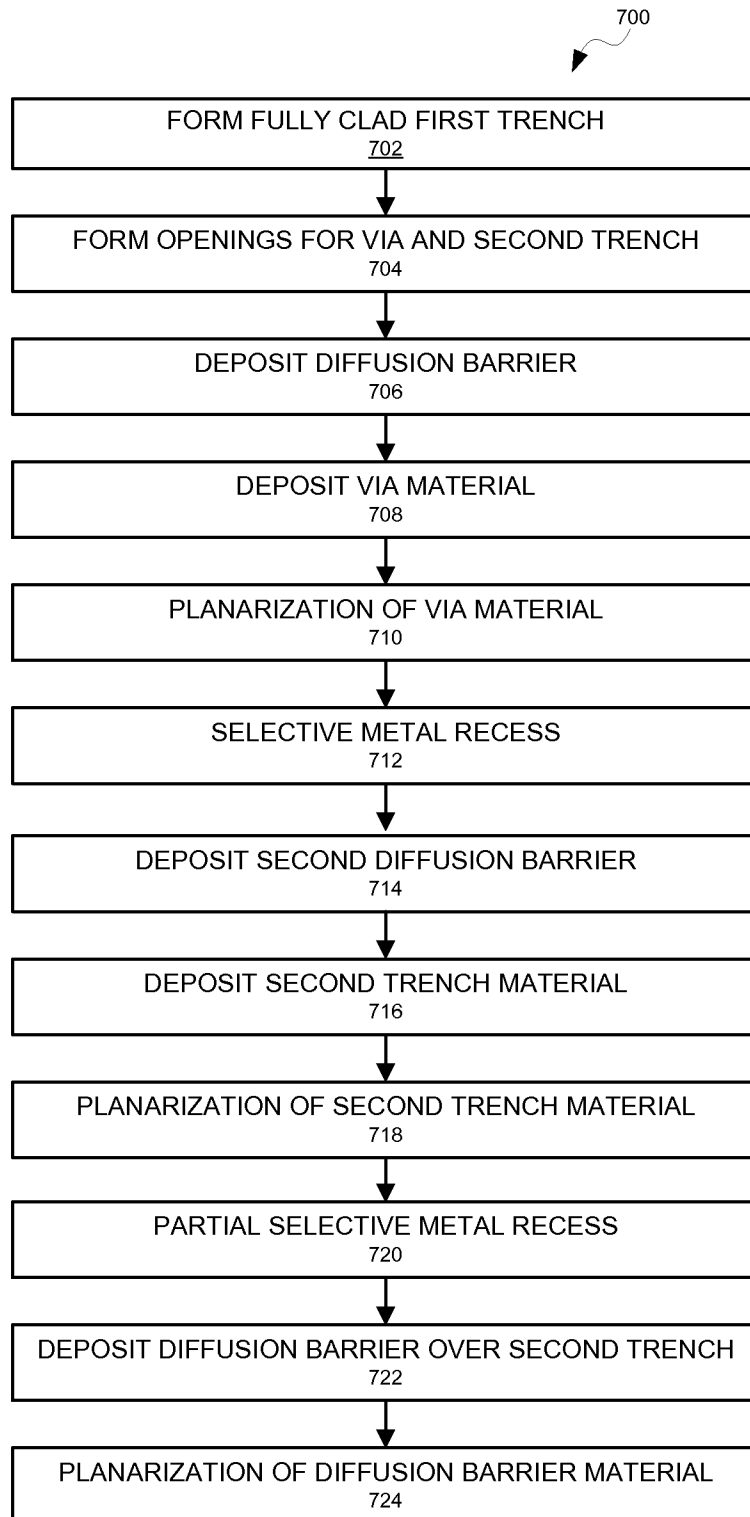
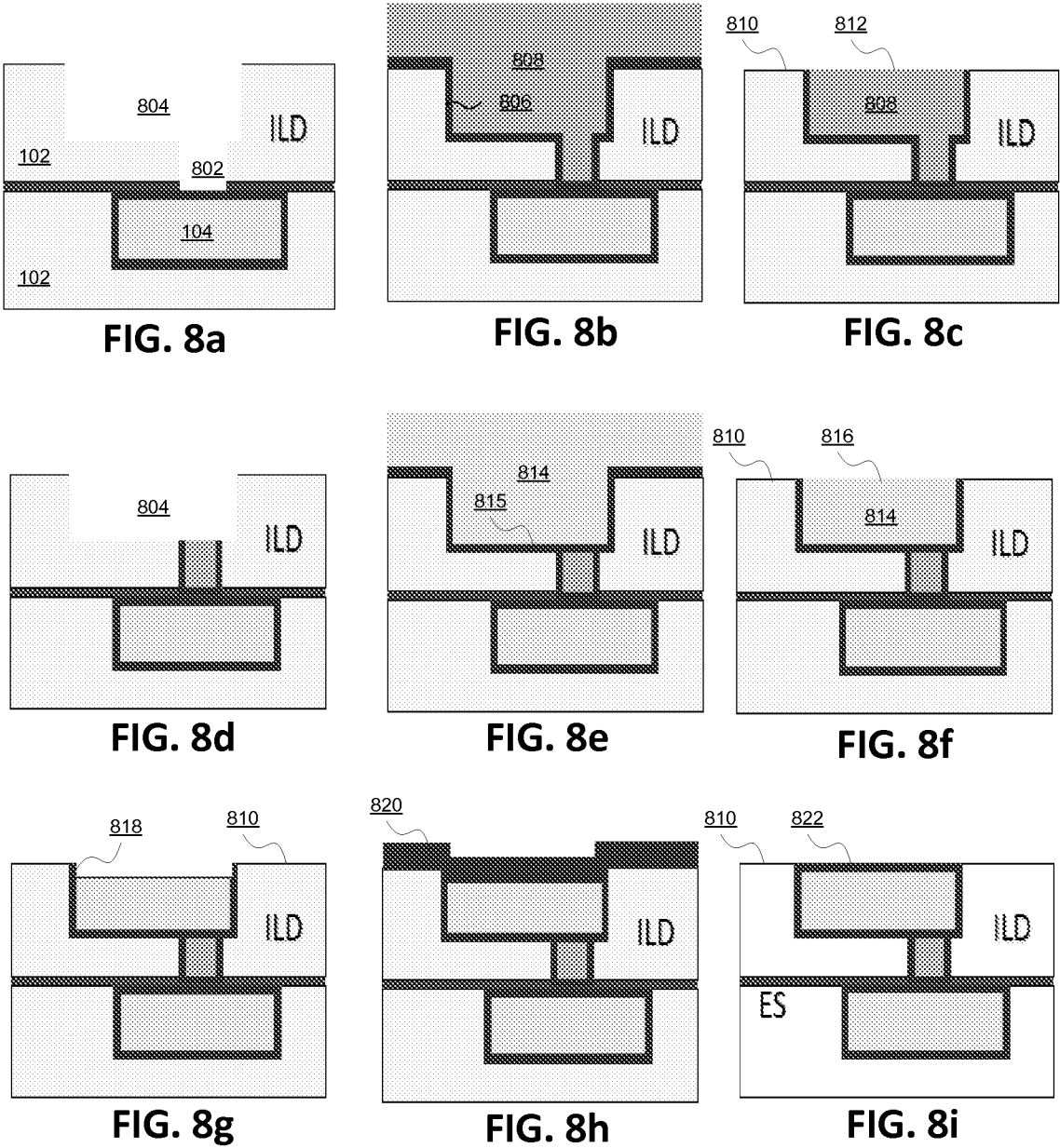


FIG. 7



7/10

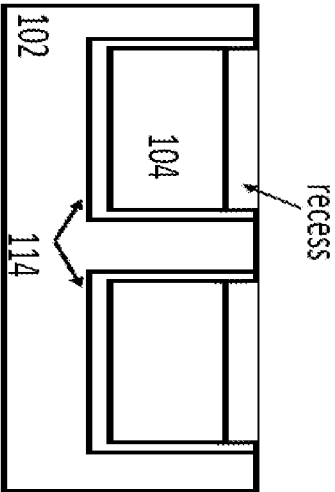


FIG. 9a

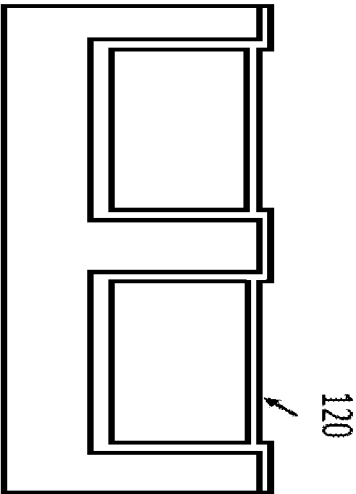


FIG. 9b

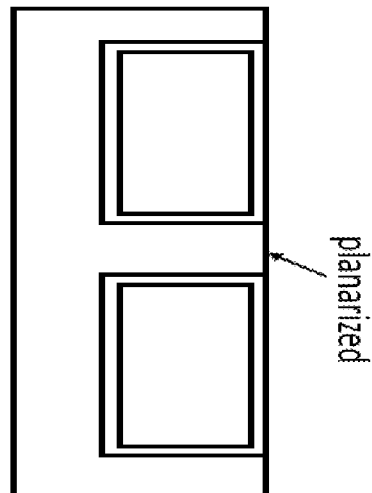


FIG. 9c

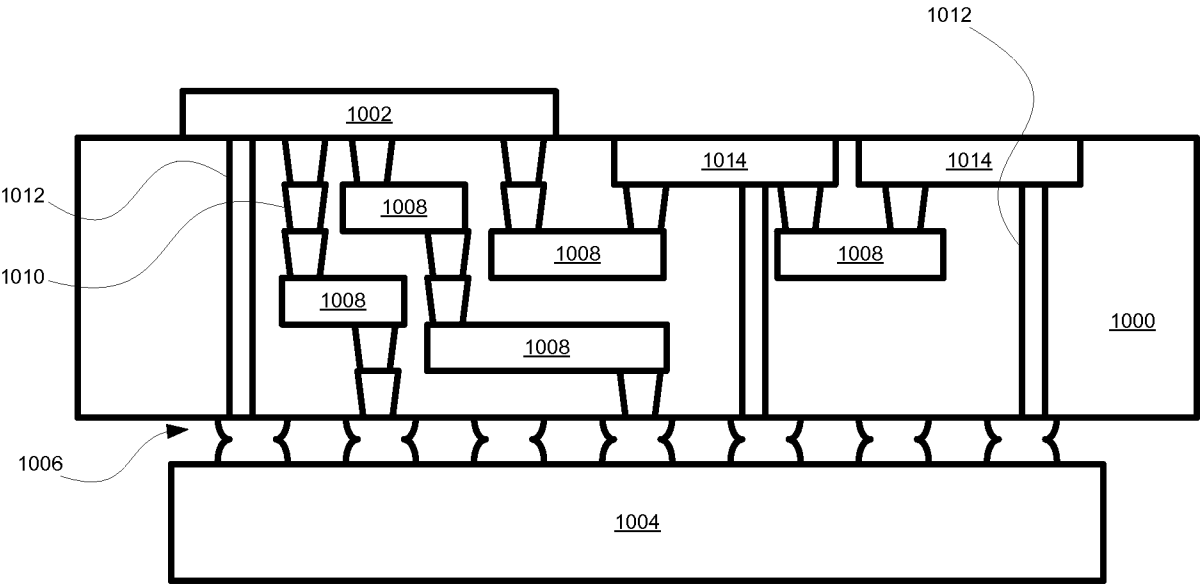


FIG. 10

9/10

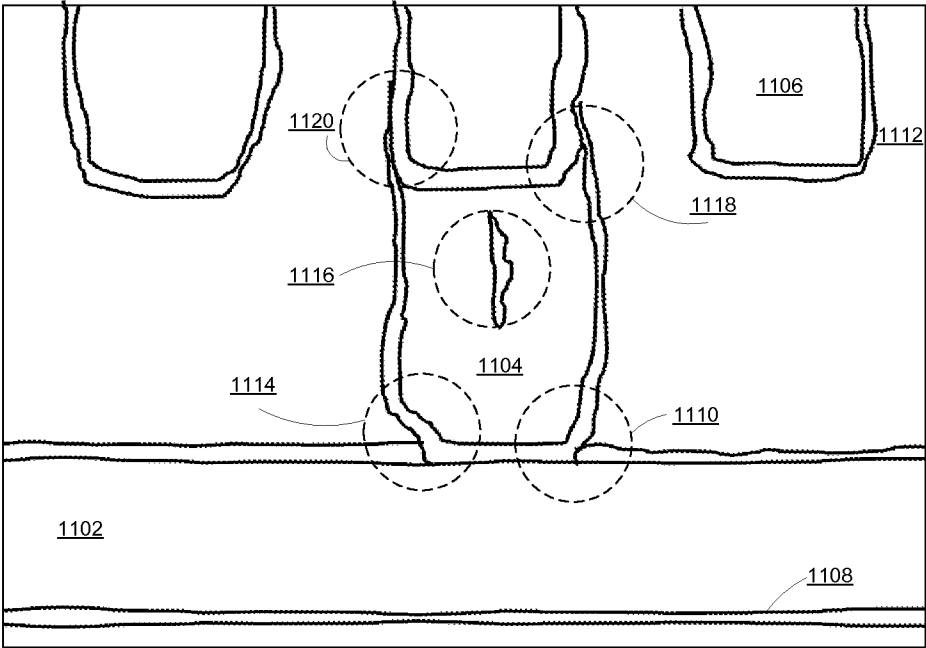


FIG. 11a

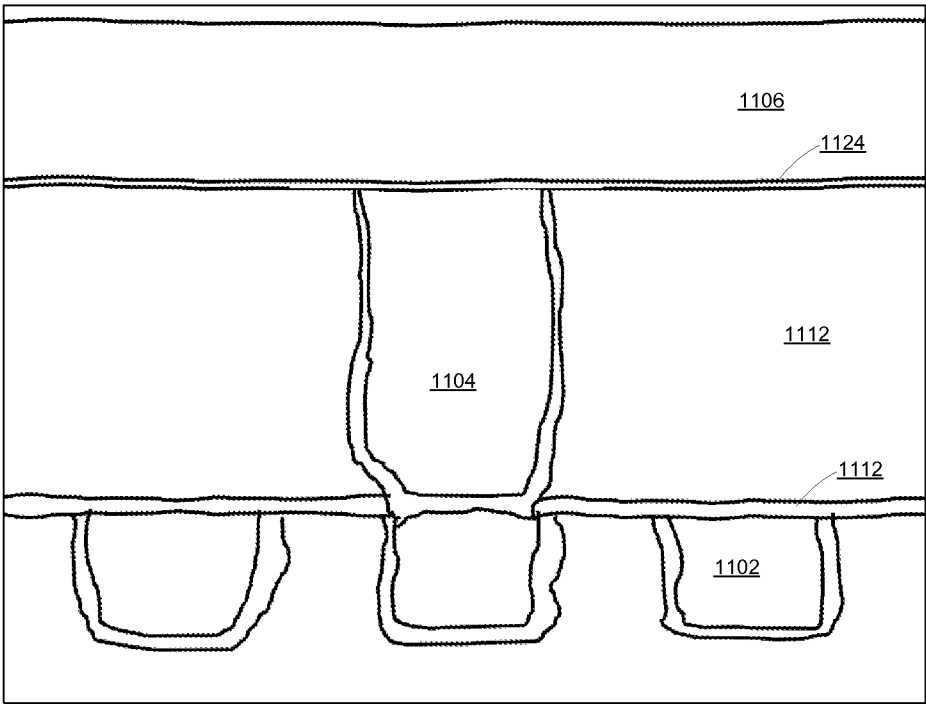


FIG. 11b

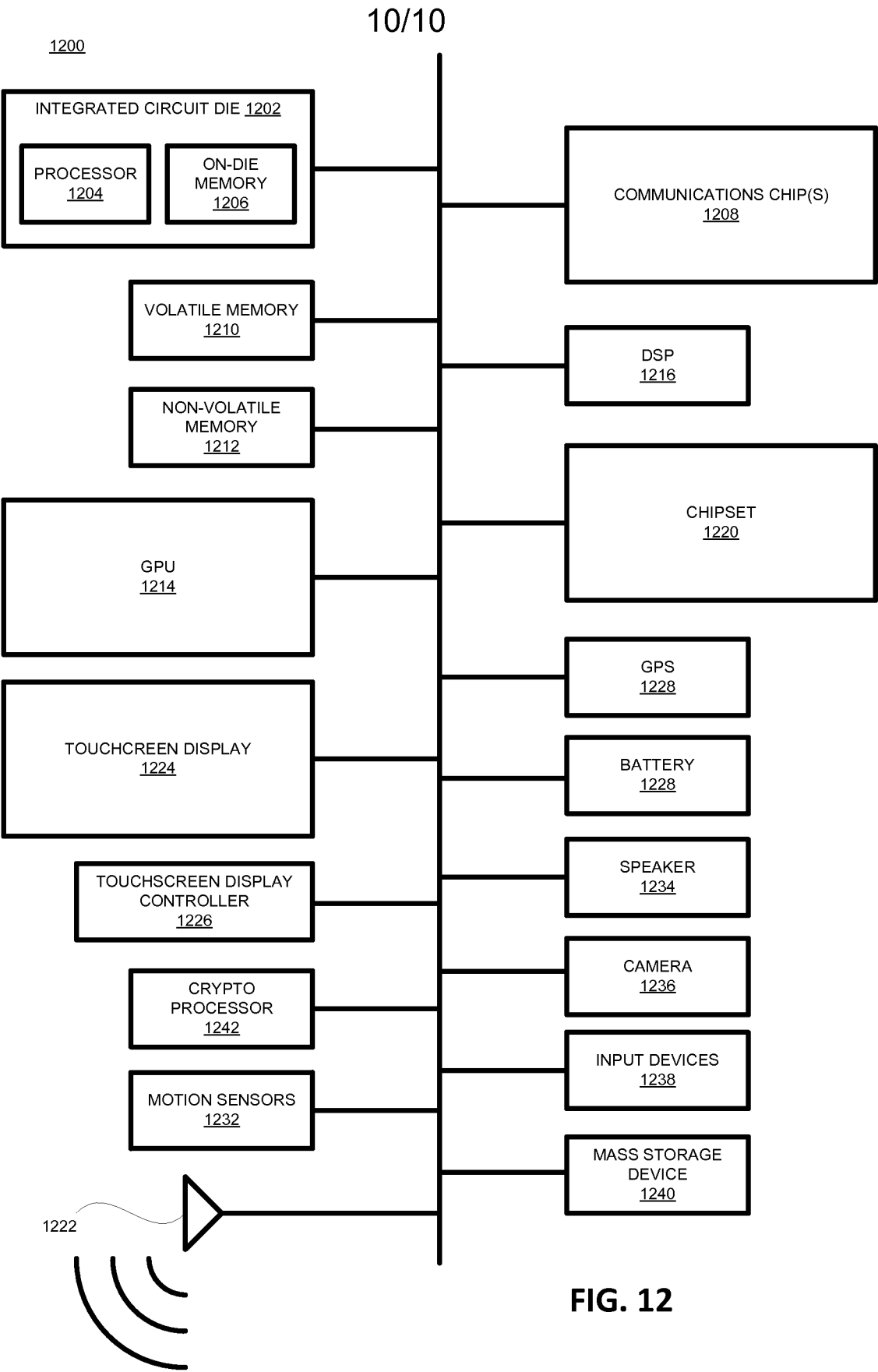


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/062031**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/48(2006.01)i, H01L 21/60(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/48; H01L 23/52; H01L 23/532; H01L 21/60

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: interconnect, via, barrier, package, IC, stack, metal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004-0183202 A1 (TATSUYA USAMI) 23 September 2004 See abstract, paragraphs [0044]-[0061] and figures 1-7(b).	1-25
X	US 2005-0029669 A1 (HIROAKI INOUE et al.) 10 February 2005 See abstract, paragraphs [0055]-[0059], claim 5 and figure 1.	1,3-9,15-16
Y		2,10-14
Y	US 2011-0079910 A1 (KEVIN O'BRIEN et al.) 07 April 2011 See abstract, paragraphs [0029]-[0031] and figures 4-7.	2,10-14
A	US 2006-0180930 A1 (DU B. NGUYEN et al.) 17 August 2006 See abstract, paragraphs [0042]-[0085] and figures 3-11.	1-25
A	US 2010-0038764 A1 (KEVIN PETER LYNE) 18 February 2010 See abstract, paragraphs [0019]-[0031] and figures 1A-1E.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 August 2016 (18.08.2016)

Date of mailing of the international search report

19 August 2016 (19.08.2016)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/062031

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004-0183202 A1	23/09/2004	JP 2004-253780 A JP 2004-253781 A US 2005-0179137 A1	09/09/2004 09/09/2004 18/08/2005
US 2005-0029669 A1	10/02/2005	JP 2005-038971 A US 7157370 B2	10/02/2005 02/01/2007
US 2011-0079910 A1	07/04/2011	CN 102171797 A EP 2356674 A2 JP 2012-505554 A KR 10-1238953 B1 KR 10-2011-0059752 A US 2010-0140804 A1 US 7867891 B2 WO 2010-068523 A2 WO 2010-068523 A3	31/08/2011 17/08/2011 01/03/2012 04/03/2013 03/06/2011 10/06/2010 11/01/2011 17/06/2010 26/08/2010
US 2006-0180930 A1	17/08/2006	US 7138714 B2	21/11/2006
US 2010-0038764 A1	18/02/2010	CN 101385149 A EP 1989739 A2 EP 1989739 A4 JP 2009-527130 A KR 10-1019793 B1 KR 10-2008-0095290 A US 2007-0187836 A1 WO 2007-095604 A2 WO 2007-095604 A3	11/03/2009 12/11/2008 10/08/2011 23/07/2009 04/03/2011 28/10/2008 16/08/2007 23/08/2007 21/08/2008