



(51) International Patent Classification:

H01L 25/075 (2006.01) *H05K 3/32* (2006.01)
H01L 33/62 (2010.01) *H05K 1/18* (2006.01)
H05K 3/40 (2006.01) *H05K 1/11* (2006.01)

(21) International Application Number:

PCT/US2017/041655

(22) International Filing Date:

12 July 2017 (12.07.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/362,609 15 July 2016 (15.07.2016) US

(71) Applicant: **3M INNOVATIVE PROPERTIES COMPANY** [US/US]; 3M Center, Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

(72) Inventors: **NARAG, Alejandro, Aldrin, II, A.**; 1 Yishun Avenue 7, 768923 Singapore (SG). **PALANISWAMY, Ravi**; 1 Yishun Avenue 7, 768923 Singapore (SG).

(74) Agent: **MOSHREFZADEH, Robert, S.** et al.; 3M Center, Office of Intellectual Property Counsel, Post Office Box 33427, Saint Paul, MN 55133-3427 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(54) Title: MULTILAYER LED SUBSTRATE

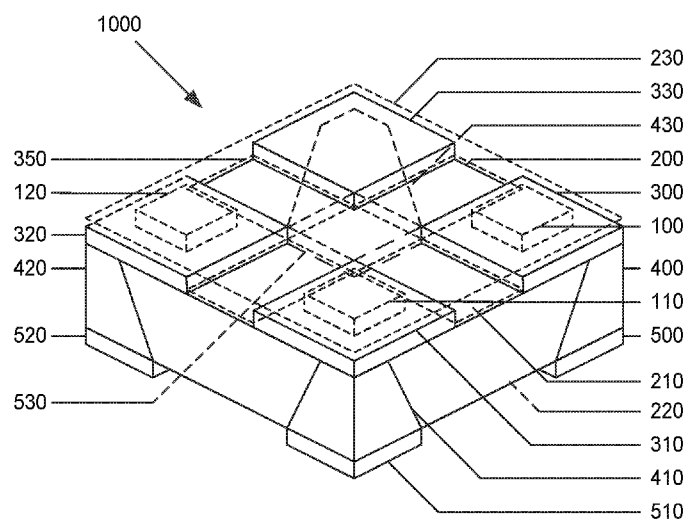


FIG. 1

(57) Abstract: A flexible multilayer construction (1000) for mounting a plurality of light emitting semiconductor devices (LEDs 100, 110, 120) includes a flexible dielectric substrate (200) comprising top (210) and bottom (220) major surfaces, and pluralities of corresponding electrically conductive top (300, 310, 320, 330) and bottom (500, 510, 520, 530) pads disposed on the top and bottom major surfaces, respectively. An electrically conductive via (400, 410, 420, 430) connects each pair of corresponding top and bottom pads, a side of each top pad partially overlapping a side of the corresponding bottom pad and a side of the substrate, such that in a plan view, each top pad fully overlaps the corresponding bottom pad.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

MULTILAYER LED SUBSTRATE**BACKGROUND**

[0001] Printed circuit boards contain multiple layers of conductive metal sheets and non-conductive substrates. Vias are used to electrically connect one or more of the conductive metal sheets between the substrate layers. Vias are conventionally manufactured by drilling holes in the circuit board after the circuit board layers have been fabricated. As chip density increases, mechanical and punched drills may not be able to form holes sufficiently small for some circuit board and chip designs.

[0002] One example of a high density application is a Red/Green/Blue (RGB) light emitting diode (LED) backlight chip. Printed circuit boards for RGB LED chips can be made from two metal layers separated by a dielectric substrate. The top metal layer may be connected to a chip, while the bottom metal layer may be soldered to a printed circuit board. The two metal layers are connected by a via structure.

SUMMARY

[0003] In general, this disclosure is directed to a flexible multilayer construction that can be used to mount and electrically couple light emitting semiconductor devices (LESsDs) to underlying electronic devices. Each multilayer construction may have a plurality of electrically conducting top pads and bottom pads electrically connected by vias. One or more LESsDs may be connected to the top pads and independently energized.

[0004] During fabrication, a multilayer film may contain an array of top pads and bottom pads disposed on opposite surfaces of a substrate and connected by a conducting path. To form the constructions, the film may be cut through these top pads, bottom pads, and conducting paths, so that the resulting constructions' top pads, bottom pads and conducting paths are a fraction of their original size and separated into electrically isolated corners of the construction. These constructions may be used in applications where via hole size may limit the size of the substrate. A conventionally-sized via hole may be divided into sections, such that the resulting via hole may be smaller, allowing for higher density chips.

[0005] In one aspect, the present disclosure is directed to a flexible multilayer construction for mounting at least three light emitting semiconductor devices includes a flexible dielectric substrate, electrically conductive first through fourth top pads, and electrically conductive vias. The flexible dielectric substrate has a top major surface, a bottom major surface, and a common LED mounting region on the top major surface for receiving the at least three LESsDs. The common LED mounting region has a maximum projected area less than about 0.25 mm². The electrically conductive first through fourth top pads are spaced apart and disposed entirely within the common LED mounting region for electrically connecting to electrically conductive terminals of the at least three LESsDs received in the common LED mounting region. The electrically conductive vias extend from each of the first through fourth top pads to the

bottom major surface. When the at least three LEDSs are received and electrically connected to the first through fourth top pads, each of the at least three LEDSs can be independently energized.

[0006] In another aspect, the present disclosure is directed to a LEDS package includes a flexible dielectric substrate, electrically conductive first through fourth pads, electrically conductive vias, and first through third LEDSs. The flexible dielectric substrate includes opposing top and bottom major surfaces and a common LEDS mounting region on the top major surface. The common LEDS mounting region has a maximum projected area less than about 1 mm². The electrically conductive first through fourth pads are spaced apart and disposed entirely within the common LEDS mounting region. The electrically conductive vias extend from each of the first through fourth pads to the bottom major surface. The first through third LEDSs are mounted in the common LEDS mounting region, an electrically conductive first terminal of each LEDS in the first through at least third LEDSs electrically connected to a different pad in the first through fourth pads, electrically conductive second terminals of at least two LEDSs in the first through third LEDSs electrically connected to a same pad in the first through fourth pads, such that each of the first through third LEDS is independently energizable.

[0007] In another aspect, the present disclosure is directed to a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LESDs) includes a flexible dielectric polygonal substrate, a plurality of spaced apart electrically conductive top pads, a plurality of electrically conductive bottom pads, and a plurality of electrically conductive vias. The flexible dielectric polygonal substrate includes a plurality of sides intersecting at a plurality of vertices and includes top and bottom major surfaces. The plurality of electrically conductive top pads are spaced apart and disposed on the top major surface of the substrate. The plurality of electrically conductive bottom pads are spaced apart and disposed on the bottom major surface of the substrate. The plurality of electrically conductive vias extend between corresponding top and bottom pads, such that for each corresponding top and bottom pad, the top and bottom pads are each polygonal having a plurality of sides intersecting at a plurality of vertices, a first vertex of the top pad coincident with a first vertex of the bottom pad and a first vertex of the substrate, the sides of the top and bottom pads and the substrate intersecting at the first vertex and partially overlapping one another.

[0008] In other embodiments, the present disclosure is directed to a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LESDs) includes a flexible dielectric substrate comprising top and bottom major surfaces, and pluralities of corresponding electrically conductive top and bottom pads disposed on the top and bottom major surfaces, respectively. An electrically conductive via connects each pair of corresponding top and bottom pads, a side of each top pad partially overlapping a side of the corresponding bottom pad and a side of the substrate, such in a plan view, each top pad fully overlaps the corresponding bottom pad.

[0009] In another aspect, the present disclosure is directed to a method of fabricating a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LESDs), includes the steps of: forming a patterned multilayer film; determining a plurality of cutting lines on the patterned multilayer film, the cutting lines dividing the first and second pads in each corresponding first

and second pads and the conductive path connecting the first and second pads each into four sections; and singulating a flexible multilayer construction by cutting through the patterned multilayer film along the determined cutting lines, resulting in the flexible multilayer construction having a plurality of corresponding top and bottom pads connected by corresponding electrically conductive vias, each top and bottom pad extending to a side of the flexible multilayer construction. Forming a patterned multilayer film further includes: providing a flexible substrate having opposing top and bottom major surfaces; forming a plurality of spaced apart electrically conductive first pads on the top major surface of the flexible substrate; forming a plurality of spaced apart electrically conductive second pads on the bottom major surface of the flexible substrate in a one to one correspondence with the first pads; and forming an electrically conductive path between corresponding first and second pads through the flexible substrate.

[0010] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF DRAWINGS

[0011] FIG. 1 is a schematic, perspective view diagram of a flexible multilayer construction.

[0012] FIG. 2 is a flowchart for a method for fabricating a flexible multilayer construction.

[0013] FIG. 3A is a schematic, top view diagram of a multilayer film.

[0014] FIG. 3B is a schematic, bottom view diagram of a multilayer film.

[0015] FIG. 3C is a schematic, top view diagram of a patterned multilayer film.

[0016] FIG. 3D is a schematic, top view diagram of a patterned multilayer film.

[0017] FIG. 3E is a schematic, sectional side view diagram of a patterned multilayer film.

[0018] FIG. 3F is a schematic, top view diagram of a flexible multilayer construction.

[0019] FIG. 3G is a schematic, sectional side view diagram of the flexible multilayer construction of FIG. 3F.

[0020] FIG. 4 is a schematic, perspective view diagram of a flexible multilayer construction.

[0021] FIG. 5A is a schematic, top view diagram of a flexible multilayer construction having three LEDs each mounted on a single respective top pad.

[0022] FIG. 5B is a schematic, sectional diagram of the flexible multilayer construction of FIG. 5A.

[0023] FIG. 5C is a schematic, top view diagram of a flexible multilayer construction having four LEDs, each mounted on two respective top pads.

[0024] FIG. 5D is a schematic, top view diagram of a flexible multilayer construction having three LEDs, each mounted on two respective top pads.

[0025] Like symbols in the drawings indicate like elements. Dotted lines indicate optional or functional components, while dashed lines indicate components out of view.

DETAILED DESCRIPTION

[0026] FIG. 1 is a schematic, perspective view diagram of a flexible multilayer construction 1000. The flexible multilayer construction 1000 may include a flexible substrate 200. The flexible substrate 200 may attach, support, and electrically isolate certain components of the flexible multilayer construction 1000.

5 The flexible substrate 200 has a top major surface 210 and a bottom major surface 220. In some embodiments, the flexible substrate 200 may be a dielectric material including, but not limited to, FR-1, FR-2, FR-3, FR-4, FR-5, FR-6, G-10, G-11, CEM-1, CEM-2, CEM-3, CEM-4, CEM-5, PTFE, RF-35, alumina, and polyimide. Properties for which the flexible substrate 200 may be selected include, but are not limited to, flame retardancy, glass transition temperature, decomposition temperature, coefficient of
10 thermal expansion, thermal conductivity, electrical resistance, dielectric constant, strength, flexibility, and moisture absorption.

[0027] The flexible multilayer construction 1000 may have a common LEDS mounting region 230 on the top major surface 210 for receiving LEDSs 100, 110, 120. The common LEDS mounting region 230 may be a functional two dimensional area at or near a surface of the flexible multilayer construction 1000
15 configured to receive one or more LEDSs 100, 110, 120. The common LEDS mounting region 230 may not be limited to the surface area of the top major surface 210, and may include the surface of other components on the flexible multilayer construction 1000. In the example of FIG. 1, the common LEDS mounting region 230 contains three LEDSs 100, 110, 120; however, in other embodiments, the common LEDS mounting region 230 may greater or fewer LEDSs, such as four LEDSs.

20 [0028] The flexible multilayer construction 1000 may include a plurality of electrically conductive top pads 300, 310, 320, 330, disposed entirely within the common LEDS mounting region 230. The plurality of electrically conductive top pads 300, 310, 320, 330, may be used for electrically connecting the LEDSs 100, 110, 120. A variety of materials may be used for the electrically conductive top pads 300, 310, 320, 330, including, but not limited to, copper, gold, nickel, and stainless steel. Properties for which the
25 electrically conductive top pads 300, 310, 320, 330, may be selected include, but are not limited to, electrical conductivity and thermal conductivity. The electrically conductive top pads 300, 310, 320, 330, may create interconnecting grooves 350 that may contain other components, such as reflective coatings, insulative coatings, or heat dissipating coatings. In some embodiments, for example, the interconnecting grooves 350 are at least partially filled with an electrically insulative reflective material having an average
30 reflectance of at least 70% in a visible range of the spectrum.

[0029] The flexible multilayer construction 1000 may also include a plurality of vias 400, 410, 420, 430, each extending from one of the top pads 300, 310, 320, 330, to the bottom major surface 220. The plurality of vias 400, 410, 420, 430 can be used to electrically connect the top pads 300, 310, 320, 330, to the bottom major surface 220. In some embodiments, the vias 400, 410, 420, 430, filled with electrically
35 conductive material to form electrically conductive paths between the top and bottom major surfaces 210, 220. A variety of materials may be used for the vias 400, 410, 420, 430, including, but not limited to, lead, tin, silver, copper, zinc, and indium. Properties for which the material of the vias 400, 410, 420, 430,

may be selected include, but are not limited to, electrical conductivity thermal conductivity, tensile strength, shear strength, toxicity, melting point.

[0030] Electrically conductive bottom pads 500, 510, 520, 530, may be disposed on and spaced apart at the bottom major surface 220. The electrically conducting bottom pads 500, 510, 520, 530, may seat and electrically connect the flexible multilayer construction 1000 with a component on which the flexible multilayer construction 1000 is mounted. Any or all of corresponding top pads 300, 310, 320, 330, vias 400, 410, 420, 430, and bottom pads 500, 510, 520, 530, may be in electrical contact. A variety of materials may be used for the electrically conductive bottom pads 500, 510, 520, 530, including, but not limited to, copper, gold, nickel, and stainless steel. Properties for which the electrically conductive bottom pads 500, 510, 520, 530, may be selected include, but are not limited to, electrical conductivity and thermal conductivity.

[0031] One or more LESDs 100, 110, 120, may be mounted and electrically connected to the flexible multilayer construction 1000 through the top pads 300, 310, 320, 330. In some embodiments, the LESDs are LEDs. The flexible multilayer construction 1000 may be configured so that each LESD 100, 110, 120, received and electrically connected to the top pads 300, 310, 320, 330, may be independently energized.

[0032] FIG. 2 is a flowchart for a method 2000 for fabricating a flexible multilayer construction such as, for example, the construction 1000 shown in FIG. 1. In some embodiments, steps of the method 2000 are carried out sequentially. A patterned multilayer film may be formed, as in step 2100. To form the patterned multilayer film, a flexible substrate having a top major surface and a bottom major surface may be provided, as in step 2110. The flexible substrate may correspond to the flexible substrate 200 of the flexible multilayer construction 1000 in FIG. 1.

[0033] A plurality of spaced apart electrically conductive first pads may be formed on the top major surface of the substrate, as in step 2120. The electrically conductive first pads may correspond to the top pads 300, 310, 320, 330, of the flexible multilayer construction 1000. The electrically conductive first pads may form a two dimensional top array circuit on the top major surface of the flexible substrate. In some embodiments, the electrically conductive first pads may be spaced close enough for an LESD to span or connect between two adjacent first pads. FIG. 3A is a schematic, top view diagram of a multilayer film 3010, such as may be fabricated in step 2120. A flexible substrate 3100 has a top major surface 3110. A plurality of spaced apart, conductive first pads 3200 are disposed on the top major surface 3110 of the flexible substrate 3100.

[0034] Referring again to FIG. 2, a plurality of spaced apart electrically conductive second pads may be formed on the bottom major surface of the substrate, as in step 2130. The electrically conductive second pads may correspond to the bottom pads 500, 510, 520, 530, of the flexible multilayer construction 1000 of FIG. 1. The electrically conductive second pads may form a two dimensional bottom array circuit that corresponds to the two dimensional top array circuit. In some embodiments, the second pads may be disposed in a one to one correspondence with the first pads. In some embodiments, the second pads are centered opposite the first pads. FIG. 3B is a schematic, bottom view diagram of a multilayer film 3020, such as may be fabricated in step 2130. The flexible substrate 3100 has a bottom major surface 3120. A

plurality of spaced apart, electrically conductive second pads 3300 are distributed on the bottom major surface 3120 of the flexible substrate 3100.

[0035] Referring back to FIG. 2, electrically conductive paths between corresponding first pads and second pads may be formed through the substrate, as in step 2140. In some embodiments, this conductive path formation may be performed after placement of the first and second pads, while in other embodiments, the conductive path formation may be performed before either of the placement of first or second pads. In some embodiments, forming the electrically conducting vias may include forming a hole in the substrate and filling the hole with electrically conducting material. As examples, which are not intended to be limiting, a laser, a drill, or an etching process may form a via through the top and bottom pads, which may subsequently be filled with solder.

[0036] The resulting patterned multilayer film from step 2100 may have a plurality of spaced apart electrically conductive first pads overlapping a plurality of electrically conductive second pads, where the first pads and the second pads are electrically coupled through an electrically conductive path. The electrically conductive first pads and second pads may form a two dimensional array along different first (x) and second (y) directions. In some embodiments, the directions are orthogonal. In some embodiments, the first pads are larger than the second pads, and each second pad is substantially centered under its corresponding first pad. FIG. 3C is a schematic, top view diagram of a patterned multilayer film 3000, such as may be fabricated in step 2100. The flexible substrate 3100 includes the top major surface 3110, the bottom major surface 3120, and the first pads 3200 overlapping the second pads 3300. Each of the first pads 3200 and second pads 3300 may be electrically connected by electrically conductive paths that extend through the substrate 3100 from the top major surface 3110 to the bottom major surface 3120.

[0037] Referring back to FIG. 2, a plurality of cutting lines are determined on the patterned multilayer film, as in step 2200. The cutting lines may be determined to divide the first pads, the second pads, and the conducting paths each into four sections. In some embodiments, each section is equal. The cutting lines may be arranged along the two dimensional arrays of the top and bottom array circuits discussed above. The cutting lines may be along the first and second directions of the array discussed above. In some embodiments, the cutting lines are orthogonal. FIG. 3D is a schematic, top view diagram of a patterned multilayer film 3000. The patterned multilayer film 3000 may include the top major surface 3110, the bottom major surface 3120, the first pads 3200, and the second pads 3300. The patterned multilayer film 3000 may be patterned with a plurality of cutting lines 3400, 3500, determined to divide the first pads 3200 and second pads 3300 into four sections. In this example, the cutting lines 3400, 3500, are oriented around the x-axis and y-axis, respectively. In other embodiments, the cutting lines may divide the first pads and second pads into three sections. FIG. 3E is a schematic, sectional diagram of the patterned multilayer film 3000. An electrically conductive path 3600 from the top major surface 3110 to the bottom major surface 3120 connects the first pads 3200 and the second pads 3300, through which a cutting line 3400 is determined.

[0038] Referring again to FIG. 2, one or more flexible multilayer constructions may be singulated from the patterned multilayer film, as in step 2300. This may be done by cutting through the patterned

multilayer film, as in step 2310, such as with a dicing saw or laser. The resulting flexible multilayer construction may have a plurality of corresponding top and bottom pads connected by corresponding electrically conductive vias, each top and bottom pad extending to an edge of the multilayer construction and isolated from other top and bottom pads on the flexible multilayer construction. The singulation process of step 2300 may result in vias that are a fraction of the size of the original vias. In some embodiments, the resulting flexible multilayer constructions have first pads, second pads, and a substrate that have at least two overlapping sides and at least one overlapping vertex. FIG. 3F is a schematic, top view diagram of a flexible multilayer construction 1000 resulting from the step 2300. A plurality of top pads and a plurality of bottom pads extend to an edge of the flexible multilayer construction 1000. A plurality of top pads 300, 310, 320, 330 on a top major surface 210 of a flexible substrate 200, as well as a plurality of bottom pads 500, 510, 520, 530 on a bottom surface 220 of the flexible substrate 200, may be formed by cutting lines 3500 and 3600. FIG. 3G is a schematic, sectional view diagram of the flexible multilayer construction 1000 of FIG. 3F. A first and second top pad 300 and 330, a first and second via 400 and 430 extending from a top major surface 210 to a bottom major surface 220, and a first and second bottom pad 500 and 530 may be formed on two sides of the flexible multilayer construction 1000 by the cutting lines 3400.

[0039] FIG. 4 is a perspective diagram of a flexible multilayer construction 1000. Only one corner of the flexible multilayer construction 1000 is shown for illustration purposes. The top pad (320 of FIG. 1), via (420 of FIG. 1), and bottom pad (520 of FIG. 1) shown may be present on one or more corners on the flexible multilayer construction 1000.

[0040] In some embodiments, the flexible multilayer construction 1000 is polygonal, such as a square or triangle shape. In some embodiments, the flexible multilayer construction has a lateral dimension along each of two orthogonal lateral directions that is less than about 0.5 mm, or less than about 0.4 mm, or less than about 0.3 mm.

[0041] The common LESD mounting region may have edges 231, 232, 233, 234 that define a functional area of the common LESD mounting region. In some embodiments, the common LESD mounting region 230 and the flexible multilayer construction 1000 may be substantially coextensive and have substantially coincident parameters. In the example of FIG. 4, top pad sides 321, 322, and bottom pad sides 521, 522, extend to common LESD mounting region edges 231, 232. In some embodiments, the common LESD mounting region 230 may have a projected area of less than about 1 mm², or less than about 0.25 mm².

[0042] The flexible substrate may have a plurality of sides 241, 242, 243, 244, intersecting at a plurality of vertices 245, 246, 247, 248. Each top pad may have a plurality of sides 321, 322, 323, 324, intersecting at a plurality of vertices 325, 326, 327, 328. Each bottom pad may have a plurality of sides 521, 522, 523, 524 intersecting at a plurality of vertices 525, 526, 527, 528. In some embodiments, each top pad, bottom pad, and substrate is polygonal, such as a square, rectangle, or triangle. In other embodiments, only one side from each top pad, each corresponding bottom pad, and the substrate may overlap.

[0043] In the example of FIG. 4, substrate sides 241, 242, top pad sides 321, 322, and bottom pad sides 521, 522, overlap each other, while substrate vertex 245, top pad vertex 325, and bottom pad vertex 525

coincide with one another. In other embodiments, the substrate sides 241, 242, top pad sides 321, 322, and bottom pad sides 521, 522, may partially overlap each other. In other embodiments, at least one of the first through fourth top pads extends laterally beyond the electrically conductive pad extending from the top pad.

[0044] Each via may have a plurality of sides 421, 422, 423, 424, extending from the top pad to the bottom pad, where one or more interior sides 423, 424, may intersect the flexible substrate. In some embodiments, an interior side 423 is coincident with a minor side surface of the flexible substrate extending between the top and bottom major surfaces, while in other embodiments, two interior sides 423, 424, are each coincident with corresponding minor side surfaces of the flexible substrate extending between the top and bottom major surfaces.

[0045] Each interior side 423, 424, may form a via angle 451, 452, with the flexible substrate at the side 241, 242 of the substrate and the side 421, 422, of the via, as viewed from a minor side perspective. In this example, the via is polygonal; however, in other embodiments, the via may have one or more interior sides that are not substantially flat. For example, if a circular drill bit is used to form the electrically conductive path in step 2140 of FIG. 2, then each via would have a pie shape, with two flat sides and a curved side, and interior sides 421 and 422 would be the same side. The degree of the via angles 451, 452, formed by the interior sides 423, 424, may be related to the method and conditions of electrically conducting path formation of step 2140. In this example, via side 241 has a via angle 452 that is substantially perpendicular to top pad side 321 and bottom pad side 521, while via side 244 forms a via angle 451 having an oblique angle with the top major surface of the substrate. In some embodiments, at least one via angle 451, 452, is in a range from about 25 degrees to about 40 degrees.

[0046] The substrate vertices 245, 246, 247, 248, formed by the substrate sides 241, 242, 243, 244, may not be present on the corner of the substrate itself, as shown in FIG. 4, but rather may be present on a corner of the via. Each via may be positioned at a different substrate vertex 245, 246, 247, 248. In the example of FIG. 4, the via is positioned at substrate vertex 245 and coincides with top pad vertex 325 and bottom pad vertex 525.

[0047] FIG. 5A is a schematic, top diagram of a flexible multilayer construction 5000 having three LEDs 100, 110, 120, each mounted on a single respective top pad 300, 310, 320. Positive top pad 330 is connected to LED 100 by a first terminal connector 101, to LED 110 by a second terminal connector 111, and to a LED 120 by a third terminal connector 121. In this example, current entering the flexible multilayer construction 5000 at bottom pad 530 flows to top pad 330, through each terminal connector 101, 111, 121, to each respective LED 100, 110, 120, each respective top pad 300, 310, 320, 330, and each respective bottom pad 500, 510, 520, 530.

[0048] FIG. 5B is a schematic, sectional diagram of the flexible multilayer construction of FIG. 5A. Current travels from bottom pad 530 through via 430 to top pad 330, where it is carried by terminal connector 101 to LED 100. The circuit is completed by top pad 300, via 100, and bottom pad 500, which may be connected to a component electrically connected to bottom pad 500.

[0049] The flexible multilayer construction 5000 of FIG. 5A and FIG. 5B may be used in RGB LED systems. For example, LED 100 may be a red LED, LED 110 may be a green LED, and LED 120 may be a blue LED. Such small RGB LEDs may be particularly suitable in display devices where a high resolution is desired.

5 [0050] FIG. 5C is a schematic, top view diagram of a flexible multilayer construction 5010 having four LEDs 600, 601, 602, 603, each mounted on two respective top pads 300, 310, 320, 330. Positive top pad 310 is electrically connected to negative top pads 300 and 320 by LEDs 601 and 602, respectively. Positive top pad 330 is electrically connected to negative top pads 300 and 320 by LEDs 600 and 603, respectively. In this example, electrical current entering bottom pads 510 and 530 flows to respective top pads 310 and 330, through respective LEDs 601 and 602, and 600 and 603, respectively, and out through respective bottom pads 501 and 502, and 500 and 503, respectively.

10 [0051] FIG. 5D is a schematic, top view diagram of a flexible multilayer construction 5020 having three LEDs 610, 611, 612, each mounted on two respective top pads 300, 310, 320, 330. Positive top pad 310 is electrically connected to negative top pads 300 and 320 by LEDs 611 and 612, respectively. Positive top pad 330 is electrically connected to negative top pad 300 by LED 610. In this example, electrical current entering bottom pads 510 and 530 flows to respective top pads 310 and 330, through respective LEDs 611 and 612, and 610, respectively, and out through respective bottom pads 501 and 502, and 500, respectively.

[0052] The following are embodiments of the present disclosure:

20 [0053] Embodiment 1 is a flexible multilayer construction for mounting at least three light emitting semiconductor devices (LEDs), comprising: a flexible dielectric substrate comprising a top major surface, a bottom major surface, and a common LED mounting region on the top major surface for receiving the at least three LEDs, the common LED mounting region having a maximum projected area less than about 0.25 mm²; spaced apart electrically conductive first through fourth top pads disposed entirely within the common LED mounting region for electrically connecting to electrically conductive terminals of the at least three LEDs received in the common LED mounting region; and an electrically conductive via extending from each of the first through fourth top pads to the bottom major surface, such that when the at least three LEDs are received and electrically connected to the first through fourth top pads, each of the at least three LEDs can be independently energized.

25 [0054] Embodiment 2 is the flexible multilayer construction of embodiment 1, wherein the flexible multilayer construction and the common LED mounting region are substantially coextensive and have substantially coincident parameters.

[0055] Embodiment 3 is the flexible multilayer construction of embodiment 1, wherein each top pad extends to an edge of the common LED mounting region.

30 [0056] Embodiment 4 is the flexible multilayer construction of embodiment 1 having a lateral dimension less than about 0.5 mm along each of two orthogonal lateral directions.

[0057] Embodiment 5 is the flexible multilayer construction of embodiment 1 having a lateral dimension less than about 0.4 mm along each of two orthogonal lateral directions.

[0058] Embodiment 6 is the flexible multilayer construction of embodiment 1 having a lateral dimension less than about 0.3 mm along each of two orthogonal lateral directions.

[0059] Embodiment 7 is the flexible multilayer construction of embodiment 1, wherein the common LESD mounting region is configured to receive up to four LESDs.

5 [0060] Embodiment 8 is the flexible multilayer construction of embodiment 1, wherein the substrate and the top pads are polygonal with a plurality of sides intersecting at a plurality of vertices, such that for each top pad, two sides of the substrate fully overlap two sides of the top pad and a vertex of the substrate coincides with a vertex of the top pad.

10 [0061] Embodiment 9 is the flexible multilayer construction of embodiment 8, wherein the electrically conductive vias connect each top pad to a corresponding bottom pad disposed on the bottom major surface of the substrate, the bottom pad being polygonal with a plurality of sides intersecting at a plurality of vertices, such that for each bottom pad, two sides of the substrate fully overlap two sides of the bottom pad and a vertex of the substrate coincides with a vertex of the bottom pad.

15 [0062] Embodiment 10 is the flexible multilayer construction of embodiment 8, wherein each conductive via comprises a plurality of sides extending between corresponding top and bottom pads, at least a first side in the plurality of sides substantially perpendicular to the top and bottom major surfaces of the substrate, at least a second side in the plurality of sides making an oblique angle with one of the top and bottom major surfaces of the substrate.

20 [0063] Embodiment 11 is the flexible multilayer construction of embodiment 10, wherein the oblique angle is in a range from about 25 degrees to about 40 degrees.

[0064] Embodiment 12 is the flexible multilayer construction of embodiment 10, wherein, in a top plan view, the at least a first side is coincident with a minor side surface of the substrate extending between the top and bottom major surfaces.

25 [0065] Embodiment 13 is the flexible multilayer construction of embodiment 10, wherein the at least a first side comprises two sides of the conductive via, and wherein, in a top plan view, each of the two sides is coincident with a corresponding minor side surface of the substrate extending between the top and bottom major surfaces.

30 [0066] Embodiment 14 is the flexible multilayer construction of embodiment 8, wherein the substrate, each top pad, and each bottom pad is rectangular, such that in a plan view, each via is positioned at a different vertex of the substrate with the vertex coinciding with vertices of the top and bottom pads corresponding to the via.

35 [0067] Embodiment 15 is the flexible multilayer construction of embodiment 8, wherein the first through fourth top pads define interconnecting grooves therebetween at least partially filled with an electrically insulative reflective material having an average reflectance of at least 70% in a visible range of the spectrum.

[0068] Embodiment 16 is the flexible multilayer construction of embodiment 1, wherein at least one of the first through fourth top pads extends laterally beyond the electrically conductive pad extending from the top pad.

[0069] Embodiment 17 is an LED package, comprising: a flexible dielectric substrate comprising opposing top and bottom major surfaces and a common LED mounting region on the top major surface, the common LED mounting region having a maximum projected area less than about 1 mm²; spaced apart electrically conductive first through fourth pads disposed entirely within the common LED mounting region; an electrically conductive via extending from each of the first through fourth pads to the bottom major surface; and first through third LEDs mounted in the common LED mounting region, an electrically conductive first terminal of each LED in the first through at least third LEDs electrically connected to a different pad in the first through fourth pads, electrically conductive second terminals of at least two LEDs in the first through third LEDs electrically connected to a same pad in the first through fourth pads, such that each of the first through third LED is independently energizable.

[0070] Embodiment 18 is the LED package of embodiment 17, wherein the first terminal of each LED is connected to a different pad in the first through third pads, and the second terminals of all three LEDs are connected to the fourth pad.

[0071] Embodiment 19 is a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LEDs), comprising: a flexible dielectric polygonal substrate having a plurality of sides intersecting at a plurality of vertices and comprising top and bottom major surfaces; a plurality of spaced apart electrically conductive top pads disposed on the top major surface of the substrate; a plurality of spaced apart electrically conductive bottom pads disposed on the bottom major surface of the substrate; and a plurality of electrically conductive vias extending between corresponding top and bottom pads, such that for each corresponding top and bottom pad: the top and bottom pads are each polygonal having a plurality of sides intersecting at a plurality of vertices, a first vertex of the top pad coincident with a first vertex of the bottom pad and a first vertex of the substrate, the sides of the top and bottom pads and the substrate intersecting at the first vertex and partially overlapping one another.

[0072] Embodiment 20 is a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LEDs), comprising: a flexible dielectric substrate comprising top and bottom major surfaces; and pluralities of corresponding electrically conductive top and bottom pads disposed on the top and bottom major surfaces, respectively, an electrically conductive via connecting each pair of corresponding top and bottom pads, a side of each top pad partially overlapping a side of the corresponding bottom pad and a side of the substrate, such in a plan view, each top pad fully overlaps the corresponding bottom pad.

[0073] Embodiment 21 is an LED package comprising four LEDs mounted on the flexible multilayer construction of embodiment 20.

[0074] Embodiment 22 is a method of fabricating a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LEDs), comprising the steps of: forming a patterned multilayer film, comprising: providing a flexible substrate having opposing top and bottom major surfaces; forming a plurality of spaced apart electrically conductive first pads on the top major surface of the flexible substrate; forming a plurality of spaced apart electrically conductive second pads on the bottom major surface of the flexible substrate in a one to one correspondence with the first pads; and

forming an electrically conductive path between corresponding first and second pads through the flexible substrate; and determining a plurality of cutting lines on the patterned multilayer film, the cutting lines dividing the first and second pads in each corresponding first and second pads and the conductive path connecting the first and second pads each into four sections; and singulating a flexible multilayer construction by cutting through the patterned multilayer film along the determined cutting lines, resulting in the flexible multilayer construction having a plurality of corresponding top and bottom pads connected by corresponding electrically conductive vias, each top and bottom pad extending to a side of the flexible multilayer construction.

[0075] Embodiment 23 is the method of embodiment 22, wherein the first and second pads are arranged in a two-dimensional regular array along different first (x) and second (y) directions.

[0076] Embodiment 24 is the method of embodiment 23, wherein the first and second directions are orthogonal to one another.

[0077] Embodiment 25 is the method of embodiment 23, wherein the cutting lines are along the first and second directions.

[0078] Embodiment 26 is the method of embodiment 22, wherein the steps of fabricating a flexible multilayer construction are carried out sequentially.

[0079] Embodiment 27 is the method of embodiment 22, wherein the cutting lines divide the first and second pads in each corresponding first and second pads and the conductive path connecting the first and second pads each into four substantially equal sections.

[0080] Embodiment 28 is the method of embodiment 22, wherein for each corresponding first and second pads, the first pad is larger, the second pad is smaller, and in a plan view, the second pad is centered inside the first pad.

[0081] Embodiment 29 is the method of embodiment 22, wherein the electrically conductive paths are vias filled with electrically conductive material.

[0082] Various embodiments of the invention have been described. These and other embodiments are within the scope of the following claims.

CLAIMS:

1. A flexible multilayer construction for mounting at least three light emitting semiconductor devices (LESDs), comprising:

5 a flexible dielectric substrate comprising a top major surface, a bottom major surface, and a common LESD mounting region on the top major surface for receiving the at least three LESDs, the common LESD mounting region having a maximum projected area less than about 0.25 mm^2 ;

spaced apart electrically conductive first through fourth top pads disposed entirely within the common LESD mounting region for electrically connecting to electrically conductive terminals of the at least three LESDs received in the common LESD mounting region; and

10 an electrically conductive via extending from each of the first through fourth top pads to the bottom major surface, such that when the at least three LESDs are received and electrically connected to the first through fourth top pads, each of the at least three LESDs can be independently energized.

15 2. The flexible multilayer construction of claim 1, wherein the flexible multilayer construction and the common LESD mounting region are substantially coextensive and have substantially coincident perimeters.

3. The flexible multilayer construction of claim 1, wherein each top pad extends to an edge of the common LESD mounting region.

4. The flexible multilayer construction of claim 1, wherein the common LESD mounting region is configured to receive up to four LESDs.

25 5. The flexible multilayer construction of claim 1, wherein at least one of the first through fourth top pads extends laterally beyond the electrically conductive pad extending from the top pad.

6. An LESD package, comprising:

30 a flexible dielectric substrate comprising opposing top and bottom major surfaces and a common LESD mounting region on the top major surface, the common LESD mounting region having a maximum projected area less than about 1 mm^2 ;

spaced apart electrically conductive first through fourth pads disposed entirely within the common LESD mounting region;

35 an electrically conductive via extending from each of the first through fourth pads to the bottom major surface; and

first through third LESDs mounted in the common LESD mounting region, an electrically conductive first terminal of each LESD in the first through at least third LESDs electrically connected to a different pad in the first through fourth pads, electrically conductive second terminals of at least two

LESDs in the first through third LEDS electrically connected to a same pad in the first through fourth pads, such that each of the first through third LEDS is independently energizable.

7. The LEDS package of claim 6, wherein the first terminal of each LEDS is connected to a different pad in the first through third pads, and the second terminals of all three LEDS are connected to the fourth pad.

8. A flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LESDs), comprising:

a flexible dielectric polygonal substrate having a plurality of sides intersecting at a plurality of vertices and comprising top and bottom major surfaces;

a plurality of spaced apart electrically conductive top pads disposed on the top major surface of the substrate;

a plurality of spaced apart electrically conductive bottom pads disposed on the bottom major surface of the substrate; and

a plurality of electrically conductive vias extending between corresponding top and bottom pads, such that for each corresponding top and bottom pad:

the top and bottom pads are each polygonal having a plurality of sides intersecting at a plurality of vertices, a first vertex of the top pad coincident with a first vertex of the bottom pad and a first vertex of the substrate, the sides of the top and bottom pads and the substrate intersecting at the first vertex and partially overlapping one another.

9. A flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LESDs), comprising:

a flexible dielectric substrate comprising top and bottom major surfaces; and

pluralities of corresponding electrically conductive top and bottom pads disposed on the top and bottom major surfaces, respectively, an electrically conductive via connecting each pair of corresponding top and bottom pads, a side of each top pad partially overlapping a side of the corresponding bottom pad and a side of the substrate, such in a plan view, each top pad fully overlaps the corresponding bottom pad.

10. A method of fabricating a flexible multilayer construction for mounting a plurality of light emitting semiconductor devices (LESDs), comprising the steps of:

forming a patterned multilayer film, comprising:

providing a flexible substrate having opposing top and bottom major surfaces;

forming a plurality of spaced apart electrically conductive first pads on the top major surface of the flexible substrate;

forming a plurality of spaced apart electrically conductive second pads on the bottom major surface of the flexible substrate in a one to one correspondence with the first pads; and

forming an electrically conductive path between corresponding first and second pads through the flexible substrate; and

determining a plurality of cutting lines on the patterned multilayer film, the cutting lines dividing the first and second pads in each corresponding first and second pads and the conductive path connecting the first and second pads each into four sections; and

singulating a flexible multilayer construction by cutting through the patterned multilayer film along the determined cutting lines, resulting in the flexible multilayer construction having a plurality of corresponding top and bottom pads connected by corresponding electrically conductive vias, each top and bottom pad extending to a side of the flexible multilayer construction.

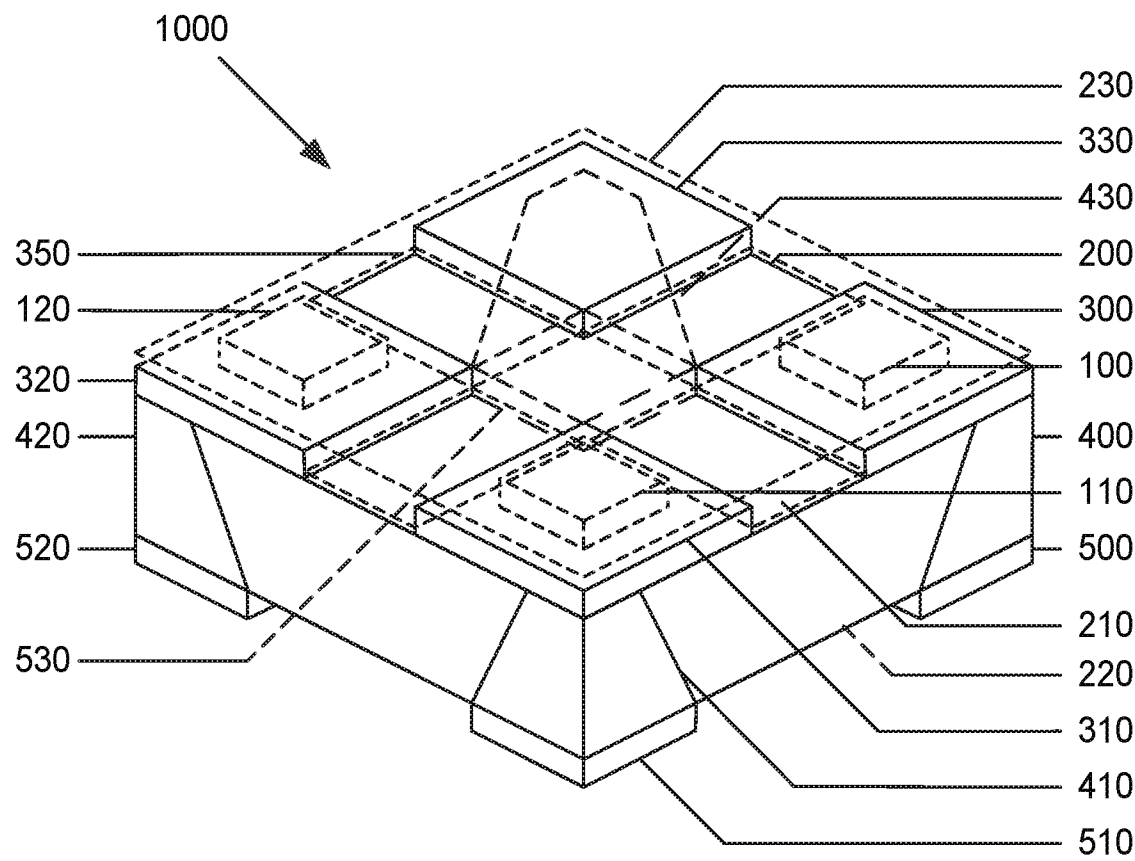


FIG. 1

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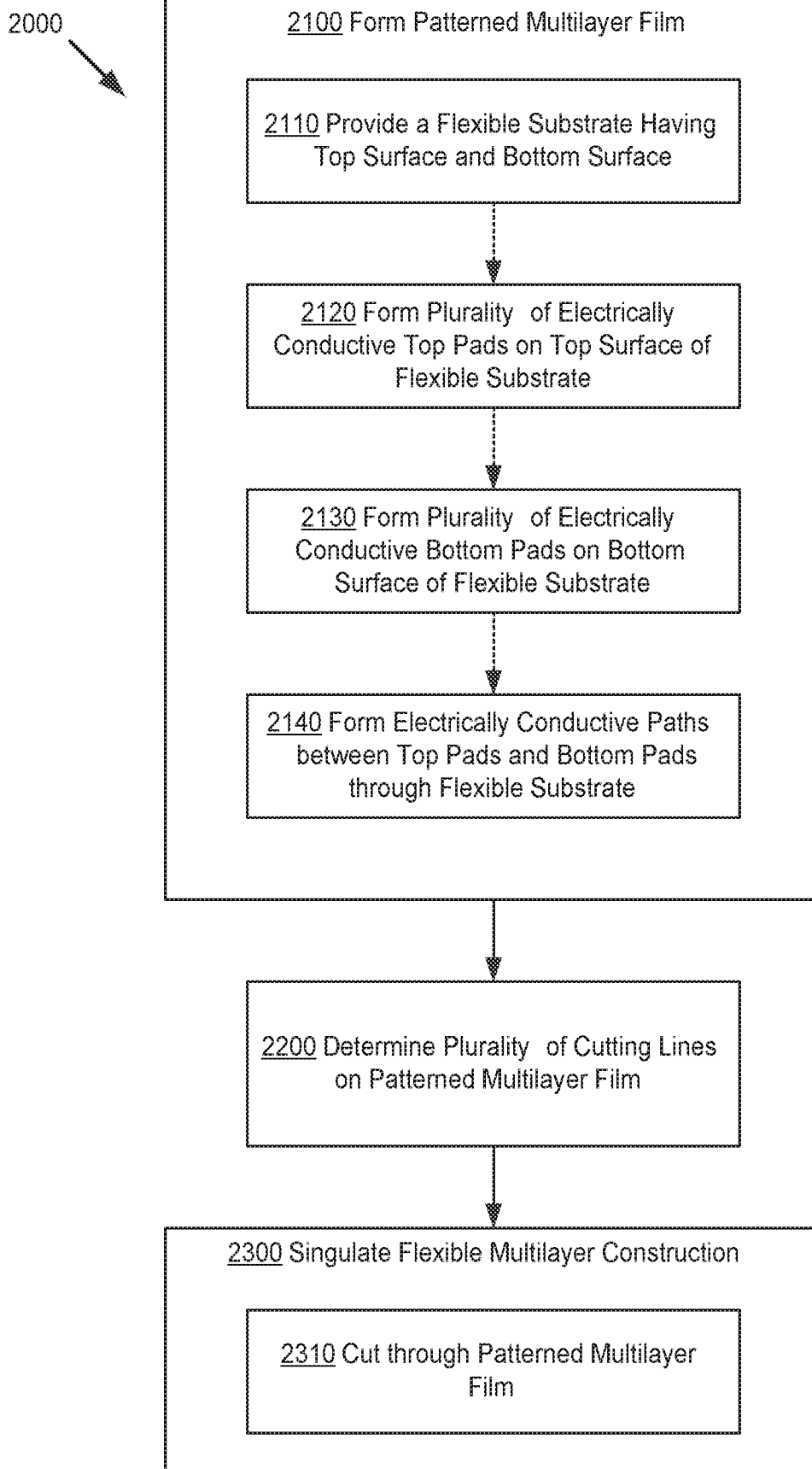


FIG. 2

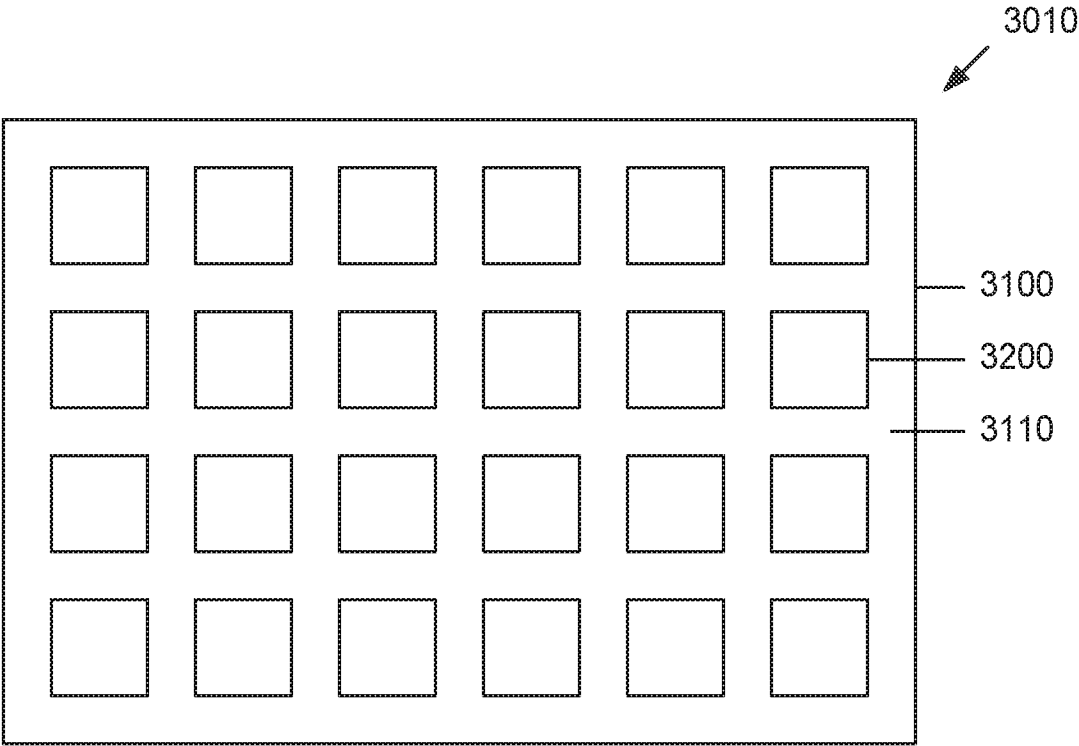


FIG. 3A

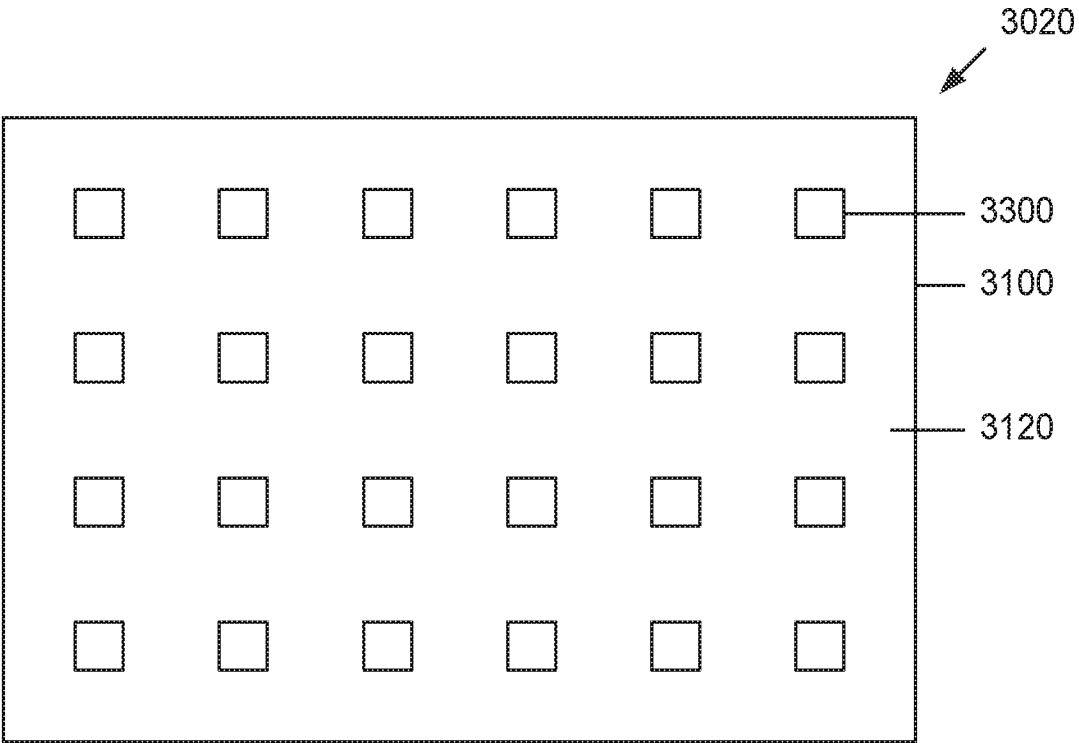


FIG. 3B

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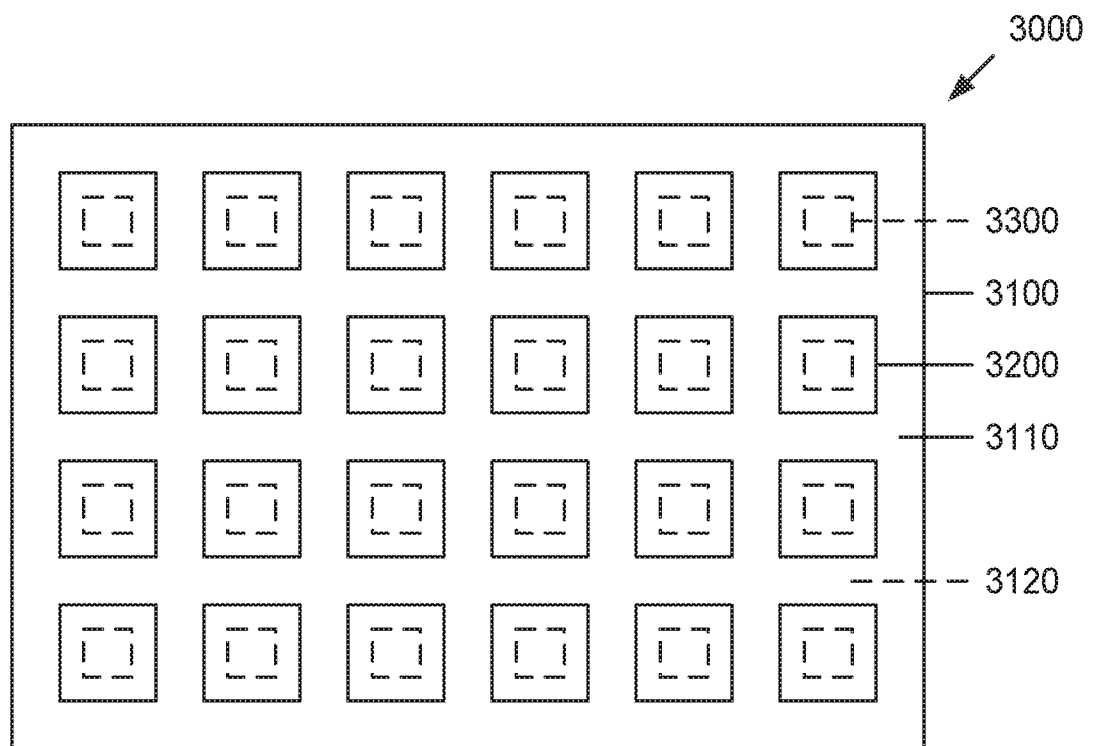


FIG. 3C

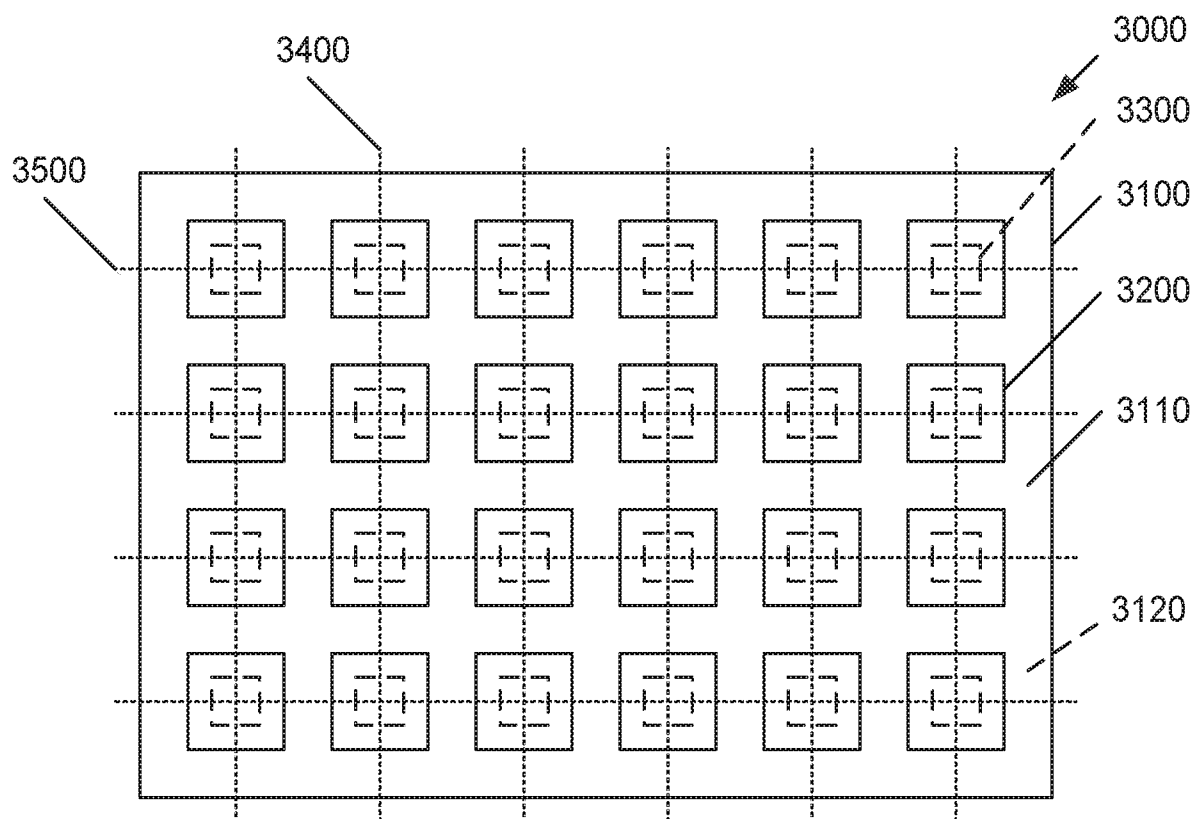


FIG. 3D

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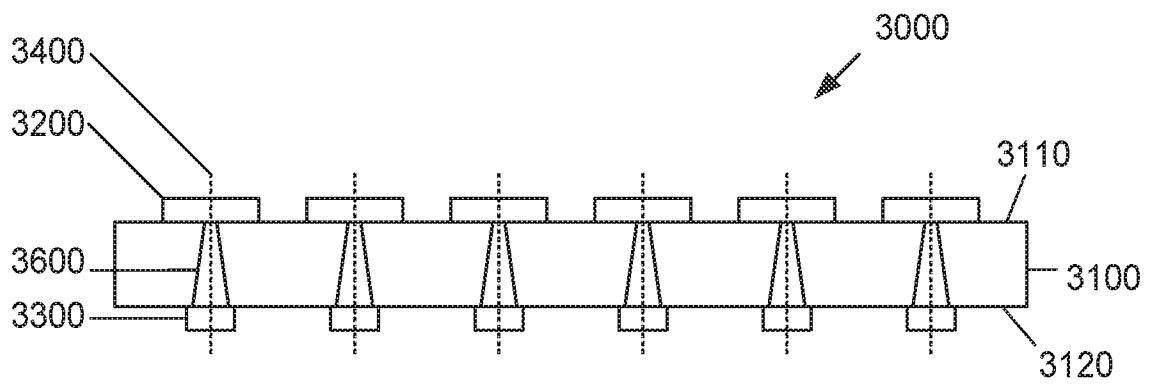


FIG. 3E

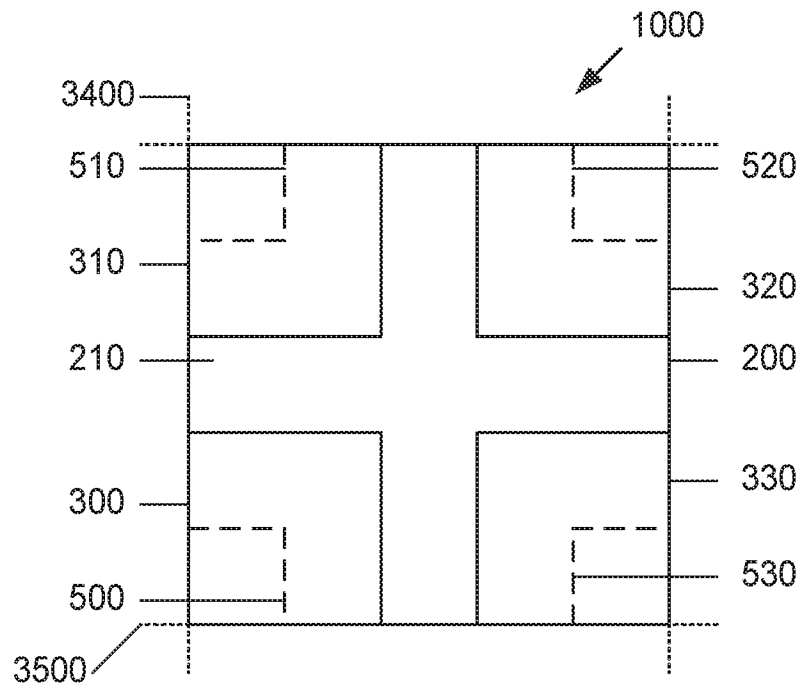


FIG. 3F

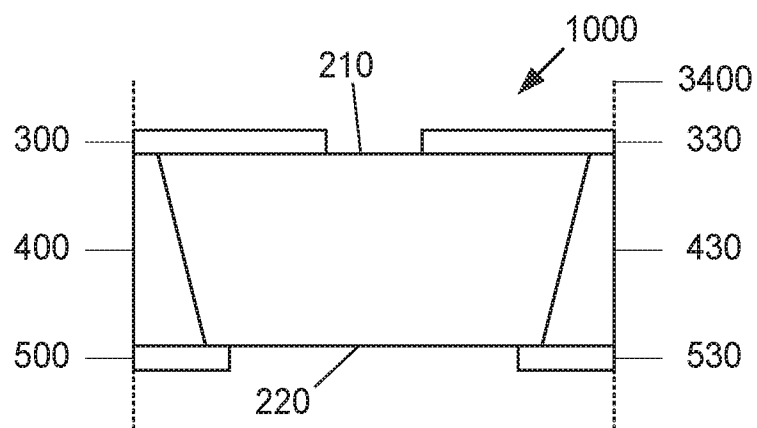
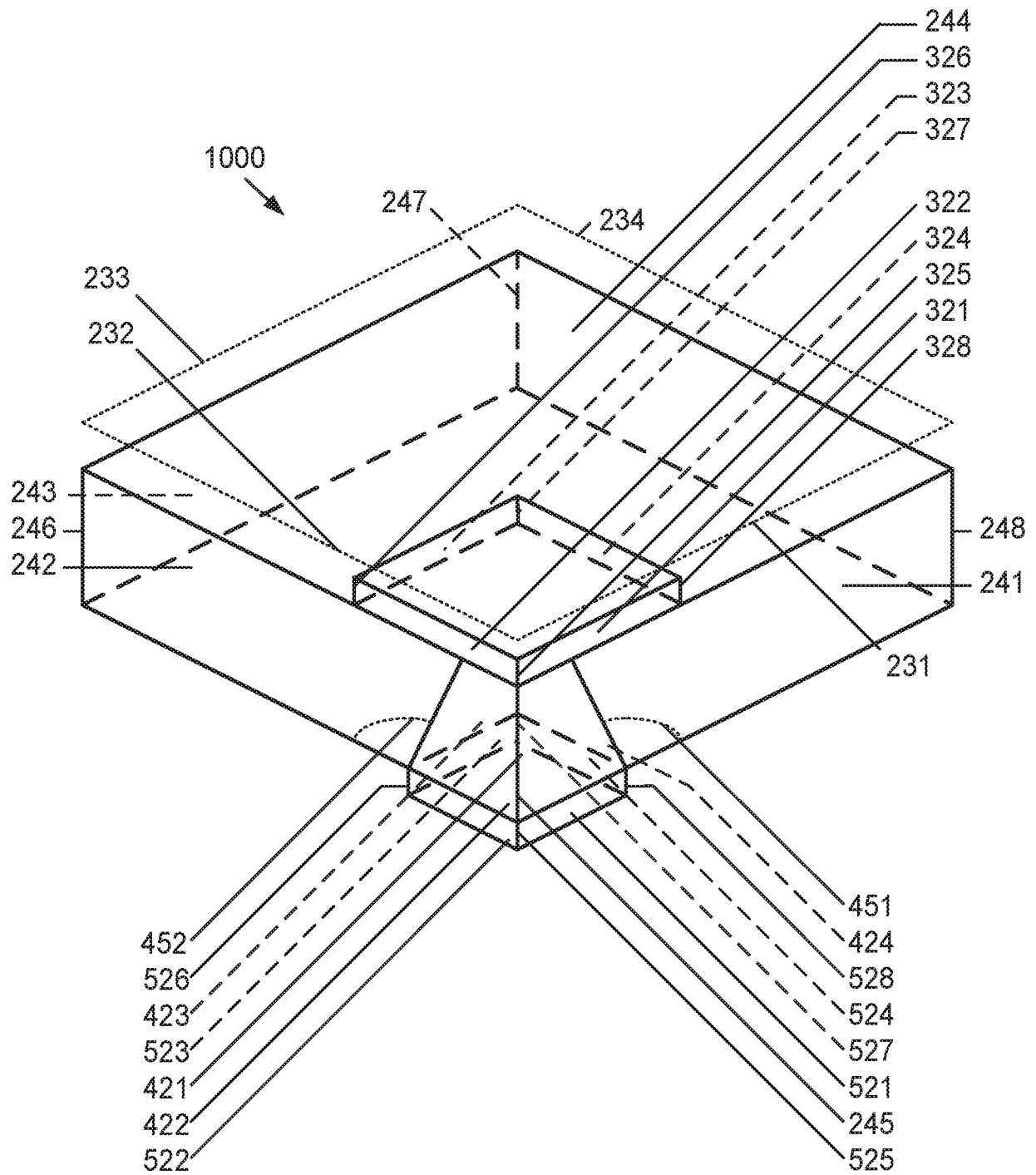


FIG. 3G

*FIG. 4*

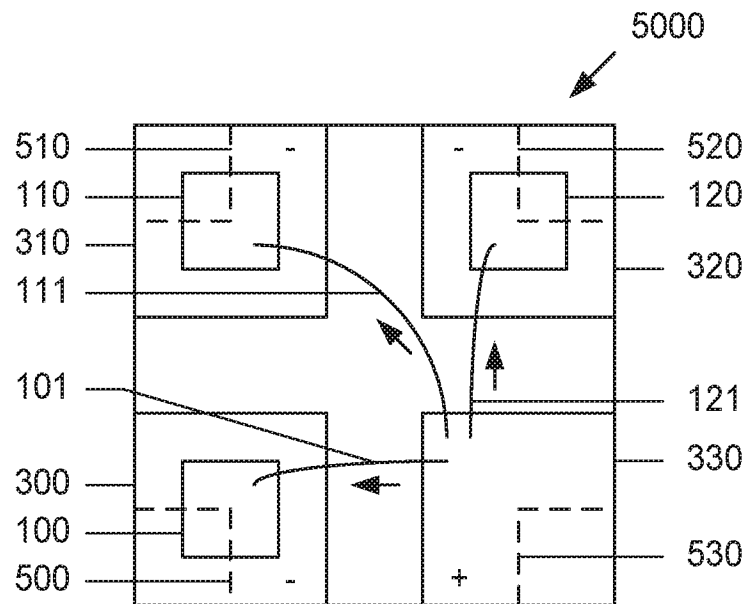


FIG. 5A

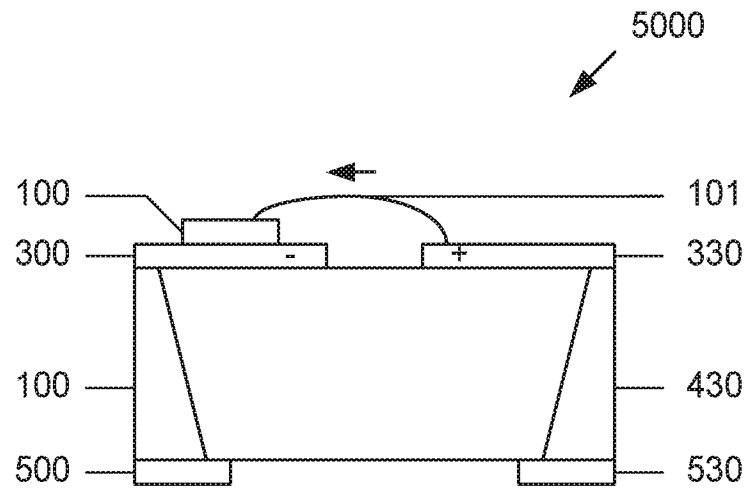


FIG. 5B

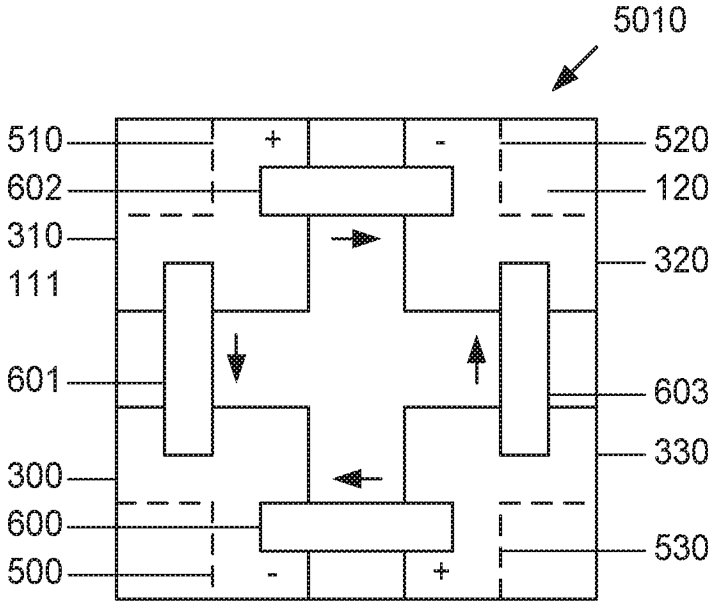


FIG. 5C

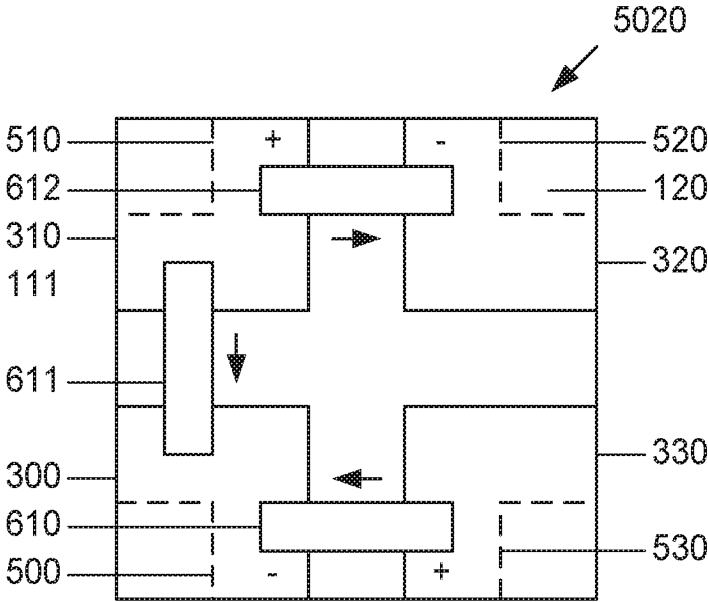


FIG. 5D

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/041655

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L25/075 H01L33/62 H05K3/40 H05K3/32 H05K1/18 H05K1/11 ADD. According to International Patent Classification (IPC) or to both national classification and IPC																				
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L H01K H05K Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data																				
C. DOCUMENTS CONSIDERED TO BE RELEVANT <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>EP 2 824 707 A1 (EVERLIGHT ELECTRONICS CO LTD [TW]) 14 January 2015 (2015-01-14)</td> <td>1-9</td> </tr> <tr> <td>Y</td> <td>paragraph [0072]</td> <td>10</td> </tr> <tr> <td>Y</td> <td>----- JP 2006 156643 A (CITIZEN ELECTRONICS) 15 June 2006 (2006-06-15) paragraph [0024] figures 4,6,7</td> <td>10</td> </tr> <tr> <td>X</td> <td>----- US 2010/259930 A1 (YAN XIANTAO [US]) 14 October 2010 (2010-10-14) paragraphs [0038], [0047]</td> <td>1-5</td> </tr> <tr> <td>X</td> <td>----- EP 2 930 748 A1 (LITE ON OPTO TECHNOLOGY CHANGZHOU CO LTD [CN]; LITE ON TECHNOLOGY CORP) 14 October 2015 (2015-10-14) paragraph [0015] figures 1,2,3,6 ----- -/-</td> <td>1-5</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	X	EP 2 824 707 A1 (EVERLIGHT ELECTRONICS CO LTD [TW]) 14 January 2015 (2015-01-14)	1-9	Y	paragraph [0072]	10	Y	----- JP 2006 156643 A (CITIZEN ELECTRONICS) 15 June 2006 (2006-06-15) paragraph [0024] figures 4,6,7	10	X	----- US 2010/259930 A1 (YAN XIANTAO [US]) 14 October 2010 (2010-10-14) paragraphs [0038], [0047]	1-5	X	----- EP 2 930 748 A1 (LITE ON OPTO TECHNOLOGY CHANGZHOU CO LTD [CN]; LITE ON TECHNOLOGY CORP) 14 October 2015 (2015-10-14) paragraph [0015] figures 1,2,3,6 ----- -/-	1-5
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Date of the actual completion of the international search 12 October 2017		Date of mailing of the international search report 25/10/2017																		
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Gijsbertsen, Hans																		

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2017/041655

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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Information on patent family members

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