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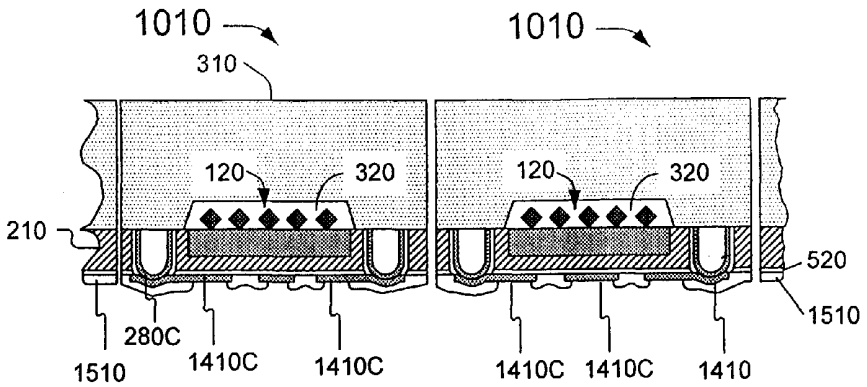
(54) Title: DEVICES HAVING SUBSTRATES WITH OPENINGS PASSING THROUGH THE SUBSTRATES AND CONDUCTORS IN THE OPENINGS, AND METHODS OF MANUFACTURE



(57) Abstract: In some embodiments, a fabrication method comprises: forming a structure that has one or more substrates (210, 310), wherein the one or more substrates are either a single substrate or a plurality of substrates bonded together, wherein the structure comprises a non-electronically-functioning component (120) which includes at least a portion of the one or more substrates and/or is attached to the one or more substrates (210); wherein the one or more substrates include a first substrate (210) which has: a first side, an opening (260) in the first side, and a conductor (280) in the opening; wherein the method comprises removing material from the structure so that the conductor becomes exposed on a second side of the first substrate. In some embodiments, the second side is a backside of the first substrate, and the exposed conductor provides backside contact pads. In some embodiments, the fabrication method comprises: forming a structure comprising a first substrate (210) which has: a first side, an opening (260) in the first side, and a conductor (280) in the opening; removing material from the structure so that the conductor becomes exposed on a second side of the first substrate; wherein removing of the material comprises removing the material from a first portion of the second side of the first substrate to cause the first portion to be recessed relative to a second portion of the second side of the first substrate. Devices are also provided.

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DEVICES HAVING SUBSTRATES WITH OPENINGS PASSING THROUGH THE SUBSTRATES AND CONDUCTORS IN THE OPENINGS, AND METHODS OF MANUFACTURE

BACKGROUND OF THE INVENTION

The present invention relates to devices having substrates with openings passing through the substrates and conductors in the openings. Some devices of the invention incorporate non-electronically-functioning components. Examples include micro-electro-mechanical systems (MEMS) and other micro-structure-technology (MST) structures.

Integrated circuit fabrication technology has been used to create micro-electro-mechanical and micro-electro-optical structures. Examples of such structures include relays, micropumps, and optical devices for fingerprint recognition. Fig. 1 illustrates one such structure 120 formed on a semiconductor die ("chip") 130. The die contains electronic circuitry (not shown) and interconnect lines (not shown) which couple the structure 120 to contact pads 140. The die has been fabricated in a batch process with other such dies on a semiconductor wafer. After the die was separated from the wafer by dicing, bond wires 150 were bonded to the contact pads 140 and lead frame pins 160. Then the lead frame was encapsulated into a ceramic substrate 170, with pins 160 protruding from the substrate. Another substrate 180 was bonded to substrate 170 to protect the die and the structure 120. If the structure 120 is an optical device (e.g. a mirror or an optical sensor), the substrate 180 is made of a suitable transparent material, e.g. glass.

Improved fabrication techniques and structures suitable for such devices are desirable. It is also desirable to increase the mechanical strength of devices with or without non-electrically functioning components.

SUMMARY

Some embodiments of the present invention combine techniques for fabricating micro-electro-mechanical and micro-electro-optical structures with backside contact fabrication technology used for vertical integration and described in PCT publication WO 98/19337 (TruSi Technologies, LLC, May 7, 1998).

The invention is not limited to such embodiments. In some embodiments, a fabrication method comprises:

forming a structure that has one or more substrates, wherein the one or more substrates are either a single substrate or a plurality of substrates bonded together, wherein the structure comprises a non-electronically-functioning component which includes at least a portion of the one or more substrates and/or is attached to the one or more substrates;

wherein the one or more substrates include a first substrate which has: a first side, an opening in the first side, and a conductor in the opening;

wherein the method comprises removing material from the structure so that the conductor becomes exposed on a second side of the first substrate.

In some embodiments, the second side is a backside of the first substrate, and the exposed conductor provides backside contact pads. The front side of the first substrate can be bonded to another substrate or substrates which protect the non-electronically-functioning component during processing, including the processing that exposes the conductor. The component is also protected during dicing. The other substrate or substrates can be transparent as needed in the case of an optical component. The other substrate or substrates can be closely positioned to the component to reduce optical distortion. Also, small system area can be achieved.

In some embodiments, the fabrication method comprises:

forming a structure comprising a first substrate which has: a first side, an opening in the first side, and a conductor in the opening;

removing material from the structure so that the conductor becomes exposed on a second side of the first substrate;

wherein removing of the material comprises removing the material from a first portion of the second side of the first substrate to cause the first portion to be recessed relative to a second portion of the second side of the first substrate.

The resulting structure may or may not have a non-electronically-functioning component. In some embodiments, the first substrate is thicker at the second portion than at the first portion. The thicker second portion improves the mechanical strength of the structure.

Other features and advantages of the invention are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a vertical cross-sectional view of a prior art device having a micro-electro-mechanical or micro-electro-optical structure.

Figs. 2A, 2B, and 3-16 are vertical cross-sectional views of devices with non-electronically-functioning components at different stages of fabrication according to the present invention.

Figs. 17 and 18 are bottom views of devices having non-electronically-functioning components according to the present invention.

Figs. 19-25 are vertical cross-sectional views of devices having non-electronically-functioning components at different stages of fabrication according to the present invention.

Fig. 26 is a bottom view of a device with non-electronically-functioning components according to the present invention.

Figs. 27-29 are vertical cross-sectional views of devices with non-electronically-functioning components at different stages of fabrication according to the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 2A illustrates miniature structures 120 fabricated in and/or on a wafer 210. Structures 120 include optical, mechanical, magnetic, and/or other kinds of non-electronically-functioning components. Non-electronically-functioning components may or may not have electronic circuitry (e.g. transistors), but their operation includes functionality not present in traditional electronic circuitry. For example, a non-

electronically-functioning component may have to move or deform during operation. Examples of such components are diaphragms of micropumps and moving parts of micro-mechanical switches. The component may emit and/or sense visible or invisible light (electromagnetic radiation). See J.E. Gulliksen, "MST vs. MEMS: WHERE ARE WE?", Semiconductor Magazine, Oct. 2000, Vol. 1, No. 10. The component may be a mirror or a lens. Such components may be present in devices for fingerprint recognition, optical disc readers, bar code readers, or other MEMS and MST structures. A component may interact with an external magnetic field. The invention is not limited to any particular kind of components. The invention provides techniques that may be used with components not yet invented.

The non-electronically-functioning components of structures 120 may include parts of substrate 210. The components may also include released components, i.e. components originally manufactured on another substrate (not shown) and then released from that substrate. See e.g. U.S. Patent 6,076,256 (released mirrors).

Structures 120 can be coupled to circuitry 220 fabricated in and/or on substrate 210. Circuitry 220 may be used in operation of the non-electronically-functioning components. The circuitry may control the components or receive signals indicative of the state of the components. Circuitry 220 may include amplifiers, filters, or any other electronic circuitry. Substrate 210 can be made from a suitable semiconductor material, for example, silicon. In some embodiments, circuitry 220 contains only interconnect lines. In some of these embodiments, substrate 210 is made from a non-semiconductor material, for example, a dielectric polymer or glass.

Circuitry 220 and/or structures 120 are connected to contact structures 230. One structure 230 is shown on a larger scale in Fig. 2B. Structures 230 can be fabricated as described, for example, in PCT publication WO 98/19337 (TruSi Technologies, LLC, May 7, 1998); U.S. Patent No. 6,184,060, issued February 6, 2001; and U.S. Patent No. 6,322,903 issued November 27, 2001; all of which are incorporated herein by reference. Briefly, vias 260 are etched in substrate 210. Insulator 270 is formed in the vias. Conductor 280 (for example, metal) is formed over the insulator 270. Optionally, another material 290 is formed over the conductor 280 to fill the vias.

Insulator 270 can be omitted if wafer 210 is made from an insulating material. Also, the vias can be filled with conductor 280.

Structures 120, circuitry 220, and contact structures 230 can be fabricated in any order. For example, circuitry 220 can be made first, contact structures 230 can be made next, and the structures 120 can be made last. Alternatively, the steps forming the elements 230, 220, 120 can be interleaved, and the same steps can be used to form more than one of these elements.

Fig. 3 shows a wafer 310 which will be bonded to wafer 210. Cavities 320 have been formed in the wafer. Alignment marks (not shown) can be formed on substrate 310 on the same or opposite side as cavities 320. In one embodiment, wafer 310 is glass polished on top and bottom. In some embodiments, wafers 310 and 210 are made of the same material (for example, silicon) to match their thermal expansion coefficients.

Cavities 320 and the alignment marks can be formed by conventional processes. See for example, U.S. Patent 6,097,140 (glass etch).

Wafers 310, 210 are bonded together (Fig. 4). Structures 120 become positioned in cavities 320. The wafers can be bonded by conventional techniques, for example, with an adhesive or a glass frit in vacuum. Before the adhesive is deposited, and even before the structures 120 are attached to wafer 210, portions of wafer 210 can be covered with an insulating material to insulate the wafer from the adhesive.

The wafers can also be bonded by solder bonding, eutectic bonding, thermocompression, with epoxy, and by other techniques, known or to be invented.

Then the backside 210B of wafer 210 (the side opposite to the side bonded to wafer 310) is processed to expose the contacts 280C formed by the conductor 280 at the bottom of vias 260. This processing can be performed by methods described in U.S. patent 6,322,903 and PCT application WO 98/19337. According to one such method, substrate 210 and insulator 270 are etched by an atmospheric pressure plasma etch to expose the contacts 280C. Then an insulator 520 (Fig. 6) is grown selectively on silicon 210 but not on conductor 280.

According to another method, after the conductor 280 has been exposed by the etch of substrate 210 and insulator 270, the structure is turned upside down (Fig. 7), and

insulator 520 is deposited by a spin-on or spraying process and then cured. Insulator 520 can be polyimide, glass, or some other flowable material (for example, a flowable thermosetting polymer.) The top surface of layer 520 is substantially planar, or at any rate the layer 520 is thinner over contact structures 230 than elsewhere. In some embodiments, layer 520 does not cover the contacts 280C. If needed, layer 520 can be etched with a blanket etch to adequately expose the contacts 280C (e.g., if insulator 520 covered the contacts). The etch does not expose the substrate 210. The resulting wafer structure is like that of Fig. 5.

According to another method, the etch of substrate 210 exposes the insulator 270 but not the conductor 280. See Fig. 8. Insulator 270 protrudes from the substrate surface. The wafer structure is turned upside down (Fig. 8), and insulating layer 520 is formed as described above in connection with Fig. 7. Layer 520 is thinner over the contact structures 230 than elsewhere. In some embodiments, layer 520 does not cover the contact structures. If needed, layer 520 can be etched with a blanket etch to adequately expose the insulator 270 (Fig. 9). Then insulator 270 is etched selectively to insulator 520 to expose the conductor 280. In some embodiments, insulator 270 is silicon dioxide and insulator 520 is polyimide. The resulting wafer structure is like that of Fig. 6.

One advantage of the processes of Figs. 5-9 is that no photolithography is required. Other techniques, including techniques involving photolithography, can also be used.

The wafer structure is diced into individual chips 1010 (Fig. 10). The structures 120 are protected by the substrates 210, 310 during dicing.

Chips 1010 can be attached to a wiring substrate (not shown), for example, a printed circuit board (PCB). Contacts 280C can be directly attached to the wiring substrate using flip chip technology. See the aforementioned U.S. patent 6,322,903. Alternatively, chips 1010 can be turned upside down, with the contacts 280C facing up, and the chips can be wire bonded to a lead frame and packaged using conventional technology. Ball grid arrays, chip scale packages, and other packaging technologies, known or to be invented, can be used.

Advantageously, after wafers 210, 310 have been bonded together, the structures 120 and circuitry 220 are protected by the two wafers. The area is small because the

substrate 310 does not extend around the substrate 210 as in Fig. 1. Cavities 320 can be made shallow so that the substrate 310 can be positioned close to structures 120. This is advantageous for optical applications because optical distortion is reduced. Further, since substrate 310 is placed directly on substrate 210, precise positioning of substrate 310 relative to structures 120 is facilitated.

For optical applications, substrate 310 can be covered by non-reflective coatings. Cavities 320 can be filled with refractive index matching materials. Lenses can be etched in substrate 310.

Substrate 310 may contain electronic circuitry coupled to structures 120 and/or circuitry 220. Substrate 310 can be fabricated from insulating or semiconductor materials. U.S. patent 6,322,903 describes some techniques that can be used to connect circuitry in substrate 310 to circuitry 220.

Fig. 11 illustrates an embodiment in which the backside contacts are redistributed along the backside 210B of wafer 210 to obtain an area matched package. After the stage of Fig. 4, mask 1110 is formed on the backside 210B of substrate 210 and photolithographically patterned. Optionally, before the mask is formed, substrate 210 can be thinned from backside 210B, but the insulator 270 does not have to be exposed. The thinning can be performed by mechanical grinding, plasma etching, or other methods, known or to be invented.

Substrate 210 and insulator 270 are etched selectively to mask 1110 to expose contact portions 280C of conductor 280 on backside 210B (Fig. 12). Suitable etching processes are described above in connection with Fig. 5. Then mask 1110 is stripped, and insulating layer 520 (Fig. 13) is formed selectively on backside 210B of substrate 210 but not on conductor 280. See the description above in connection with Fig. 6.

Conductive layer 1410 (Fig. 14), for example, a metal suitable for integrated circuit bond pads, is deposited and patterned on the wafer backside to provide conductive pads 1410C and conductive lines connecting these pads to conductor 280. Then a suitable insulator 1510 (Fig. 15) is deposited and patterned to expose the conductive pads 1410C.

Then the wafer structure is diced (Fig. 16). Pads 1410C of the resulting chips 1010 can be attached directly to a wiring substrate, for example, a PCB. The bottom view of a single chip 1010 is shown in Fig. 17. Fig. 17 also shows an outline of mask 1110 of Fig. 11.

One advantage of the embodiment of Figs. 11-17 is as follows. The position of contact structures 230 is limited by the layout of circuitry 220 and structures 120. For example, the contact structures 230 may have to be restricted to the periphery of chips 1010. Since contacts 280C are not directly attached to a wiring substrate, their size can be reduced. The size of contact pads 1410C is sufficiently large to allow direct attachment to a wiring substrate, but the position of contact pads 1410C is not restricted by circuitry 220 and structures 120. The chip area can therefore be smaller.

In Fig. 18, the mask 1110 has four extensions 1110E extending to the boundary (e.g. corners) of chip 1010. These extensions increase the mechanical strength of the chip. The extensions may come as close, or closer, to the chip boundary as the contacts 280C. In some embodiments, the extensions reach the chip boundary and merge with the extensions on the adjacent chips. The extensions may extend between the contacts. More or fewer than four extensions can be provided.

The extensions can be formed in structures that do not have non-electronically-functioning components.

In another embodiment, the wafer structure is processed to the stage of Fig. 6 by any of the methods described above in connection with Figs. 5-9. Then conductive layer 1410 (Fig. 19) is deposited and patterned on backside 210B over insulator 520 to form contact pads 1410C and conductive lines connecting the contact pads to conductor 280, as described above in connection with Fig. 14. Mask 1110 is not used. Then insulator 1510 is deposited and patterned to expose the contact pads 1410C, as described above in connection with Fig. 15.

The wafer structure is tested and diced to form individual chips 1010 (Fig. 20).

Fig. 21 illustrates alternative processing of wafer 310. No cavities are etched in the wafer. Stand-off features 2110 are formed on the wafer surface. Features 2110 can be formed by depositing an appropriate material and patterning the material

photolithographically, or by silk-screen printing, or by dispensing the material using a needle, or by other techniques, known or to be invented. Suitable materials include epoxy, thermosetting polymers, glass frit.

Wafer 210 is processed as in Fig. 3. Then wafers 310, 210 are aligned and bonded as shown in Fig. 22. Stand-off features 2110 are bonded to wafer 210. Structures 120 are located between the stand-off features. Then the wafer structure is processed by any of the methods described above in connection with Figs. 5-20.

In the embodiment of Fig. 22, material 2110 is used to fill the vias 260. Material 290 that fills the vias in Fig. 2B is absent in Fig. 22, or is used to fill the vias only partially. Material 2110 is not fully hardened when the wafers are bonded. Material 2110 fills the vias 260 during the bonding process. The bonding is performed in vacuum to make it easier for the material 2110 to fill the vias 260.

In some embodiments in which the bonding process starts before the material 2110 is hardened, spacers are formed on wafer 310 or 210, or both, to maintain a minimum distance between the two wafers to prevent the wafer 210 from damaging the structures 120. The spacers can be fixed hard features formed on the wafers. Alternatively, the spacers can be hard balls 2120 floating in material 2110. The balls can be made of glass, resin, or some other suitable material (possibly a dielectric). Balls 2120 maintain the minimum distance between the wafers 310, 210 when the wafers are bonded together. An exemplary diameter of balls 2120 is 10-30 μm. The diameter is determined by the distance to be maintained between the two wafers. See U.S. Patent 6,094,244, issued July 25, 2000.

In some embodiments, the stand-off features 2110 completely surround the structures 120 and maintain the vacuum in the regions in which the structures 120 are located. The vacuum helps to hermetically isolate the structures 120 when the ambient pressure increases to atmospheric pressure. The strength of the bond between the two wafers is also improved.

In some embodiments, the material 2110 is deposited on wafer 210 rather than wafer 310.

In some embodiments, the material 2110 covers and contacts the structures 120.

In some embodiments, the material 2110 is hardened before the wafers are bonded, and is not used to fill the vias 260.

In Fig. 23, structures 120 do not protrude from the top surface of substrate 210. No cavities or stand-off features are made on wafer 310. This provides close positioning between the substrate 310 and structures 120. This is particularly advantageous if the structures 120 have optical components.

In Figs. 24-26, at least some of the contact structures 230 are positioned on the chip boundaries (on the dicing lines). In other respects, fabrication can proceed according to any method described above in connection with Figs. 5-23. Fig. 24 illustrates the wafer structure processed as in Fig. 4. Fig. 25 illustrates the structure after dicing. Fig. 26 is a bottom view of a resulting chip 1010. One advantage of placing the contact structures 230 on the chip boundaries is reduced area. Also, the contact structures 230 can be contacted on a side of the chip, especially if the material 290 is conductive or is omitted. If the wafer structure is processed as in Fig. 16 or 20, contacts 1410C are available on the backside while contact structures 230 can be contacted on the sides. In some embodiments, the large width of vias 260 in which the contact structures are formed allows the vias to be etched by an isotropic etching process. Isotropic etching can be less expensive than anisotropic etching.

In some embodiments, the vias 260 are filled with material 2110, as in Fig. 22.

In Figs. 24-26, the wafer 310 is as in Fig. 21. In other embodiments with contact structures 230 on the chip boundaries, wafer 310 is as in Fig. 3 or 23.

In Fig. 27, cavities 2710 have been formed in wafer 310 on the top side along the dicing lines. Cavities 2710 can be formed before or after the wafers 310, 210 are bonded together. Cavities 2710 can extend the whole length of the dicing lines, or can be scattered along the dicing lines in any pattern. Fig. 28 shows the structure after dicing. Cavities 2710 reduce the stress during dicing and also reduce the time that the structure is exposed to the stress. The dicing damage is therefore less. This is particularly advantageous if substrate 310 is a transparent substrate used for optical purposes, since damage to substrate 310 can cause optical distortion.

Cavities 2710 can be used in conjunction with any of the structures and processes described above in connection with Figs. 2-26.

Structures 120 can be manufactured using multiple wafers. In the example of Fig. 29, structures 120 include portions of wafer 210 and of wafers 2904 bonded to the front side of wafer 210. Examples of such structures include micropumps. See for example U.S. patent 6,116,863 issued September 12, 2000, entitled "Electromagnetically Driven Microactuated Device and Method of Making the Same". In Fig. 29, passages 2910 in wafer 310 represent the pumps' inlets and outlets. During fabrication, the wafers 2904 and the front side of wafer 210 are processed as needed to manufacturer the structures 120. Wafers 210, 2904 are bonded together. Wafer 310 is processed as needed (for example, to form cavities 320 of Fig. 3, or stand-off features 2110 of Fig. 24, or passages 2910). Then wafer 310 is bonded to the top wafer 2904. After that, fabrication proceeds as described above in connection with Figs. 4-28. The backside of wafer 210 is processed to expose the contact structures 230. The wafer backside in Fig. 29 is as in Fig. 19, but other processes described above can also be used. Fig. 29 shows the structure after dicing.

The embodiments described above illustrate but do not limit the invention. The invention is not limited to any particular materials, processes, dimensions, layouts, or to any particular types of structures 120. Structures 120 may have mechanical components, that is, components that move during operation. Other embodiments and variations are within the scope of the invention, as defined by the appended claims.

CLAIMS

What is claimed is:

1. A fabrication method comprising:

forming a structure that has one or more substrates, wherein the one or more substrates are either a single substrate or a plurality of substrates bonded together, wherein the structure comprises a non-electronically-functioning component which includes at least a portion of the one or more substrates and/or is attached to the one or more substrates;

wherein the one or more substrates include a first substrate which has: a first side, an opening in the first side, and a conductor in the opening;

wherein the method comprises removing material from the structure so that the conductor becomes exposed on a second side of the first substrate.

2. The method of Claim 1 wherein the conductor in the opening is part of a circuit formed in the one or more substrates and used in operation of the non-electronically-functioning component.

3. The method of Claim 1 wherein the one or more substrates are a plurality of substrates bonded together.

4. The method of Claim 3 wherein forming the structure comprises:

forming a stand-off feature on a substrate S1 which is one of said substrates, the feature standing off on the substrate S1; and

bonding the substrates together so that the stand-off feature is positioned between the substrate S1 and another substrate S2 which is one of the substrates, wherein the first substrate is one of the substrates S1 and S2.

5. The method of Claim 4 wherein the material from which the stand-off feature is made fills the opening at least partially.

6. The method of Claim 5 wherein the bonding of the substrate S1 to the substrate S2 is performed before the material of the stand-off feature is hardened, the material of the stand-off feature flowing into the opening during this bonding.

7. The method of Claim 4 further comprising a spacer made on the substrate S1 or S2, to maintain a minimum distance between the substrates S1 and S2 and thus protect the non-electronically-functioning component at least part of which is positioned between the substrates S1 and S2.

8. The method of Claim 7 wherein the bonding of the substrate S1 to the substrate S2 is performed before material of the stand-off feature is hardened, and the spacer comprises hard substance in the non-hardened material of the stand-off feature.

9. The method of Claim 1 wherein removing of the material comprises removing the material from a first portion of the second side of the first substrate to cause the first portion to be recessed relative to a second portion of the second side of the first substrate.

10. The method of Claim 3 further comprising dicing the structure after the conductor has been exposed on the second side.

11. The method of Claim 3 wherein the plurality of substrates comprises a second substrate which at least partially protects the non-electronically-functioning component during said removing of material from the structure.

12. The method of Claim 1 further comprising attaching the conductor's surface exposed on the second side to a wiring substrate.

13. The method of Claim 1 wherein the second side is opposite from the first side.

14. The method of Claim 1 wherein the first substrate is a semiconductor substrate.

15. The method of Claim 14 further comprising forming an insulator over the semiconductor material on the second side, the insulator not completely covering the conductor on the second side.

16. The method of Claim 1 wherein:

the opening is one or a plurality of openings in the first side, each of the openings containing a conductor for carrying an electrical signal; and

the operation of removing material from the second side causes the conductors to be exposed in the openings.

17. The method of Claim 1 wherein operation of the non-electronically-functioning component requires the component to be able to (a) move or deform; and/or (b) emit, sense, or otherwise interact with electromagnetic radiation.

18. A device comprising:

a structure that has one or more substrates, wherein the one or more substrates are either a single substrate or a plurality of substrates bonded together, wherein the one or more substrates include a first substrate which has a first side, a second side, an opening passing through the first substrate from the first side to the second side, and a conductor in the opening, the conductor being exposed on the second side;

wherein the structure comprises a non-electronically-functioning component which includes at least a portion of the first substrate at the first side of the first substrate, and/or is attached to the first side of the first substrate.

19. The device of Claim 18 wherein the conductor in the opening is part of a circuit formed in the one or more substrates and used in operation of the non-electronically-functioning component.

20. The device of Claim 18 wherein the one or more substrates are a plurality of substrates bonded together.

21. The device of Claim 20 wherein the structure comprises a stand-off feature between substrates S1 and S2 which are two of said substrates, the first substrate being one of the substrates S1 and S2.

22. The device of Claim 21 wherein the material from which the stand-off feature is made fills the opening at least partially.

23. The device of Claim 21 further comprising a spacer made on the substrate S1 or S2.

24. The device of Claim 23 wherein the spacer comprises a glass or resin ball embedded into the stand-off feature.

25. The device of Claim 18 wherein the conductor is exposed at a first portion of the second side, and the second side has a second portion protruding from the second side relative to the first portion.

26. The device of Claim 25 further comprising:

one or more interconnect lines which overlay the second side and extend from the exposed conductor on the second side to the second portion; and

an insulator overlaying the conductor on the second side but exposing a contact on the second portion, the contact being electrically connected to the conductor by one or more of the interconnect lines.

27. The device of Claim 18 in combination with a wiring substrate attached to the conductor's surface exposed on the second side.

28. The device of Claim 18 wherein the second side is opposite from the first side.

29. The device of Claim 18 wherein the opening is one or a plurality of openings each of which passes through the first substrate from the first side to the second side, and the device comprising a conductor in each of the openings, the conductor being exposed on the second side.

30. The device of Claim 18 wherein operation of the non-electronically-functioning component requires the component to be able to (a) move or deform; and/or (b) emit, sense, or otherwise interact with electromagnetic radiation.

31. A fabrication method comprising:

forming a structure comprising a first substrate which has: a first side, an opening in the first side, and a conductor in the opening;

removing material from the structure so that the conductor becomes exposed on a second side of the first substrate;

wherein removing of the material comprises removing the material from a first portion of the second side of the first substrate to cause the first portion to be recessed relative to a second portion of the second side of the first substrate.

32. The method of Claim 9 or 31 wherein:

the structure is to provide a chip;

the opening is positioned adjacent to a boundary of said chip; and

the second portion comprises a part extending towards the boundary of said chip.

33. The method of Claim 32 wherein:

the first substrate has a plurality of openings in the first side, and a conductor in each of the openings;

removing of the material exposes the conductor on the second side in each of the openings;

the part extending towards the boundary of the chip extends between the openings.

34. The method of Claim 33 wherein the part extending towards the boundary comes at least as close to the boundary as the opening.

35. The method of Claim 32 wherein the part extending towards the boundary reaches the boundary.

36. The method of Claim 32 wherein the part reaches a corner of the chip.

37. The method of Claim 32 wherein the part extending towards the boundary comes at least as close to the boundary as the exposed conductor on the second side.

38. The method of Claim 32 wherein the part extends towards a corner of the chip.

39. The method of Claim 9 or 31 further comprising forming, over the second side, one or more interconnect lines which extend from the exposed conductor to the

second portion, and forming an insulator overlaying the conductor on the second side but exposing a contact on the second portion, the contact being electrically connected to the conductor by one or more of the interconnect lines.

40. The method of Claim 31 wherein the first substrate is a semiconductor substrate.

41. The method of Claim 14 or 40 wherein:

the opening contains a first insulator insulating the conductor from sidewalls of the opening; and

removing the material from the structure comprises:

(A) removing semiconductor material from the second side to expose the first insulator; and

(B) removing the first insulator on the second side to expose the conductor.

42. The method of Claim 41 further comprising forming a second insulator over the semiconductor material on the second side, the second insulator not completely covering the conductor on the second side.

43. The method of Claim 42 wherein the second insulator is formed after the operation (B).

44. The method of Claim 42 wherein the second insulator is formed after the operation (A) but before the conductor is exposed by the operation (B).

45. The method of Claim 42 wherein forming the second insulator comprises:

forming the second insulator over the semiconductor material and over the conductor; and

etching the second insulator with a blanket etch to completely remove the second insulator over at least a portion of the conductor but not completely remove the second insulator over the semiconductor material.

46. A device comprising:

a structure comprising a first substrate which has a first side, a second side, an opening passing through the first substrate from the first side to the second side, and a conductor in the opening, the conductor being exposed on the second side;

wherein the conductor is exposed at a first portion of the second side, and the second side has a second portion protruding from the second side relative to the first portion.

47. The device of Claim 25 or 46 wherein:

the opening is positioned adjacent to a boundary of the structure; and

the second portion comprises a part extending towards the boundary of the structure.

48. The device of Claim 47 wherein:

the first substrate has a plurality of openings passing from the first side to the second side, and a conductor in each of the openings;

the part extending towards the boundary of the structure extends between the openings.

49. The device of Claim 47 wherein the part extending towards the boundary reaches the boundary.

50. The device of Claim 47 wherein the part extending towards the boundary comes at least as close to the boundary as the opening.

51. The device of Claim 47 wherein the part extending to the boundary comes at least as close to the boundary as the exposed conductor on the second side.

52. The device of Claim 47 wherein the part reaches a corner of the structure.

53. The device of Claim 47 further comprising:

one or more interconnect lines which extend from the exposed conductor on the second side to the second portion; and

an insulator overlaying the conductor on the second side but exposing a contact on the second portion, the contact being electrically connected to the conductor by one or more of the interconnect lines.

54. The device of Claim 18 or 31 wherein the first substrate is a semiconductor substrate.

55. The device of Claim 54 wherein the opening contains a first insulator insulating the conductor from sidewalls of the opening.

56. The device of Claim 55 further comprising a second insulator formed over the semiconductor material on the second side, the second insulator not completely covering the conductor on the second side.

57. The device of Claim 54 further comprising an insulator formed over the semiconductor material on the second side, said insulator not completely covering the conductor on the second side.

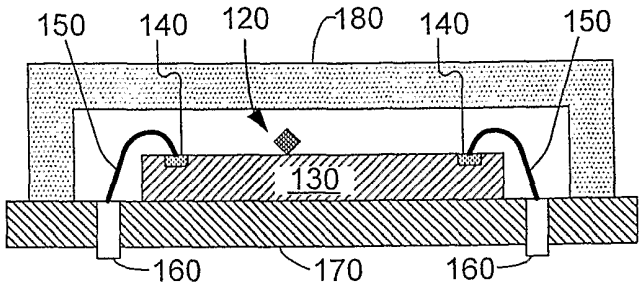


FIG. 1 PRIOR ART

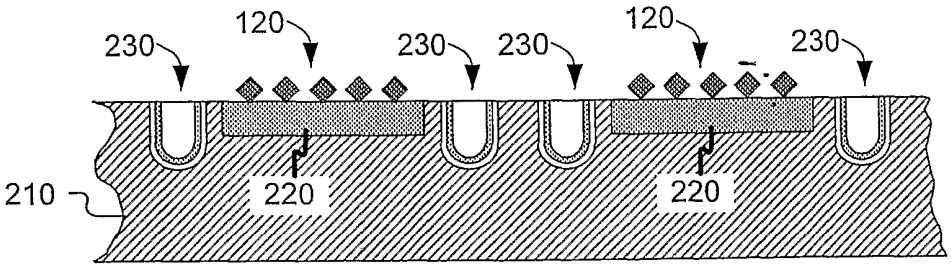


FIG. 2A

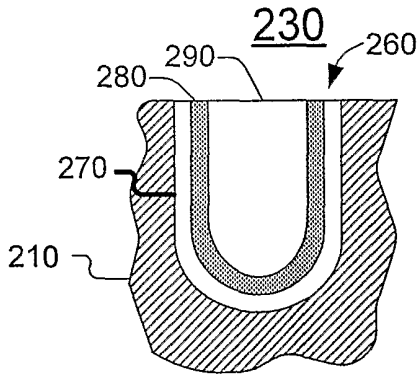


FIG. 2B

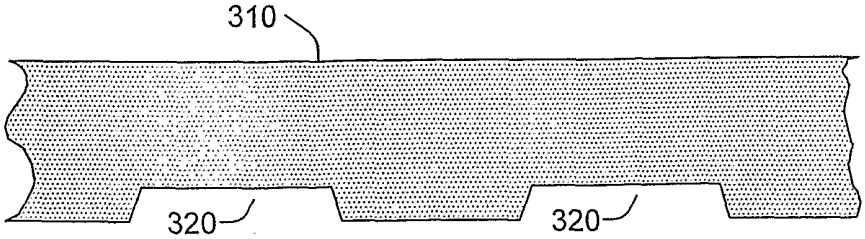


FIG. 3

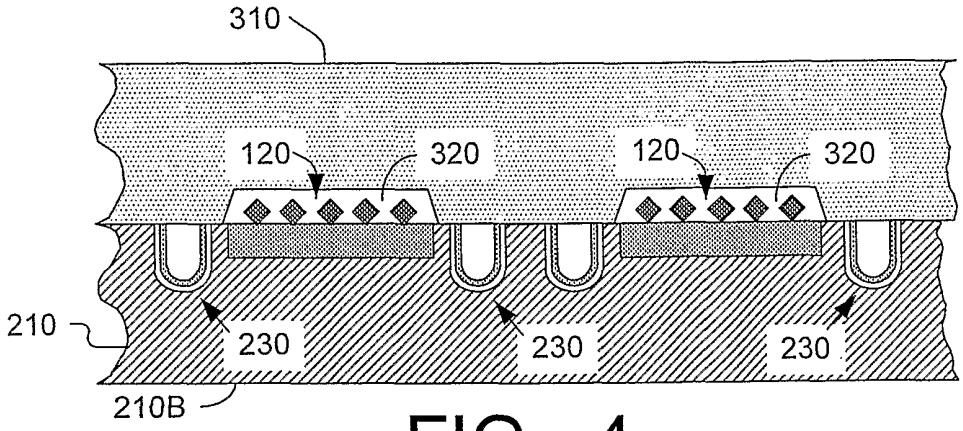


FIG. 4

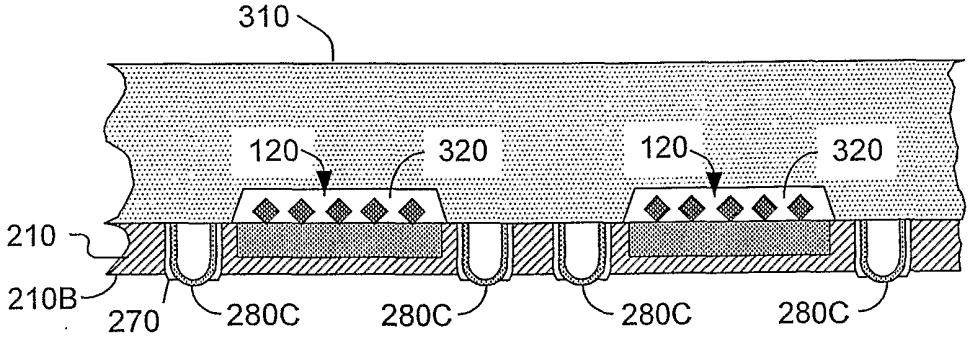


FIG. 5

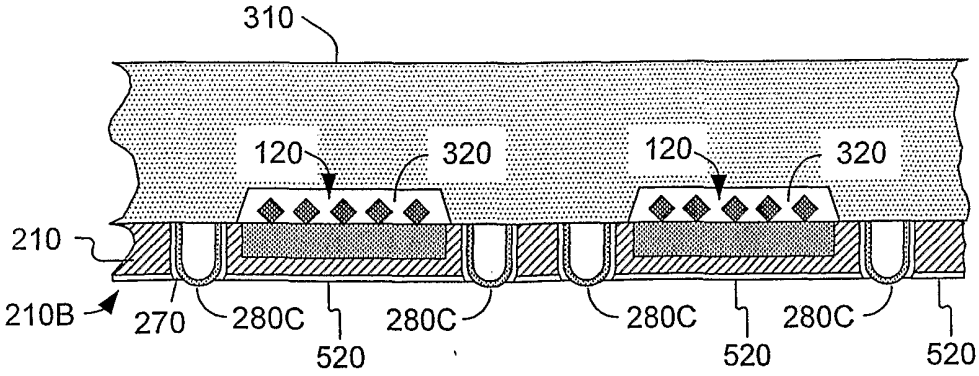


FIG. 6

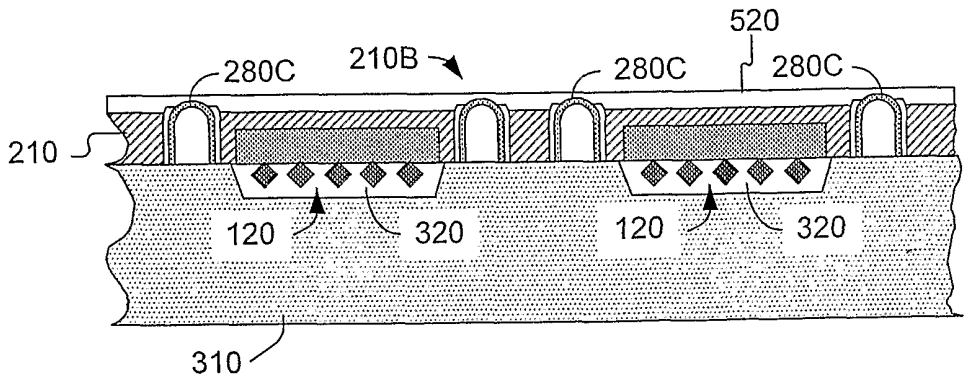


FIG. 7

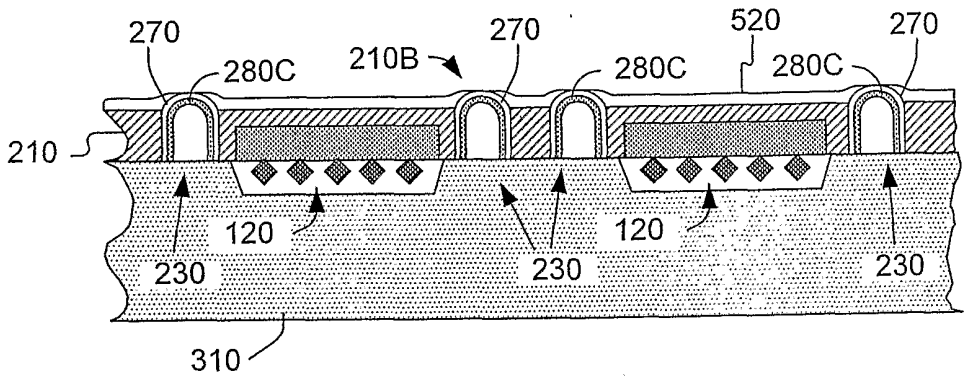


FIG. 8

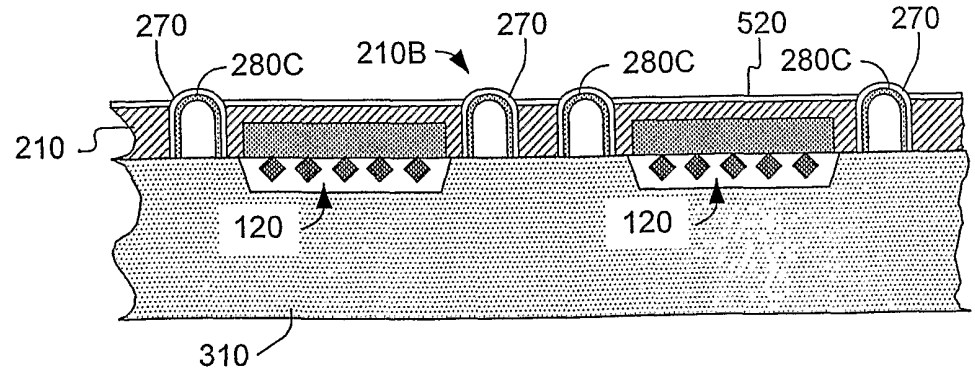


FIG. 9

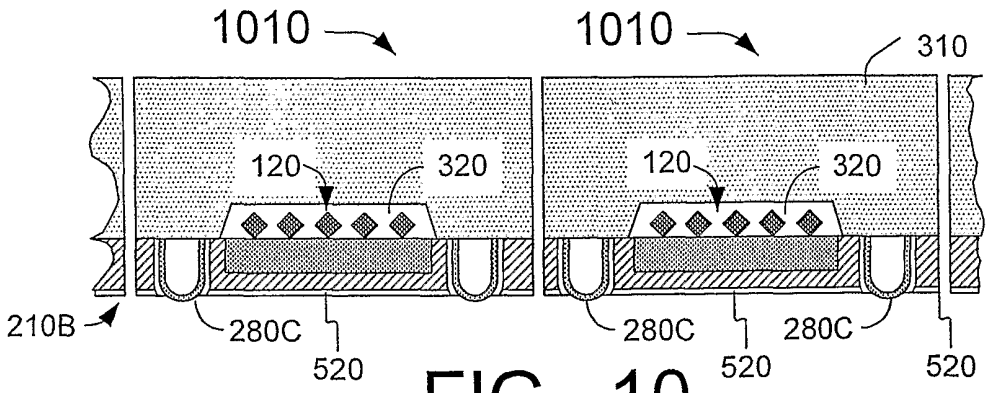


FIG. 10

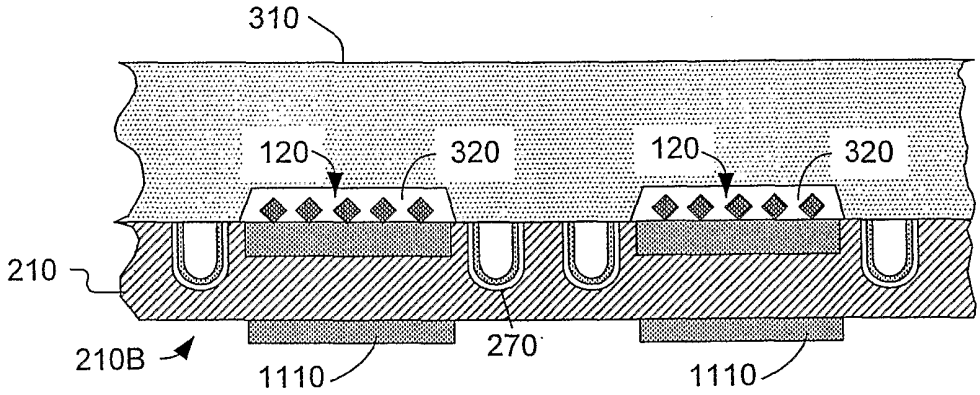
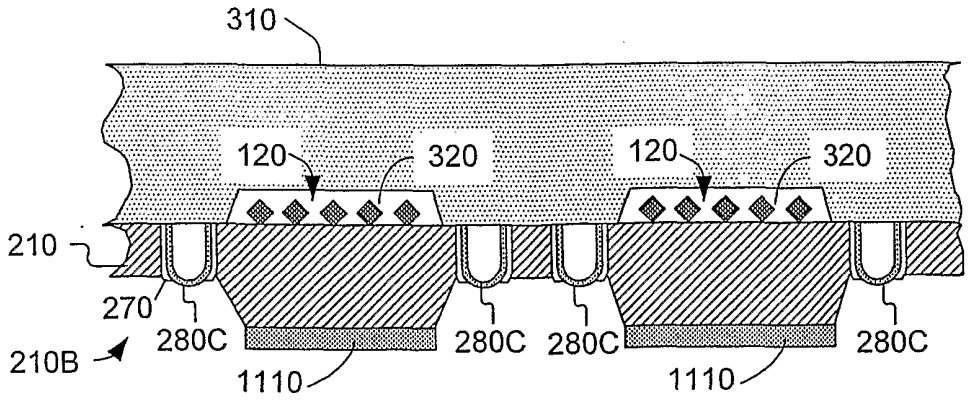


FIG. 11



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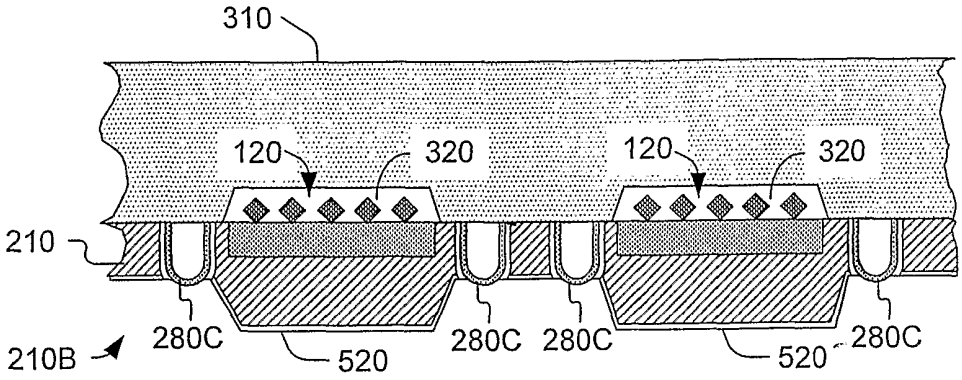

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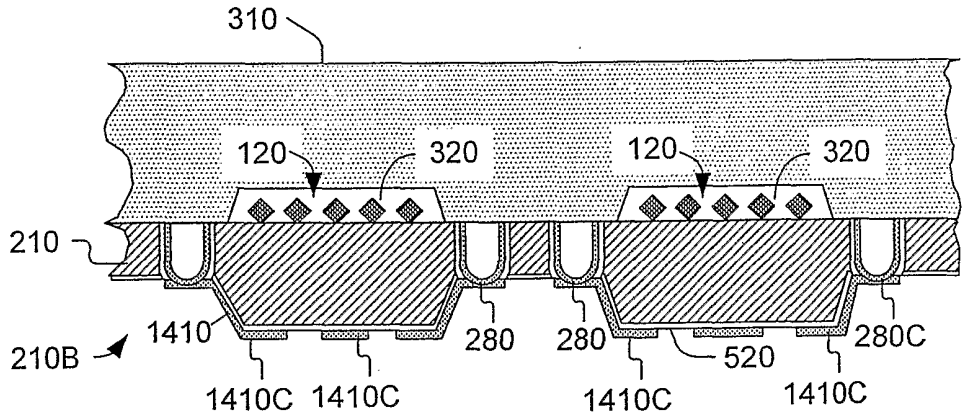

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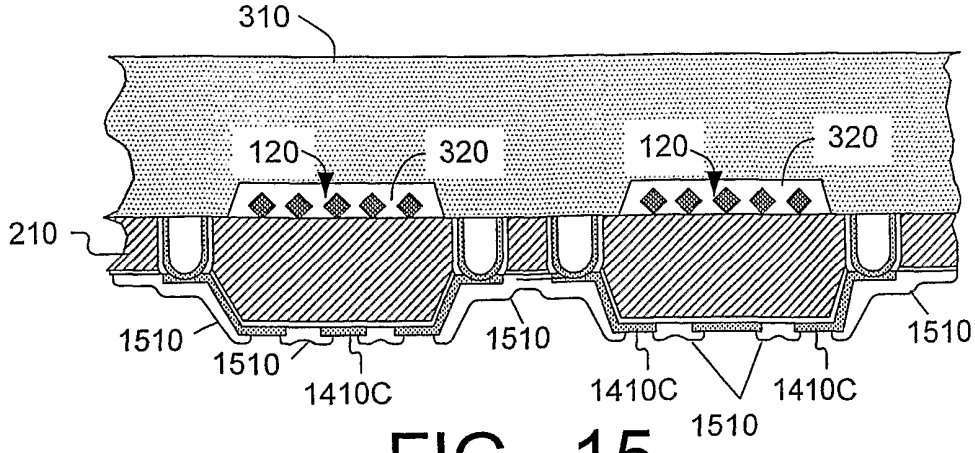


FIG. 15

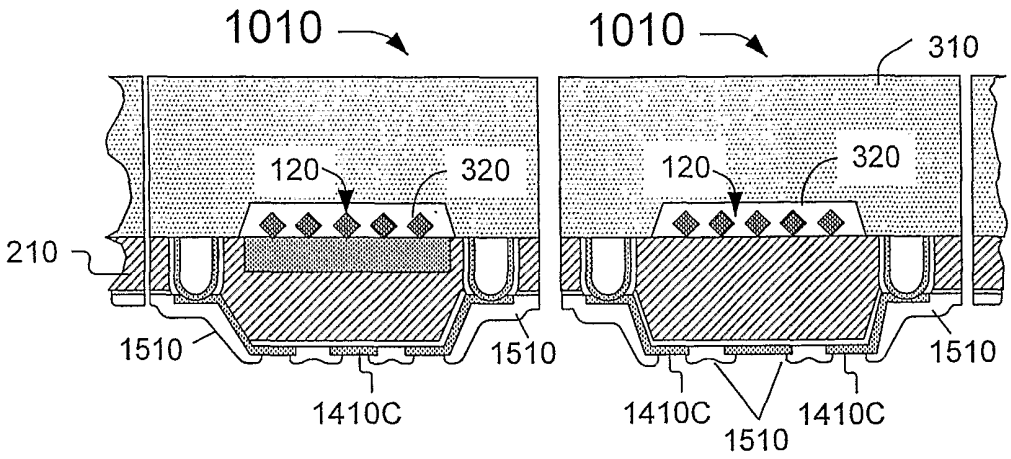


FIG. 16

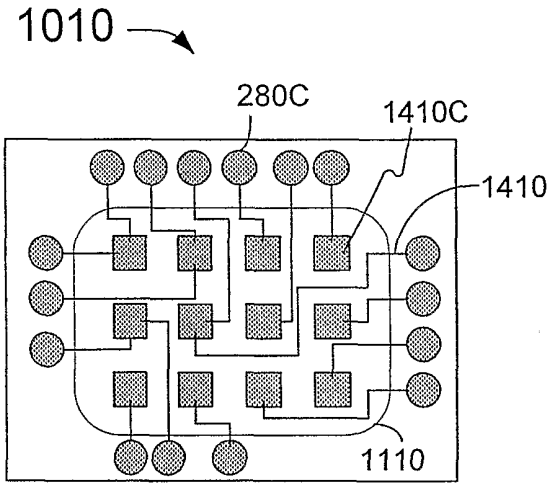


FIG. 17

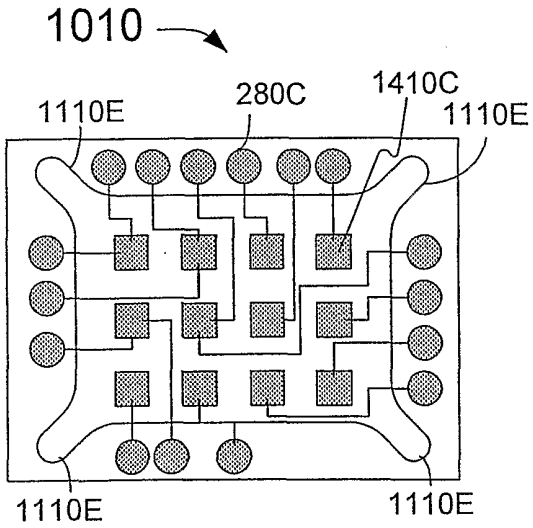
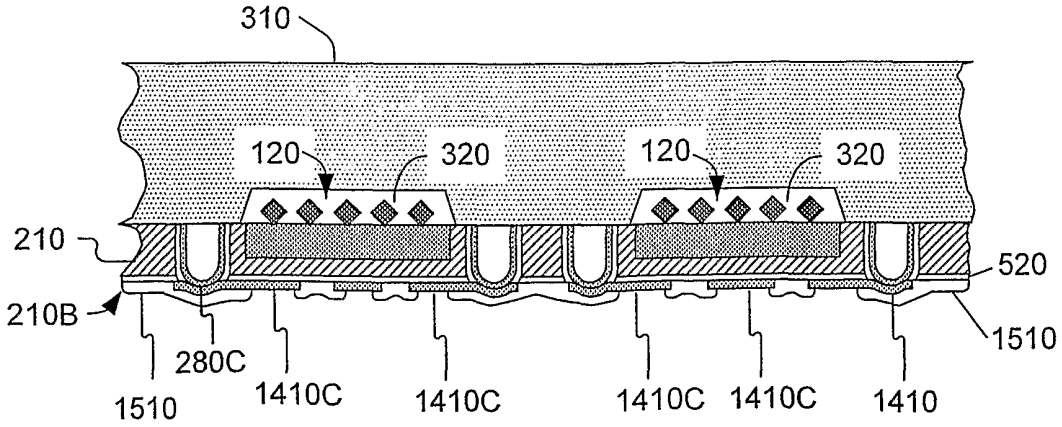


FIG. 18



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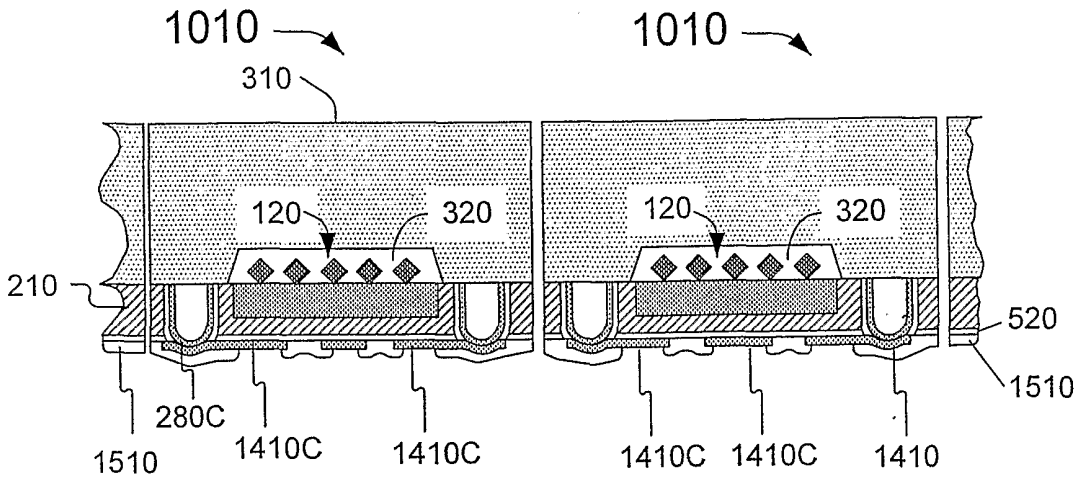

FIG. 20

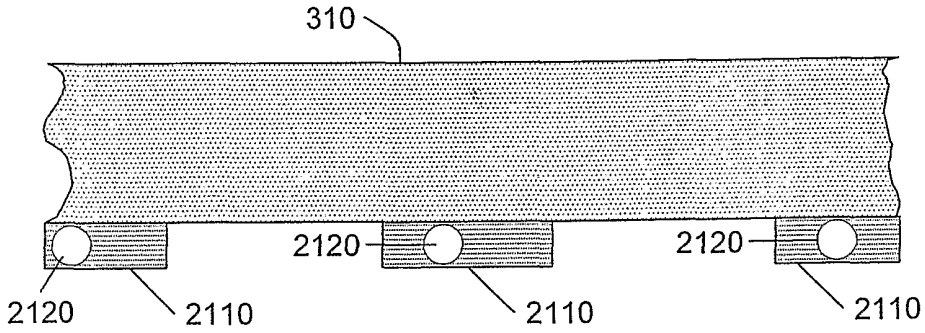

FIG. 21

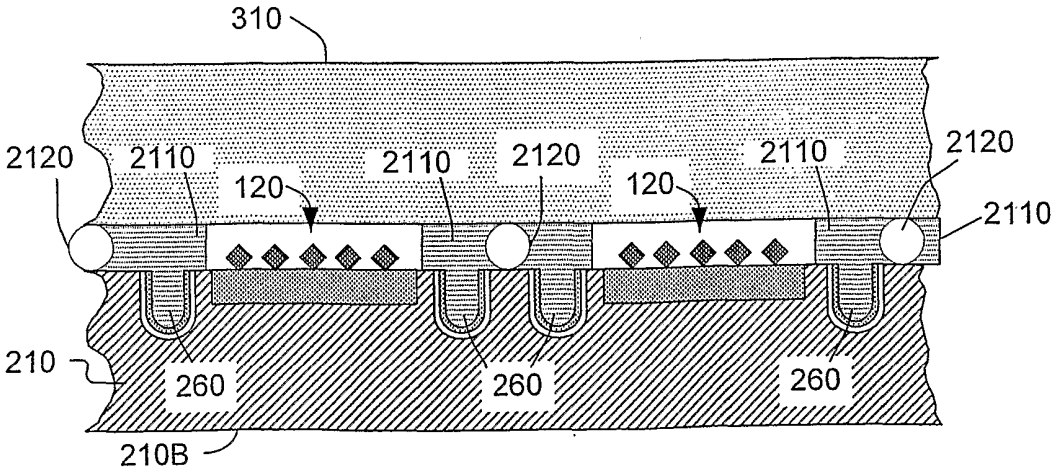

FIG. 22

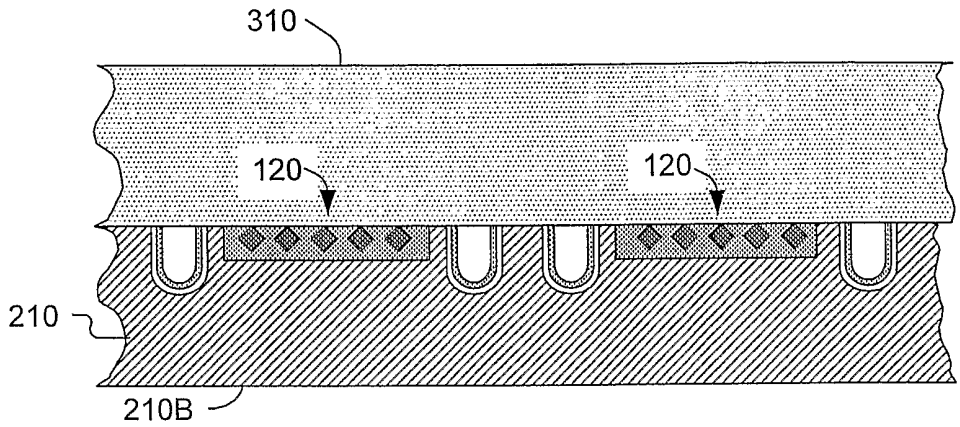

FIG. 23

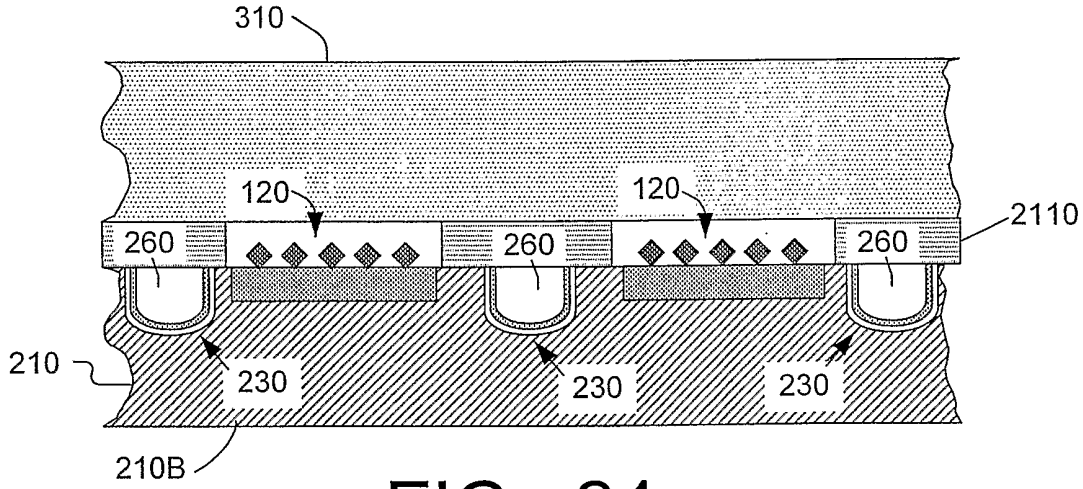

FIG. 24

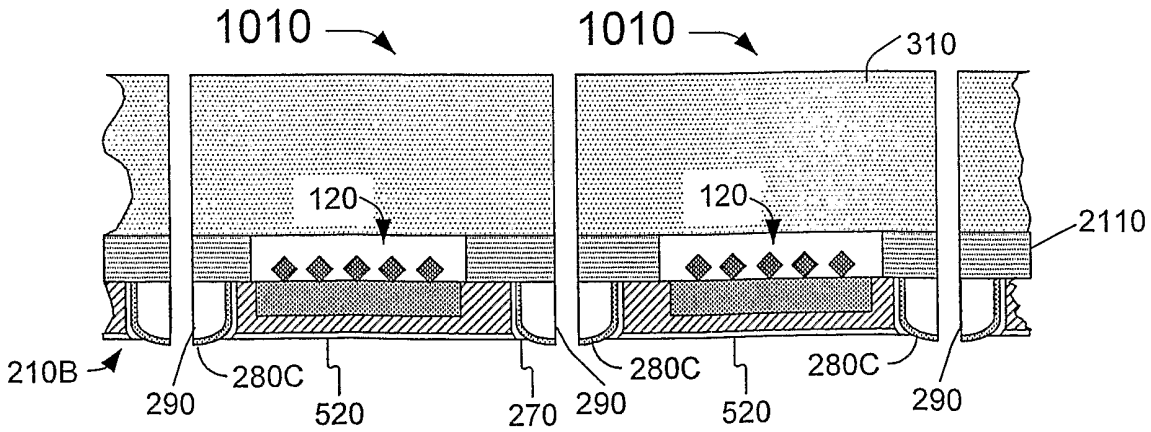

FIG. 25

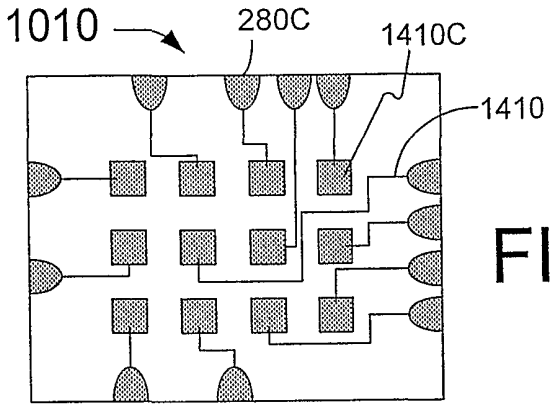

FIG. 26

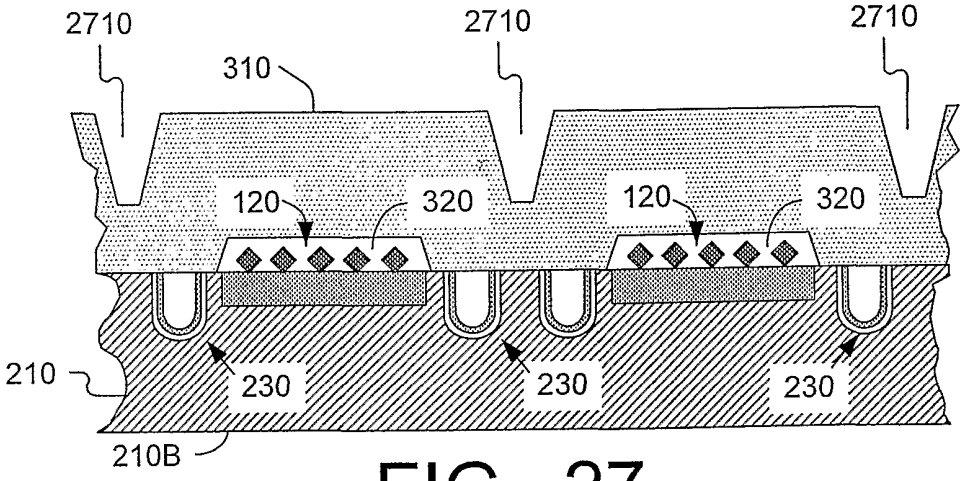

FIG. 27

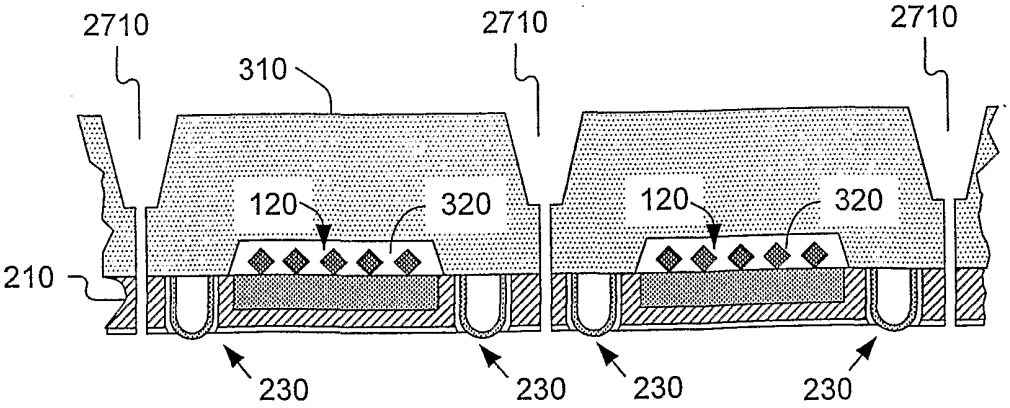

FIG. 28

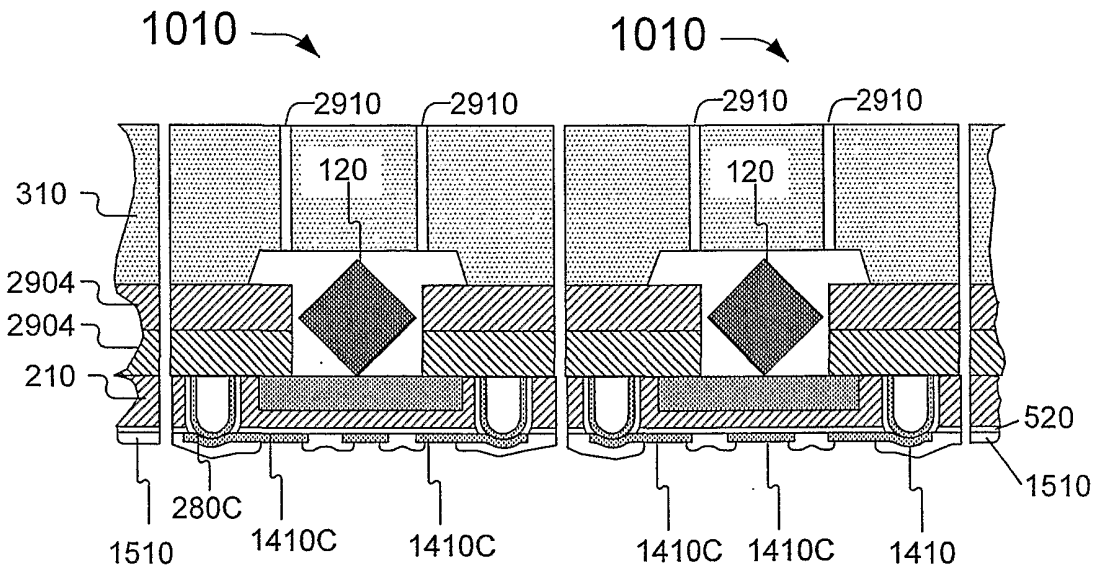
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FIG. 29