



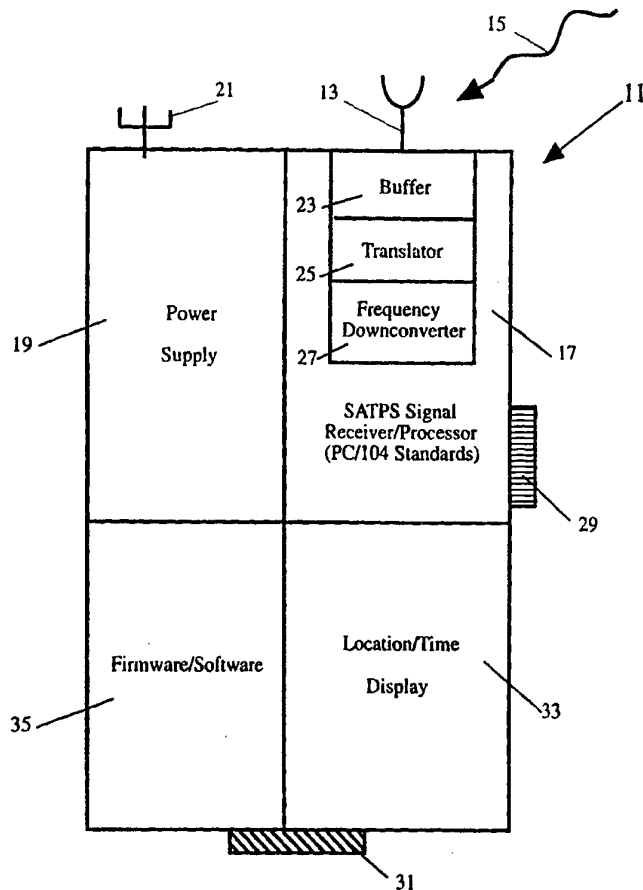
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(54) Title: COMBINED PC/104 AND SATELLITE POSITIONING SYSTEM

(57) Abstract

Apparatus for determining the present location of, or time of observation by, an observer on or in the vicinity of the Earth's surface. The apparatus provides a Satellite Positioning System (SATPS), such as GPS or GLONASS, in a portable device or card that is built to PC/104 standards. The PC/104/SATPS card (11) includes an SATPS antenna (13) to receive (and frequency downconvert, if necessary) SATPS signals (15) from one or more SATPS satellites, a microprocessor (17) programmed to receive the SATPS signals from the antenna and to perform calculations to determine the location of the antenna and/or the time of observation. The PC/104/SATPS card optionally has a buffer/translator (23, 25) to compensate for differences in SATPS signal arrival rate and signal processing rate and/or to translate signals from SATPS format to whatever format the microprocessor uses. The PC/104/SATPS card optionally has a keyboard, pen-and-tablet or other information entry means (31) and optionally has an information transfer module (29) for transferring information from the PC/104/SATPS card to another electronic apparatus for further processing or for display of the location of, or time of observation by, the antenna. Optionally, the PC/104/SATPS card also includes a display module (33) for displaying the location of, or time of observation by, the antenna in a visually perceptible manner on the card itself.



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COMBINED PC/104 AND SATELLITE POSITIONING SYSTEM

Background of the Invention

5 In the past 12 years, the personal computer PC architecture has become an accepted standard for applications for personal computing, control microprocessors, point-of-sale registers, vending machines, laboratory instruments, and medical and other laboratory data-gathering instruments. Many other interesting applications are available, if the PC
10 bus and CPU can be made sufficiently compact and the power requirements can be reduced. The PC/104 is a standard being developed by the PC/104 Consortium for such purpose by an extension of the IEEE-P996 specification, originally developed for the PC and PC/AT buses. The number of bus connector pins used in such architecture is 64 pins for P1
15 and 40 pins for P2, for a total of 104 pins, from which the standard takes its name. The PC/104 is a de facto standard that is now recognized as such, rather than the result of a theoretical standard developed by a group of diligent nerds over an extended period of time.

 The PC/104 standard differs from the earlier IEEE-P996 standard
20 in several ways: (1) the PC/104 form factor is much smaller, measuring approximately 9 cm by 9.5 cm by 1.5 cm, which allows use of a PC/104 module in limited space environments; (2) the PC/104 standard calls for use of a unique self-stacking bus that eliminates most of the bulk and cost of backplanes; (3) the PC/104 standard uses 64-pin and 40-pin male/female
25 connectors rather than the card edge connectors used on the IEEE-P996 standard; and (4) power consumption is typically lowered to 1-2 Watts per module, and component count is reduced. Two adjacent PC/104 modules may be spaced apart by a distance of 1.5 cm in an installed stack, using the self-stacking buses. These and other differences are summarized in a
30 publication by the PC/104 Committee, "PC/104: A Compact Embedded-PC Standard", Specification 1.0, March 1992, available from the PC/104 Consortium, 990 Almanor Avenue, Sunnyvale, California 94086. The relevant parts of the PC/104 Standard are reproduced verbatim from this

Specification in Appendix A. The IEEE-P996 specification itself, incorporated by reference herein, is available from the I.E.E.E. Standards Office, 455 Hoes Lane, Piscataway, New Jersey 08854.

The PC/104 module can have an 8-bit bus or a 16-bit bus, corresponding to the PC and PC/AT buses, respectively. Each of these buses offers two options, according to whether the P1 and P2 bus connectors extend through the module as "stackthrough" connectors, or do not extend through the module. These options provide additional flexibility and allow design choices that facilitate minimum space planning for the PC/104 module. A typical stack of modules could accommodate a mix of stack-through and non-stack-through configurations or a configuration that is purely stack-through or purely non-stackthrough. All PC/104 bus signals are identical in definition, in function and in signal timing to the P-996 bus signals, and signals are assigned in the same order on the edgecard connectors. High and low logic levels for the PC/104 module are identical to the corresponding logic levels for the P-996.

Some ground pins have been added to the PC/104 module to improve bus integrity. To reduce component count and minimize power consumption and heat dissipation, most bus signals have a reduced bus current drive requirement, 6 milliamps (mA). However, four signals, MEMCS16, IOCS16, MASTER and ENDXFR, require drive currents of 20 mA. Bus termination, if it is included, must be AC termination. One suitable choice for termination is a resistor-capacitor network of 40-60 Ohms connected in series with a 30-70 picofarads (pF) capacitor circuit and connected between each bus signal and ground. The PC/104 Specification, version 1.0, sets forth the bus signal assignments for about 100 of the pin connections.

All bus devices that share a common interrupt signal must be equipped with a suitable interrupt-sharing circuit, with the following restrictions: (1) the shared interrupt line must not have a voltage pull-up resistance smaller than 10 kilo-ohms anywhere in the system; and (2) the shared interrupt line must have precisely one pull-down resistor (with a value of about 1 kilo-ohm) connected between the interrupt request line

and ground. Because of these restrictions, some of the IEEE-P996 interrupt circuits will not work well in a PC/104 module.

As yet, the PC/104 module has been a versatile product in search of an application. Applications of small size microprocessors and related products have appeared from time to time in other technical areas.

A special purpose peripheral circuit or add-on card for connection to a computer is disclosed by Brockman in U.S. Patent No. 4,702,189. The card provides time and date information and continuously updates the normal computer clock whenever the computer is rebooted. The card connects to the computer in parallel with, but does not interfere with normal operation of, a printer or other input/output device.

United States Patent No. 4,748,320, issued to Yorimoto et al, discloses an integrated circuit card including a central processing unit (CPU), program memory, random access memory, a data bus and an address bus. An input/output device, such as a keyboard, is connected to the card entry and readout of information and instructions. The card provides expansion of existing files.

Miyano, in U.S. Patent No. 4,847,803, discloses an "IC card", containing an integrated circuit, that has a control unit for data processing, a data memory and a software program memory. The IC card memory stores several personal identification numbers (PINs) and contains a program that compares an externally entered PIN index and the internally stored PINs, to determine whether the data or instructions sought to be entered by the cardholder can be accepted and executed. Data and instruction entry occurs by a conventional card reader.

A "smart" IC card, having a CPU, data memory, a "keyboard" and on-board visual display is disclosed by Tanaka in U.S. Patent No. 4,924,075. The CPU operates in three modes, namely time display, numerical or calculational, and accounting or transactional. The keyboard includes a numerical keypad and the five numerical operations (+, -, *, / and =) and several pre-programmed transaction keys.

A universal connector device for communication of instructions and data between a CPU of a host computer CPU, a CPU bus of an external

co-processor, and a host computer expansion card is disclosed by Rubin in U.S. Patent No. 4,954,949. Compatibility between the host computer and co-processor is provided by a bridge card that connects the buses of the two processors to each other and to a memory device for use by the co-processor.

U.S. Patent No. 4,965,802, issued to Shinigawa, discloses an IC card with data memory segmented into externally entered information and information generated internally from the externally entered information, including a history of transactions using the card. The card contains a data processing unit, an input/output unit, and what appears to be a read only memory (ROM) for on-board storage of fixed data processing programs. An error detection unit is optionally included on the card.

Dethloff et al disclose a smart IC card for storing and using the present currency exchange rates, in U.S. Patent No. 4,968,873. Exchange rates for several currencies are stored and updated as required. A maximum transaction limit for the cardholder is included, which limit can be translated into the currency presently being used to determine if the transaction is permissible. The card carries a keyboard for data entry, data memory for the currency exchange rates, and a CPU to translate the currency value and compare the transaction value with the transaction limit.

An integrated circuit with an access-controlled data memory contained on an IC card, for protecting secret code data, is disclosed by Schrenk in U.S. Patent No. 5,014,311. Access to certain parts of memory is limited to one or more predetermined time periods.

Wilhelm, in U.S. Patent No. 5,020,926, discloses a printer assembly with a form factor that is as small as a disk drive assembly for a microcomputer. The printer assembly slides between a first position, inside the microcomputer, and a second position, generally outside the microcomputer, for use in printing data provided by the microcomputer. The printer assembly carries its own power supply and has a standard bus arrangement for receipt of instructions and data from the microcomputer.

U.S. Patent No. 5,038,025, issued to Koder, discloses a method of downloading a software program to an IC card. The IC card contains program memory, data memory, a CPU, and an input/output interface that transfers program information to the card from an external keyboard or work station. The card keeps track of available memory on board and informs the keyboard user if insufficient memory remains to accept and store a program or data. The program instructions entered from the keyboard can be stored in specified memory locations or in memory locations chosen by the CPU. Absolute addressing and/or relative addressing is available for program instruction storage.

A computer bus interconnection plug-in device to provide PC compatibility with a VME computer is disclosed in U.S. Patent No. 5,083,259, issued to Maresh et al. A circuit board containing a PC/AT bus and a PC/AT CPU and associated random access memory. Provision of input/output devices, such as a keyboard and a video display, for the PC/AT CPU is also mentioned.

Buxton et al, in U.S. Patent No. 5,123,092, disclose an external expansion bus interface for a microcomputer that can select and de-select any devices connected to the expansion device. Device selection and de-selection are implemented by selectively enabling and disabling buffers that intercept signals passing between the external bus and the microcomputer bus.

None of these inventions provides for straightforward entry of data into the microprocessor, for example, through an antenna, or use of a PC/104 card with satellite or other radiowave signals to provide navigation, location and tracking information for the carrier of a card configured to the PC/104 standard. These inventions also do not provide for reconciliation of data entered in a format that is initially incompatible with the format adopted for the PC/104 card. What is needed is an enhanced or improved PC/104 card that provides these features.

Summary of the Invention

These needs are met by the invention, which provides a PC/104/SATPS Card, built compatible with the above-discussed PC/104

- standards and specifications, that receives and processes Satellite Positioning System (SATPS) signals from one or more SATPS satellites. In one embodiment, the Card includes an SATPS antenna positioned to receive SATPS signals from one or more SATPS satellites, with each
- 5 signal being characteristic of a particular satellite, and to issue these signals as antenna output signals. The Card also includes a radiofrequency downconverter to receive the antenna output signals, to convert the primary frequency of each of these signals to a selected lower frequency, and to issue these down-converted signals as downconverter output signals.
- 10 The Card further includes a programmed digital signal processor and associated memory that receives the downconverter output signals corresponding to each SATPS signal received by the antenna, determines the present location of, or time of observation by, the antenna, and issues these signals as processor output signals. Finally, the Card includes an
- 15 information transfer module that receives the digital signal processor output signals and transmits these output signals to an electronic device that is linked to, but not a part of, the PC/104/SATPS Card, for further signal processing or for display of the location of and/or time of observation by the antenna.
- 20 In a second embodiment, the Card includes an image display module in place of the information transfer module of the first embodiment. The image display module receives the digital signal processor output signals and displays the present location of, and/or time of observation by, the antenna in a visually perceptible manner.
- 25 PC/104 is a new CPU form factor standard, discussed in some detail above, that can be used to provide various I/O and signal processing services. The invention provides an SATPS signal antenna and receiver/processor card that adheres to the PC/104 standard. The card may include other features, such as (1) a memory buffer and (2) firmware
- 30 that senses the UTC time and resets the CPU clock to UTC time or to some other acceptable standard. Use of a buffer is advisable here because the SATPS antenna output signals are serial, and the host computer may have difficulty digesting serial data that arrives at a 1-10 MHz rate. Provision

of SATPS signals in serial form may require a latency period, which many host computers do not deal with well. The memory buffer can examine the incoming signals and accept only the data segments of interest for provision of an SATPS location fix; these data segments could be brought
5 directly from the buffer when these segments are needed.

Brief Description of the Drawings

Figure 1 is a schematic view of an embodiment of the invention.

Description of Best Mode of the Invention

Figure 1 illustrates one embodiment of the invention, a
10 PC/104/SATPS card 11 that includes: an antenna 13 that receives Satellite Positioning System (SATPS) signals 15 from one or more SATPS satellites, an SATPS receiver/processor or microprocessor or CPU 17 that receives the SATPS signals from the SATPS antenna and is programmed to perform calculations using these signals to determine the antenna
15 location and/or time of observation; a power supply 19 and electrical power connector 21 that provide power for the SATPS antenna 13 and receiver/processor 17.

Optionally, the antenna 13 and/or receiver/processor 17 includes one or more of the following: a signal buffer 23 that receives and temporarily
20 stores SATPS signals until the receiver/processor 17 is ready to process these signals; a signal reformatter or translator 25 that receives SATPS signals and reformats these signals or translates the signals into a format and form that the receiver/processor 17 can accept and process; and/or a frequency downconverter 27 that receives the SATPS signals and converts
25 these signals to a selected lower frequency.

The SATPS signals are often presented in a serial format, whereas the PC/104 CPU 17 only receives and processes signals in a particular parallel format. Further, the PC/104 CPU 17 may operate at a high processing rate (≥ 25 MHz) and may have difficulty operating with the
30 time delays or latency periods that are often necessary for SATPS signal processing. The buffer module 23 and translator module 25 provide for off-line time delays and for format translation between an SATPS platform and whatever PC platform is used in the PC/104 CPU 17.

Optionally, the receiver/processor 17 can access the buffer module 23 and/or the translator module 25 directly and call out particular information needed by the CPU to perform CPU tasks.

5 Optionally, the receiver/processor 17 also includes an information transfer module 29 that transfers SATPS signal information, or the results of processing such signals in the receiver/processor, to another electronic device (not a part of the PC/104/SATPS card itself) for further processing or display.

10 Optionally, the PC/104/SATPS card also includes data/instruction entry means 31, such as a keyboard or pen-and-tablet. Optionally, the PC/104/SATPS card includes a location/time display module 33 that displays in a visually perceptible manner the antenna location and/or time of observation determined by the receiver/processor 17 from the SATPS signals 15. Optionally, the PC/104/SATPS card includes one or more
15 expansion modules to perform other tasks. Optionally, the PC/104 card 11 also includes firmware or software module 35 that resets a CPU system clock to the appropriate UTC time.

20 As used herein, the phrase "PC/104 card" refers to any embedded-PC module that complies with the PC/104 Specification, version 1.0 or later, that was discussed earlier

25 A Satellite Positioning System (SATPS) is a system of satellite signal transmitters, with receivers located on the Earth's surface or adjacent to the Earth's surface, that transmits information from which an observer's present location and/or the time of observation can be determined. Two operational systems, each of which qualifies as an SATPS, are the Global Positioning System and the Global Orbiting Navigational System.

30 The Global Positioning System (GPS) is part of a satellite-based navigation system developed by the United States Defense Department under its NAVSTAR satellite program. A fully operational GPS includes up to 24 satellites approximately uniformly dispersed around six circular orbits with four satellites each, the orbits being inclined at an angle of 55° relative to the equator and being separated from each other by multiples of 60° longitude. The orbits have radii of 26,560 kilometers and are

approximately circular. The orbits are non-geosynchronous, with 0.5 sidereal day (11.967 hours) orbital time intervals, so that the satellites move with time relative to the Earth below. Theoretically, three or more GPS satellites will be visible from most points on the Earth's surface, and visual access to two or more such satellites can be used to determine an observer's position anywhere on the Earth's surface, 24 hours per day. Each satellite carries a cesium or rubidium atomic clock to provide timing information for the signals transmitted by the satellites. Internal clock correction is provided for each satellite clock.

Each GPS satellite transmits two spread spectrum, L-band carrier signals: an L1 signal having a frequency $f_1 = 1575.42$ MHz and an L2 signal having a frequency $f_2 = 1227.6$ MHz. These two frequencies are integral multiples $f_1 = 1540 f_0$ and $f_2 = 1200 f_0$ of a base frequency $f_0 = 1.023$ MHz. The L1 signal from each satellite is binary phase shift key (BPSK) modulated by two pseudo-random noise (PRN) codes in phase quadrature, designated as the C/A-code and P-code. The L2 signal from each satellite is BPSK modulated by only the C/A-code. The nature of these PRN codes is described below.

One motivation for use of two carrier signals L1 and L2 is to allow partial compensation for propagation delay of such a signal through the ionosphere, which delay varies approximately as the inverse square of signal frequency f ($\text{delay} \propto f^{-2}$). This phenomenon is discussed by MacDoran in U.S. Patent No. 4,463,357, which discussion is incorporated by reference herein. When transit time delay through the ionosphere is determined, a phase delay associated with a given carrier signal can be determined.

Use of the PRN codes allows use of a plurality of GPS satellite signals for determining an observer's position and for providing navigation information. A signal transmitted by a particular GPS signal is selected by generating and matching, or correlating, the PRN code for that particular satellite. All PRN codes are known and are generated or stored in GPS satellite signal receivers carried by ground observers. A first PRN code for each GPS satellite, sometimes referred to as a precision code or

P-code, is a relatively long, fine-grained code having an associated clock or chip rate of $10 f_0 = 10.23$ MHz. A second PRN code for each GPS satellite, sometimes referred to as a clear/acquisition code or C/A-code, is intended to facilitate rapid satellite signal acquisition and hand-over to the

5 P-code and is a relatively short, coarser-grained code having a clock or chip rate of $f_0 = 1.023$ MHz. The C/A-code for any GPS satellite has a length of 1023 chips or time increments before this code repeats. The full P-code has a length of 259 days, with each satellite transmitting a unique portion of the full P-code. The portion of P-code used for a given GPS

10 satellite has a length of precisely one week (7.000 days) before this code portion repeats. Accepted methods for generating the C/A-code and P-code are set forth in the document GPS Interface Control Document ICD-GPS-200, published by Rockwell International Corporation, Satellite Systems Division, Revision A, 26 September 1984, which is incorporated

15 by reference herein.

The GPS satellite bit stream includes navigational information on the ephemeris of the transmitting GPS satellite and an almanac for all GPS satellites, with parameters providing corrections for ionospheric signal propagation delays suitable for single frequency receivers and for an

20 offset time between satellite clock time and true GPS time. The navigational information is transmitted at a rate of 50 Baud. A useful discussion of the GPS and techniques for obtaining position information from the satellite signals is found in Tom Logsdon, The NAVSTAR Global Positioning System, Van Nostrand Reinhold, New York, 1992,

25 incorporated by reference herein.

A second configuration for global positioning is the Global Orbiting Navigation Satellite System (GLONASS), placed in orbit by the former Soviet Union and now maintained by the Russian Republic. GLONASS also uses 24 satellites, distributed approximately uniformly in three orbital

30 planes of eight satellites each. Each orbital plane has a nominal inclination of 64.8° relative to the equator, and the three orbital planes are separated from each other by multiples of 120° longitude. The GLONASS circular orbits have smaller radii, about 25,510 kilometers, and a satellite period of

revolution of 8/17 of a sidereal day (11.26 hours). A GLONASS satellite and a GPS satellite will thus complete 17 and 16 revolutions, respectively, around the Earth every 8 days. The GLONASS system uses two carrier signals L1 and L2 with frequencies of $f_1 = (1.602 + 9k/16)$ GHz and $f_2 =$
5 $(1.246 + 7k/16)$ GHz, where $k (= 0, 1, 2, \dots, 23)$ is the channel or satellite number. These frequencies lie in two bands at 1.597-1.617 GHz (L1) and 1,240-1,260 GHz (L2). The L1 code is modulated by a C/A-code (chip rate = 0.511 MHz) and by a P-code (chip rate = 5.11 MHz). The L2 code is presently modulated only by the P-code. The GLONASS satellites also
10 transmit navigational data at a rate of 50 Baud. Because the channel frequencies are distinguishable from each other, the P-code is the same, and the C/A-code is the same, for each satellite. The methods for receiving and analyzing the GLONASS signals are similar to the methods used for the GPS signals.

15 Reference to a Satellite Positioning System or SATPS herein refers to a Global Positioning System, to a Global Orbiting Navigation System, and to any other compatible satellite-based system that provides information by which an observer's position and the time of observation can be determined, all of which meet the requirements of the present
20 invention.

A Satellite Positioning System (SATPS), such as the Global Positioning System (GPS) or the Global Orbiting Navigation Satellite System (GLONASS), uses transmission of coded radio signals, with the structure described above, from a plurality of Earth-orbiting satellites. A
25 single passive receiver of such signals is capable of determining receiver absolute position in an Earth-centered, Earth-fixed coordinate reference system utilized by the SATPS.

APPENDIX

PC/104

A Compact Embedded-PC Standard

Specification Version 1.0

5 March 1992

PC/104 is a trademark of the PC/104 Consortium

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1. Introduction

While the PC and PC/AT architectures have become extremely popular in both general purpose (desktop) and dedicated applications, its use in embedded microcomputer applications has been limited due to the large size of standard PC and PC/AT motherboards and expansion cards.

This document supplies the mechanical and electrical specifications for a compact version of the IEEE P996 (PC and PC/AT) bus, optimized by the unique requirements of embedded systems applications. The specification is herein referred to as "PC/104", based on the 104 signal contacts on the two bus connections (64 pins on P1, 40 pins on P2).

Briefly, the needs of embedded applications have been satisfied by PC/104, through the following key differences from standard P996:

- reducing the form-factor to 3.6 by 3.8 inches;
- eliminating the need for backplanes or card cages, through its self-stacking bus;
- minimizing component count and power consumption (to typically 1-2 Watts per module), by reducing required bus drive to 6 mA.

PC/104 specifies two module versions - 8-bit and 16-bit versions - which correspond to the PC and PC/AT bus implementations, respectively.

The remainder of this specification covers the differences from the IEEE P996 specification, which is available from:

IEEE Standards Office
445 Hoes Lane
Piscataway, NJ 08854

If errors are found in this document, please send a written copy of the suggested corrections to:

PC/104 Consortium
990 Almanor Avenue
Sunnyvale, CA 94086

2. Mechanical Specifications

2.1 Module Dimensions

PC/104 modules can be of two bus types, 8-bit and 16-bit. These correspond to the PC and PC/AT buses, respectively. The detailed

mechanical dimensions of these two PC/104 bus types are provided in Appendix A.

2.2 Bus Options

As shown in the figures in Appendix A, each of the two bus types (8-bit and 16-bit) offers two bus options, according to whether or not the P1 and/or P2 bus connectors extend through the module as "stackthrough" connectors. These bus options maximize efficiency and flexibility of configurations to help meet the tight space requirements of embedded applications.

These are the differences between, and configuration issues pertaining to, the various bus options.

2.2.1 8-bit, Option 1 - Stackthrough P1

This version provides a self-stacking 8-bit PC bus. It can be placed anywhere in a multi-module stack.

2.2.2 8-bit, Option 2 - Non-Stackthrough P1

This version offers minimum module thickness, by omitting the P1 bus stackthrough pins. It must be positioned at one end of a stack. If required, additional bus expansion can be accomplished through the right-angle P1 connector. This module version cannot coexist with 16-bit stackthrough P2 version modules.

2.2.3 16-bit, Option 1 - Stackthrough P2

In this 16-bit configuration, both the P1 and P2 bus connectors are stackthrough. This version eliminates the need for a P2 daisy-chain cable. This version module cannot coexist with 8-bit non-stackthrough P1 version modules, or with 16-bit non-stackthrough P2 version modules.

2.2.4 16-bit, Option 2 - Non-Stackthrough P2

This 16-bit configuration has a stackthrough P1 bus connector and a right-angle P2 bus connector. It can be placed anywhere in a multi-module stack, and coexist with 8-bit, stackthrough P1 version modules. A short ribbon cable is normally used to daisy-chain the P2 bus connectors of the 16-bit modules in a stack.

2.3 Typical Module Stack

Figure 1 illustrates a typical module stack of 8-bit modules, and shows the use of the "stackthrough" and "non-stackthrough" P1 bus connector options.

5 3. Electrical Specifications

3.1 Signal Functions and Assignments

3.1 Signal Definitions

All PC/104 bus signals are identical in definition and function to their P996 counterparts.

10 3.1.2 Signal Assignments

Signals are assigned in the same order as on the edgecard of P996, but transformed to the corresponding header connector pins. Signal assignments for the J1/P1 and J2/P2 connectors are given in Appendix B.

15 3.1.3 Added Grounds

Several ground pins have been added, to maximize bus integrity. See Appendix B.

3.1.4 Key Locations

20 Key locations consisting of omitted pins on P1 and P2, and plugged holes on J1 and J2, have been designated on each bus connector, to help assure proper connector mating. See Appendix B.

3.2 AC Signal Timing

All PC/104 bus signals are identical in signal timing to their P996 counterparts.

25 3.3 DC Signal Levels

All PC/104 bus signal DC logic high and logic low voltage levels are identical to their P996 counterparts.

3.4 Bus Drive Current

30 To reduce component count and minimize power consumption and heat dissipation, most bus signals have a reduce drive requirement of 6 mA. The exception is open collector driven signals which must have 330 ohm pullup resistors defined by the P996 specification. This allows direct driving of the bus by many ASIC devices, and by HCT family logic.

Specifically, the following signals must be driven with devices capable of providing 20 mA sink current (as indicated in P996):

- MEMCS16*
- IOCS16*
- 5 MASTER*
- ENDXFR*

All other signals may be driven with devices capable of providing 6 mA sink current.

3.5 Interrupt-Sharing Option

- 10 The P996 specification briefly mentions an optional means to share a single bus interrupt line among multiple interrupting devices. Appendix C provides a design guideline which can help assure compatibility of interrupt-sharing among PC/104 modules.

3.6 Bus Termination Option

- 15 As in P996, termination of at least the control signals is recommended, to increase data integrity and system reliability. When termination is included, AC termination networks must be used to provide termination close to the characteristic impedance of the signal lines without exceeding the DC output current capabilities of the drivers.
- 20 As in the P996 specification, the recommended network consists of a resistor-capacitor network of 40-60 ohms in series with 30-70 pF, connected between each bus signal and ground.

Appendix B. PC/104 Bus Signal Assignments

	Pin Number	J1/P1 Row A	J1/P1 Row B	J2/P2 Row A	J2/P2 Row B
5	0	-	-	0 V	0 V
	1	IOCHCHK*	0 V	SBHE*	MEMCS16*
	2	SD7	RESETDRV	LA23	IOCS16*
	3	SD6	+5 V	LA22	IRQ10
	4	SD5	IRQ9	LA21	IRQ11
10	5	SD4	-5 V	LA20	IRQ12
	6	SD3	DRQ2	LA19	IRQ15
	7	SD2	-12 V	LA18	IRQ14
	8	SD1	ENDXFR*	LA17	DACK0*
	9	SD0	+12 V	MEMR*	DRQ0
15	10	IOCHRDY	(KEY)	MEMW*	DACK0*
	11	AEN	SMEMW*	SD8	DRQ5*
	12	SA19	SMEMR*	SD9	DACK8*
	13	SA18	IOW*	SD10	DRQ6
	14	SA17	IOR*	SD11	DACK7*
20	15	SA16	DACK3*	SD12	DRQ7*
	16	SA15	DRQ3	SD13	+5 V
	17	SA14	DACK1*	SD14	MASTER*
	18	SA13	DRQ1	SD15	0 V
	19	SA12	REFRESH*	(KEY)	0 V
25	20	SA11	SYCLK	-	-
	21	SA10	IRQ7	-	-
	22	SA9	IRQ6	-	-
	23	SA8	IRQ5	-	-
	24	SA7	IRQ4	-	-
30	25	SA6	IRQ3	-	-
	26	SA5	DACK2*	-	-
	27	SA4	TC	-	-
	28	SA3	BALE	-	-

			18		
29	SA2	+5 V	-	-	
30	SA1	OSC	-	-	
31	SA0	0 V	-	-	
32	0 V	0 V	-	-	

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Notes:

1. Rows C and D are not used on 8-bit modules.
2. P2 has two connector options with differing physical pinout orientation.
3. B10 and C19 are key locations.
- 10 4. Signal timing and function are as specified in P996.
5. Signal source/sink current differ from P996 values.

Appendix C. Interrupt-Sharing Option

A.1 Introduction

The Interrupt Request lines (IRQn's) on the P996 bus are active high. Consequently, the usual technique of wire-oring open collector driven active low bus signals cannot be used for interrupt sharing in the PC bus architecture.

A.2 Recommended Circuit

A circuit similar to that shown in the figure below can provide interrupt-sharing of the active high IRQ signals on the P996 bus, given a few system-level restrictions (see below).

NOTE: This recommendation does not comply with the P996 specification, since it is not possible to implement interrupt-sharing in a P996 compatible manner.

A.3 Restrictions

All bus devices sharing a common interrupt must be equipped with a suitable interrupt-sharing circuit (see Figure above), and must meet the following two restrictions:

The interrupt line being shared must not have a pullup resistance (to +5 volts) smaller than 10K ohms anywhere in the system. (Typically, the pullup resistance is located on the CPU module, so this is generally a restriction on the design of the CPU module.). Resistive bus termination will generally violate this restriction; use AC termination instead.

The interrupt line being shared must have one (and only one) pulldown resistor (1 Kohms) connected between the IRQ line and ground. Resistive bus termination will generally violate this restriction; use AC termination instead.

A.4 "P996 Compatibility" Option

The P996 specification calls for using a 2.2 K pullup resistor on each of the IRQ lines, which violates the 10 K minimum resistance allowed with the recommended interrupt-sharing circuit. In systems having this value of pullup, devices with the circuit shown in the above figure can be made compatible by disabling their interrupt-sharing circuit. This is

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accomplished by unshorting both JP1 and JP2, resulting in a normal P996 (non-shared) interrupt configuration (but with reduced bus drive common to other PC/104 bus signals.)

Claims

1. Apparatus for determining the present position of, or time of observation by, an observer on or in the vicinity of the Earth's surface, the apparatus comprising:
- 5 a PC/104/SATPS Card, built compatible with PC/104 standards, that receives and processes Satellite Positioning System (SATPS) signals from one or more SATPS satellites, the PC/104/SATPS Card comprising:
- 10 an SATPS antenna positioned to receive SATPS signals from one or more SATPS satellites, with each signal being characteristic of a particular satellite, and to issue these signals as antenna output signals;
- a radiofrequency downconverter to receive the antenna output signals, to convert the primary frequency of each of these signals to a selected lower frequency, and to issue these down-converted signals as
- 15 downconverter output signals;
- a programmed digital signal processor and associated memory that receives the downconverter output signals corresponding to each SATPS signal received by the antenna, determines the present location of, or time of observation by, the antenna, and issues these signals as
- 20 processor output signals; and
- an information transfer module that receives the digital signal processor output signals and transmits these output signals to an electronic device that is linked to, but not a part of, the PC/104/SATPS Card, for further signal processing or for display of the location of, or time of
- 25 observation by, the antenna.
2. The apparatus of claim 1, further comprising signal buffer means, connected between said antenna and said frequency downconverter, for receiving and temporarily storing said SATPS signals until said signals
- 30 can be processed by said digital signal processor.
3. The apparatus of claim 1, further comprising signal buffer means, connected between said frequency downconverter and said digital

signal processor, for receiving and temporarily storing said SATPS signals until said signals can be processed by said digital signal processor.

4. The apparatus of claim 1, further comprising signal format
5 translator means, connected to said digital signal processor, for receiving said SATPS signals and converting said signals into a format that can be accepted and processed by said digital signal processor.

5. Apparatus for determining the present location of, or time of
10 observation by, an observer on or in the vicinity of the Earth's surface, the apparatus comprising:

a PC/104/SATPS card, built compatible with PC/104 standards, that receives and processes Satellite Positioning System (SATPS) signals from one or more SATPS satellites, the PC/104/SATPS card comprising:

15 an SATPS antenna positioned to receive SATPS signals from one or more SATPS satellites, with each signal being characteristic of a particular satellite, and to issue these signals as antenna output signals;

a radiofrequency downconverter to receive the antenna output
signals, to convert the primary frequency of each of these signals to a
20 selected lower frequency, and to issue these down-converted signals as downconverter output signals;

a programmed digital signal processor and associated memory
that receives the downconverter output signals corresponding to each
SATPS signal received by the antenna, determines the present location of,
25 or time of observation by, the antenna, and issues these signals as processor output signals; and

an image display module that receives the digital signal
processor output signals and displays the present location of, or time of
observation by, the antenna in a visually perceptible manner.

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6. The apparatus of claim 5, further comprising signal buffer means, connected between said antenna and said frequency downconverter,

for receiving and temporarily storing said SATPS signals until said signals can be processed by said digital signal processor.

5 7. The apparatus of claim 5, further comprising signal buffer means, connected between said frequency downconverter and said digital signal processor, for receiving and temporarily storing said SATPS signals until said signals can be processed by said digital signal processor.

10 8. The apparatus of claim 5, further comprising signal format translator means, connected to said digital signal processor, for receiving said SATPS signals and converting said signals into a format that can be accepted and processed by said digital signal processor.

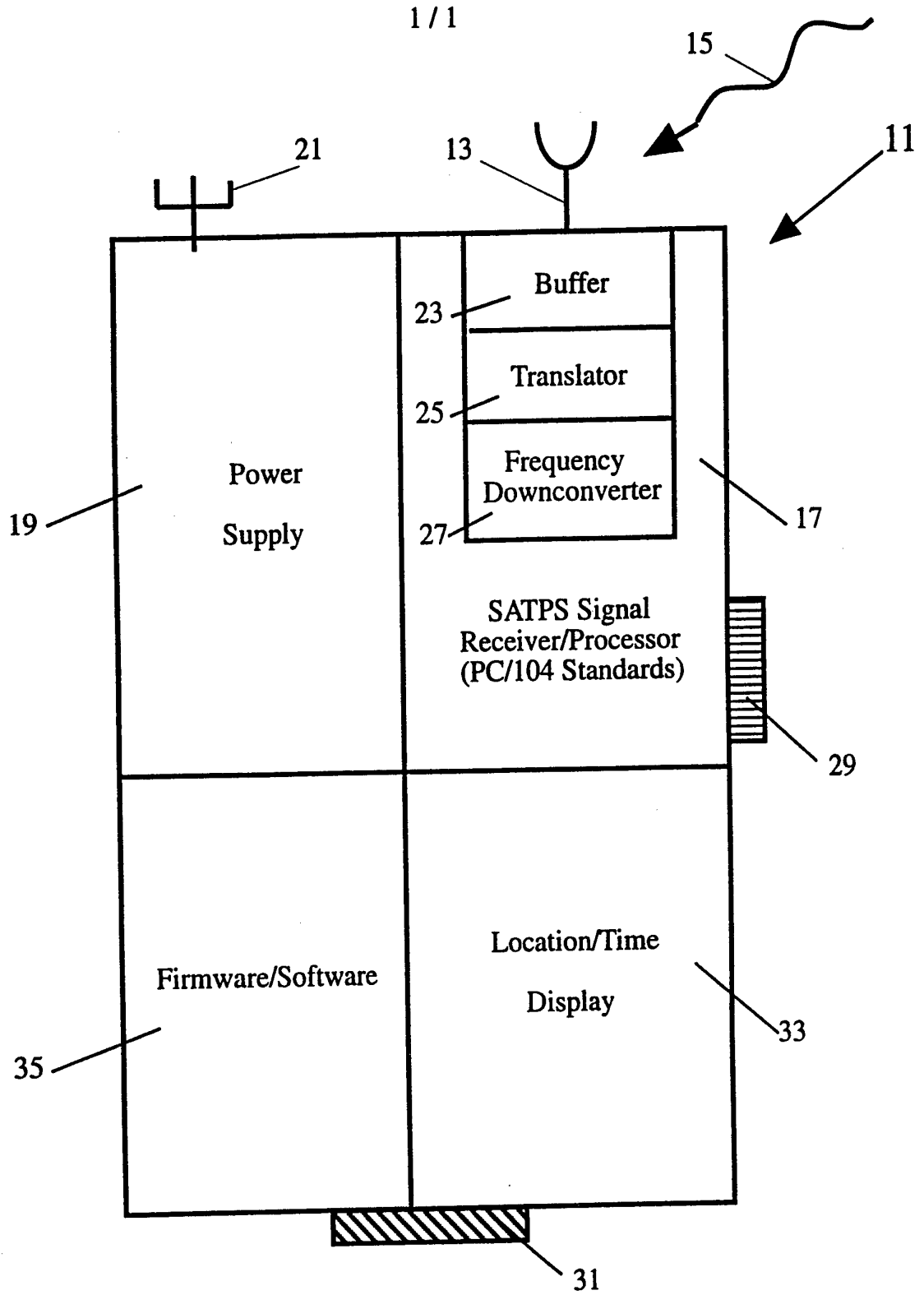


FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/06013

A. CLASSIFICATION OF SUBJECT MATTER IPC(5) :G01C 21/00; G06F 15/50 US CL :364/449 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 364/449, 443, 460; 342/450, 451; 340/988, 990, 991, 995; 73/178R Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) IEEE CD-ROM DATABASE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, P	US, 5,270,936 (Fukushima et al.) 14 December 1993, figure 2; col. 1, line 45 through col. 2, line 4.	1-8
Y, P	US, 5,268,844 (Carver et al.) 7 December 1993, col. 1, line 62 through col. 4, line 48.	1-8
Y	US, 5,185,610 (Ward et al.) 9 February 1993, figure 5; col. 18, line 43 through col. 19, line 7.	1-8
A	US, 5,214,757 (Mauney et al.) 25 May 1993, figure 1; col. 2, lines 54-55.	1-8
A	US, 5,34,407 (Lorenz et al.) 28 July 1992, col. 1, lines 10-23.	1-8
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: *A* document defining the general state of the art which is not considered to be part of particular relevance *E* earlier document published on or after the international filing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) *O* document referring to an oral disclosure, use, exhibition or other means *P* document published prior to the international filing date but later than the priority date claimed *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art *Z* document member of the same patent family		
Date of the actual completion of the international search 07 JULY 1994		Date of mailing of the international search report 19 AUG 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-9564		Authorized officer KEVIN TESKA <i>B. Nardella for</i> Telephone No. (703) 305-9704

INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US94/06013

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, 5,119,504 (Durboraw, III) 2 June 1992, figure 1.	1-8
A	US, 5,075,693 (McMillan et al.) 24 December 1991, col. 4, lines 19-22.	1-8