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(54) **SEMICONDUCTOR SWITCH**

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(57) **ABSTRACT**

The present invention, which aims at providing a semiconductor switch capable of reducing harmonic distortion, is made up of: an input terminal **101**; an output terminal **102**; a through FET **106** that is connected serially to the signal path between the input terminal **101** and the output terminal **102**; a shunt FET **107** that is connected in between the output terminal **102** and the ground; and a distortion reducing circuit **120** that is connected in parallel with the through FET **106**. In this semiconductor switch, the distortion reducing circuit **120** includes: a first diode **109** and a second diode **110** that are placed in parallel with each other; a first constant voltage source **111** and a second constant voltage source **112** that are placed in parallel with each other; and a FET **108**.

FIG. 1

501   502
503
505
507
504
508   506

FIG. 2

104   115   108   112   110
120
101   102
103   106
113   107
105   114

FIG. 3

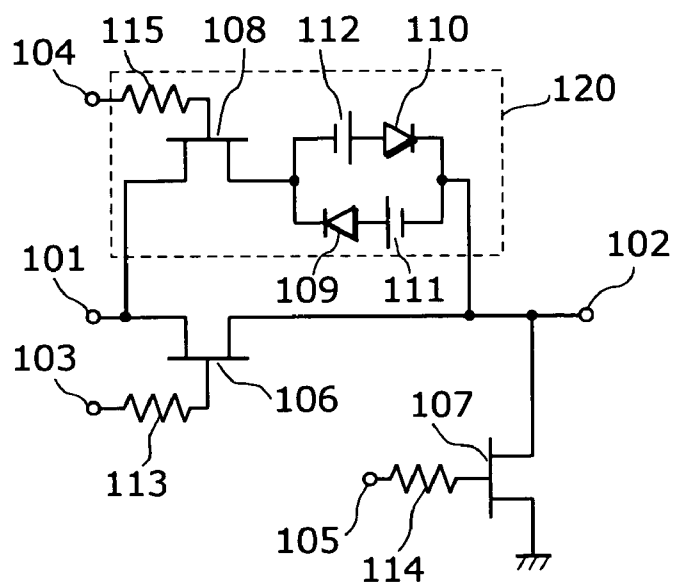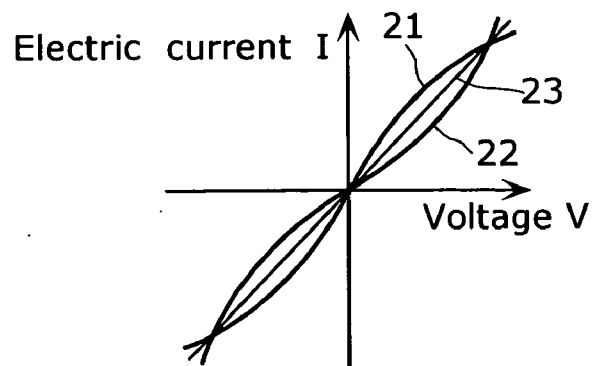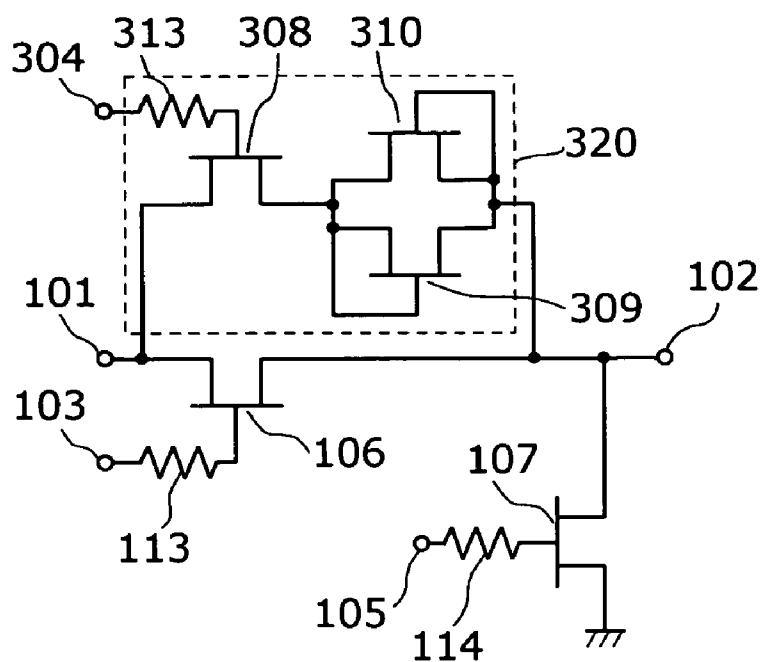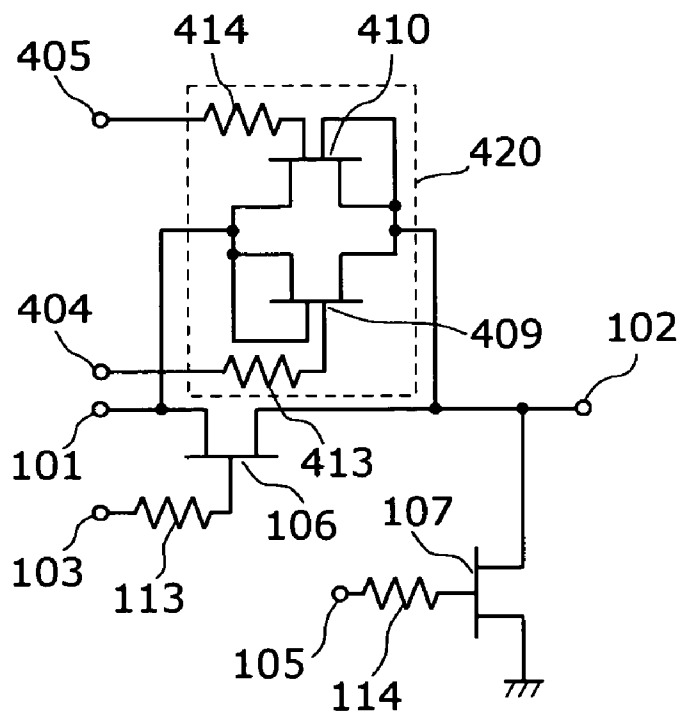Electric current I   21
23
22
Voltage V

FIG. 4

FIG. 5

SEMICONDUCTOR SWITCH

BACKGROUND OF THE INVENTION

[0001] (1) Field of the Invention

[0002] The present invention relates to a semiconductor switch for use with a mobile communication device, and particularly to a high-frequency semiconductor switch that is used for switching between signal transmission and reception in an antenna of a mobile phone or the like.

[0003] (2) Description of the Related Art

[0004] With the recent developments in the field of mobile communications, a small, low-power high-frequency semiconductor switch has been desired as a semiconductor switch dedicated to switching between signal transmission and reception in an antenna of a mobile phone or the like. In these days, a semiconductor switch that utilizes a gallium arsenide field-effect transistor that is superior in terms of power consumption is used instead of the mainstream semiconductor switch that utilizes a silicon PIN diode.

[0005] The following describes a high-frequency semiconductor switch that utilizes such a field-effect transistor (FET). **FIG. 1** is a circuit diagram showing a conventional semiconductor switch.

[0006] This semiconductor switch is made up of an input terminal 501, an output terminal 502, a through FET 505 that allows or interrupts the transmission of a high-frequency signal between the input terminal 501 and the output terminal 502, and a shunt FET 506 that connects and disconnects the output terminal 502 and the ground. In this case, the gate electrode of the through FET 505 is connected to a control terminal 503 via a resistance 507, and the gate electrode of the shunt FET 506 is connected to a control terminal 504 via a resistance 508. These resistances 507 and 508 are inserted for the protection of the gate electrodes. In general, resistances whose resistance values are several times as great as those of the characteristic impedance of a line are selected as the resistances 507 and 508.

[0007] In the semiconductor switch with the above structure, the input terminal 501 and the output terminal 502 become connected when the through FET 505 is turned to the ON-state and the shunt FET 506 is turned to the OFF-state by applying, to the control terminal 503, a voltage higher than the pinch-off voltage of the through FET 505 and by applying, to the control terminal 504, a voltage lower than the pinch-off voltage of the shunt FET 506, respectively. Meanwhile, when the through FET 505 is turned to the OFF-state and the shunt FET 506 is turned to the ON-state, the connection of the input terminal 501 and the output terminal 502 are broken, and the output terminal 502 becomes connected to the ground.

[0008] Technologies for improving the linearity in the transmission property of such a semiconductor switch described above include, for example, a method that uses FETs with different pinch-off voltages as a through FET and a shunt FET. Japanese Laid-Open Patent application No. 07-106937 discloses a semiconductor switch using this method. This technology reduces a distortion in a semiconductor switch by controlling power leakage that occurs when the shunt FET is in the OFF-state by using, for example, a FET with a pinch-off voltage of –1.0V as the through FET

and a FET with a pinch-off voltage lower than 0.5V as the shunt FET. However, such a semiconductor switch has a problem of poor controllability of pinch-off voltage and an increase in the manufacturing costs since FETs with different pinch-off voltages are formed in the same substrate.

SUMMARY OF THE INVENTION

[0009] The conventional semiconductor switch has a problem as described below.

[0010] The current-voltage characteristics between the source and the drain of a FET in the ON-state are not completely linear. Thus, while the conventional semiconductor switch is capable of reducing a distortion attributable to the shunt FET, it cannot reduce a distortion attributable to the through FET because a harmonic distortion is generated without fail at a point in time when a high-frequency signal passes through the through FET that is connected serially to the signal path. The value of such a harmonic distortion is greater as the voltage amplitude of a high-frequency signal is larger. In the case where a semiconductor switch with such harmonic distortion is used for a mobile phone or the like, power leakage into another frequency band occurs. Thus, a semiconductor switch for use with a mobile phone or the like is particularly required to be capable of reducing harmonic distortion of a signal passing through such semiconductor switch.

[0011] The present invention has been conceived in view of the above problem, and it is an object of the present invention to provide a semiconductor switch that is capable of reducing harmonic distortion of a signal passing through such semiconductor switch.

[0012] In order to achieve the above object, the semiconductor switch according to the present invention is a semiconductor switch including a first semiconductor circuit having a nonlinear characteristic and a second semiconductor circuit having a nonlinear characteristic, each allowing or interrupting transmission of a signal, wherein the first semiconductor circuit and the second semiconductor circuit reduce each other's nonlinear characteristic. Here, a current-voltage characteristic of the first semiconductor circuit may satisfy $I1=\Sigma a_i{}^*(V1)^i$, where V1 is a voltage applied to the first semiconductor circuit, I1 is an electric current that passes through the first semiconductor circuit when the V1 is applied, and a_i is a constant, and a current-voltage characteristic of the second semiconductor circuit may satisfy $I2=\Sigma b_i{}^*(V2)^i$, where V2 is a voltage applied to the second semiconductor circuit, I2 is an electric current that passes through the second semiconductor circuit when the V2 is applied, and b_i is a constant, wherein the signs of a_j and b_j of at least one pair of a_i and b_i are different, where j is 2 or a larger integer.

[0013] Accordingly, harmonic distortion of a signal passing through the semiconductor switch is reduced since it is possible to reduce the ith-order harmonic distortion by causing the first semiconductor circuit and the second semiconductor circuit to reduce each other's absolute value of the ith order coefficient included in the power series obtained by expanding the current-voltage characteristics.

[0014] Furthermore, the first semiconductor circuit and the second semiconductor circuit may be connected in parallel with each other, the first semiconductor circuit may include

a field-effect transistor, and the second semiconductor circuit may include a diode. The diode of the second semiconductor circuit may include a first diode and a second diode that are placed in parallel with each other, wherein a forward current of the first diode may be in a direction from a signal output side to a signal input side of the second semiconductor circuit, and a forward current of the second diode may be in a direction from the signal input side to the signal output side of the second semiconductor circuit. The second semiconductor circuit may include: a first voltage generating circuit that is connected to the first diode and that shifts an ON-voltage of the first diode; and a second voltage generating circuit that is connected to the second diode and that shifts an ON-voltage of the second diode.

[0015] Accordingly, it is possible to reduce the third-order harmonic distortion of a signal passing through the semiconductor switch.

[0016] Moreover, the first semiconductor circuit and the second semiconductor circuit may be connected in parallel with each other, the first semiconductor circuit may include a field-effect transistor, and the second semiconductor circuit may include a field-effect transistor in which a gate and one of a source and a drain are short-circuited. Here, each of the first field-effect transistor and the second field-effect transistor may be a multi-gate field-effect transistor.

[0017] Accordingly, it becomes possible to provide a semiconductor switch that is easier to manufacture since the distortion reducing circuit is formed only by a FET.

[0018] Furthermore, the second semiconductor circuit may include a first field-effect transistor and a second field-effect transistor that are placed in parallel with each other, wherein a gate and one of a source and a drain of the first field-effect transistor may be short-circuited at a signal input side of the second semiconductor circuit, and a gate and one of a source and a drain of the second field-effect transistor may be short-circuited at a signal output side of the second semiconductor circuit. Here, the field-effect transistor of the second semiconductor circuit may be a multi-gate field-effect transistor.

[0019] Accordingly, it becomes possible to provide a small semiconductor switch since there is no need to be equipped with a FET dedicated to turning the distortion reducing circuit to the OFF-state. In other words, it becomes possible to provide a semiconductor switch whose chip area can be reduced.

[0020] As is obvious from the above description, the semiconductor switch according to the present invention is capable of improving the linearity of the current-voltage characteristics of the semiconductor switch since the second semiconductor circuit reduces the current-voltage characteristics of the first semiconductor circuit so as to approximate such current-voltage characteristics to be linear. In other words, it is possible for the semiconductor switch of the present invention to reduce a harmonic distortion that is generated by a high-frequency signal passing through the semiconductor switch.

[0021] The disclosure of Japanese Patent Application No. 2004-161036 filed on May 31, 2004 including specification, drawings and claims is incorporated herein by reference in its entirety.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings that illustrate a specific embodiment of the invention. In the Drawings:

[0023] FIG. 1 is a circuit diagram showing the conventional semiconductor switch;

[0024] FIG. 2 is a circuit diagram showing a semiconductor switch according to a first embodiment of the present invention;

[0025] FIG. 3 is a diagram showing the current-voltage characteristics of a through FET and a distortion reducing circuit;

[0026] FIG. 4 is a circuit diagram showing a semiconductor switch according to a second embodiment of the present invention; and

[0027] FIG. 5 is a circuit diagram showing a semiconductor switch according to a third embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] The following describes a semiconductor switch according to the preferred embodiments of the present invention with reference to the drawings.

First Embodiment

[0029] FIG. 2 is a circuit diagram showing a semiconductor switch according the first embodiment of the present invention.

[0030] Such semiconductor switch is made up of: an input terminal 101; an output terminal 102; a through FET 106 that is connected serially to the signal path between the input terminal 101 and the output terminal 102; a shunt FET 107 that is connected in between the output terminal 102 and the ground; and a distortion reducing circuit 120 that is connected in parallel with the through FET 106. Note that the through FET 106 forms a first semiconductor circuit and the distortion reducing circuit 120 forms a second semiconductor circuit.

[0031] The distortion reducing circuit 120, which is a circuit for approximating the current-voltage characteristics of the semiconductor switch to be linear, is made up of: a first diode 109 and a second diode 110 that are placed in parallel with each other; a first constant voltage source 111 and a second constant voltage source 112 that are placed in parallel with each other and that have a voltage of 0.64V, for example; and a FET 108. In this structure, the first diode 109 has reverse characteristics in the direction from the input terminal 101 to the output terminal 102, i.e., a forward current of the first diode 109 is in the direction from the output terminal 102 to the input terminal 101, whereas the second diode 110 has forward characteristics in the direction from the input terminal 101 to the output terminal 102, i.e., a forward current of the second diode 110 is in the direction from the input terminal 101 to the output terminal 102. The FET 108 serves as a switch that prevents an electric current from flowing through the distortion reducing circuit 120

when the through FET **106** turns to the OFF-state. The first constant voltage source **111** is connected to the first diode **109** so as to shift the ON voltage of the first diode **109**, whereas the second constant voltage source **112** is connected to the second diode **110** so as to shift the ON voltage of the second diode **110**. Note that the first constant voltage source **111** and the second constant voltage source **112** form a first voltage generating circuit and a second voltage generating circuit, respectively.

[0032] Here, the gate electrode of the through FET **106** is connected to the control terminal **103** via a resistance **113**, the gate electrode of the shunt FET **107** is connected to a control terminal **105** via a resistance **114**, and the gate electrode of the FET **108** is connected to a control terminal **104** via a resistance **115**. As the through FET **106**, the shunt FET **107**, and the FET **108**, FETs with a gate width of 0.5 mm, a gate length of 0.2 μm, and a pinch-off voltage of –0.7V are used, for example. As the resistances **113**, **114**, and **115**, resistances of 50 kΩ are used.

[0033] **FIG. 3** is a diagram showing the current-voltage characteristics of the through FET **106** and the distortion reducing circuit **120**.

[0034] **FIG. 3** shows that current-voltage characteristics **21** of the through FET **106** when it is in the ON-state exhibit an upward convex shape in the positive domains of electric current and voltage. This is attributable to the current-voltage characteristics peculiar to a FET. Thus, the following is derived by expanding the current-voltage characteristics **21** of the through FET **106** into power series:

$$I1 = \Sigma a_i * (V1)^i$$

$$= a_0 + a_1 * V1 + a_2 * (V1)^2 + a_3 * (V1)^3 + \ldots$$

[0035] This equation shows that the third-order coefficient a_3 is a negative value. In the above equation, V1 denotes a voltage to be applied to the through FET **106**, I1 denotes an electric current that flows through the through FET **106** when V1 is applied, and a_i (i is an integer) denotes a constant.

[0036] Meanwhile, **FIG. 3** also shows that current-voltage characteristics **22** of the distortion reducing circuit **120** that is connected in parallel with the through FET **106** exhibit a downward convex shape in the positive domains of electric current and voltage. This is attributable to the current-voltage characteristics peculiar to a diode. Thus, the following is derived by expanding the current-voltage characteristics **22** of the distortion reducing circuit **120** into power series:

$$I2 = \Sigma b_i * (V2)^i$$

$$= b_0 + b_1 * V2 + b_2 * (V2)^2 + b_3 * (V2)^3 + \ldots$$

[0037] This equation shows that the third-order coefficient b_3 is a positive value. In the above equation, V2 denotes a voltage to be applied to the distortion reducing circuit **120**, I2 denotes an electric current that flows through the distortion reducing circuit **120** when V2 is applied, and b_i (i is an integer) denotes a constant.

[0038] Consequently, in the semiconductor switch in which the through FET **106** and the distortion reducing circuit **120** are connected in parallel with each other, the through FET **106** and the distortion reducing circuit **120** reduce each other's nonlinear characteristics, resulting in a very small absolute value of a nonlinear component of the semiconductor switch that corresponds to the third-order coefficient included in the power series obtained by performing power series expansion. As a result, the current-voltage characteristics **23** of the semiconductor switch becomes closer to linear. In general, there is a correlation between (1) the absolute value of the n-th order coefficient that is derived by expanding, into power series, the current-voltage characteristics of the signal path between the input terminal and the output terminal and (2) the size of the n-th order harmonic distortion that is generated when a high-frequency power inputted from the input terminal reaches the output terminal. In other words, the greater the absolute value of the n-th order coefficient, the bigger the n-th order harmonic distortion generated at the through FET. It should be noted, however, that a range of voltages obtained by a power series expansion is equal to or lower than the range of the voltage amplitude of a maximum signal that passes through the through FET.

[0039] As described above, it is possible to provide a semiconductor switch that is capable of reducing harmonic distortion, since the semiconductor switch according to the present embodiment reduces, through the use of the distortion reducing circuit **120**, the absolute value of the third-order coefficient that is derived by expanding the current-voltage characteristics of the through FET into power series, thereby reducing the third-order harmonic distortion generated at the through FET.

[0040] For example, the following result was obtained by a simulation: in the semiconductor switch shown in **FIG. 2**, when the through FET **106** and the FET **108** are turned to the ON-state and the shunt FET **107** is turned to the OFF-state respectively by the control terminals **103**, **104**, and **105**, and then a high-frequency signal of 1 GHz and 30 dBm is inputted to the input terminal **101**, the output value representing the third-order harmonic detected at the output terminal **102** is –49 dBm; and in the conventional semiconductor switch shown in **FIG. 1** having no distortion reducing circuit, the output value representing the third-order harmonic detected at the output terminal **102** is –37 dBm. In other words, the distortion reducing circuit improves the value of the third-order harmonic distortion. Note that in the above simulation, the gate width of the through FET shown in **FIG. 1** is 1 mm.

Second Embodiment

[0041] **FIG. 4** is a circuit diagram showing a semiconductor switch according to the second embodiment of the present invention.

[0042] Such semiconductor switch is different from the semiconductor switch of the first embodiment in the structure of its distortion reducing circuit **320** that is connected in parallel with the through FET **106**. The semiconductor switch of the second embodiment is made up of an input terminal **101**, an output terminal **102**, a through FET **106**, a shunt FET **107**, and a distortion reducing circuit **320** that is connected in parallel with the through FET **106**. Note that the distortion reducing circuit **320** forms the second semiconductor circuit.

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[0043] The distortion reducing circuit 320, which is a circuit for approximating the current-voltage characteristics of the semiconductor switch to be linear, is made up of: a first FET 309 and a second FET 310 that are connected in parallel with each other; and a FET 308 that is connected serially to the first FET 309 and the second FET 310. In this structure, the gate and one of the source and the drain of the first FET 309 are short-circuited at the input terminal 101 side, whereas the gate and one of the source and the drain of the second FET 310 are short-circuited at the output terminal 102 side. The FET 308 serves as a switch that prevents an electric current from flowing through the distortion reducing circuit 320 when the through FET 106 turns to the OFF-state.

[0044] Here, the gate electrode of the FET 308 is connected to a control terminal 304 via a resistance 313.

[0045] As described above, according to the semiconductor switch of the second embodiment, it is possible to provide a semiconductor switch that is capable of reducing harmonic distortion, as in the case of the semiconductor switch of the first embodiment.

[0046] Moreover, since the distortion reducing circuit 320 of the semiconductor switch of the second embodiment does not have a voltage generating circuit, it is possible to provide a semiconductor switch that is easier to manufacture than the semiconductor switch of the first embodiment.

Third Embodiment

[0047] FIG. 5 is a circuit diagram showing a semiconductor switch according to the third embodiment of the present invention.

[0048] Such semiconductor switch is different from the semiconductor switch of the second embodiment in the structure of its distortion reducing circuit 420 that is connected in parallel with a through FET 106. The semiconductor switch of the third embodiment is made up of an input terminal 101, an output terminal 102, a through FET 106, a shunt FET 107, and a distortion reducing circuit 420 that is connected in parallel with the through FET 106. Note that the distortion reducing circuit 420 forms the second semiconductor circuit.

[0049] The distortion reducing circuit 420, which is a circuit for approximating the current-voltage characteristics of the semiconductor switch to be linear, is made up of a first dual gate FET 409 and a second dual gate FET 410 that are connected in parallel with each other. In this structure, one of the gates and the source or the drain of the first dual gate FET 409 are short-circuited at the input terminal 101 side, whereas one of the gates and the source or the drain of the second dual gate FET 410 are short-circuited at the output terminal 102 side. The other gate of the first dual gate FET 409 is connected to a control terminal 404 via a resistance 413, whereas the other gate of the second dual gate FET 410 is connected to a control terminal 405 via a resistance 414. The first dual gate 409 and the second dual gate 410 serve as switches that prevent an electric current from flowing through the distortion reducing circuit 420 when the through FET 106 turns to the OFF-state.

[0050] As described above, according to the semiconductor switch of the third embodiment, it is possible to provide

a semiconductor switch that is capable of reducing harmonic distortion, as in the case of the semiconductor switch of the first embodiment.

[0051] Moreover, it is possible to provide a small semiconductor switch since the multi-gate FETs are used in the distortion reducing circuit 420 of the semiconductor switch of the third embodiment, and thus there is no need to be equipped with a FET dedicated to preventing an electric current from flowing through the distortion reducing circuit 420. In other words, it is possible to provide a semiconductor switch whose chip area can be reduced.

[0052] Although only some exemplary embodiments of this invention have been described in detail above, those skilled in the art will readily appreciate that many modifications are possible in the exemplary embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention.

[0053] For example, the semiconductor switch according to the present invention has a distortion reducing circuit in which the sign of the third-order coefficient that is derived by expanding the current-voltage characteristics into power series, is different from that of the through FET. However, the distortion reducing circuit is not limited to this so long as the current-voltage characteristics of a distortion reducing circuit have a linear shape representing desired current-voltage characteristics, e.g., a shape that is axisymmetric to the current-voltage characteristics of the through FET with respect to the straight line going through the point of origin. Thus, the semiconductor switch may include a distortion reducing circuit in which the sign of the second or greater-order coefficient that is derived by expanding the current-voltage characteristics into power series is different from that of the through FET.

INDUSTRIAL APPLICABILITY

[0054] The present invention is suited for use as a semiconductor switch and particularly as a high-frequency semiconductor switch or the like that is used for switching between signal transmission and reception in an antenna of a mobile communication device such as a mobile phone and the like.

What is claimed is:

1. A semiconductor switch comprising

a first semiconductor circuit having a nonlinear characteristic and a second semiconductor circuit having a nonlinear characteristic, each allowing or interrupting transmission of a signal,

wherein said first semiconductor circuit and said second semiconductor circuit reduce each other's nonlinear characteristic.

2. The semiconductor switch according to claim 1,

wherein a current-voltage characteristic of said first semiconductor circuit satisfies $I1 = \Sigma a_i{}^* (V1)^i$, where V1 is a voltage applied to said first semiconductor circuit, I1 is an electric current that passes through said first semiconductor circuit when the V1 is applied, and a_i is a constant, and

a current-voltage characteristic of said second semiconductor circuit satisfies $I2 = \Sigma b_i * (V2)^i$, where $V2$ is a voltage applied to said second semiconductor circuit, $I2$ is an electric current that passes through said second semiconductor circuit when the $V2$ is applied, and b_i is a constant,

wherein the signs of a_j and b_j of at least one pair of a_i and b_i are different, where j is 2 or a larger integer.

3. The semiconductor switch according to claim 2,

wherein said first semiconductor circuit and said second semiconductor circuit are connected in parallel with each other,

said first semiconductor circuit includes a field-effect transistor, and

said second semiconductor circuit includes a diode.

4. The semiconductor switch according to claim 3,

wherein said diode of said second semiconductor circuit includes a first diode and a second diode that are placed in parallel with each other,

wherein a forward current of said first diode is in a direction from a signal output side to a signal input side of said second semiconductor circuit, and

a forward current of said second diode is in a direction from the signal input side to the signal output side of said second semiconductor circuit.

5. The semiconductor switch according to claim 4,

wherein said second semiconductor circuit includes:

a first voltage generating circuit that is connected to said first diode and that shifts an ON-voltage of said first diode; and

a second voltage generating circuit that is connected to said second diode and that shifts an ON-voltage of said second diode.

6. The semiconductor switch according to claim 2,

wherein said first semiconductor circuit and said second semiconductor circuit are connected in parallel with each other,

said first semiconductor circuit includes a field-effect transistor, and

said second semiconductor circuit includes a field-effect transistor in which a gate and one of a source and a drain are short-circuited.

7. The semiconductor switch according to claim 6,

wherein said second semiconductor circuit includes a first field-effect transistor and a second field-effect transistor that are placed in parallel with each other,

wherein a gate and one of a source and a drain of said first field-effect transistor are short-circuited at a signal input side of said second semiconductor circuit, and

a gate and one of a source and a drain of said second field-effect transistor are short-circuited at a signal output side of said second semiconductor circuit.

8. The semiconductor switch according to claim 7,

wherein each of said first field-effect transistor and said second field-effect transistor is a multi-gate field-effect transistor.

9. The semiconductor switch according to claim 6,

wherein said field-effect transistor of said second semiconductor circuit is a multi-gate field-effect transistor.

10. The semiconductor switch according to claim 1,

wherein said first semiconductor circuit and said second semiconductor circuit are connected in parallel with each other,

said first semiconductor circuit includes a field-effect transistor, and

said second semiconductor circuit includes a diode.

11. The semiconductor switch according to claim 1,

wherein said first semiconductor circuit and said second semiconductor circuit are connected in parallel with each other,

said first semiconductor circuit includes a field-effect transistor, and

said second semiconductor circuit includes a field-effect transistor in which a gate and one of a source and a drain are short-circuited.

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