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(54) **COUPLING WELL STRUCTURE FOR IMPROVING HVMOS PERFORMANCE**

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(63) Continuation of application No. 12/362,307, filed on Jan. 29, 2009, now Pat. No. 7,816,214, which is a continuation of application No. 11/594,508, filed on Nov. 8, 2006, now abandoned.

(60) Provisional application No. 60/852,183, filed on Oct. 17, 2006.

(51) **Int. Cl.**
H01L 29/02 (2006.01)

(52) **U.S. Cl.** **257/487; 257/409; 257/E29.063**

(58) **Field of Classification Search** 257/487,
257/500, 409, E29.063, E21.443
See application file for complete search history.

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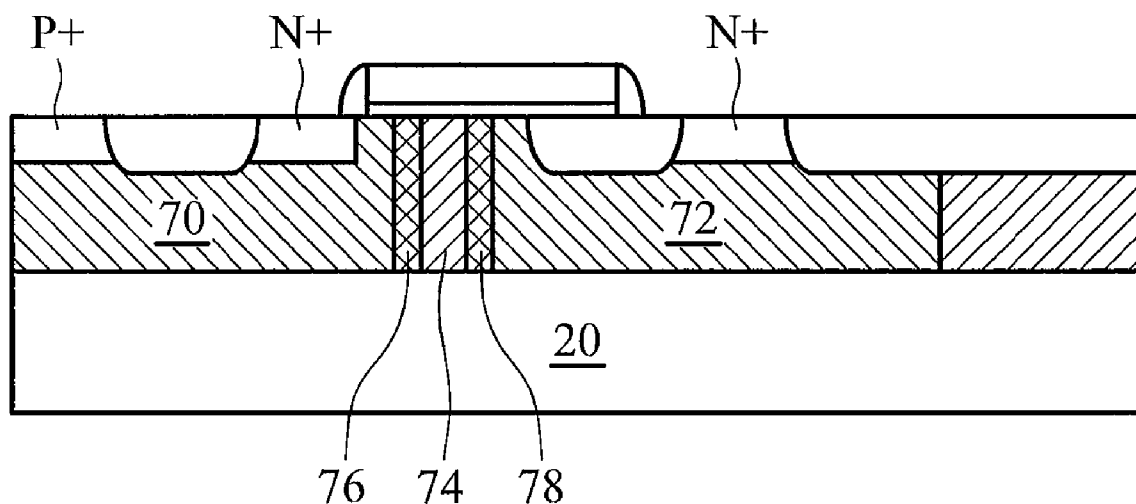
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(57) **ABSTRACT**

A semiconductor structure includes a substrate, a first well region of a first conductivity type overlying the substrate, a second well region of a second conductivity type opposite the first conductivity type overlying the substrate, a cushion region between and adjoining the first and the second well regions, an insulation region in a portion of the first well region and extending from a top surface of the first well region into the first well region, a gate dielectric extending from over the first well region to over the second well region, wherein the gate dielectric has a portion over the insulation region, and a gate electrode on the gate dielectric.

11 Claims, 7 Drawing Sheets



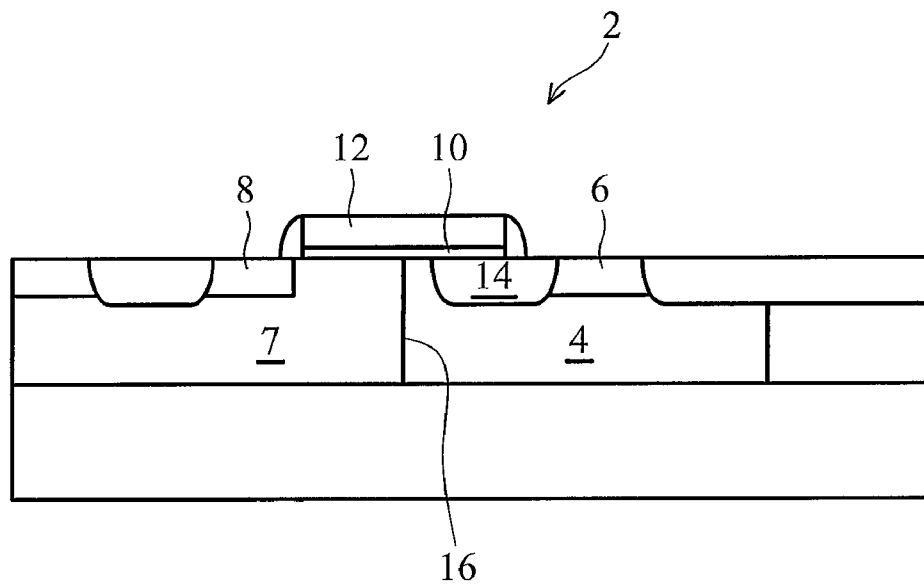


FIG. 1 (PRIOR ART)

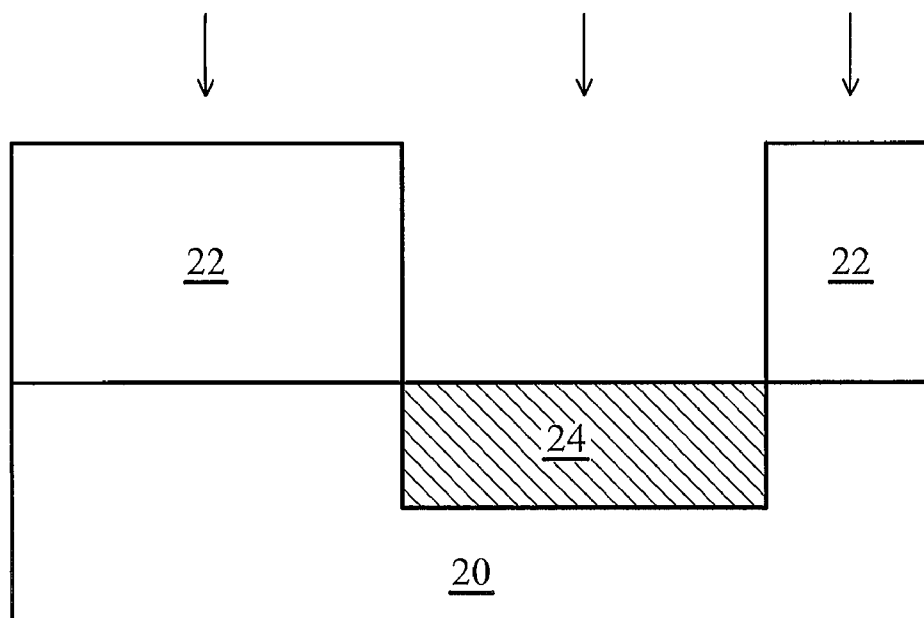


FIG. 2

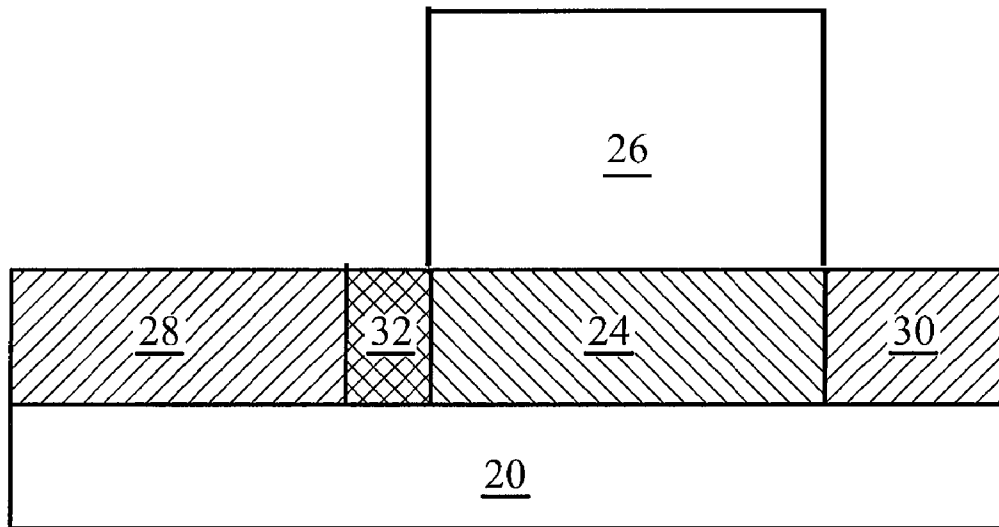


FIG. 3A

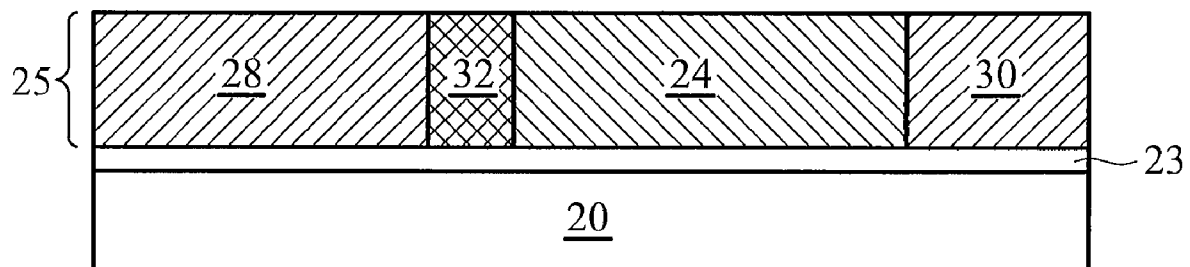


FIG. 3B

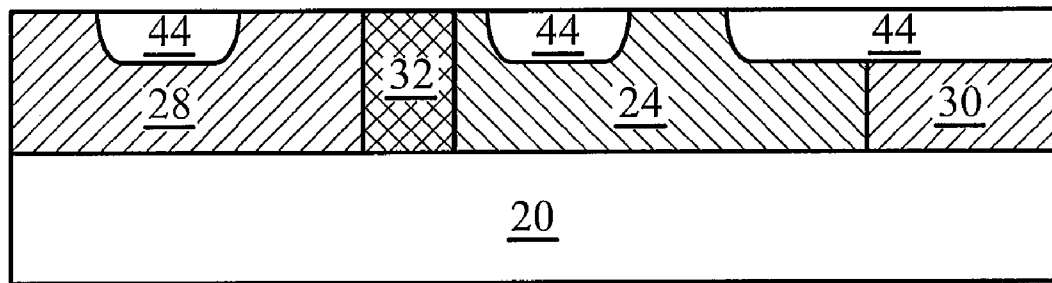


FIG. 4

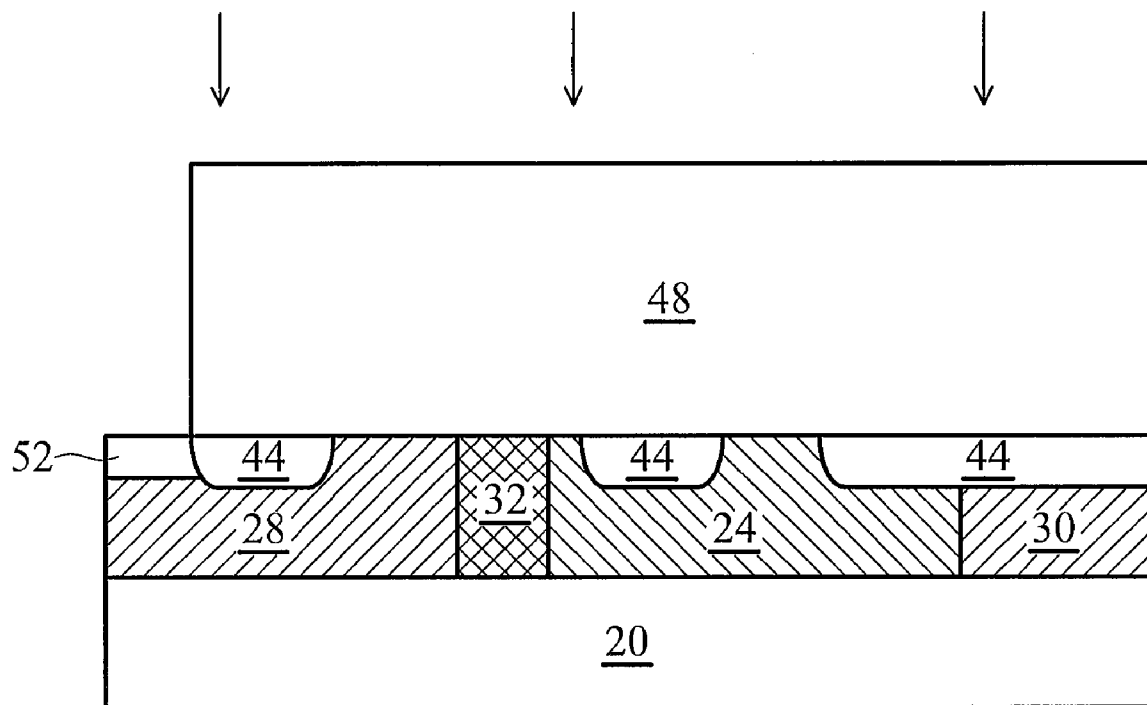


FIG. 5

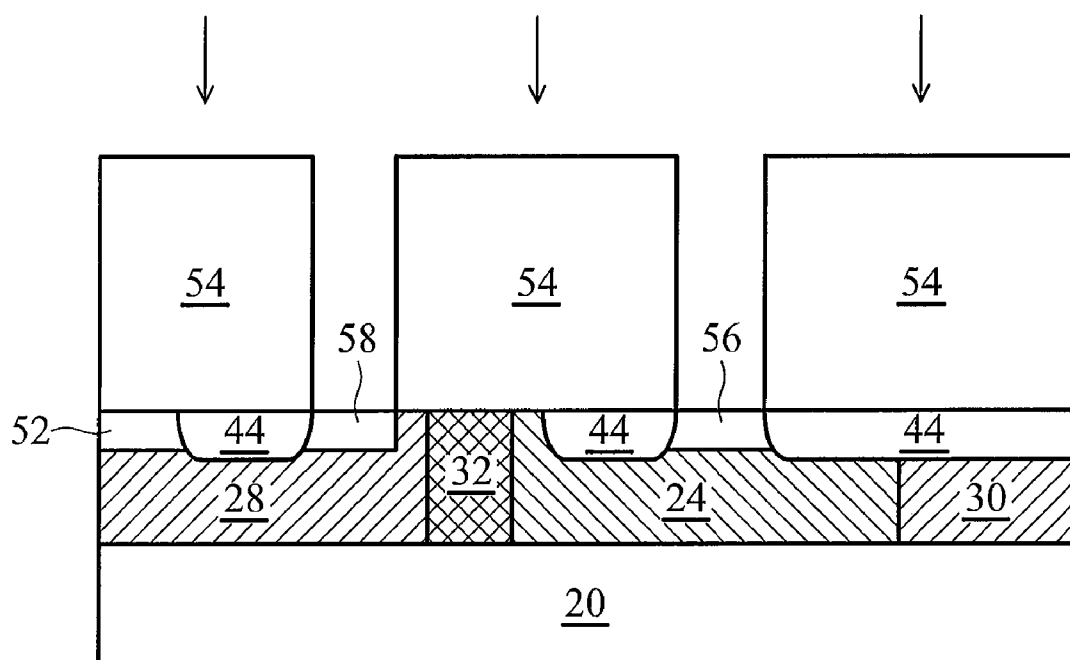


FIG. 6

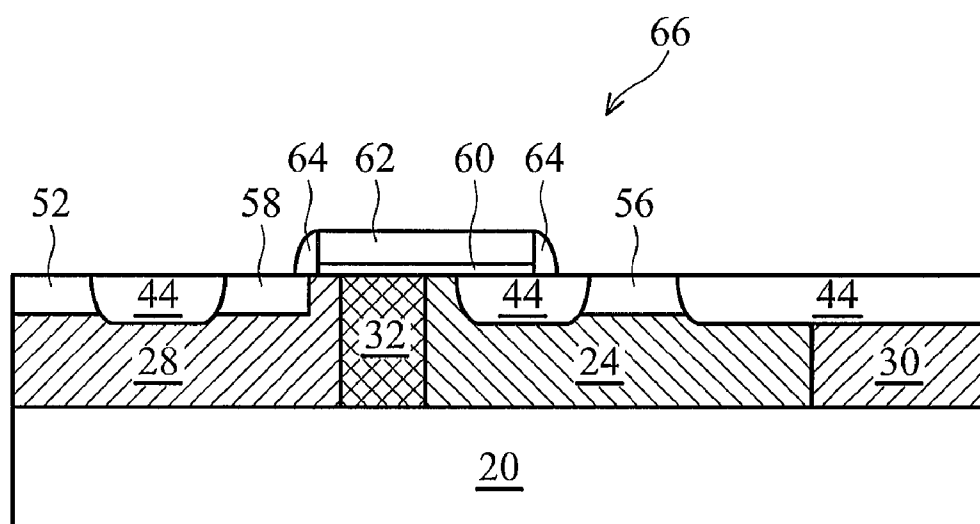


FIG. 7

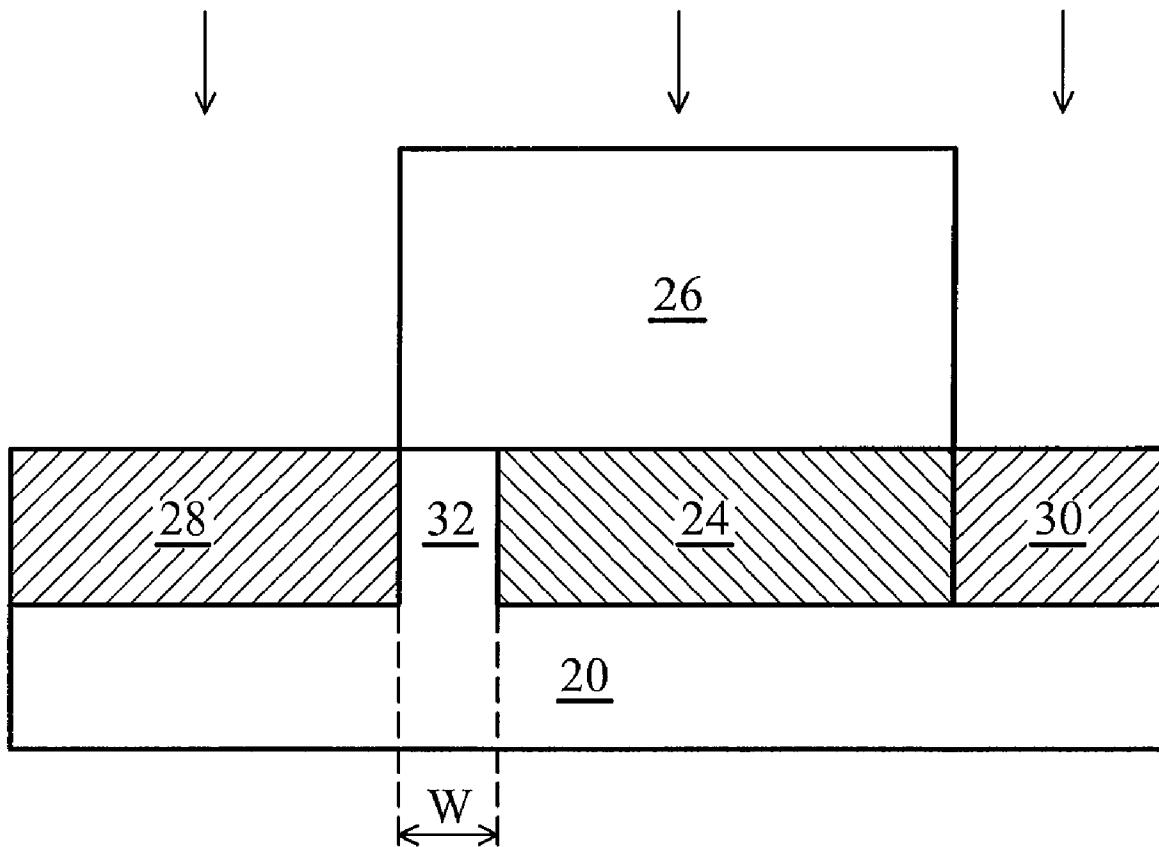


FIG. 8

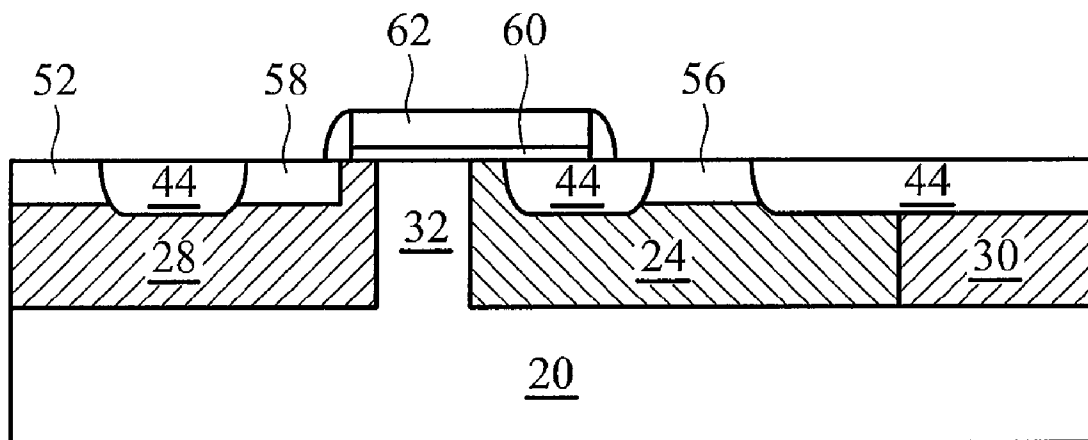


FIG. 9

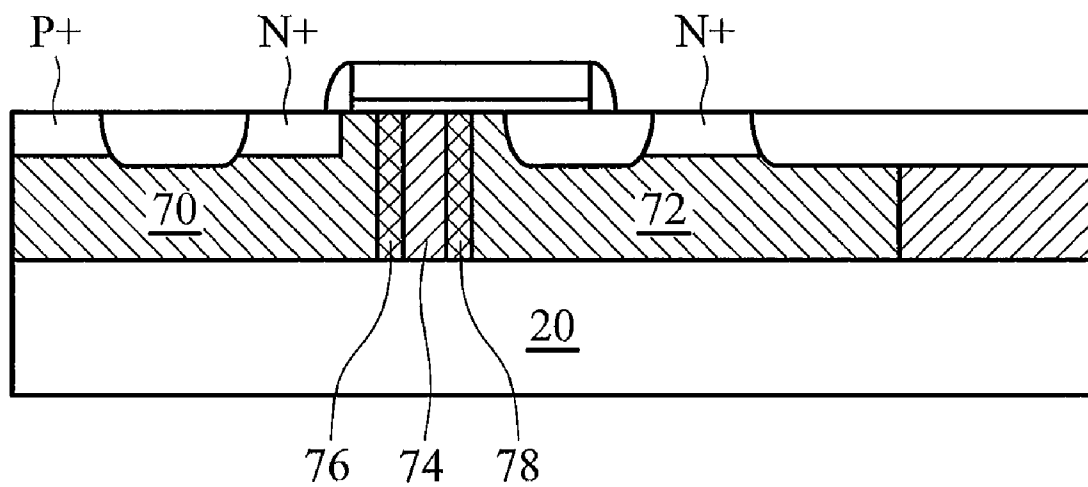


FIG. 10

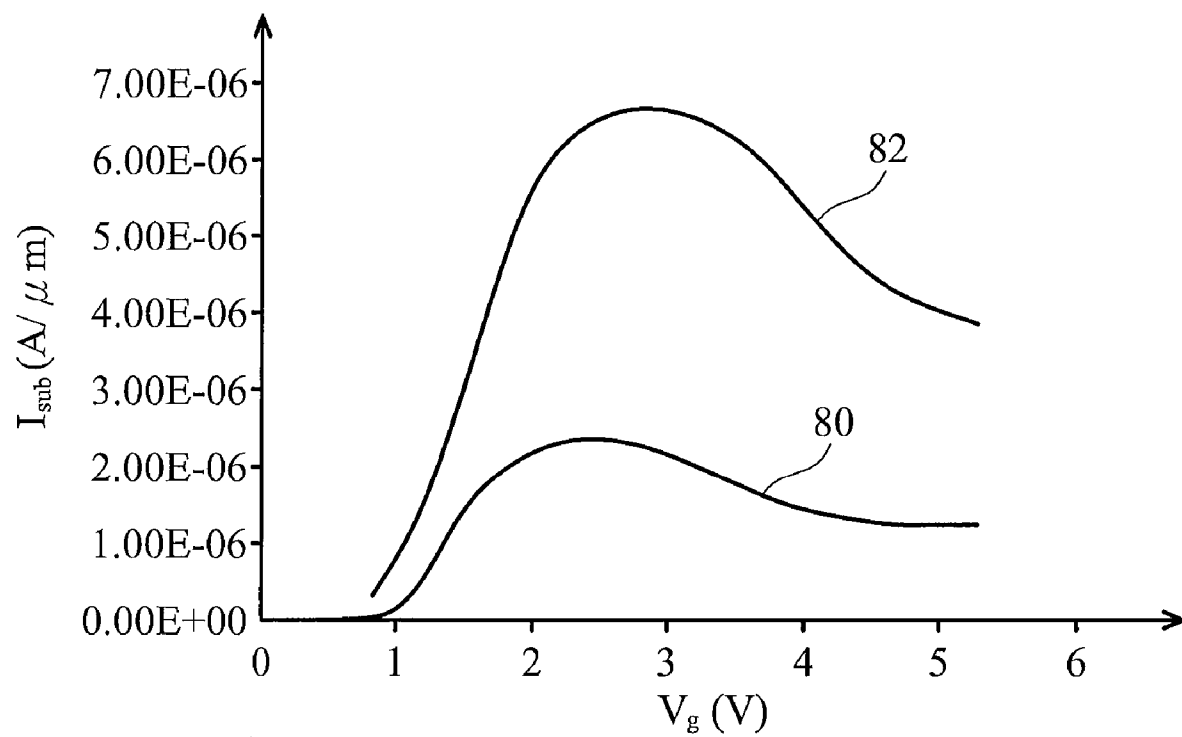


FIG. 11

1

COUPLING WELL STRUCTURE FOR IMPROVING HVMOS PERFORMANCE

This application is a continuation of U.S. patent application Ser. No. 12/362,307, filed Jan. 29, 2009, and entitled "Coupling Well Structure for Improving HVMOS Performance," which further claims the benefit of U.S. patent application Ser. No. 11/594,508, filed Nov. 8, 2006, and entitled "Coupling Well Structure for Improving HVMOS Performance," which claims the benefit of U.S. Provisional Application No. 60/852,183, filed on Oct. 17, 2006, entitled "Coupling Well Structure for Improving HVMOS Performance," which applications are hereby incorporated herein by reference.

TECHNICAL FIELD

This invention relates generally to semiconductor devices, and more particularly to metal-oxide-semiconductor (MOS) devices, and even more particularly to the structure and manufacturing methods of high-voltage MOS devices.

BACKGROUND

High-voltage metal-oxide-semiconductor (HVMOS) devices are widely used in many electrical devices, such as input/output (I/O) circuits, CPU power supplies, power management systems, AC/DC converters, etc. HVMOS devices typically include drain regions and laterally-diffused drain regions enclosing drain regions. Laterally-diffused drain regions are typically well regions having lower doping concentrations than the drain regions, thus having high breakdown electrical fields.

FIG. 1 illustrates a conventional HVNMOS device 2, which includes gate oxide 10, gate electrode 12 on gate oxide 10, drain region 6 in n-well region 4, and source region 8 in p-well region 7. Shallow trench isolation (STI) region 14 spaces drain region 6 apart from gate electrode 12 so that a high drain-to-gate voltage can be applied.

It is known that high electrical fields are typically generated at interface regions. For HVNMOS device 2, when a high voltage is applied between drain region 6 and source region 8, a high electrical field is generated at a region proximate p-n junction 16, which becomes the weak point of the HVNMOS device 2. The generation of the high electrical field causes the reduction in breakdown voltage of HVNMOS device 2. This problem worsens when the device dimensions become smaller, and thus the electrical fields become higher.

Novel methods for reducing electrical fields at p-n junctions are thus needed to improve breakdown voltages of high-voltage MOS devices.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a semiconductor structure includes a substrate, a first well region of a first conductivity type overlying the substrate, a second well region of a second conductivity type opposite the first conductivity type overlying the substrate, a cushion region between and adjoining the first and the second well regions, an insulation region in a portion of the first well region and extending from a top surface of the first well region into the first well region, a gate dielectric extending from over the first well region to over the second well region, wherein the gate dielectric has a portion over the insulation region, and a gate electrode on the gate dielectric.

2

In accordance with another aspect of the present invention, a semiconductor structure includes a substrate, a first well region of a first conductivity type overlying the substrate, a second well region of a second conductivity type opposite the first conductivity type overlying the substrate, wherein the first and the second well regions have an overlap region, an insulation region extending from a top surface of the first well region into the first well region, a gate dielectric extending from over the first well region to over the second well region, wherein the gate dielectric has an edge directly over the insulation region, and a gate electrode on the gate dielectric.

In accordance with yet another aspect of the present invention, a semiconductor structure includes a substrate, a first well region having a first impurity of a first conductivity type overlying the substrate, a second well region having a second impurity of a second conductivity type opposite the first conductivity type overlying the substrate, wherein the first and the second well regions have a space therebetween, an insulation region in a portion of the first well region and extending from a top surface of the first well region into the first well region, a gate dielectric extending from over the first well region to over the second well region, wherein the gate dielectric has an edge directly over the insulation region, and a gate electrode on the gate dielectric.

In accordance with yet another aspect of the present invention, a method of forming a semiconductor structure includes providing a substrate, forming a first well region of a first conductivity type overlying the substrate, forming a second well region of a second conductivity type opposite the first conductivity type overlying the substrate, wherein a cushion region is formed adjoining the first and the second well regions, forming an insulation region in a portion of the first well region and extending from a top surface of the first well region into the first well region, forming a gate dielectric extending from over the first well region to over the second well region, wherein the gate dielectric has a portion over the insulation region, and forming a gate electrode on the gate dielectric.

In accordance with yet another aspect of the present invention, a method of forming a semiconductor structure includes providing a substrate, forming a first well region of a first conductivity type overlying the substrate, forming a second well region of a second conductivity type opposite the first conductivity type overlying the substrate, wherein the first and the second well regions have an overlap region, forming an insulation region in a portion of the first well region and extending from a top surface of the first well region into the first well region, forming a gate dielectric extending from over the first well region to over the second well region, wherein the gate dielectric has an edge directly over the insulation region, and forming a gate electrode on the gate dielectric.

The cushion region between the p-well region and the n-well region increases the breakdown electrical field at the interface region of the p-well region and the n-well region. The breakdown voltage of the respective high-voltage device is thus increased.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates a conventional HVNMOS device;

FIGS. 2 through 7 are cross-sectional views of intermediate stages in the manufacture of a first embodiment of the

3

present invention, wherein a cushion region is formed by overlapping a p-well region and an n-well region;

FIGS. 8 and 9 illustrate a second embodiment of the present invention, wherein a cushion region formed by spacing a p-well region apart from an n-well region;

FIG. 10 illustrates a symmetric embodiment of the present invention; and

FIG. 11 illustrates a comparison between substrate currents of a conventional high-voltage MOS device and an embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

The preferred embodiments of the present invention are described with reference to FIGS. 1 through 7. Variations of the preferred embodiments are then discussed. Throughout the various views and illustrative embodiments of the present invention, like reference numbers are used to designate like elements.

Referring to FIG. 2, substrate 20 is provided. Substrate 20 preferably includes a semiconductor material such as silicon, SiGe, or a compound of group III and group IV elements. Substrate 20 may be a bulk material or have a silicon-on-insulator (SOI) structure. Preferably, substrate 20 is lightly doped with a p-type impurity, although it can also be doped with an n-type impurity.

FIG. 2 also illustrates the formation of n-well region 24. Photoresist 22 is first applied and patterned. In the preferred embodiment, n-well region 24 is implanted with n-type impurities, such as phosphorous and/or arsenic. Preferably, n-well region 24 is a high-voltage n-well region, which has a low impurity concentration. In alternative embodiments, n-well region 24 is a low-voltage n-well (LVNW) region that is formed simultaneously with the formation of the n-well regions of low-voltage PMOS devices (not shown). In an exemplary embodiment, the n-type impurity concentration in n-well region 24 is between about $10^{14}/\text{cm}^3$ to about $10^{17}/\text{cm}^3$. After the formation of n-well region 24, photoresist 22 is removed.

Referring to FIG. 3A, photoresist 26 is applied, and p-well regions 28 and 30 are formed, which are implanted with p-type impurities, such as boron and/or indium. Preferably, p-well regions 28 and 30 are high-voltage n-well regions with a low impurity concentration. In alternative embodiments, p-well regions 28 and 30 are low-voltage p-well (LVPW) regions that are formed simultaneously with the formation of the p-well regions of low-voltage NMOS devices (not shown). In an exemplary embodiment, the p-type impurity concentration in p-well regions 28 and 30 is between about $10^{14}/\text{cm}^3$ to about $10^{17}/\text{cm}^3$. After the formation of p-well regions 28 and 30, photoresist 26 is removed.

In the embodiments discussed in preceding paragraphs, p-well regions 28 and 30 and n-well region 24 are formed by implanting substrate 20. In alternative embodiments, the well regions are formed by epitaxial growth. In an exemplary embodiment, as shown in FIG. 3B, an N+ buried layer (NBL) 23 is formed in a top region of the substrate 20. NBL 23 is preferably formed by implanting or in-situ doping impurities into the top surface of substrate 20. For example, antimony

4

and/or arsenic may be implanted or in-situ doped to an impurity concentration of about $10^{16}/\text{cm}^3$ to about $10^{18}/\text{cm}^3$.

An epitaxial layer 25 is then epitaxially grown on NBL 23. Epitaxial layer 25 preferably comprises a semiconductor such as silicon, and more preferably the same material as substrate 20, and is preferably doped with one of the p-type and n-type impurities. Assuming p-type impurities are doped, the impurity concentration is then equal to the desired concentration of p-well regions 28 and 30. A photoresist (not shown) is then formed and patterned, exposing region 24. An n-type impurity implantation is then performed. The implanted n-type impurity neutralizes the p-type impurities in epitaxial layer 25 and converts the implanted region to n-well region 24. Un-implanted epitaxial regions thus form p-well regions 28 and 30. Alternatively, the epitaxial layer 25 may be doped with n-type impurities when grown, and implanted with p-type impurities.

In both FIGS. 3A and 3B, p-well region 28 and n-well region 24 have an overlap region 32, which is referred to as cushion region 32 hereinafter. Preferably, width C of cushion region 32 is between about 10 Å and about 3 μm, and more preferably between about 0.3 μm and about 0.5 μm.

FIG. 4 illustrates the formation of insulation regions 44. In the preferred embodiment, insulation regions 44 are formed by forming shallow trenches, filling the trenches with a dielectric material, such as high-density plasma (HDP) oxide, and performing a chemical mechanical polish to remove excess dielectric material. The resulting shallow trench isolation (STI) regions are insulation regions 44. In other embodiments, a mask layer (not shown), for example, a SiN layer, is formed over the previously formed structure. The mask layer is then patterned to form openings. An oxidation is then performed, and insulation regions (also referred to as field oxides) 44 are formed in the openings.

Referring to FIG. 5, photoresist 48 is applied and patterned. A p-type impurity implantation is performed, forming P+ region 52. Preferably, P+ region 52 comprises boron and/or other p-type impurities, and is heavily doped to a concentration of greater than about $10^{20}/\text{cm}^3$. P+ region 52 may act as the pick-up region of the p-well region 28. After the implantation, photoresist 48 is removed.

Referring to FIG. 6, photoresist 54 is applied and patterned, and an n-type impurity implantation is performed, forming N+ regions 56 and 58. The implanted impurities may comprise phosphorus and/or arsenic. Preferably, the n-type impurities are heavily doped to a concentration of greater than about $10^{20}/\text{cm}^3$. N+ regions 56 and 58 act as a drain contact region and source region, respectively. Photoresist 54 is then removed.

Alternatively, N+ regions 56 and 58 may be formed before the formation of P+ region 52, or formed after the formation of gate dielectric, gate electrode and gate spacers. One skilled in the art will realize the respective process steps.

FIG. 7 illustrates the formation of gate dielectric 60, gate electrode 62 and gate spacers 64. As is known in the art, gate dielectric 60 preferably comprises silicon oxide, although other dielectric materials such as silicon nitride, silicon carbide, silicon oxynitride, combinations thereof, and multi-layers thereof, can be used. Gate electrode 62 preferably includes doped polysilicon. Alternatively, metals, metal nitrides, metal silicides, and other conductive materials can be used. Gate spacers 64 are preferably formed by blanket forming a dielectric material, and removing undesired portions from horizontal surfaces. The details for forming gate dielectric 60, gate electrode 62 and gate spacers 64 are well known in the art, and thus are not repeated herein. Preferably,

5

an edge of gate electrode 62 is located directly over insulation region 44 in n-well region 24. HVNMOS device 66 is thus formed.

A second embodiment of the present invention is illustrated in FIGS. 8 and 9. This embodiment is similar to the embodiment shown in FIG. 7, except that cushion region 32 is a space between p-well region 28 and n-well region 24. In an exemplary embodiment, a structure as shown in FIG. 2 is formed. Photoresist 26, as shown in FIG. 8 is then formed for the formation of p-well regions 28 and 30. P-well region 28 and n-well region 24 are thus spaced apart, forming cushion region 32. It is to be realized that impurities in n-well region 24 and p-well region 28 are likely to diffuse into cushion region 32. However, the diffused impurity concentration will be low compared to the impurity concentrations in respective n-well region 24 and p-well region 28. In an exemplary embodiment, the p-type and n-type impurities diffuse into cushion region 32 and form a p-n junction therein. The ratios of p-type and n-type impurities concentration at the p-n junction to the p-type and n-type impurities in respective n-well region 24 and p-well region 28 are likely to be less than $\frac{1}{2}$, even less than 0.1. With an adequate width W of cushion region 32, the ratios may even be less than about 0.01. Similar to the first embodiment, width C of cushion region 32 is preferably between about 10 Å and about 3 μm, and more preferably between about 0.3 μm and about 0.5 μm.

The previously illustrated embodiments have asymmetric structures, wherein source and drain regions are in well regions with different conductivity types. FIG. 10 illustrates a HVNMOS embodiment having a symmetric structure, wherein the HVNMOS device includes two n-well regions 70, 72 and a p-well region 74 therebetween. Similar to the embodiment illustrated in FIG. 7, cushion regions 76 and 78 are formed, wherein each of the cushion regions 76 and 78 may be an overlap region or a spacing between the neighboring p-well and n-well regions. In alternative embodiments, p-well region 74 only overlaps (or spaced apart from) one of the n-well regions 70 and 72, so that only one of the cushion regions 76 and 78 are formed, while a conventional interface is formed between p-well region 74 and the other adjacent n-well region.

Although the preferred embodiments illustrate the formation of HVNMOS devices, one skilled in the art will realize the respective formation steps for forming HVMOS devices, with the conductivity type of n-well region 24, p-well regions 28 and 30, and N+ regions 56 and 58, etc., reversed (refer to FIGS. 7 and 9). It should also be appreciated that HVMOS devices have various different layouts. However, the concept of the present invention may still be applied. Similarly, a symmetric HVMOS device may be formed by reversing the conductivity types of the doped regions in FIG. 10.

Besides forming HVMOS devices, the concept of forming a cushion region to affect the distribution of electrical fields may be applied to the formation of other devices, such as diodes. By forming cushion regions between p-type and n-type regions of p-n junctions, the breakdown voltage of diodes can be improved.

An advantageous feature of the present invention is that n-well region 24 and p-well region 28 are separated from each other by cushion region 32. Inside cushion region 32, the net impurity concentration is low. In the embodiment shown in FIG. 7, in cushion region 32, the p-type impurities and n-type impurities neutralize each other, and thus the net impurity concentration is reduced. In the embodiment shown in FIG. 9, cushion region 32 is not doped during the formation of well regions, and thus the impurity concentration is low. There-

6

fore, the cushion region 32 form an interface region with lower net impurity concentrations, and thus the performance of the HVMOS devices is improved. Experiments have revealed that the breakdown voltages of the embodiment of the present invention are improved about 3 volts to about 5 volts over the breakdown voltages of conventional HVMOS devices with similar structures (except no cushion regions are formed). In addition, as is shown in FIG. 11, substrate currents I_{sub} of embodiments of the present invention are significantly lower than substrate currents of conventional HVMOS devices. The I_{sub} of an embodiment of the present invention is illustrated as line 80, which has a maximum I_{sub} of about only $2E-06$ A/μm, while I_{sub} of a conventional HVMOS device is illustrated as line 82, which has a maximum I_{sub} of about $6.5E-06$ A/μm. As is known in the art, the lifetime of HVMOS devices is strongly related to I_{sub} . With I_{sub} reduced, the lifetime of HVMOS devices will be increased.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A semiconductor structure comprising:

- a substrate;
- a first well region of a first conductivity type overlying the substrate;
- a second well region of a second conductivity type opposite the first conductivity type overlying the substrate;
- a first cushion region between the first and the second well regions, wherein the cushion region is an overlap region of the first and the second well regions;
- a third well region of the first conductivity type overlying the substrate;
- a second cushion region between the second and the third well regions, wherein the second cushion region is an overlap region of the second and the third well regions;
- an insulation region extending from a top surface of the first well region into the first well region, wherein the first and the second cushion regions are horizontally spaced apart from the insulation region;
- a gate dielectric extending from directly over the first well region to directly over the second and the third well regions;
- a gate electrode on the gate dielectric;
- a gate spacer on a sidewall of the gate electrode;
- a drain region in the first well region and adjoining the insulation region; and
- a source region in the third well region and underlying an edge of the gate spacer.

7

2. The semiconductor structure of claim 1, wherein an entirety of the first cushion region and an entirety of the second cushion region are directly underlying the gate dielectric.

3. The semiconductor structure of claim 1, wherein a portion of the second well region not overlapping any of the first and the third well regions spaces the first and the second cushion regions apart from each other.

4. The semiconductor structure of claim 3, wherein the width of at least one of the first cushion region and the second cushion region is between about 0.3 μm and about 3 μm .

5. The semiconductor structure of claim 1, wherein one of the first and the second cushion regions has a width between about 10 $\text{\AA}$ and about 3 μm .

6. The semiconductor structure of claim 1, wherein the first and the third well regions have impurity concentrations between about $10^{14}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$, and wherein the second well region has an impurity concentration between about $10^{14}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$.

7. A semiconductor structure comprising:

a p-type substrate;

a first n-well region overlying the p-type substrate;

a p-well region overlying the p-type substrate;

a first cushion region between the first n-well region and the p-well region, wherein the first cushion region is an overlap region of the first n-well region and the p-well region, and wherein the first cushion region has a width greater than about 0.3 μm ;

a second n-well region overlying the p-type substrate;

a second cushion region between the second n-well region and the p-well region, wherein the second cushion

8

region is an overlap region of the second n-well region and the p-well region, wherein the second cushion region has a width greater than about 0.3 μm , and wherein a portion of the p-well region not overlapping any of the first and the second n-well regions spaces the first and the second cushion regions apart from each other;

an insulation region extending from a top surface of the first n-well region into the first n-well region;

a gate dielectric directly over portions of the first and the second n-well regions and the p-well region, and directly over a portion of the insulation region;

a gate electrode over the gate dielectric;

a sidewall spacer on a sidewall of the gate electrode;

a drain region in the first n-well region and adjoining the insulation region; and

a source region in the second n-well region and underlying the sidewall spacer.

8. The semiconductor structure of claim 7, wherein the first and the second cushion regions are horizontally spaced apart from the insulation region.

9. The semiconductor structure of claim 7, wherein one of the first and the second cushion regions has a width between about 0.3 μm and about 3 μm .

10. The semiconductor structure of claim 7, wherein the first and the second n-well regions have impurity concentrations between about $10^{14}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$.

11. The semiconductor structure of claim 7, wherein the p-well region has an impurity concentration between about $10^{14}/\text{cm}^3$ and about $10^{17}/\text{cm}^3$.

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