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(54) **CONDUCTIVE LAYERS FOR HAFNIUM SILICON OXYNITRIDE FILMS**

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(57) **ABSTRACT**

Electronic apparatus and methods of forming the electronic apparatus include HfSiON for use in a variety of electronic systems. In various embodiments, conductive material is coupled to a dielectric containing HfSiON, where such conductive material may include one or more monolayers of titanium nitride, tantalum, or combinations of titanium nitride and tantalum.

100

102

| 112 | Ta LAYER |
| 110 | HfSiON FILM |

103

| TiN LAYER | 117 |
| HfSiON FILM | 115 |

| SUBSTRATE | 105 |

FIG. 1

201

203

217

215

211

213   208

202

212

210

206

p+   p+   n+   n+

n-well   p-well

FIG. 2

300

350

332

340

| 320 | | 330 |

334

310

FIG. 3

400

455 {

450

442

452

432

440

420

430

434

410

FIG. 4

500

530

520

510

FIG. 5

620

600

605-N

605-2

605-1

610

FIG. 6

700

CONTROLLER ~705

~715

ELECTRONIC DEVICE ~725

FIG. 7

800

805

CONTROLLER

845

PERIPHERAL DEVICES

825

MEMORY

815 ~ BUS

835

ELECTRONIC APPARATUS
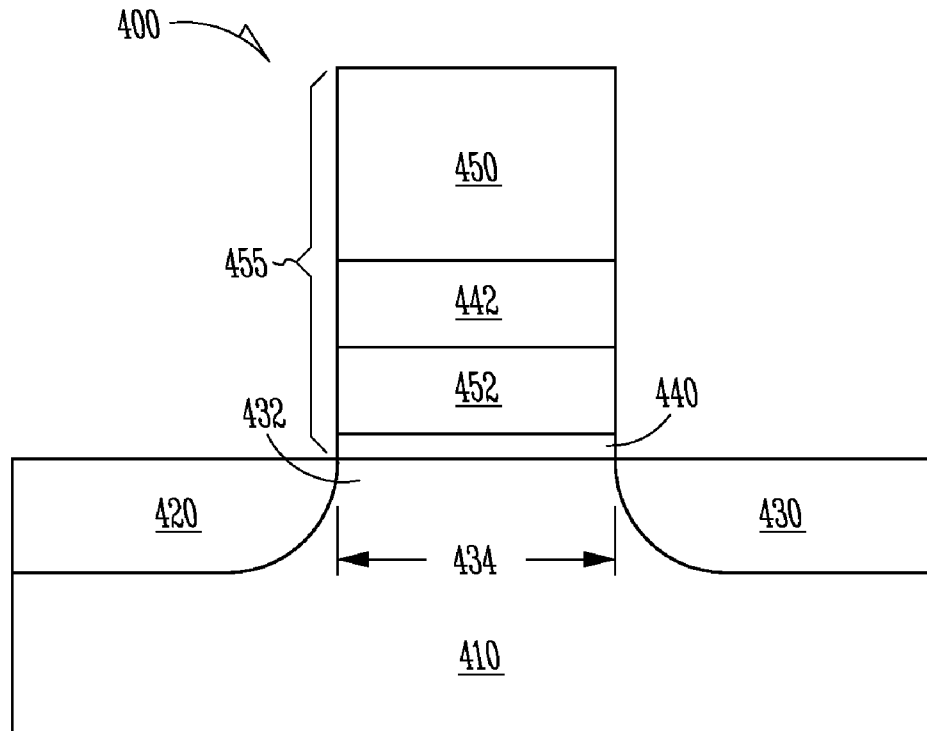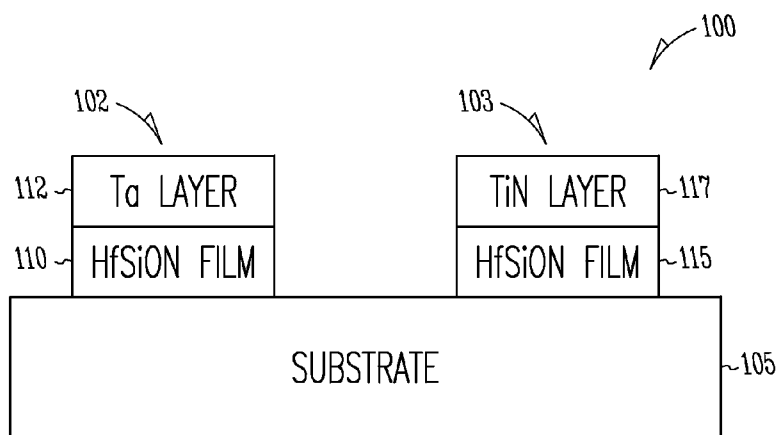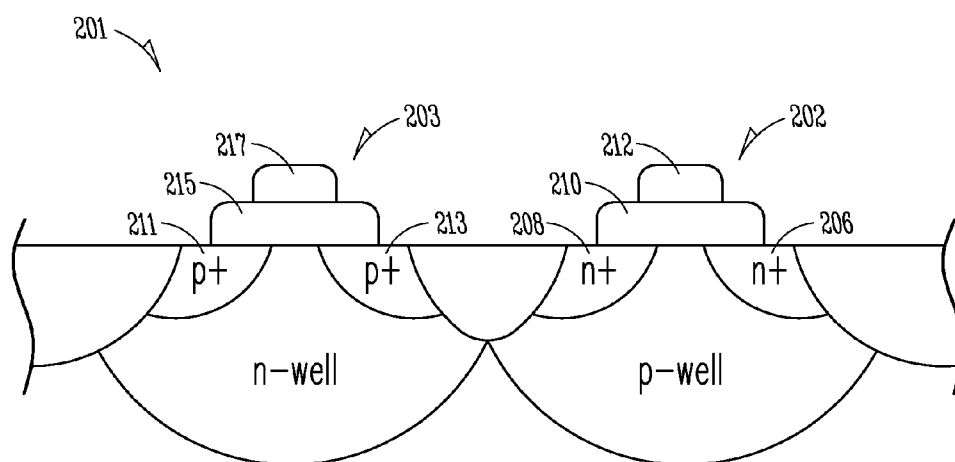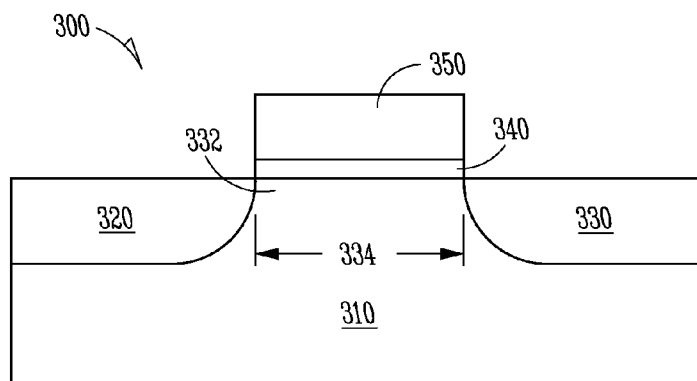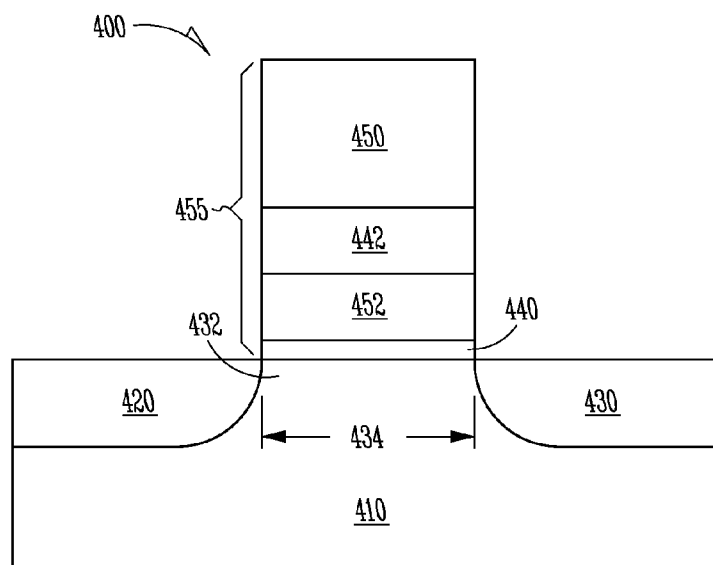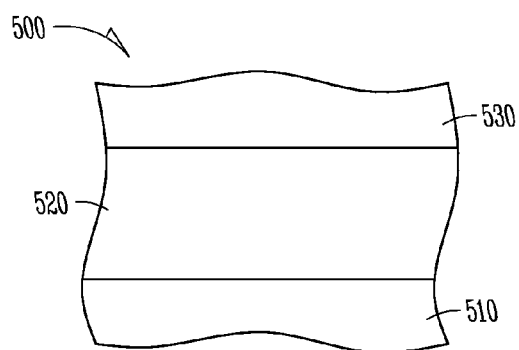
FIG. 8

CONDUCTIVE LAYERS FOR HAFNIUM SILICON OXYNITRIDE FILMS

RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 13/305,338, filed Nov. 28, 2011, which is a continuation of U.S. application Ser. No. 12/772,473, filed May 3, 2010, now issued as U.S. Pat. No. 8,067,794, which is a divisional of U.S. application Ser. No. 11/355,490 filed Feb. 16, 2006, now issued as U.S. Pat. No. 7,709,402, all of which are incorporated herein by reference in their entirety.

[0002] This application is related to the commonly assigned application U.S. application Ser. No. 10/229,903, filed on 28 Aug. 2002, now issued as U.S. Pat. No. 7,199,023, which application is incorporated herein by reference.
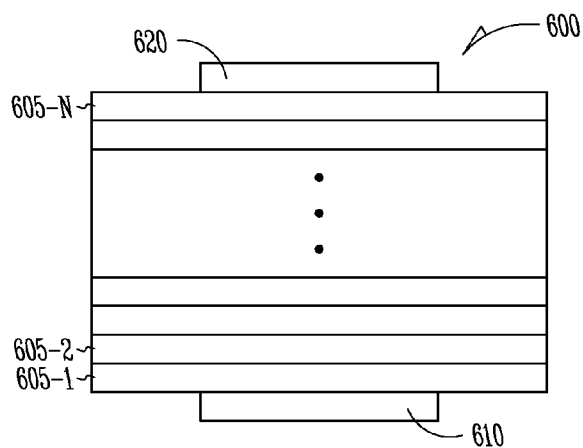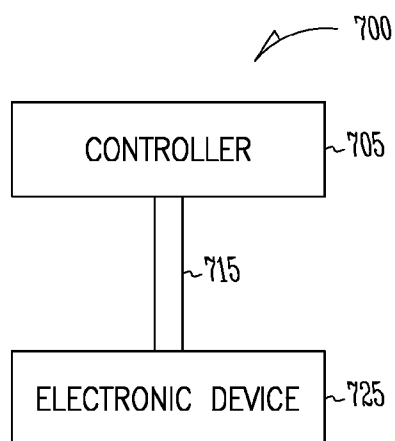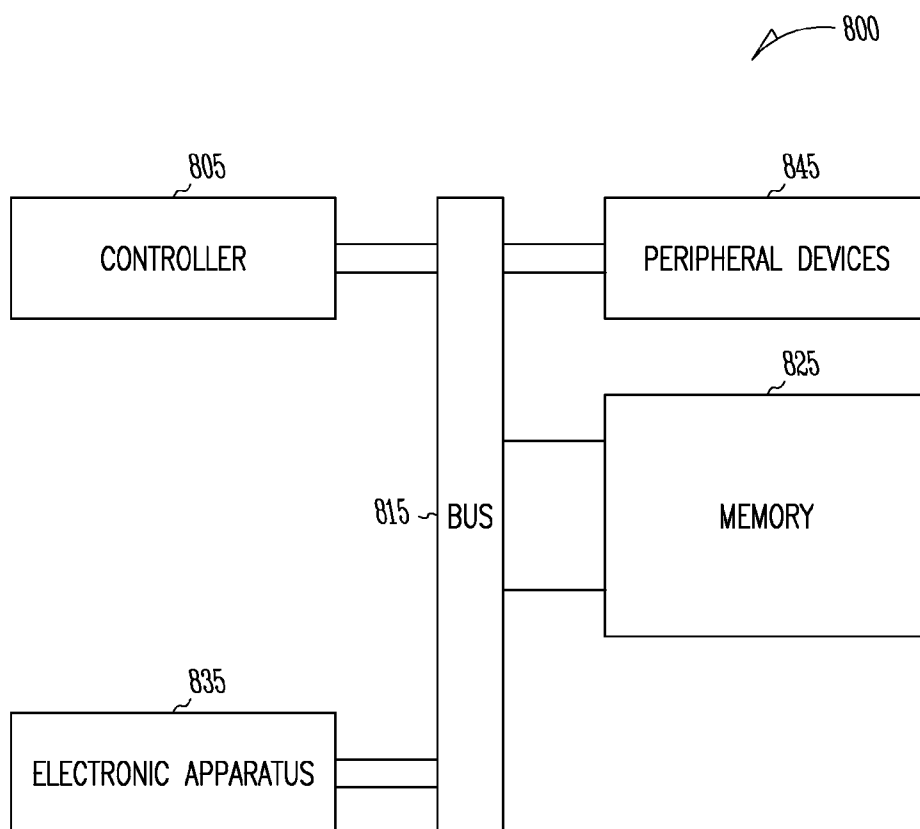
TECHNICAL FIELD

[0003] This application relates generally to semiconductor devices and device fabrication.

BACKGROUND

[0004] The semiconductor device industry has a market driven need to reduce the size of devices used in products such as processor chips, mobile telephones, and memory devices such as dynamic random access memories (DRAMs). Currently, the semiconductor industry relies on the ability to reduce or scale the dimensions of its basic devices. This device scaling includes scaling dielectric layers in devices such as, for example, capacitors and silicon based metal oxide semiconductor field effect transistors (MOSFETs), which have primarily been fabricated using silicon dioxide. A thermally grown amorphous SiO_2 layer provides an electrically and thermodynamically stable material, where the interface of the SiO_2 layer with underlying silicon provides a high quality interface as well as superior electrical isolation properties. However, increased scaling and other requirements in microelectronic devices have created the need to use other materials as dielectric regions in a variety of electronic structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 illustrates a block diagram of an embodiment of an electronic apparatus having two devices on a substrate, where one device has a tantalum layer contacting a hafnium silicon oxynitride film and the other device has a titanium nitride layer contacting a hafnium silicon oxynitride film.

[0006] FIG. 2 shows a simplified view of an embodiment of a complementary metal oxide semiconductor transistor having a gate containing a tantalum layer contacting a gate insulator containing a hafnium silicon oxynitride film and a gate containing a titanium nitride layer contacting a gate insulator containing a hafnium silicon oxynitride film.

[0007] FIG. 3 shows an embodiment of a transistor having a dielectric layer containing a hafnium silicon oxynitride film and having a gate containing a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer.

[0008] FIG. 4 shows an embodiment of a floating gate transistor having a dielectric layer containing a hafnium silicon oxynitride film and having a gate containing a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer.

[0009] FIG. 5 shows an embodiment of a capacitor having a dielectric layer containing a hafnium silicon oxynitride film and having an electrode containing a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer.

[0010] FIG. 6 depicts an embodiment of a dielectric layer having multiple layers including a hafnium silicon oxynitride layer and having a contact containing a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer.

[0011] FIG. 7 is a simplified diagram for an embodiment of a controller coupled to an electronic device having a dielectric layer containing a hafnium silicon oxynitride film and having a contact to the dielectric layer, where the contact contains a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer.

[0012] FIG. 8 illustrates a diagram for an embodiment of an electronic system having devices with a dielectric film containing a hafnium silicon oxynitride film and having a contact to the dielectric layer, where the contact contains a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer.

DETAILED DESCRIPTION

[0013] The following detailed description refers to the accompanying drawings that show, by way of illustration, embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0014] The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC) structure. The term substrate is understood to include a semiconductor wafer. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to generally include n-type and p-type semiconductors and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense.

[0015] To scale a dielectric region to minimize feature sizes to provide high density electronic devices, the dielectric region typically should have a reduced equivalent oxide thickness (t_{eq}). The equivalent oxide thickness quantifies the electrical properties, such as capacitance, of the dielectric in terms of a representative physical thickness. t_{eq} is defined as the thickness of a theoretical SiO_2 layer that would be required to have the same capacitance density as a given dielectric, ignoring leakage current and reliability considerations.

[0016] A SiO_2 layer of thickness, t, deposited on a Si surface will have a t_{eq} larger than its thickness, t. This t_{eq} results from the capacitance in the surface on which the SiO_2 is

deposited due to the formation of a depletion/inversion region. This depletion/inversion region can result in t_{eq} being from 3 to 6 Angstroms (Å) larger than the SiO_2 thickness, t. Thus, with the semiconductor industry driving to someday scale a gate dielectric equivalent oxide thickness to less than 10 Å, the physical thickness requirement for a SiO_2 layer used for a gate dielectric may need to be approximately 4 to 7 Å. Additional requirements on a SiO_2 layer would depend on the electrode used in conjunction with the SiO_2 dielectric. Using a conventional polysilicon electrode may result in an additional increase in t_{eq} for the SiO_2 layer. This additional thickness may be eliminated by using a metal electrode, though such metal electrodes are not universally used for all devices. Thus, future devices would be designed towards a physical SiO_2 dielectric layer of about 5 Å or less. Such a small thickness requirement for a SiO_2 oxide layer creates additional problems.

[0017] Silicon dioxide is used as a dielectric layer in devices, in part, due to its electrical isolation properties in a SiO_2-Si based structure. This electrical isolation is due to the relatively large band gap of SiO_2 (8.9 eV), making it a good insulator from electrical conduction. Significant reductions in its band gap may eliminate it as a material for a dielectric region in an electronic device. As the thickness of a SiO_2 layer decreases, the number of atomic layers, or monolayers of the material decreases. At a certain thickness, the number of monolayers will be sufficiently small that the SiO_2 layer will not have a complete arrangement of atoms as in a larger or bulk layer. As a result of incomplete formation relative to a bulk structure, a thin SiO_2 layer of only one or two monolayers may not form a full band gap. The lack of a full band gap in a SiO_2 dielectric may cause an effective short between an underlying Si electrode and an overlying polysilicon electrode. This undesirable property sets a limit on the physical thickness to which a SiO_2 layer can be scaled. The minimum thickness due to this monolayer effect is thought to be about 7-8 Å. Therefore, for future devices to have a t_{eq} less than about 10 Å, other dielectrics than SiO_2 need to be considered for use as a dielectric region in such future devices.

[0018] In many cases, for a typical dielectric layer, the capacitance may be determined as a capacitance for a parallel plate capacitor: $C = \kappa \epsilon_0 A/t$, where κ is the dielectric constant, ϵ_0 is the permittivity of free space, A is the area of the capacitor, and t is the thickness of the dielectric. The thickness, t, of a material is related to its t_{eq} for a given capacitance, with SiO_2 having a dielectric constant $\kappa_{ox} = 3.9$, as

$$t = (\kappa/\kappa_{ox})t_{eq} = (\kappa/3.9)t_{eq}.$$

[0019] Thus, materials with a dielectric constant greater than that of SiO_2 will have a physical thickness that can be considerably larger than a desired t_{eq}, while providing the desired equivalent oxide thickness. For example, an alternate dielectric material with a dielectric constant of 10 could have a thickness of about 25.6 Å to provide a t_{eq} of 10 Å, not including any depletion/inversion layer effects. Thus, a reduced equivalent oxide thickness for transistors can be realized by using dielectric materials with higher dielectric constants than SiO_2.

[0020] The thinner equivalent oxide thickness required for lower device operating voltages and smaller device dimensions may be realized by a significant number of materials, but additional fabricating requirements make determining a suitable replacement for SiO_2 difficult. The current view for the microelectronics industry is still for Si based devices. This

may require that the dielectric material employed be grown on a silicon substrate or a silicon layer, which places significant constraints on the substitute dielectric material. During the formation of the dielectric on the silicon layer, there exists the possibility that a small layer of SiO_2 could be formed in addition to the desired dielectric. The result would effectively be a dielectric layer consisting of two sublayers in parallel with each other and the silicon layer on which the dielectric is formed. In such a case, the resulting capacitance would be that of two dielectrics in series. As a result, the t_{eq} of the dielectric layer would be the sum of the SiO_2 thickness and a multiplicative factor of the thickness, t, of the dielectric being formed, written as

$$t_{eq} = t_{SiO2} + (\kappa_{ox}/\kappa)t.$$

Thus, if a SiO_2 layer is formed in the process, the t_{eq} is again limited by a SiO_2 layer. In the event that a barrier layer is formed between the silicon layer and the desired dielectric in which the barrier layer prevents the formation of a SiO_2 layer, the t_{eq} would be limited by the layer with the lowest dielectric constant. However, whether a single dielectric layer with a high dielectric constant or a barrier layer with a higher dielectric constant than SiO_2 is employed, the layer interfacing with the silicon layer should provide a high quality interface.

[0021] One of the advantages of using SiO_2 as a dielectric layer in a device has been that the formation of the SiO_2 layer results in an amorphous dielectric. Having an amorphous structure for a dielectric may reduce problems of leakage current associated with grain boundaries in polycrystalline dielectrics that provide high leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline dielectric can cause variations in the film's dielectric constant, along with uniformity and surface topography problems. Typically, materials having a high dielectric constant relative to SiO_2 also have a crystalline form, at least in a bulk configuration. The best candidates for replacing SiO_2 as a dielectric in a device are those that can be fabricated as a thin layer with an amorphous form and that have high dielectric constants.

[0022] An embodiment of a method may include forming a hafnium silicon oxynitride film using atomic layer deposition and forming, on the hafnium silicon oxynitride film, a titanium nitride layer or a tantalum layer by atomic layer deposition. Embodiments include structures and methods to form such structures for capacitors, transistors, memory devices, and electronic systems with dielectric layers containing a hafnium silicon oxynitride oxide layer structured as one or more monolayers with a conductive tantalum layer or a conductive titanium nitride layer structured as one or more monolayers.

[0023] In an embodiment, a hafnium silicon oxynitride dielectric film coupled to a titanium nitride layer, a tantalum layer, or a combination of a titanium nitride layer and a tantalum layer may be formed using atomic layer deposition (ALD) including forming the titanium nitride layer and the tantalum layer a by atomic layer deposition. Various approaches for forming a hafnium silicon oxynitride dielectric film by atomic layer deposition are discussed in application Ser. No. 10/229,903, entitled "ATOMIC LAYER DEPOSITED HfSiON DIELECTRIC FILMS," filed on 28 Aug. 2002, which application is incorporated herein by reference. Forming such structures using atomic layer deposition may allow control of transitions between material layers. As a result of such control, atomic layer deposited hafnium

silicon oxynitride dielectric films can have an engineered transition with a substrate surface and with atomic layer deposited conductive layers contacting the hafnium silicon oxynitride dielectric films.

[0024] ALD, also known as atomic layer epitaxy (ALE), is a modification of chemical vapor deposition (CVD) and is also called "alternatively pulsed-CVD." In ALD, gaseous precursors are introduced one at a time to the substrate surface mounted within a reaction chamber (or reactor). This introduction of the gaseous precursors takes the form of pulses of each gaseous precursor. In a pulse of a precursor gas, the precursor gas is made to flow into a specific area or region for a short period of time. Between the pulses, the reaction chamber may be purged with a gas, where the purging gas may be an inert gas. Between the pulses, the reaction chamber may be evacuated. Between the pulses, the reaction chamber may be purged with a gas and evacuated.

[0025] In a chemisorption-saturated ALD (CS-ALD) process, during the first pulsing phase, reaction with the substrate occurs with the precursor saturatively chemisorbed at the substrate surface. Subsequent pulsing with a purging gas removes precursor excess from the reaction chamber.

[0026] The second pulsing phase introduces another precursor on the substrate where the growth reaction of the desired film takes place. Subsequent to the film growth reaction, reaction byproducts and precursor excess are purged from the reaction chamber. With favourable precursor chemistry where the precursors adsorb and react with each other aggressively on the substrate, one ALD cycle can be performed in less than one second in properly designed flow type reaction chambers. Typically, precursor pulse times range from about 0.5 sec to about 2 to 3 seconds. Pulse times for purging gases may be significantly longer, for example, pulse times of about 5 to about 30 seconds.

[0027] In ALD, the saturation of all the reaction and purging phases makes the growth self-limiting. This self-limiting growth results in large area uniformity and conformality, which has important applications for such cases as planar substrates, deep trenches, and in the processing of porous silicon and high surface area silica and alumina powders. Atomic layer deposition provides control of film thickness in a straightforward manner by controlling the number of growth cycles.

[0028] The precursors used in an ALD process may be gaseous, liquid or solid. However, liquid or solid precursors should be volatile. The vapor pressure should be high enough for effective mass transportation. Also, solid and some liquid precursors may need to be heated inside the reaction chamber and introduced through heated tubes to the substrates. The necessary vapor pressure should be reached at a temperature below the substrate temperature to avoid the condensation of the precursors on the substrate. Due to the self-limiting growth mechanisms of ALD, relatively low vapor pressure solid precursors can be used, though evaporation rates may vary somewhat during the process because of changes in their surface area.

[0029] There are several other characteristics for precursors used in ALD. The precursors should be thermally stable at the substrate temperature, because their decomposition may destroy the surface control and accordingly the advantages of the ALD method that relies on the reaction of the precursor at the substrate surface. A slight decomposition, if slow compared to the ALD growth, may be tolerated.

[0030] The precursors should chemisorb on or react with the surface, though the interaction between the precursor and the surface as well as the mechanism for the adsorption is different for different precursors. The molecules at the substrate surface should react aggressively with the second precursor to form the desired solid film. Additionally, precursors should not react with the film to cause etching, and precursors should not dissolve in the film. Using highly reactive precursors in ALD contrasts with the selection of precursors for conventional CVD.

[0031] The by-products in the reaction should be gaseous in order to allow their easy removal from the reaction chamber. Further, the by-products should not react or adsorb on the surface.

[0032] In a reaction sequence ALD (RS-ALD) process, the self-limiting process sequence involves sequential surface chemical reactions. RS-ALD relies on chemistry between a reactive surface and a reactive molecular precursor. In an RS-ALD process, molecular precursors are pulsed into the ALD reaction chamber separately. A metal precursor reaction at the substrate is typically followed by an inert gas pulse to remove excess precursor and by-products from the reaction chamber prior to pulsing the next precursor of the fabrication sequence.

[0033] By RS-ALD, films can be layered in equal metered sequences that may all be identical in chemical kinetics, deposition per cycle, composition, and thickness. RS-ALD sequences generally deposit less than a full layer per cycle. Typically, a deposition or growth rate of about 0.25 to about 2.00 Å per RS-ALD cycle may be realized.

[0034] Processing by RS-ALD provides continuity at an interface avoiding poorly defined nucleating regions that are typical for chemical vapor deposition (<20 Å) and physical vapor deposition (<50 Å), conformality over a variety of substrate topologies due to its layer-by-layer deposition technique, use of low temperature and mildly oxidizing processes, lack of dependence on the reaction chamber, growth thickness dependent solely on the number of cycles performed, and ability to engineer multilayer laminate films with a resolution of one to two monolayers. RS-ALD processes allow for deposition control on the order of monolayers and the ability to deposit monolayers of amorphous films.

[0035] Herein, a sequence refers to the ALD material formation based on an ALD reaction of a precursor with its reactant precursor. For example, forming titanium nitride from a $TiCl_4$ precursor and NH_3, as its reactant precursor, forms an embodiment of a titanium/nitrogen sequence. In various ALD processes that form a nitride or a compound that contains nitrogen, a reactant precursor that contains nitrogen is used to supply nitrogen. Herein, a precursor that contains nitrogen and that supplies nitrogen to be incorporated in the ALD compound formed, which may be used in an ALD process with precursors supplying the other elements in the ALD compound, is referred to as a nitrogen reactant precursor. In the above example, NH_3 is a nitrogen reactant precursor. Similarly, an ALD sequence for a binary metal oxide may be referenced with respect to the metal and oxygen. For example, an ALD sequence for hafnium oxide may also be referred to as a hafnium/oxygen sequence. In various ALD processes that form an oxide or a compound that contains oxygen, a reactant precursor that contains oxygen is used to supply the oxygen. Herein, a precursor that contains oxygen and that supplies oxygen to be incorporated in the ALD compound formed, which may be used in an ALD process with

precursors supplying the other elements in the ALD compound, is referred to as an oxygen reactant precursor. With an ALD process using HfCl$_4$ and water vapor to form hafnium oxide, water vapor is an oxygen reactant precursor. An ALD cycle may include pulsing a precursor, pulsing a purging gas for the precursor, pulsing a reactant precursor, and pulsing the reactant precursor's purging gas. An ALD cycle may include pulsing a precursor, evacuating the reactant chamber, pulsing a reactant precursor, and evacuating the reactant chamber. An ALD cycle may include pulsing a precursor, pulsing a purging gas for the precursor and evacuating the reactant chamber, pulsing a reactant precursor, and pulsing the reactant precursor's purging gas evacuating the reactant chamber.

[0036] In forming a layer of a metal species, an ALD sequence may deal with pulsing a reactant precursor to the substrate surface on which a metal-containing species has been adsorbed such that the reactant precursor reacts with the metal-containing species resulting in the metal and a gaseous by-product that can be removed during the subsequent purging/evacuating process. Alternatively, in forming a layer of a metal species, an ALD sequence may deal with reacting a precursor containing the metal species with a substrate surface. A cycle for such a metal forming sequence may include pulsing a purging gas after pulsing the precursor containing the metal species to deposit the metal. Additionally, deposition of a semiconductor material may be realized in a manner similar to forming a layer of a metal, given the appropriate precursors for the semiconductor material.

[0037] In an ALD formation of a compound having more than two elements, a cycle may include a number of sequences to provide the elements of the compound. For example, a cycle for an ALD formation of an ABO$_x$ compound may include sequentially pulsing a first precursor/a purging gas for the first precursor/a first reactant precursor/the first reactant precursor's purging gas/a second precursor/a purging gas for the second precursor/a second reactant precursor/the second reactant precursor's purging gas, which may be viewed as a cycle having two sequences. In an embodiment, a cycle may include a number of sequences for element A and a different number of sequences for element B. There may be cases in which ALD formation of an ABO$_x$ compound uses one precursor that contains the elements A and B, such that pulsing the AB containing precursor followed by its reactant precursor onto a substrate may include a reaction that forms ABO$_x$ on the substrate to provide an AB/oxygen sequence. A cycle of an AB/oxygen sequence may include pulsing a precursor containing A and B, pulsing a purging gas for the precursor, pulsing an oxygen reactant precursor to the A/B precursor, and pulsing a purging gas for the reactant precursor. A cycle may be repeated a number of times to provide a desired thickness of the compound. In an embodiment, a cycle for an ALD formation of the quaternary compound, hafnium silicon oxynitride, may include sequentially pulsing a first precursor/a purging gas for the first precursor/a first reactant precursor/the first reactant precursor's purging gas/a second precursor/a purging gas for the second precursor/a second reactant precursor/the second reactant precursor's purging gas/a third precursor/a purging gas for the third precursor/a third reactant precursor/the third reactant precursor's purging gas, which may be viewed as a cycle having three sequences. In an embodiment, a layer substantially of a hafnium silicon oxygen nitrogen compound is formed on a substrate mounted in a reaction chamber using ALD in repetitive hafnium/oxygen and silicon/nitrogen sequences using precursor gases individually pulsed into the reaction chamber. After forming the hafnium silicon oxygen nitrogen layer, an ALD tantalum sequence may be conducted to form a tantalum layer on the hafnium silicon oxygen nitrogen layer. After forming the hafnium silicon oxygen nitrogen layer, an ALD titanium/nitrogen sequence may be conducted to form a titanium nitride layer on the hafnium silicon oxygen nitrogen layer. Solid or liquid precursors can be used in an appropriately designed reaction chamber.

[0038] In an embodiment, a hafnium silicon oxynitride layer may be structured as one or more monolayers. A film of hafnium silicon oxynitride, structured as one or more monolayers, may have a thickness that ranges from a monolayer to thousands of angstroms or more. The film may be processed using atomic layer deposition. Embodiments of an atomic layer deposited hafnium silicon oxynitride layer have a larger dielectric constant than silicon dioxide. Such dielectric layers provide a significantly thinner equivalent oxide thickness compared with a silicon oxide layer having the same physical thickness. Alternatively, such dielectric layers provide a significantly thicker physical thickness than a silicon oxide layer having the same equivalent oxide thickness. This increased physical thickness aids in reducing leakage current.

[0039] In an embodiment, a tantalum layer may be structured as one or more monolayers. A layer of tantalum, structured as one or more monolayers, may have a thickness that ranges from a monolayer to thousands of angstroms or more. The tantalum film may be processed using atomic layer deposition. In an embodiment, a titanium nitride layer may be structured as one or more monolayers. A layer of titanium nitride, structured as one or more monolayers, may have a thickness that ranges from a monolayer to thousands of angstroms or more. The titanium nitride film may be processed using atomic layer deposition.

[0040] The term hafnium silicon oxynitride is used herein with respect to a compound that essentially consists of hafnium, silicon, oxygen, and nitrogen in a form that may be stoichiometric, non-stoichiometric, or a combination of stoichiometric and non-stoichiometric. A hafnium silicon oxynitride film may also be referred to as a hafnium silicon oxygen nitrogen film. Other nomenclature for a compound that essentially consists of hafnium, silicon, oxygen, and nitrogen may be known to those skilled in the art. In an embodiment, hafnium silicon oxynitride may be formed substantially as stoichiometric hafnium silicon oxynitride. In an embodiment, hafnium silicon oxynitride may be formed substantially as a non-stoichiometric hafnium silicon oxynitride. In an embodiment, hafnium silicon oxynitride may be formed substantially as a combination of non-stoichiometric hafnium silicon oxynitride and stoichiometric hafnium silicon oxynitride. Herein, a hafnium silicon oxynitride compound may be expressed as HfSiON, HfSiON$_x$, Hf$_x$Si$_y$O$_z$N$_r$, or other equivalent form. The expression HfSiON or its equivalent forms may be used to include a stoichiometric hafnium silicon oxynitride. The expression HfSiON or its equivalent forms may be used to include a non-stoichiometric hafnium silicon oxynitride. The expression HfSiON or its equivalent forms may be used to include a combination of a stoichiometric hafnium silicon oxynitride and a non-stoichiometric hafnium silicon oxynitride. The expression HfO$_x$ may be used to include a stoichiometric hafnium oxide. The expression HfO$_x$ may be used to include a non-stoichiometric hafnium oxide. The expression HfO$_x$ may be used to include a combination of a stoichiometric hafnium oxide and a non-stoichio-

metric hafnium oxide. Expressions SiO_x, SiN_r, HfN_t, and TiN_x may be used in the same manner as HfO_x. In various embodiments, a hafnium silicon oxynitride film may be doped with elements or compounds other than hafnium, silicon, oxygen, and nitrogen.

[0041] In an embodiment, a $HfSiON_x$ film may be structured as one or more monolayers. In an embodiment, the $HfSiON_x$ film may be constructed using atomic layer deposition. Prior to forming the $HfSiON_x$ film using ALD, the surface on which the $HfSiON_x$ film is to be deposited may undergo a preparation stage. The surface may be the surface of a substrate for an integrated circuit. In an embodiment, the substrate used for forming a transistor may include a silicon or silicon containing material. In other embodiments, germanium, gallium arsenide, silicon-on-sapphire substrates, or other suitable substrates may be used. A preparation process may include cleaning the substrate and forming layers and regions of the substrate, such as drains and sources, prior to forming a gate dielectric in the formation of a metal oxide semiconductor (MOS) transistor. Alternatively, active regions may be formed after forming the dielectric layer, depending on the over-all fabrication process implemented. In an embodiment, the substrate is cleaned to provide an initial substrate depleted of its native oxide. In an embodiment, the initial substrate is cleaned also to provide a hydrogen-terminated surface. In an embodiment, a silicon substrate undergoes a final hydrofluoric (HF) rinse prior to ALD processing to provide the silicon substrate with a hydrogen-terminated surface without a native silicon oxide layer.

[0042] Cleaning immediately preceding atomic layer deposition aids in reducing an occurrence of silicon oxide as an interface between a silicon based substrate and a hafnium silicon oxynitride dielectric formed using the atomic layer deposition process. The material composition of an interface layer and its properties are typically dependent on process conditions and the condition of the substrate before forming the dielectric layer. Though the existence of an interface layer may effectively reduce the dielectric constant associated with the dielectric layer and its substrate interface layer, a SiO_2 interface layer or other composition interface layer may improve the interface density, fixed charge density, and channel mobility of a device having this interface layer.

[0043] The sequencing of the formation of the regions of an electronic device, such as a transistor, being processed may follow typical sequencing that is generally performed in the fabrication of such devices as is well known to those skilled in the art. Included in the processing prior to forming a dielectric may be the masking of substrate regions to be protected during the dielectric formation, as is typically performed in semiconductor fabrication. In an embodiment, the unmasked region includes a body region of a transistor; however, one skilled in the art will recognize that other semiconductor device structures may utilize this process.

[0044] In various embodiments, between each pulsing of a precursor used in an atomic layer deposition process, a purging gas may be pulsed into the ALD reaction chamber. Between each pulsing of a precursor, the ALD reactor chamber may be evacuated using vacuum techniques as is known by those skilled in the art. Between each pulsing of a precursor, a purging gas may be pulsed into the ALD reaction chamber and the ALD reactor chamber may be evacuated.

[0045] In an embodiment, alternate layers of hafnium oxide and silicon nitride may be formed by atomic layer deposition.

The alternating hafnium oxide and silicon nitride layers may be annealed to form hafnium silicon oxynitride.

[0046] To form hafnium oxide by atomic layer deposition, a hafnium-containing precursor is pulsed onto a substrate in an ALD reaction chamber. A number of precursors containing hafnium may be used to provide the hafnium to a substrate for an integrated circuit. In an embodiment, a precursor containing hafnium may include anhydrous hafnium nitride, $Hf(NO_3)_4$. In an embodiment using a $Hf(NO_3)_4$ precursor on a hydrogen-terminated silicon, the substrate temperature may be maintained at a temperature ranging from about 160° C. to about 180° C. In an embodiment, a hafnium precursor may include $HfCl_4$. In an embodiment using a $HfCl_4$ precursor, the substrate temperature may be maintained at a temperature ranging from about 180° C. to about 600° C. In an embodiment using a $HfCl_4$ precursor, the substrate temperature may be maintained at a temperature ranging from about 300° C. to about 940° C. In an embodiment, a hafnium precursor may be HfI_4. In an embodiment using a HfI_4 precursor, the substrate temperature may be maintained at a temperature of about 300° C. Hafnium oxide may be grown by ALD using a $Hf[N(CH_3)(C_2H_5)]_4$, which may be known as a homoleptic tetrakis (dialkylamino) hafnium(IV) compound, and water as an oxygen reactant. Other types of tetrakis(dialkylamino) hafnium compounds may also be used, such as hafnium tetrakis dimethylamine, $Hf[N(CH_3)_2]_4$, or hafnium tetrakis diethylamine, $Hf[N(C_2H_5)_2]_4$, as a hafnium-containing precursor. In various embodiments, after pulsing the hafnium-containing precursor and purging the reaction chamber of excess precursor and by-products from pulsing the precursor, a reactant precursor may be pulsed into the reaction chamber. The reactant precursor may be an oxygen reactant precursor including, but not limited to, one or more of water vapor, atomic oxygen, molecular oxygen, ozone, hydrogen peroxide, a water-hydrogen peroxide mixture, alcohol, or nitrous oxide. In various embodiments, use of the individual hafnium-containing precursors is not limited to the temperature ranges of the above example embodiments. Further, forming hafnium oxide by atomic layer deposition is not limited to the abovementioned precursors. In addition, the pulsing of the hafnium precursor may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during a hafnium sequence.

[0047] To form silicon nitride by atomic layer deposition, a silicon-containing precursor is pulsed onto a substrate in an ALD reaction chamber. In an embodiment, a silicon halide, such as $SiCl_4$, may be used. Other silicon halides, such as SiI_4, may be used. For the pulsing of the $SiCl_4$ precursor, the substrate may be maintained at a temperature ranging from about 340 EC to about 375 EC at a gas pressure in reaction chamber at about 170 Torr. In an embodiment, the substrate may be maintained at a temperature less than 550° C. In an embodiment, NH_3 may be used as the nitrogen-containing precursor for a silicon/nitrogen sequence. In various embodiments, use of the individual silicon-containing precursors is not limited to the temperature ranges of the above example embodiments. Further, forming silicon nitride by atomic layer deposition is not limited to the abovementioned precursors. In addition, the pulsing of the silicon precursor may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during a silicon sequence.

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[0048] In various embodiments, nitrogen may be used as a purging gas and a carrier gas for one or more of the sequences. Alternatively, hydrogen, argon gas, or other inert gases may be used as the purging gas. Excess precursor gas and reaction by-products may be removed by the purge gas. Excess precursor gas and reaction by-products may be removed by evacuation of the reaction chamber using various vacuum techniques. Excess precursor gas and reaction by-products may be removed by the purge gas and by evacuation of the reaction chamber.

[0049] In an embodiment, alternate layers of hafnium nitride and silicon oxide may be formed by atomic layer deposition. The alternating hafnium nitride and silicon oxide layers may be annealed to form hafnium silicon oxynitride.

[0050] To form hafnium nitride by atomic layer deposition, a hafnium-containing precursor is pulsed onto a substrate in an ALD reaction chamber. A number of precursors containing hafnium may be used to provide the hafnium to a substrate for an integrated circuit. The hafnium-containing precursor may be a hafnium halide precursor. In an embodiment, a hafnium precursor may include $HfCl_4$. In an embodiment using a $HfCl_4$ precursor, the substrate temperature may be maintained at a temperature ranging from about 180° C. to about 600° C. In an embodiment using a $HfCl_4$ precursor, the substrate temperature may be maintained at a temperature ranging from about 300° C. to about 940° C. In an embodiment, a hafnium precursor used may be HfI_4. In an embodiment using a HfI_4 precursor, the substrate temperature may be maintained at a temperature of about 300° C. In addition to halide precursors, the hafnium nitride may be grown by ALD using a $Hf[N(CH_3)(C_2H_5)]_4$ and ammonia, NH_3. In an embodiment, the substrate may be held at a temperature ranging from about 150° C. to about 300° C. Other types of tetrakis(dialkylamino) metal compounds may also be used, such as hafnium tetrakis dimethylamine, $Hf[N(CH_3)_2]_4$, or hafnium tetrakis diethylamine, $Hf[N(C_2H_5)_2]_4$, as a hafnium-containing precursor with ammonia as a nitrogen reactant precursor. In various embodiments, after pulsing the hafnium-containing precursor and purging the reaction chamber of excess precursor and by-products from pulsing the precursor, a reactant precursor may be pulsed into the reaction chamber. The reactant precursor may be a nitrogen reactant precursor including, but not limited to, ammonia. In various embodiments, use of the individual hafnium-containing precursors is not limited to the temperature ranges of the above embodiments. Further, forming hafnium nitride by atomic layer deposition is not limited to the abovementioned precursors. In addition, the pulsing of the hafnium precursor may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during a hafnium sequence.

[0051] To form silicon oxide by atomic layer deposition, a silicon-containing precursor is pulsed onto a substrate in an ALD reaction chamber. A silicon halide precursor may be used as the silicon-containing precursor. In an embodiment, $SiCl_4$ is used as the silicon-containing precursor. Other silicon halides, such as SiI_4, may be used. In an embodiment, during pulsing of the $SiCl_4$, the substrate may be held between about 340° C. and about 375° C. For a silicon sequence using $SiCl_4$ as the precursor, oxygen, in the form of O_2 or O_3, may be used as the precursor acting as an oxidizing reactant to interact at the substrate. In an embodiment, during the oxygen pulsing, the substrate may be raised to a temperature significantly higher than the temperature used during the pulsing of the precursor containing silicon. In an embodiment, the temperature for the substrate may be at about 550° C. during the oxygen pulsing. In various embodiments, use of the individual silicon-containing precursors is not limited to the temperature ranges of the above embodiments. Further, forming silicon oxide by atomic layer deposition is not limited to the abovementioned precursors. In addition, the pulsing of the silicon precursor may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface during a silicon sequence. In an embodiment, forming a silicon oxide by atomic layer deposition is conducted after an initial hafnium nitride layer is formed on a silicon-based substrate to limit the size or occurrence of a silicon oxide interface between a HfSiON layer and the silicon-based substrate.

[0052] Atomic layer deposition of the individual components or layers of HfO_x, SiN_r, SiO_z, and/or HfN_t allows for individual control of each precursor pulsed into the reaction chamber. Thus, each precursor is pulsed into the reaction chamber for a predetermined period, where the predetermined period can be set separately for each precursor. Additionally, for various ALD formations, each precursor may be pulsed into the reaction chamber under separate environmental conditions. The substrate may be maintained at a selected temperature and the reaction chamber maintained at a selected pressure independently for pulsing each precursor. Appropriate temperatures and pressures may be maintained, whether the precursor is a single precursor or a mixture of precursors.

[0053] The layers of hafnium oxide and silicon nitride and/or layers of hafnium nitride and silicon oxide may be annealed to form hafnium silicon oxynitride. In an embodiment, a laminated stack of alternating layers of HfO_2 and Si_2N_3 are formed prior to annealing. In an embodiment, a laminated stack of alternating layers of Hf_3N_4 and SiO_2 are formed prior to annealing. In various embodiments, the order of forming HfO_x and SiN_r layers may be permutated. In various embodiments, the order of forming SiO_z and HfN_t layers may be permutated. In an embodiment, alternating layers of HfO_x and SiN_r are formed with alternating layers of SiO_x and HfN_t to form a dielectric stack, which is annealed to form hafnium silicon oxynitride. The dielectric stack may be formed as a layer of hafnium silicon oxynitride. The annealing may be conducted in a nitrogen ambient. In an embodiment, annealing may be conducted in a nitrogen ambient having a small amount of oxygen. However, annealing is not limited to these ambient conditions.

[0054] In an embodiment, a layer of hafnium oxide and a layer of silicon nitride are each grown by atomic layer deposition to a thickness such that annealing these layers at appropriate temperatures essentially converts these layers to a layer of hafnium silicon oxynitride. In an embodiment, each layer of HfO_x and SiN_r may be formed to a thickness of 10 Å or less. In the various embodiments, the thickness of a hafnium silicon oxynitride film is related to the number of ALD cycles performed and the growth rate associated with forming each layer of HfO_x and SiN_r.

[0055] In an embodiment, a layer of hafnium nitride and a layer of silicon oxygen are each grown by atomic layer deposition to a thickness such that annealing these layers at appropriate temperatures essentially converts these layers to a layer of hafnium silicon oxynitride. In an embodiment, each layer of SiO_z and HfN_t may be formed to a thickness of 10 Å or less.

In the various embodiments, the thickness of a hafnium silicon oxynitride film is related to the number of ALD cycles performed and the growth rate associated with forming each layer of SiO_x and HfN_t.

[0056] In an embodiment, a HfSiON film may be grown to a desired thickness by repetition of a process including atomic layer deposition of layers of HfO_x and SiN_t and/or layers of SiO_z and HfN_t followed by annealing. In an embodiment, a base thickness may be formed according to various embodiments such that forming a predetermined thickness of a HfSiON film may be conducted by forming a number of layers having the base thickness. As can be understood by one skilled in the art, determining the base thickness depends on the application and can be determined during initial processing without undue experimentation. Relative amounts of hafnium, silicon, oxygen, and nitrogen in a HfSiON film may be controlled by regulating the relative thicknesses of the individual layers of oxides and nitrides formed. In addition, relative amounts of hafnium, silicon, oxygen, and nitrogen in a HfSiON film may be controlled by forming a layer of HfSiON as multiple layers of different base thickness and by regulating the relative thicknesses of the individual layers of oxides and nitrides formed in each base layer prior to annealing. As can be understood by those skilled in the art, particular effective growth rates for the engineered hafnium silicon oxynitride film can be determined during normal initial testing of the ALD system used in processing a hafnium silicon oxynitride dielectric for a given application without undue experimentation.

[0057] In an alternative embodiment, an ALD cycle for forming HfSiON may include sequencing component-containing precursors in the order of hafnium, oxygen, silicon, and nitrogen with appropriate purging between the different component-containing precursors, in which partial coverage of a monolayer on a substrate surface is attained for pulsing of a metal-containing precursor. An ALD cycle for forming HfSiON may include sequencing the component-containing precursors in various permutations. In an embodiment, an ALD cycle to form hafnium silicon oxynitride may include a number, x, of hafnium/oxygen sequences and a number, y, of silicon/nitrogen sequences. The number of sequences x and y may be selected to engineer the relative amounts of hafnium, silicon, oxygen, and nitrogen. In an embodiment, the number of sequences x and y may be selected to form a hafnium-rich hafnium silicon oxynitride. Alternatively, the number of sequences x and y may be selected to form a silicon-rich hafnium silicon oxynitride. In an embodiment, an ALD cycle to form hafnium silicon oxynitride may include a number, z, of hafnium/nitrogen sequences and a number, r, of silicon/oxygen sequences. The number of sequences z and r may be selected to engineer the relative amounts of hafnium, silicon, oxygen, and nitrogen. In an embodiment, the number of sequences z and r may be selected to form a hafnium-rich hafnium silicon oxynitride. Alternatively, the number of sequences z and r may be selected to form a silicon-rich hafnium silicon oxynitride.

[0058] After repeating a selected number of ALD cycles, a determination may be made as to whether the number of cycles equals a predetermined number to form the desired hafnium silicon oxynitride layer. If the total number of cycles to form the desired thickness has not been completed, a number of cycles is repeated. The thickness of a hafnium silicon oxynitride layer formed by atomic layer deposition may be determined by a fixed growth rate for the pulsing periods and

precursors used, set at a value such as N nm/cycle, and the number of cycles conducted. Depending on the precursors used for ALD formation of a HfSiON film, the process may be conducted in an ALD window, which is a range of temperatures in which the growth rate is substantially constant. If such an ALD window is not available, the ALD process may be conducted at the same set of temperatures for each ALD sequence in the process. For a desired hafnium silicon oxynitride layer thickness, t, in an application, the ALD process is repeated for t/N total cycles. Once the t/N cycles have completed, no further ALD processing for the hafnium silicon oxynitride layer is required. A hafnium silicon oxynitride layer processed at relatively low temperatures associated with atomic layer deposition may provide an amorphous layer.

[0059] In various embodiments, either before or after forming a HfSiON film, other dielectric layers such as nitride layers, dielectric metal silicates, insulating materials including HfO_x, SiN_t, and SiO_x, and lanthanide oxides or combinations thereof may be formed as part of a dielectric layer or dielectric stack. These one or more other layers of dielectric material may be provided in stoichiometric form, in non-stoichiometric form, or a combination of stoichiometric dielectric material and non-stoichiometric dielectric material. Depending on the application, a dielectric stack containing a $HfSiON_x$ film may include a silicon oxide layer. In an embodiment, the dielectric layer may be formed as a nanolaminate. An embodiment of a nanolaminate may include a layer of a hafnium oxide and a $HfSiON_x$ film, a layer of silicon nitride and a $HfSiON_x$ film, a layer of silicon oxide and a $HfSiON_x$ film, layers of hafnium oxide, silicon nitride, and silicon oxide along with a $HfSiON_x$ film, or various other combinations. Alternatively, a dielectric layer may be formed substantially as the hafnium silicon oxynitride film.

[0060] In various embodiments, the structure of an interface between a dielectric layer and a substrate on which it is disposed is controlled to limit the inclusion of silicon oxide, since a silicon oxide layer would reduce the effective dielectric constant of the dielectric layer. The material composition and properties for an interface layer may be dependent on process conditions and the condition of the substrate before forming the dielectric layer. Though the existence of an interface layer may effectively reduce the dielectric constant associated with the dielectric layer and its substrate, the interface layer, such as a silicon oxide interface layer or other composition interface layer, may improve the interface density, fixed charge density, and channel mobility of a device having this interface layer.

[0061] In an embodiment, the hafnium silicon oxynitride layer may be doped with other elements. The doping may be employed to enhance the leakage current characteristics of the dielectric layer containing the $HfSiON_x$ film by providing a disruption or perturbation of the hafnium silicon oxynitride structure. Such doping may be realized by substituting a sequence of one of these elements for a hafnium sequence, a silicon sequence, or various combinations of sequences. The choice for substitution may depend on the form of the hafnium silicon oxynitride structure with respect to the relative amounts of hafnium atoms and silicon atoms desired in the oxide. To maintain a substantially hafnium silicon oxynitride, the amount of dopants inserted into the oxynitride may be limited to a relatively small fraction of the total number of hafnium and silicon atoms.

[0062] In an embodiment, a $HfSiON_x$ film may be engineered to have a dielectric constant, the value of which lies in

the range from about 7 to about 14. As the hafnium content increases, the dielectric constant increases such that a value above 20 may be attained for a hafnium-rich $HfSiON_x$ film. In an embodiment, a dielectric layer containing a hafnium silicon oxynitride layer may have a t_{eq} ranging from about 5 Å to about 20 Å. In an embodiment, a dielectric layer containing a hafnium silicon oxynitride layer may have a t_{eq} of less than 5 Å. In an embodiment, a hafnium silicon oxynitride film may be formed with a thickness ranging from a monolayer to thousands of angstroms or more. Further, dielectric films of hafnium silicon oxynitride formed by atomic layer deposition may provide not only thin t_{eq} films, but also films with relatively low leakage current. Additionally, embodiments may be implemented to form transistors, capacitors, memory devices, and other electronic systems including information handling devices.

[0063] In various embodiments, the composition of an HfSiON film relative to the amounts of component elements may be changed to change the characteristics of a HfSiON film including such properties as the work function, electron affinity, and other electrical characteristics. A HfSiON film may be structured to match conductive layers that are formed on the HfSiON to provide electrical contact. In an embodiment, a HfSiON film may be formed as a high-κ dielectric insulator with conductive layers selected to provide operating characteristics for the electronic device in which the HfSiON film is disposed. In an embodiment, conductive layers are formed to contact a HfSiON film to configure a transistor with an optimum threshold voltage. In an embodiment, a gate dielectric having a HfSiON film is coupled to a gate having a tantalum layer. Tantalum as a low work function metal may be used in n-channel MOS (NMOS) transistors with a HfSiON gate dielectric to provide a threshold voltage of around 0.2 or 0.3 Volts. In an embodiment, a gate dielectric having a HfSiON film may be coupled to a gate having a titanium nitride layer. Titanium nitride having a higher work function than tantalum may be used as a gate in p-channel MOS (PMOS) transistors with a HfSiON gate dielectric to provide a threshold voltage of around 0.2 or 0.3 Volts. Titanium nitride may also be used as a gate in a NMOS transistor. In various embodiments, tantalum or titanium nitride may be used as capacitor plates in capacitor structures having a capacitor dielectric containing a HfSiON film. The choice of tantalum or titanium nitride may depend on considerations such as reliability, ease of process, and other factors. Embodiments having tunneling structures, such as flash and non-volatile read only memory (NROM) devices, choice of tantalum or titanium nitride may depend on the desired tunnel barrier, using a large work function to provide a high barrier to reduce tunneling or using a lower work function to provide a low barrier.

[0064] A tantalum layer may be formed with a $HfSiON_x$ film by atomic layer deposition using a tantalum-containing precursor that is pulsed onto the $HfSiON_x$ film in an ALD reaction chamber. In an embodiment, a tantalum halide precursor, such as TaF_5 or $TaCl_5$, may be used with hydrogen as a reactant precursor. In an embodiment, a $TaCl_5$ precursor may be used with an atomic hydrogen reactant precursor. The atomic hydrogen reactant precursor may be provided using a plasma. In an embodiment, the substrate temperature may be held at a temperature ranging from about 250° C. to about 400° C. The hydrogen reactant precursor reacts at the substrate to remove the halogen, which forms the selected tantalum halide precursor, leaving tantalum on the substrate sur-

face. After pulsing a tantalum-containing precursor and after pulsing its reactant precursor, the reaction chamber may be purged of excess precursor and/or by-products. In various embodiments, use of the individual tantalum-containing precursors is not limited to the temperature ranges of the above example embodiments. Further, forming tantalum by atomic layer deposition is not limited to the abovementioned precursors. In addition, the pulsing of the tantalum precursor may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface. The tantalum layer may be structured as one or more monolayers. The tantalum layer may a thickness ranging from a monolayer to thousands of angstroms or more.

[0065] A titanium nitride layer may be formed with a $HfSiON_x$ film by atomic layer deposition using a titanium-containing precursor that is pulsed onto the $HfSiON_x$ film in an ALD reaction chamber. A nitrogen-containing precursor may be used as the reactant precursor for the titanium-containing precursor. The titanium-containing precursor and the nitrogen-containing precursor may be selected such that their use does not form a titanium oxide in the layer of titanium nitride being formed. The titanium-containing precursor and the nitrogen-containing precursor may be selected such that these precursors do not include oxygen as an elemental component. In an embodiment, a titanium halide precursor, such as $TiCl_4$, TiI_4, or TiF_4, may be used with NH_3 as a reactant precursor. In an embodiment, a $TiCl_4$ precursor may be used with a NH_3 reactant precursor. In an embodiment, the substrate temperature may be held at a temperature ranging from about 380° C. to about 500° C. In an embodiment, the substrate temperature may be held at a temperature less than 600° C. After pulsing a titanium-containing precursor and after pulsing its reactant precursor, the reaction chamber may be purged of excess precursor and/or by-products. In various embodiments, use of the individual titanium-containing precursors is not limited to the temperature ranges of the above example embodiments. Further, forming titanium nitride by atomic layer deposition is not limited to the abovementioned precursors. In addition, the pulsing of the titanium precursor may use a pulsing period that provides uniform coverage of a monolayer on the surface or may use a pulsing period that provides partial coverage of a monolayer on the surface. The titanium nitride layer may be structured as one or more monolayers. The titanium nitride layer may a thickness ranging from a monolayer to thousands of angstroms or more.

[0066] FIG. 1 illustrates a block diagram of an embodiment of an electronic apparatus 100 having two devices 102, 103 on a substrate 105, where device 102 has a tantalum layer 112 contacting a hafnium silicon oxynitride film 110 and device 103 has a titanium nitride layer 117 contacting a hafnium silicon oxynitride film 115. Device 102 may include a transistor with hafnium silicon oxynitride film 110 as a gate dielectric and tantalum layer 112 as part of the corresponding gate. The transistor may be a NMOS transistor. Device 102 may include a capacitor with hafnium silicon oxynitride film 110 as a capacitor dielectric and tantalum layer 112 as part of the capacitor electrode. Such a capacitor may be structured as a DRAM capacitor. Such a capacitor may be structured as a capacitor in analog circuit, a radio frequency (RF) circuit, a mixed signal circuit, or combinations of these circuits. Mixed signal integrated circuits are integrated circuits that may operate with digital and analog signals. Device 103 may include a transistor with hafnium silicon oxynitride film 115 as a gate

dielectric and titanium nitride layer **117** as part of the corresponding gate. The transistor may be a PMOS transistor. The transistor may be a NMOS transistor. Device **103** may include a capacitor with hafnium silicon oxynitride film **115** as a capacitor dielectric and titanium nitride layer **117** as part of the capacitor electrode. Such a capacitor may be structured as a DRAM capacitor. Such a capacitor may be structured as a capacitor in analog circuit, a RF circuit, a mixed signal circuit, or combinations of these circuits. In an embodiment, device **103** may be a PMOS transistor and device **102** may be a NMOS transistor in an integrated circuit.

[0067] FIG. 2 shows a simplified view of an embodiment of a complementary metal oxide semiconductor (CMOS) transistor **201** having a PMOS transistor **203** including a titanium nitride layer and a hafnium silicon oxynitride film and a NMOS transistor **202** including a tantalum layer and a hafnium silicon oxynitride film. NMOS transistor **202** includes source/drain regions **206**, **208**, a gate **212** containing a tantalum layer contacting a gate insulator **210** containing a hafnium silicon oxynitride film. PMOS transistor **203** includes source/drain regions **211**, **213**, a gate **217** containing a titanium nitride layer contacting a gate insulator **215** containing a hafnium silicon oxynitride film. In various embodiments, a masking process may be employed such that one HfSiON layer is matched to a Ta gate and the second HfSiON layer is matched to a TiN gate. Such masking processes are known to those skilled in the art. Other arrangements may be used for a CMOS transistor using hafnium silicon oxynitride films with a titanium nitride gate and a tantalum gate.

[0068] Though a silicide layer may be selected for use as an electrode with various high-K gate dielectrics, work function tuning by selecting the appropriate silicide to control threshold voltage may be limited by Fermi-level pinning. A CMOS structure using hafnium silicon oxynitride films with a titanium nitride gate and a tantalum gate provides a threshold voltage control technique that uses two different conductive layers with different work functions for the PMOS and NMOS transistors of the CMOS structure. In an embodiment, the use of two such different conductive layers as gates may be structured to provide substantially symmetrical threshold voltages. In an embodiment, a CMOS structure may have symmetrical threshold voltages in the range from about ±0.3V to about ±0.5V. Atomic layer deposition may be used to structure the HfSiON layers, the TiN layers, and the Ta layers to provide a high quality high-K dielectric with TiN and Ta contacts and to reduce or minimize process damage in the formation of these layers.

[0069] The use of TiN and Ta as electrodes for HfSiON films may address the problems associated with gate depletion that is inherent in conventional poly-Si gates and the problems associated with Fermi-level pinning with poly-Si gates on high-κ gate dielectrics. Various embodiments of device structures having ALD-deposited TiN or ALD-deposited Ta as electrodes for ALD-deposited HfSiON films may address problems associated with electron mobilities being significantly less for transistors having metal/high-K structures than for transistors having a poly-Si/SiO$_2$ structures. Such degradation of electron mobilities may be related to damage caused in typical transistor fabrication in addition to remote coulomb scattering due to a large number of residual charges in the metal electrodes to the high-K dielectric. Fabrication problems in standard processes may include degrading the quality of the gate dielectric as a metal gate is formed on the gate dielectric by physical vapor deposition (PVD). In

a PVD process, dielectric degradation may occur due to plasma radiation and mixing of elements at the metal/high-κ dielectric interface. Using a CVD process, unwanted residual impurities may be incorporated the metal/high-κ structures. In addition, annealing after forming a metal gate in these typical processes may further degrade the high-κ dielectric on which the metal gate is formed due to high temperatures associated with metal annealing, where elements of the high-κ dielectric may diffuse into the metal. Forming a HfSiON film with TiN or Ta electrodes in which all the components are formed by atomic layer deposition may avoid the problems accompanying other deposition techniques.

[0070] FIG. 3 shows an embodiment of a transistor **300** having a dielectric layer **340** containing a HfSiON$_x$ film. Transistor **300** may include a source region **320** and a drain region **330** in a silicon-based substrate **310** where source and drain regions **320**, **330** are separated by a body region **332**. Body region **332** defines a channel having a channel length **334**. A gate dielectric **340** may be disposed on substrate **310** with gate dielectric **340** formed as a dielectric layer containing HfSiON$_x$. Gate dielectric **340** may be realized as a dielectric layer formed substantially of HfSiON$_x$. Gate dielectric **340** may be constructed as multiple dielectric layers, that is, as a dielectric stack, containing at least one HfSiON$_x$ film and one or more layers of insulating material other than a hafnium silicon oxynitride film. The HfSiON$_x$ film may be structured as one or more monolayers. An embodiment of a HfSiON$_x$ film may be formed using atomic layer deposition. In an embodiment, gate dielectric **340** may be realized as a gate insulator in a silicon-based CMOS transistor.

[0071] A gate **350** may be formed over and contact gate dielectric **340**. Gate **350** may include a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer. Gate **350** may include a tantalum layer structured as one or more monolayers. The tantalum layer may be an ALD tantalum layer. The thickness of the tantalum layer may range from a monolayer to thousands of angstroms or more. Gate **350** may be configured substantially as a tantalum layer. Gate **350** may include a titanium nitride layer structured as one or more monolayers. The titanium nitride layer may be an ALD titanium nitride layer. The thickness of the titanium nitride layer may range from a monolayer to thousands of angstroms or more. Gate **350** may be configured substantially as a titanium nitride layer.

[0072] An interfacial layer may form between body region and gate dielectric **340**. In an embodiment, an interfacial layer may be limited to a relatively small thickness compared to gate dielectric **340**, or to a thickness significantly less than gate dielectric **340** as to be effectively eliminated. Forming the substrate and the source and drain regions may be performed using standard processes known to those skilled in the art. Additionally, the sequencing of the various elements of the process for forming a transistor may be conducted with fabrication processes known to those skilled in the art. Transistor **300** may be an NMOS transistor. Transistor **300** may be a PMOS transistor. Transistor **300** is not limited to the arrangement illustrated in FIG. 3. Use of a gate dielectric containing hafnium silicon oxynitride is not limited to silicon based substrates, but may be used with a variety of semiconductor substrates.

[0073] FIG. 4 shows an embodiment of a floating gate transistor **400** having a dielectric layer containing a HfSiON$_x$ film. The HfSiON$_x$ film may be structured as one or more monolayers. The HfSiON$_x$ film may be formed using atomic

layer deposition techniques. Transistor **400** may include a silicon-based substrate **410** with a source **420** and a drain **430** separated by a body region **432**. Body region **432** between source **420** and drain **430** defines a channel region having a channel length **434**. Located above body region **432** is a stack **455** including a gate dielectric **440**, a floating gate **452**, a floating gate dielectric **442**, and a control gate **450**. An interfacial layer may form between body region **432** and gate dielectric **440**. In an embodiment, an interfacial layer may be limited to a relatively small thickness compared to gate dielectric **440**, or to a thickness significantly less than gate dielectric **440** as to be effectively eliminated.

[0074] In an embodiment, gate dielectric **440** includes a dielectric containing an atomic layer deposited $HfSiON_x$ film formed in embodiments similar to those described herein. Gate dielectric **440** may be realized as a dielectric layer formed substantially of $HfSiON_x$. Gate dielectric **440** may be a dielectric stack containing at least one $HfSiON_x$ film and one or more layers of other insulating materials.

[0075] In an embodiment, floating gate **452** may be formed over and contact gate dielectric **440**. Floating gate **452** may include a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer. Floating gate **452** may include a tantalum layer structured as one or more monolayers. The tantalum layer may be an ALD tantalum layer. The thickness of the tantalum layer may range from a monolayer to thousands of angstroms or more. Floating gate **452** may be configured substantially as a tantalum layer. Floating gate **452** may include a titanium nitride layer structured as one or more monolayers. The titanium nitride layer may be an ALD titanium nitride layer. The thickness of the titanium nitride layer may range from a monolayer to thousands of angstroms or more. Floating gate **452** may be configured substantially as a titanium nitride layer.

[0076] In an embodiment, floating gate dielectric **442** includes a dielectric containing a $HfSiON_x$ film. The $HfSiON_x$ film may be structured as one or more monolayers. In an embodiment, the $HfSiON_x$ may be formed using atomic layer deposition techniques. Floating gate dielectric **442** may be realized as a dielectric layer formed substantially of $HfSiON_x$. Floating gate dielectric **442** may be a dielectric stack containing at least one $HfSiON_x$ film and one or more layers of other insulating materials.

[0077] In an embodiment, control gate **450** may be formed over and contact floating gate dielectric **442**. Control gate **450** may include a tantalum layer, a titanium nitride layer, or a combination of a tantalum layer and a titanium nitride layer. Control gate **450** may include a tantalum layer structured as one or more monolayers. The tantalum layer may be an ALD tantalum layer. The thickness of the tantalum layer may range from a monolayer to thousands of angstroms or more. Control gate **450** may be configured substantially as a tantalum layer. Control gate **450** may include a titanium nitride layer structured as one or more monolayers. The titanium nitride layer may be an ALD titanium nitride layer. The thickness of the titanium nitride layer may range from a monolayer to thousands of angstroms or more. Control gate **450** may be configured substantially as a titanium nitride layer.

[0078] Alternatively, both gate dielectric **440** and floating gate dielectric **442** may be formed as dielectric layers containing a $HfSiON_x$ film structured as one or more monolayers. Control gate **450** and floating gate **452** may be formed as conductive layers containing a Ta layer, a TiN_s layer, or a combination of a Ta layer and a TiN_s layer with each layer

structured as one or more monolayers. Gate dielectric **440**, floating gate dielectric **442**, control gate **450**, and floating gate **452** may be realized by embodiments similar to those described herein, with the remaining elements of the transistor **400** formed using processes known to those skilled in the art. In an embodiment, gate dielectric **440** forms a tunnel gate insulator and floating gate dielectric **442** forms an inter-gate insulator in flash memory devices, where gate dielectric **440** and floating gate dielectric **442** may include a hafnium silicon oxynitride film structured as one or more monolayers. Floating gate transistor **400** is not limited to the arrangement illustrated in FIG. **4**. Such structures are not limited to silicon-based substrates, but may be used with a variety of semiconductor substrates.

[0079] Embodiments of a hafnium silicon oxynitride film structured as one or more monolayers having a Ta or a TiN_s electrode structured as one or more monolayers may also be applied to capacitors in various integrated circuits, memory devices, and electronic systems. In an embodiment for a capacitor **500** illustrated in FIG. **5**, a method includes forming a first conductive layer **510**, forming a dielectric layer **520** containing a hafnium silicon oxynitride film structured as one or more monolayers on first conductive layer **510**, and forming a second conductive layer **530** on dielectric layer **520**. Second conductive layer **530**, first conductive layer **510** or both second and first conductive layers **530, 510** may include a Ta layer, a TiN_s layer, or combination of a Ta layer and a TiN_s layer. Dielectric layer **520**, containing a $HfSiON_x$ film, and conductive layers **510, 520** may be formed using various embodiments described herein. Dielectric layer **520** may be realized as a dielectric layer formed substantially of $HfSiON_x$. Dielectric layer **520** may be a dielectric stack containing at least one $HfSiON_x$ film and one or more layers of other insulating materials. Embodiments for a hafnium silicon oxynitride film having a Ta conductive layer, a TiN_s conductive layer, or a combination of a Ta conductive layer and a TiN_s conductive layer structured as one or more monolayers may include, but are not limited to, a capacitor in a DRAM and capacitors in analog, radio frequency (RF), and mixed signal integrated circuits.

[0080] FIG. **6** depicts an embodiment of a dielectric structure **600** having multiple dielectric layers **605-1, 605-2, . . . 605**-N, in which at least one layer is a hafnium silicon oxynitride layer. Layers **610** and **620** may provide means to contact dielectric layers **605-1, 605-2, . . . 605**-N. Each layer **610, 620** or both layers may be conductive layers containing a Ta layer, a TiN_s layer, or a combination of a Ta layer and a TiN_s layer. Layers **610** and **620** may be electrodes forming a capacitor. Layer **610** may be a body region of a transistor with layer **620** being a gate. Layer **610** may be a floating gate electrode with layer **620** being a control gate.

[0081] In an embodiment, dielectric structure **600** includes one or more layers **605-1, 605-2 . . . 605**-N as dielectric layers other than a HfSiON layer, where at least one layer is a HfSiON layer. Dielectric layers **605-1, 605-2 . . . 605**-N may include a HfO_x layer, a SiN_r layer, a SiO_z layer, a HfSiO layer, a SiON layer, or various combinations of these layers. Dielectric layers **605-1, 605-2 . . . 605**-N may include an insulating metal oxide layer, whose metal is selected to be a metal different from hafnium. Dielectric layers **605-1, 605-2, . . . 605**-N may include an insulating nitride layer. Dielectric layers **605-1, 605-2, . . . 605**-N may include an insulating oxynitride layer. Dielectric layers **605-1, 605-2, . . . 605**-N may include an insulating silicate layer.

[0082] Various embodiments for a dielectric layer containing a hafnium silicon oxynitride film structured as one or more monolayers may provide for enhanced device performance by providing devices with reduced leakage current. Such improvements in leakage current characteristics may be attained by forming one or more layers of a hafnium silicon oxynitride in a nanolaminate structure with other metal oxides, non-metal-containing dielectrics, or combinations thereof. The transition from one layer of the nanolaminate to another layer of the nanolaminate provides disruption to a tendency for an ordered structure in the nanolaminate stack. The term "nanolaminate" means a composite film of ultra thin layers of two or more materials in a layered stack. Typically, each layer in a nanolaminate has a thickness of an order of magnitude in the nanometer range. Further, each individual material layer of the nanolaminate may have a thickness as low as a monolayer of the material or as high as 20 nanometers. In an embodiment, a HfO_x/HfSiON nanolaminate contains alternating layers of a hafnium oxide and HfSiON. In an embodiment, a SiN_y/HfSiON nanolaminate contains alternating layers of silicon nitride and HfSiON. In an embodiment, a SiO_z/HfSiON nanolaminate contains alternating layers of silicon oxide and HfSiON. In an embodiment, a HfO_x/SiN_y/SiO_z/HfSiON nanolaminate contains various permutations of hafnium oxide layers, silicon nitride layers, silicon oxide layers, and hafnium silicon oxynitride layers.

[0083] In an embodiment, dielectric structure 600 may be structured as a nanolaminate structure 600 including a $HfSiON_x$ film structured as one or more monolayers. Nanolaminate structure 600 includes a plurality of layers 605-1, 605-2 to 605-N, where at least one layer contains a $HfSiON_x$ film structured as one or more monolayers. The other layers may be insulating nitrides, insulating oxynitrides, and other dielectric materials such as insulating metal oxides. The sequencing of the layers depends on the application. The effective dielectric constant associated with nanolaminate structure 600 is that attributable to N capacitors in series, where each capacitor has a thickness defined by the thickness and composition of the corresponding layer. By selecting each thickness and the composition of each layer, a nanolaminate structure can be engineered to have a predetermined dielectric constant. Embodiments for structures such as nanolaminate structure 600 may be used as nanolaminate dielectrics in NROM flash memory devices as well as other integrated circuits. In an embodiment, a layer of the nanolaminate structure 600 is used to store charge in a NROM device. The charge storage layer of a nanolaminate structure 600 in a NROM device may be a silicon oxide layer.

[0084] Transistors, capacitors, and other devices may include dielectric films containing a layer of a hafnium silicon oxynitride compound structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. The hafnium silicon oxynitride layer, tantalum, and the titanium nitride may be formed by atomic layer deposition. Dielectric films containing a hafnium silicon oxynitride layer with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride may be implemented into memory devices and electronic systems including information handling devices. Further, embodiments of electronic devices and electronic apparatus may be realized as integrated circuits. Embodiments of information handling devices may include wireless systems, telecommunication systems, and computers.

[0085] FIG. 7 illustrates a block diagram for an electronic system 700 having one or more devices having a dielectric structure including a $HfSiON_x$ film structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. Electronic system 700 includes a controller 705, a bus 715, and an electronic device 725, where bus 715 provides electrical conductivity between controller 705 and electronic device 725. In various embodiments, controller 705 may include an embodiment of a $HfSiON_x$ film with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride. In various embodiments, electronic device 725 may include an embodiment of a $HfSiON_x$ film with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride. In various embodiments, controller 705 and electronic device 725 may include embodiments of a $HfSiON_x$ film with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride. Electronic system 700 may include, but is not limited to, fiber optic systems, electro-optic systems, and information handling systems such as wireless systems, telecommunication systems, and computers.

[0086] FIG. 8 depicts a diagram of an embodiment of a system 800 having a controller 805 and a memory 825. Controller 805 may include a $HfSiON_x$ film structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. Memory 825 may include a $HfSiON_x$ film structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. Controller 805 and memory 825 may each include a $HfSiON_x$ film structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. System 800 also includes an electronic apparatus 835 and a bus 815, where bus 815 provides electrical conductivity between controller 805 and electronic apparatus 835, and between controller 805 and memory 825. Bus 815 may include an address bus, a data bus, and a control bus, each independently configured. Alternatively, bus 815 may use common conductive lines for providing one or more of address, data, or control, the use of which is regulated by controller 805. In an embodiment, electronic apparatus 835 may be additional memory configured in a manner similar to memory 825. An embodiment may include an additional peripheral device or devices 845 coupled to bus 815. In an embodiment, controller 805 is a processor. One or more of controller 805, memory 825, bus 815, electronic apparatus 835, or peripheral devices 845 may include an embodiment of a dielectric layer having a $HfSiON_x$ film structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. System 800 may include,

but is not limited to, information handling devices, telecommunication systems, and computers.

[0087] Peripheral devices **845** may include displays, additional storage memory, or other control devices that may operate in conjunction with controller **805**. Alternatively, peripheral devices **845** may include displays, additional storage memory, or other control devices that may operate in conjunction with memory **825**, or controller **805** and memory **825**.

[0088] Memory **825** may be realized as a memory device containing a HfSiON$_x$ film structured as one or more monolayers with a tantalum electrode, a titanium nitride electrode, or an electrode having a combination of a tantalum and a titanium nitride, the tantalum and titanium nitride structured as one or more monolayers. A HfSiON$_x$ structure with a Ta conductive layer, a TiN$_s$ conductive layer, or a combination of a Ta conductive layer and a TiN$_s$ conductive layer may be formed in a memory cell of a memory array. Such a structure may be formed in a capacitor in a memory cell of a memory array. Such a structure may be formed in a transistor in a memory cell of a memory array. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device. Memory types include a DRAM, SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as other emerging DRAM technologies.

[0089] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. It is to be understood that the above description is intended to be illustrative, and not restrictive, and that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon studying the above description.

What is claimed is:

1. An electronic device comprising:

a dielectric including hafnium silicon oxynitride, the hafnium silicon oxynitride doped with elements or compounds other than hafnium or silicon; and

a conductive material coupled to the dielectric.

2. The electronic device of claim **1**, wherein the dielectric is structured as a stack of dielectrics.

3. The electronic device of claim **1**, wherein the electronic device includes:

tantalum as the conductive material coupled to the hafnium silicon oxynitride such that the tantalum is disposed as a gate with the hafnium silicon oxynitride as a gate insulator in a PMOS transistor of a CMOS structure; and

a titanium nitride as a gate on another region of hafnium silicon oxynitride in a NMOS transistor of the CMOS structure such that the NMOS transistor and the PMOS transistor have substantially symmetrical threshold voltages.

4. The electronic device of claim **1**, wherein the electronic device includes a memory device structured with the hafnium silicon oxynitride disposed in a nanolaminate containing silicon oxide as a charge storage region of the nanolaminate.

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