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(56) Documents Cited:
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(58) Field of Search:
INT CL^7 **H01L**
Other: **EPODOC, WPI, JAPIO**

(54) Abstract Title: **Noise eliminating system on chip and method of manufacture**

(57) A noise filtering device 50, possibly a de-coupling capacitor, is mounted on the upper surface of a chip 60, for eliminating the simultaneous switching noise caused by rapid switching between the wire bonding and the trace of the chip-carrying substrate. An embodiment is described, whereby a conductive trace on the chip surface comprises guiding devices (fig 6 : 61', 62'), for example inner circuits of the chip, which connect to bonding pads 41 of the power supply terminal 30 and grounding terminal 40, and to connecting ports 53 of the noise filtering device.

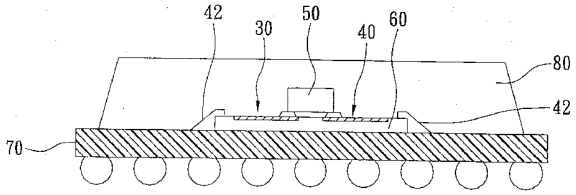

FIG. 4

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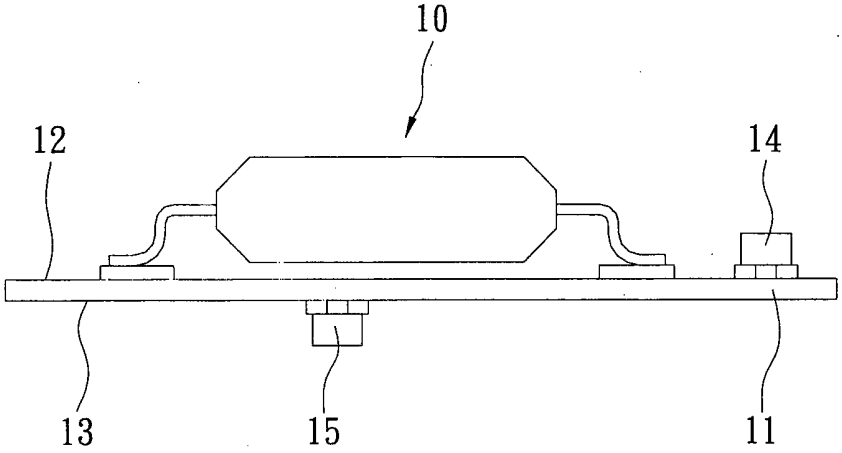

FIG. 1
PRIOR ART

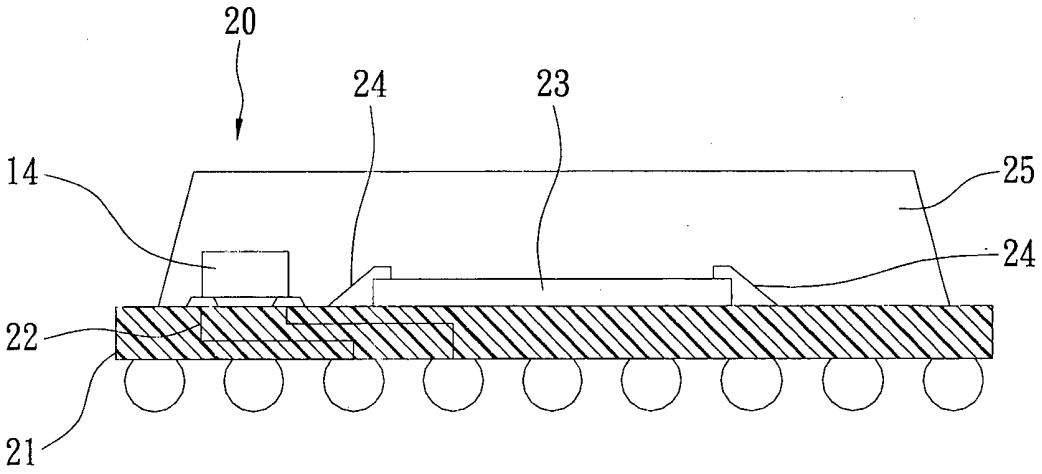

FIG. 2
PRIOR ART

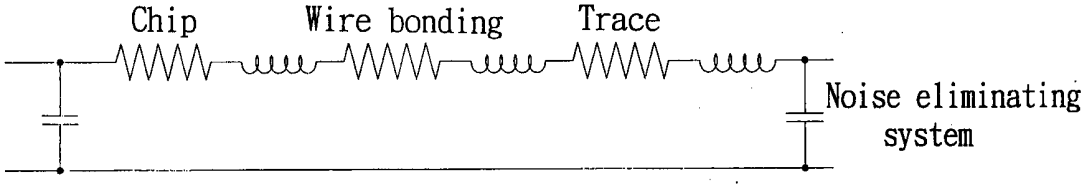

FIG. 3
PRIOR ART

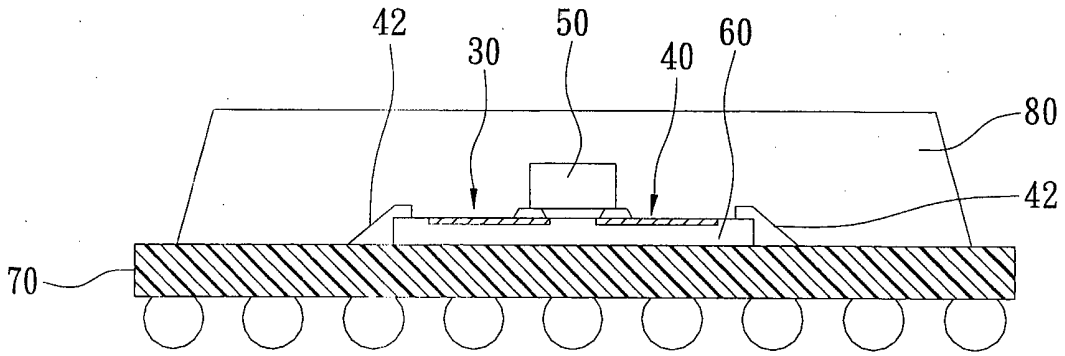

FIG. 4

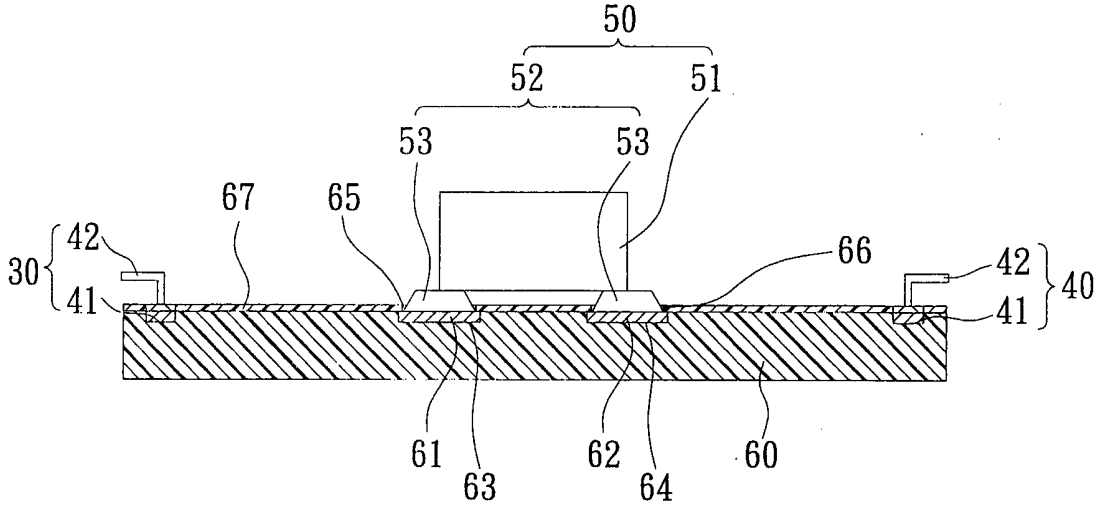
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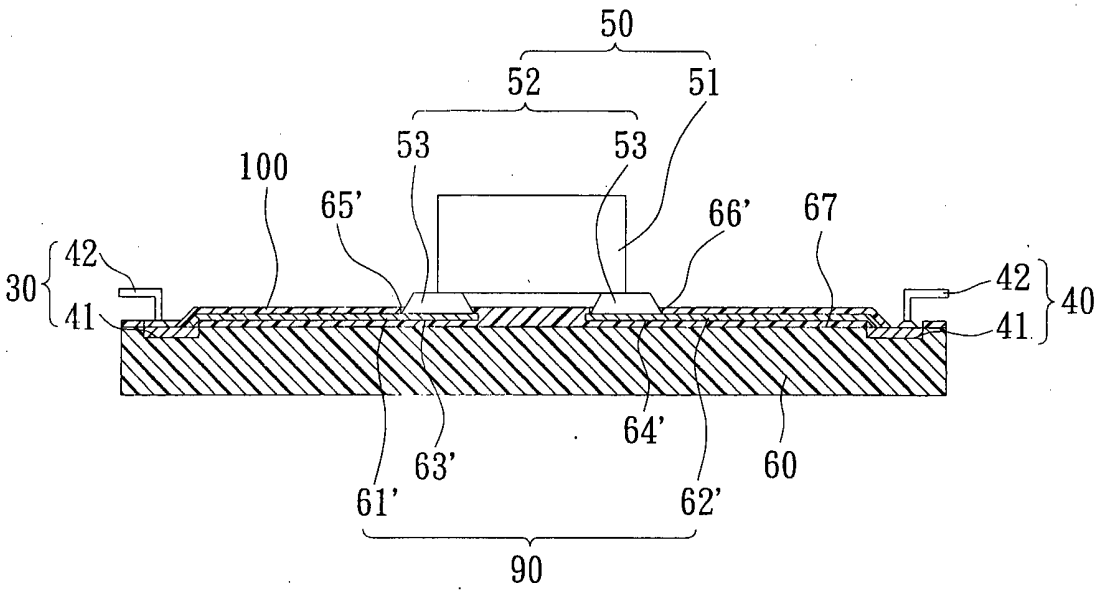
FIG. 5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100
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90

FIG. 6

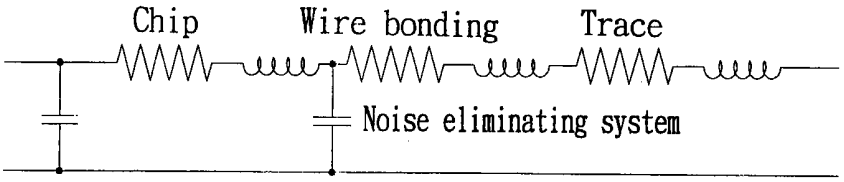

FIG. 7

NOISE FILTERING DEVICE ON CHIP AND METHOD OF MAKING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a packaged chip or die with a noise-suppressing system. More particularly, the present invention relates to a noise-suppressing system, which is electrically connected to a chip, capable of reducing or eliminating excess noise.

2. Description of the Prior Art

Please refer to Fig.1. Fig.1 illustrates a cross section of a conventional leadframe package structure 10 mounted on a printed circuit board 11. The printed circuit board 11 comprises an upper surface 12 and a lower surface 13. For a four-layer printed circuit board 11, the upper surface 12 and the lower surface 13 may be one of the power supply layer, grounded layer, signal layer, or device layer. Passive components 14 and 15 are mounted on either upper surface 12 or lower surface 13 by surface mount technology (SMT) known in the art. For example, the passive components 14 and 15 may be de-coupling capacitors used to reduce or eliminate undesired coupling between circuits or simultaneous switching noise (SSN) between the power supply layer and the grounded layer of a high-frequency circuit.

Please refer to Fig.2. Fig.2 is a cross-sectional view of a prior art ball grid array (BGA) package 20. As shown in Fig.2, a trace 22 is provided in a substrate 21 of the BGA package 20. A chip 23 is mounted on the substrate 21 and is connected with the trace 22 of the substrate 21 via a wire bonding 24. A passive component 14 is mounted

on an upper surface of the substrate 21 by SMT. The chip 23 and the passive component 14 on the substrate 21 are encapsulated with encapsulant 25. Again, the passive component 14 may be a de-coupling capacitor used to reduce or eliminate undesired coupling between circuits or SSN between the power supply layer and the grounded layer of a high-frequency circuit.

Typically, the de-coupling capacitor is preferably mounted in the proximity of the chip 23 to enhance the performance of the de-coupling capacitor to reduce SSN of the chip 23. However, as the prior art examples shown in Fig.1 and Fig.2, the chip 23 and the de-coupling capacitor(s) are rested on the substrate 21 or the printed circuit board 11. In such case, referring to Fig.3, the efficiency of the de-coupling capacitor is reduced by the accumulated inductance and resistance in the coupling path. This causes a significant performance reducing of the de-coupling capacitor. Further, with reference to Fig.1, in practice, the passive components 14 and 15 occupy a portion of the area of the upper surface 12 or the lower surface 13 of the printed circuit board 11. With reference to Fig.2, the passive component 14 is disposed on the substrate 21. Under the above-described circumstance, when the number of the passive components 14 and 15 increases, there will be no more capacity for additional bonding route or other devices on the printed circuit board 11 or on the substrate 21. In other words, the prior art packaging geometry limits the possibility of shrinking the dimension of the printed circuit board 11 or the substrate 21.

Thus, there is a strong need for an improved chip package, which is reliable, cost-effective and is capable

of effectively eliminating SSN.

SUMMARY OF THE INVENTION

Accordingly, the main object of the invention is to provide an improved chip package in combination with a noise-eliminating system and a fabrication method thereof to solve the above-mentioned problems. The noise filtering device is mounted on the upper surface of the chip, such that the noise filtering device can approach the power supply terminal and the grounding terminal as close as possible, thereby enhancing the performance of the passive component.

Another object of the present invention is to provide a noise filtering device on chip and method of making the same to minimize the number of devices needed to be installed between the chip and the noise filtering device, thereby decreasing accumulated impedance caused by high-frequency circuit between the chip and the noise filtering device, thereby enhancing the performance of the passive component.

Still another object of the present invention is to provide a noise filtering device on chip and method of making the same, in which the noise filtering device is directly mounted on the upper surface of the chip, thereby saving a great deal of substrate space and making it possible to shrink the size of the printed circuit board or the substrate, and thus reduce the cost.

To achieve the above goals, a noise filtering device on chip and method of fabricating the same are provided.

A noise filtering device is connected to a chip. There are conductor trace provided on the chip for connecting with the noise filtering device, thereby reducing simultaneous switching noise of the chip.

According to one aspect of this invention, a noise filtering device on chip is provided. The noise filtering device on chip comprises a chip; a power supply terminal provided on the chip and being electrically connected to the chip; a grounding terminal provided on the chip and being electrically connected to the chip; a conductor trace installed on an upper surface of the chip and being electrically connected to the power supply terminal and the grounding terminal; and at least one noise filtering device comprising a connecting unit and a noise filtering unit, wherein the connecting unit is electrically connected to the noise filtering unit, and wherein the connecting unit is electrically connected to the conductor trace.

According to one aspect of this invention, a method for fabricating a noise filtering device on chip, which comprises the steps of:

providing a chip having thereon a power supply terminal and a grounding terminal;

forming a guiding device layer on an upper surface of the chip;

etching the guiding device layer to form the guiding devices;

providing a noise filtering device;

using surface mount technology to install the noise filtering device on the upper surface of the chip, and the noise filtering device connects to the guiding devices; and

jointing the junction between the noise filtering device and the guiding devices such that the noise filtering device is electrically connected to the guiding devices.

Other objects, advantages and novel features of the invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 illustrates a cross section of a conventional leadframe package structure mounted on a printed circuit board.

Fig.2 is a cross-sectional view of a prior art ball grid array (BGA) package.

Fig.3 illustrates the simultaneous switching noise (SSN) accumulated from the chip, the wire bonding, and the trace.

Fig.4 is a cross-sectional diagram illustrating the BGA package according to the present invention.

Fig.5 is a cross sectional view of this invention.

Fig.6 is a cross sectional view of this invention.

Fig.7 is a circuit diagram of this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Please refer to Fig.4 to Fig.6. The present invention is directed to chip package in combination with a noise filtering device and a fabrication method thereof. As shown in Fig.4, power supply terminal 30, grounding

terminal 40, and noise filtering device 50 are directly disposed on the chip 60 and electrically connected to each other, such that the noise filtering device 50 can eliminate undesired coupling between circuits or SSN between the power supply layer and the grounded layer of a high-frequency circuit in a more effective way. Such chip 60 with the noise filtering device 50 directly built thereon is then mounted on a substrate 70. Necessary electric connection is provided. Finally, the chip 60 with the noise filtering device 50 is packaged on the substrate 70 by using encapsulant 80.

As shown in Fig.4 to Fig.6, in the chip 60, the power supply terminal 30 and the grounding terminal 40 are provided. Both of the power supply terminal 30 and the grounding terminal 40 have corresponding bonding pads 41 and wire bonds 42. The bonding pads 41 are disposed on the chip 60 and electrically connected to each other. The wire bonds 42, which are electrically connected to conductive trace (not shown) on the substrate 70, are soldered on the corresponding bonding pads 41.

As best seen in Fig.5, in accordance with the first preferred embodiment of this invention, a first guiding device 61 and a second guiding device 62 are installed in the chip 60. The first guiding device 61 is installed in a first region 63 in the chip 60 and the second guiding device 62 is installed in the second region 64 in the chip 60, where the first and second regions 63 and 64 are connected with outer environment. The first guiding device 61 is connected to the bonding pad 41 of the power supply terminal 30 and the second guiding device 62 is connected to the bonding pad 41 of the grounding terminal 40 (not shown). On the upper surface67 of the chip 60

there is provided a protection layer. A first guiding device opening 65 and a second guiding device opening 66 are formed in the protection layer, wherein the first guiding device opening 65 is connected to the first guiding device 61 in the first region 63, and the second guiding device opening 66 is connected to the second guiding device 62 in the second region 64, wherein the first region 63 and the second region 64 are located on the chip 60, such that the first and second guiding devices 61 and 62 are connected to outer environment. The noise filtering device 50 comprises connecting unit 51 and noise filtering unit 52 and both are electrically connected to each other. The connecting unit 51 comprises two connecting ports 53, which are respectively protrude from the first guiding device openings 65 and 66 and are respectively connected to the first guiding device 61 in the first region 63 and the second guiding device 62 in the second region 64. The noise filtering device 50 may be a passive component such as a de-coupling capacitor, and the above-described guiding devices 61 and 62 are inner circuits of the chip 60. The power supply terminal 30, the grounding terminal 40, and the noise filtering device 50 can be installed at one side of the chip 60.

As best seen in Fig.6, in accordance with the second preferred embodiment of this invention, a noise filtering device 50 and an additional conductor trace 90 are installed on the upper surface 67 of the chip 60. The conductor trace 90 comprises a first guiding device 61′ and a second guiding device 62′, which are respectively located in the first region 63′ and second region 64′ of the chip 60. The first guiding device 61′ is electrically connected to the bonding pad 41 of the power supply terminal 30 and the second guiding device 62′ is

electrically connected to the bonding pad 41 of the grounding terminal 40. A protection layer 100 is provided over the guiding devices 61′ and 62′ and over the chip 60. A first guiding device opening 65′ and a second guiding device opening 66′ are formed in the protection layer 100. The first guiding device opening 65′ and the second guiding device opening 66′ correspond to the first guiding device 61′ in the first region 63′ and the second guiding device 62′ in the second region 64′, respectively. The first and second regions 63′ and 64′ are located on the chip 60. The connecting unit 51 of the noise filtering unit 52comprises two connecting ports 53, which respectively protrude from the first and second guiding device openings 65′ and 66′, and are electrically connected to the first guiding device 61′ in the first region 63′ and the second guiding device 62′ in the second region 64′, respectively. The above-described guiding devices 61′ and 62′ may be circuit, and the noise filtering device 50 may be a de-coupling capacitor.

As shown in Fig.4, a chip 60 in combination with a noise filtering device 50 is installed on a ball grid array (BGA) substrate 70. The substrate 70 comprises conductive trace (not shown) connecting to respective power supply and grounding. The power supply terminal 30 and the grounding terminal 40 of the chip 60 are electrically connected to the power trace and the grounding trace of the substrate 70 through the wire bonding 42. The chip 60 with the noise filtering device 50 is encapsulated on the substrate 70 with encapsulant 80. Preferably, the conductor trace 90 is a metal redistribution layer.

Fig.7 illustrates an equivalent circuit showing the

noise filtering device 50 on chip 60. The simultaneous switching noise (SSN) caused by rapid switching between the wire bonding 42 and the trace of the substrate 70 is eliminated.

In accordance with the present invention, a method for fabricating the noise filtering device on chip comprising the steps of:

providing a chip having a grounding terminal and a power supply terminal;

forming a guiding layer on the upper surface of the chip;

etching the guiding layer to form the guiding devices;

providing a noise filtering device;

using surface mount technology to install the noise filtering device on the upper surface of the chip, and the noise filtering device connects to the guiding devices; and

jointing the junction between the noise filtering device and the guiding devices such that the noise filtering device is electrically connected to the guiding devices.

The guiding layer is made of conductive materials sputtered on the upper surface of the chip and is selectively etched away to form a plurality of guiding devices.

To sum up, the present invention has the following advantages:

1. The noise filtering device is directly installed on the chip and is electrically connected to the chip, thereby shrinking the connecting distance between the chip and the

noise filtering device.

2. The simultaneous switching noise (SSN) is effectively eliminated.

3. The number of devices that are needed on the substrate or printed circuit board is reduced, such that the size of the substrate or printed circuit board is shrinkable, thereby reducing cost.

It is to be understood, however, that even though numerous characteristics and advantages of the present invention have been set forth in the foregoing description, together with details of the structure and function of the invention, the disclosure is illustrative only, and changes may be made in detail, especially in matters of shape, size, and arrangement of parts within the principles of the invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

CLAIMS

1. A noise filtering device on chip, comprising:

a chip;

a power supply terminal provided on the chip and being electrically connected to the chip;

a grounding terminal provided on the chip and being electrically connected to the chip;

a conductor trace installed on an upper surface of the chip and being electrically connected to the power supply terminal and the grounding terminal; and

at least one noise filtering device electrically connected to said conductor trace and mounted on said upper surface.

2. The noise filtering device on chip as claimed in claim 1 wherein said noise filtering device comprising a connecting unit and a noise filtering unit, wherein the connecting unit is electrically connected to the noise filtering unit, and wherein the connecting unit is electrically connected to the conductor trace.

3. The noise filtering device on chip as claimed in claim 2 further comprises a protection layer, which is provided on the conductor trace and the chip, and at least one guiding device opening is formed on the protection layer and provided at the joint between the conductor trace and the connecting unit of the noise filtering device.

4. The noise filtering device on chip as claimed in claim 2 wherein the conductor trace comprises at least one first guiding device and at least one second guiding device, which are installed in a first region and second

region of the chip respectively, and wherein the first guiding device is electrically connected to the power supply terminal and the second guiding device is electrically connected to the grounding terminal.

5. The noise filtering device on chip as claimed in claim 4 wherein the a first guiding device opening and a second guiding device opening corresponding to the first guiding device in the first region and the second guiding device in the second region respectively are provided in the protection layer that covers the conductor trace and the chip.

6. The noise filtering device on chip as claimed in claim 5 wherein the connecting unit of the noise filtering device comprises two connecting ports which protrude through respective first and second guiding openings to electrically connect to the first and second guiding devices.

7. The noise filtering device on chip as claimed in claim 4 wherein the first and second regions are located on the chip.

8. The noise filtering device on chip as claimed in claim 4 wherein the guiding device is a circuit.

9. The noise filtering device on chip as claimed in claim 1 wherein the noise filtering device is a passive component.

10. The noise filtering device on chip as

claimed in claim 1 wherein the noise filtering device is a de-coupling capacitor.

11. A noise filtering device on chip, comprising:

a chip; and

at least one noise filtering device electrically connected to one surface of the chip.

12. The noise filtering device on chip as claimed in claim 11 wherein the noise filtering device is a de-coupling capacitor.

13. The noise filtering device on chip as claimed in claim 11 wherein the noise filtering device has two terminals which are electrically connected to guiding devices on the upper layer of the chip and are electrically connected to power supply terminal and grounding terminal of the chip respectively.

14. The noise filtering device on chip as claimed in claim 11 wherein the two terminals of the noise filtering device are electrically connected to an additional guiding device on the chip and are connected to respective power supply and grounding.

15. The noise filtering device on chip as claimed in claim 14 wherein the additional guiding device on the chip is a redistribution layer.

16. A method for fabricating a noise filtering device on chip, comprising the steps of:

providing a chip having thereon a power supply terminal and a grounding terminal;

forming a guiding device layer on an upper surface of

the chip;

etching the guiding device layer to form the guiding devices;

providing a noise filtering device;

using surface mount technology to install the noise filtering device on the upper surface of the chip, and the noise filtering device connects to the guiding devices; and

jointing the junction between the noise filtering device and the guiding devices such that the noise filtering device is electrically connected to the guiding devices.

17. The noise filtering device on chip as claimed in claim 16 wherein the guiding device layer is made of conductive material sputtered on the upper surface of the chip.

18. The noise filtering device on chip as claimed in claim 16 wherein the noise filtering device is a passive component.

19. The noise filtering device on chip as claimed in claim 16 wherein the noise filtering device is a de-coupling capacitor.

20. The noise filtering device on chip as claimed in claim 16 wherein the guiding devices are circuit layers inside the chip.

21. A semiconductor package substantially as described hereinabove with reference to Figures 4, 5 and 7 optionally modified in accordance with Figure 6 of the accompanying drawings.

22. A method of forming an on-chip noise-filtering arrangement substantially as described hereinabove with reference to Figures 4, 5 and 7 optionally modified in Figure 6 of the accompanying drawings.

INVESTOR IN PEOPLE

16

Application No: GB 0310609.3 **Examiner:** Anna Brandon
Claims searched: 1-11 **Date of search:** 6 November 2003

Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
X	1-11	JP4326565 A	(NIPPON ELECTRIC) English language abstract, figs a & b
X	1, 2, 4, 7-11	US5095402 A	(ROGERS) figs 5A & B, 6 A& B, col 6 lines 47-56
X	1, 4, 7-11	JP8241958 A	(IBM) English language abstract, figs 1-8
X	1, 2, 4, 7-11	US6084464 A	(KONINK PHILIPS ELECTRONICS) abstract, col 2 lines 34-38
X	1, 2, 4, 7-11	US2002145180 A	(ANZAI) figs 10, 12, 31 & 33, paras 103-113, 181-196 (4th, 5th, 14th & 15 embodiments)
X	1, 2, 4, 7-11	EP0656658 A	(IBM) col 5 line 46- col 6 line 21, fig 3

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X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[V]:

Worldwide search of patent documents classified in the following areas of the IPC[7]:

H01L

The following online and other databases have been used in the preparation of this search report :

EPODOC, WPI, JAPIO