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(19) **United States**(12) **Patent Application Publication**
Kim(10) **Pub. No.: US 2005/0178505 A1**(43) **Pub. Date: Aug. 18, 2005**(54) **ELECTRODE FOR DRY ETCHING A WAFER****Publication Classification**(76) Inventor: **Young Yul Kim, Sungham (KR)**(51) **Int. Cl.⁷ C23F 1/00**(52) **U.S. Cl. 156/345.47**

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SQUIRE, SANDERS & DEMPSEY LLP**600 HANSEN WAY****PALO ALTO, CA 94304-1043 (US)**(57) **ABSTRACT**(21) Appl. No.: **10/506,558**(22) PCT Filed: **Apr. 19, 2002**(86) PCT No.: **PCT/KR02/00715**(30) **Foreign Application Priority Data**

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Disclosed is an electrode for dry etching a wafer. The electrode includes a first electrode and a second electrode. The first electrode includes a first flat plate and a ring-shaped first protrusion corresponding to one surface of the edge of a wafer, and the second electrode includes a second flat plate and a ring-shaped second protrusion corresponding to the other surface of the edge of the wafer. The first plate and the second flat plate are the same dimension, and the first protrusion and the second protrusion are the same dimension.

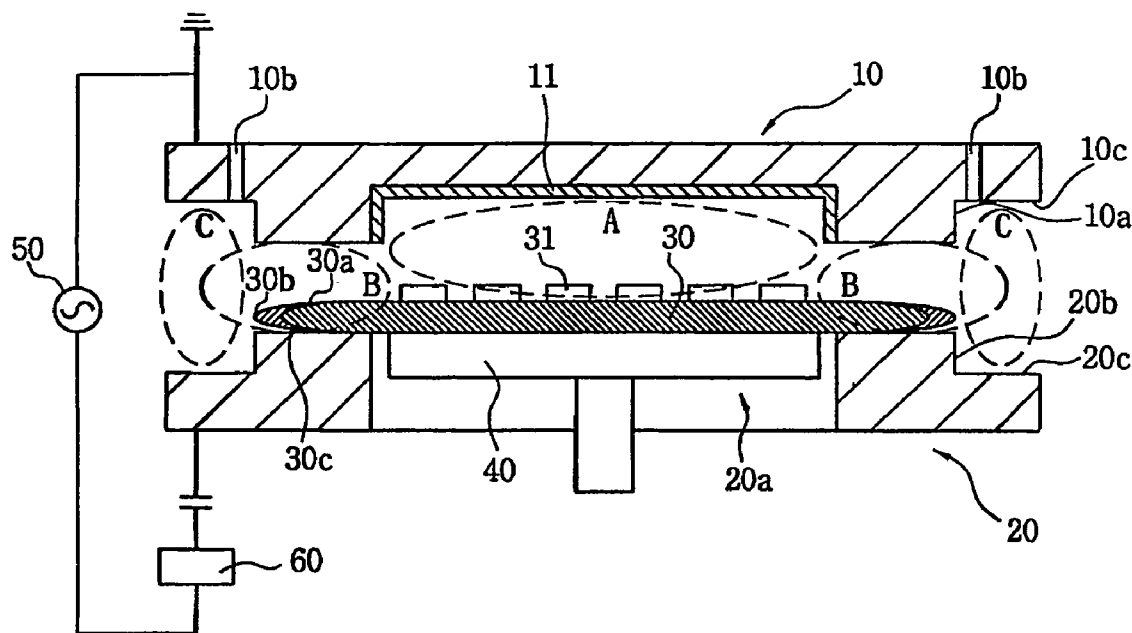


Fig. 1

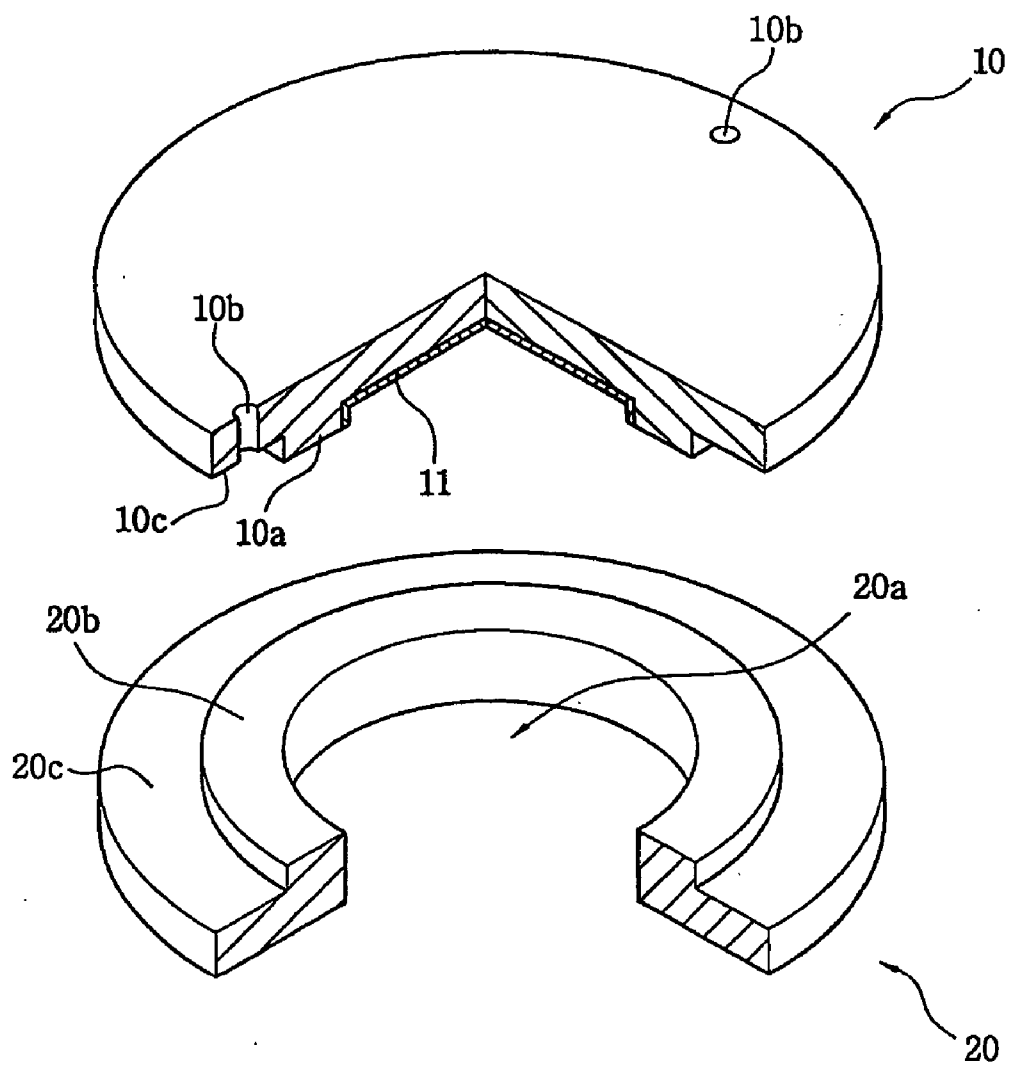


Fig. 2

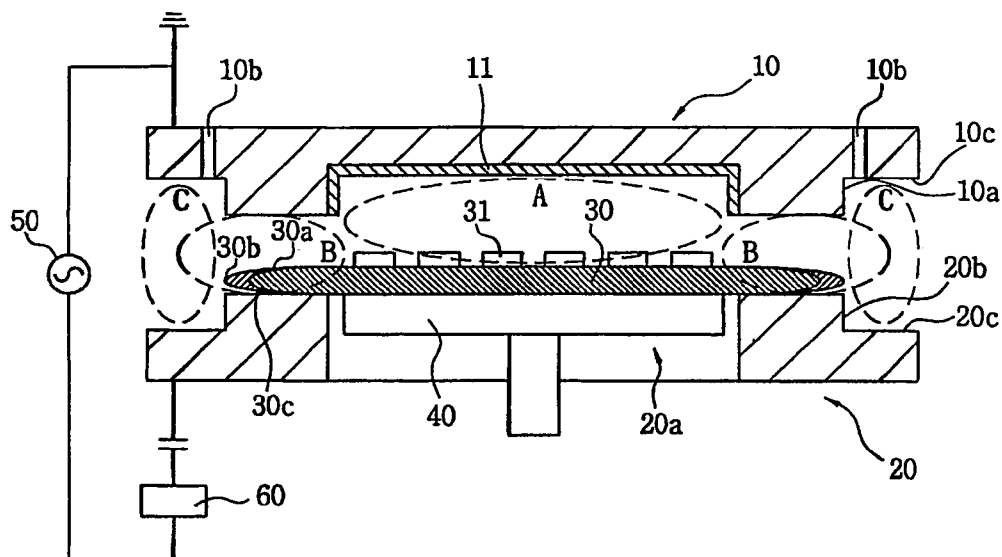


Fig. 3

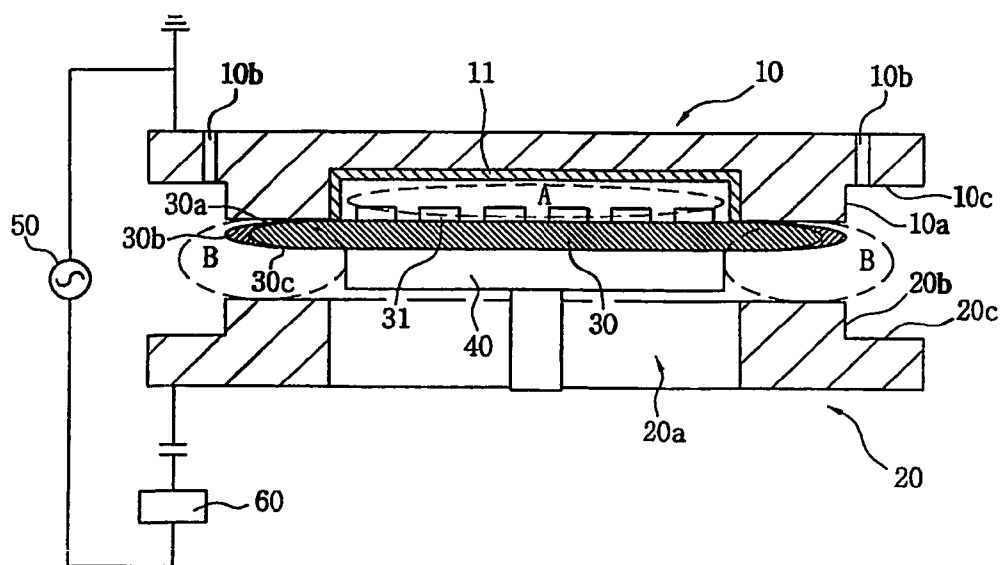


Fig. 4

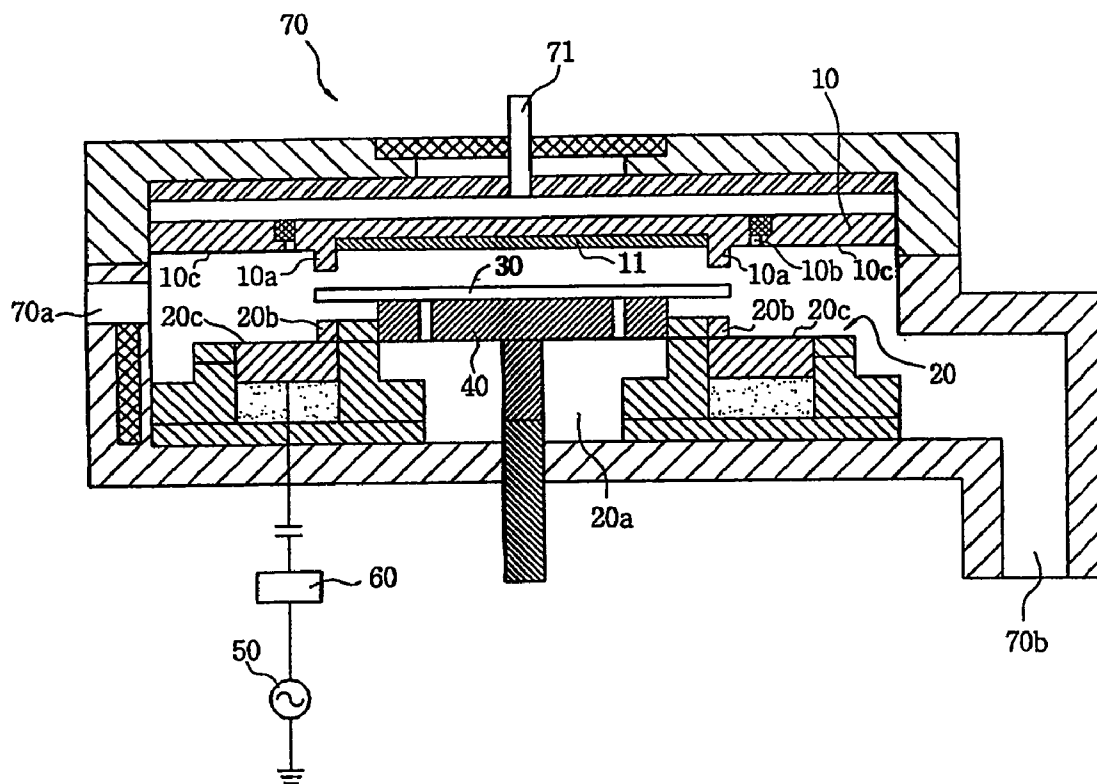


Fig. 5

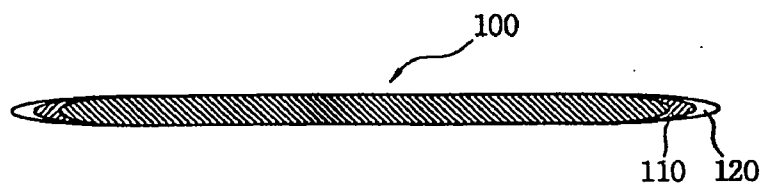


Fig. 6

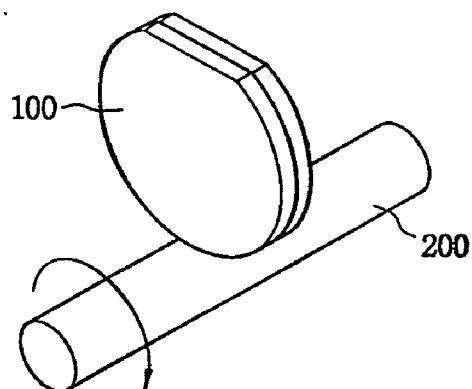


Fig. 7a

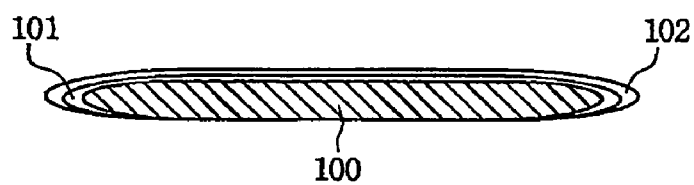


Fig. 7b

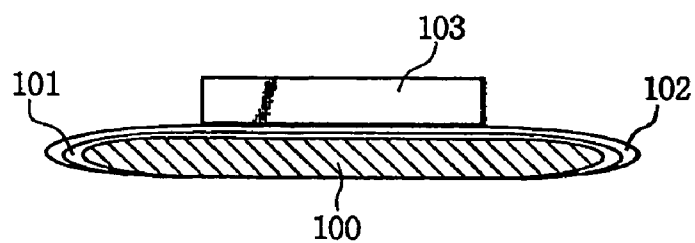


Fig. 7c

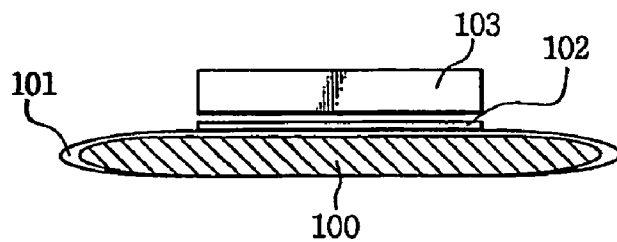


Fig. 7d

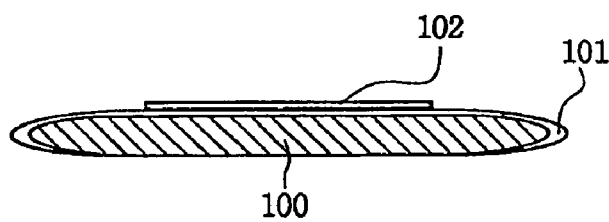
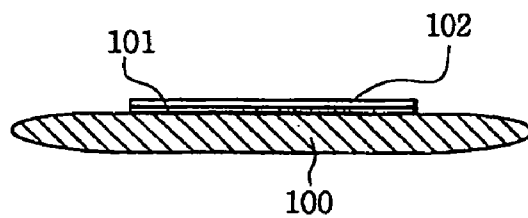


Fig. 7e



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Fig. 8a

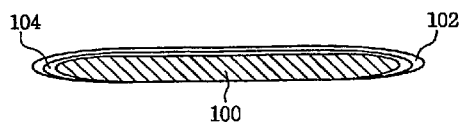


Fig. 8b

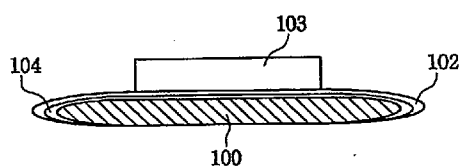
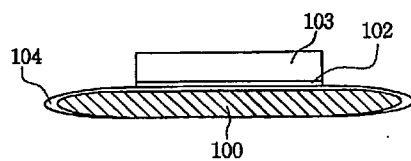


Fig. 8c



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Fig. 8d

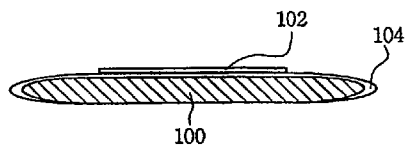


Fig. 8e

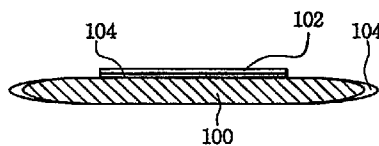
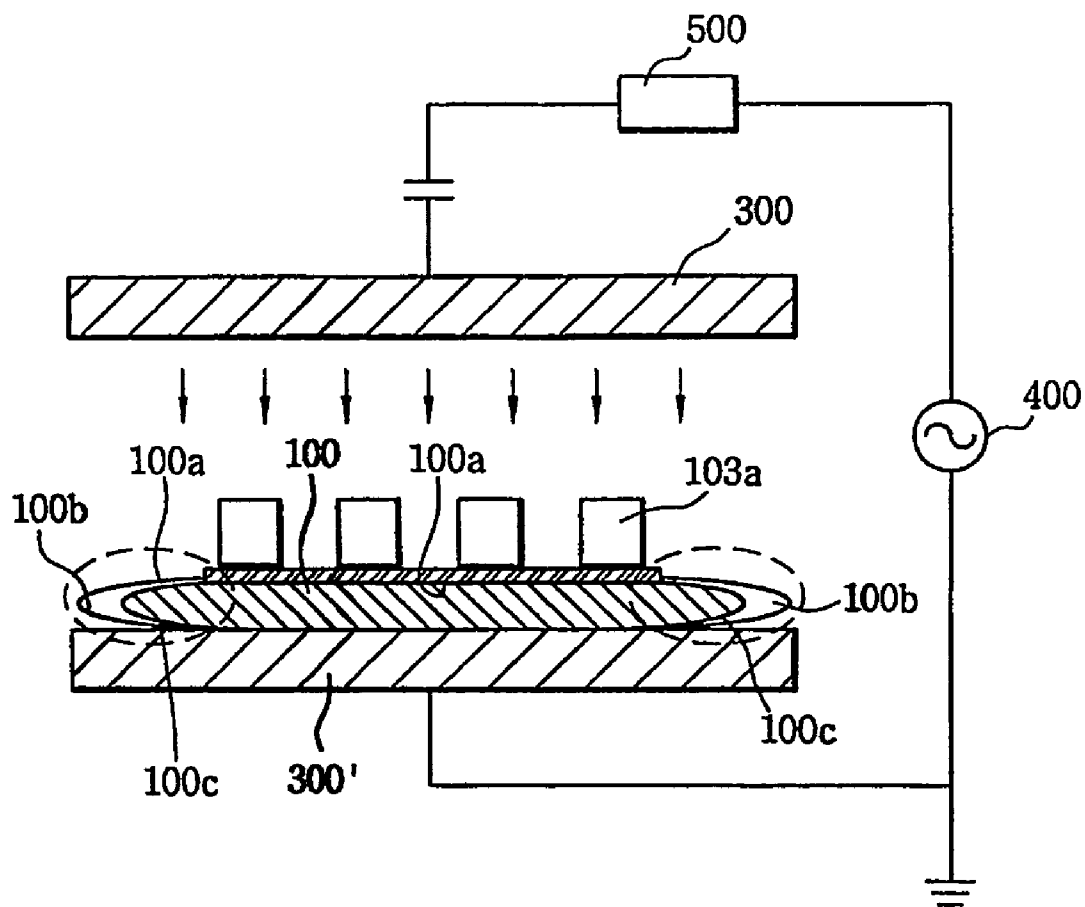


Fig. 9



ELECTRODE FOR DRY ETCHING A WAFER

TECHNICAL FIELD

[0001] The present invention relates to a dry etching of a semiconductor wafer, and more particularly to an electrode for dry etching a semiconductor wafer using plasma, thereby removing foreign material deposited on the edge of the semiconductor wafer for manufacturing integrated circuit chips.

BACKGROUND ART

[0002] As well known to those skilled in the art, during the fabrication of high integrated semiconductor chips, multiple layers **110** and **120** such as a poly-silicon layer, a nitride layer, a metal layer, etc. are deposited and accumulated on the edge of a semiconductor wafer **100**, as shown in **FIG. 5**. Further, as shown in **FIG. 6**, particles broken off the deposited layers on the edge of the semiconductor wafer **100** are generated while transferring the semiconductor wafer **100** or by equipment **200**, and introduced into the central portion of the semiconductor wafer **100**, thereby contaminating the integrated circuit chips.

[0003] Moreover, a gate electrode of a semiconductor chip has been recently changed from tungsten silicide to tungsten, and an insulation layer of a capacitor has been changed from an ONO (oxide-nitride-oxide) structure to tantalum oxide. An organic bottom anti-reflective coating (hereinafter, referred to as ARC) layer and an inorganic ARC layer such as SiON have been recently used to form fine photoresist patterns, and Ti and TiN layers have been used as a barrier metal layer. Therefore, these materials contaminate the semiconductor wafer by the aforementioned route during fabrication.

[0004] That is, these materials act as a particle source during fabrication and contaminate the semiconductor wafer **100**. Particularly, in case that the diameter of the wafer increases from 200 mm to 300 mm, the radius of the edge of the wafer also increases, thereby more increasing the contamination of the semiconductor wafer by the particles.

[0005] Since the materials deposited and accumulated on the edge of the semiconductor wafer **100** reduce the yield and the reliability of the semiconductor chip, these materials need to be fully removed.

[0006] Accordingly, in order to remove the materials deposited and accumulated on the edge of the semiconductor wafer, several methods have been used as follows.

[0007] For example, hereinafter, a wet etching process for removing a nitride layer, which comprises five steps, is described with reference to **FIGS. 7a to 7e**.

[0008] i. An oxide layer **102** is deposited on the nitride layer **101** of the silicon semiconductor wafer **100** by a plasma depositing apparatus (**FIG. 7a**).

[0009] ii. A photoresist layer **103** is formed on the oxide layer **102** by coating photosensitizer, and the photoresist layer **103** on the edge of the semiconductor wafer **100** is removed, thereby exposing the oxide layer **102** of the edge of the semiconductor wafer **100** (**FIG. 7b**).

[0010] iii. The exposed oxide layer **102** of the edge of the semiconductor wafer **100** is removed by a chemical solution ($\text{NH}_4\text{F}+\text{HF}$) using a wet etching device (**FIG. 7c**).

[0011] iv. The photoresist layer **103** on the oxide layer **102** is removed using a dry etching device and residual photoresist **103** is washed by a chemical solution ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) using a washing apparatus (**FIG. 7d**).

[0012] v. The exposed nitride layer **101** of the edge of the semiconductor wafer **100** is removed by a phosphoric acid (H_3PO_4) solution of high temperature using a wet etching device (**FIG. 7e**).

[0013] The above-described wet etching process of the nitride layer is complex. Further, this wet etching process of the nitride layer requires different apparatuses for performing the deposition of the oxide layer, the coating of the photoresist, the removal of the photoresist by dry etching, the removal of the oxide layer by wet etching, the full removal of the residual photoresist, the washing, and the wet etching of the nitride layer.

[0014] On the other hand, a dry etching process for removing the poly-silicon layer, which comprises five steps, is described with reference to **FIGS. 8a to 8e**.

[0015] i. The oxide layer **102** is deposited on the poly-silicon layer **104** on the silicon semiconductor wafer **100** using a plasma depositing apparatus (**FIG. 8a**).

[0016] ii. A photoresist layer **103** is formed on the oxide layer **102** by coating photosensitizer, and the photoresist layer **103** on the edge of the semiconductor wafer **100** is removed, thereby exposing the oxide layer **102** on the edge of the semiconductor wafer **100** (**FIG. 8b**).

[0017] iii. The exposed oxide layer **102** on the edge of the semiconductor wafer **100** is removed by a chemical solution ($\text{NH}_4\text{F}+\text{HF}$) using a wet etching device (**FIG. 8c**).

[0018] iv. The photoresist layer **103** on the oxide layer **102** is removed using a dry etching device and residual photoresist **103** is washed by a chemical solution ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) using a washing apparatus (**FIG. 8d**).

[0019] v. The exposed poly-silicon layer **104** of the edge of the semiconductor wafer **100** is removed using the conventional dry etching device (**FIG. 8e**).

[0020] Identically with the aforementioned wet etching of the nitride layer, the above-described dry etching process of the poly-silicon layer is complex. Further, this dry etching process of the poly-silicon layer requires different apparatuses for performing the deposition of the oxide layer, the coating of the photoresist, the removal of the photoresist by dry etching, the removal of the oxide layer by wet etching, the washing, and the dry etching of the poly-silicon layer.

[0021] When the poly-silicon layer of the edge of the semiconductor wafer is removed using the conventional dry etching apparatus, the poly-silicon layer on the upper surface of the edge of the semiconductor wafer can be removed but the poly-silicon layer on the lower and the side surfaces of the edge of the semiconductor wafer cannot be fully removed, or can only be imperfectly removed.

[0022] Further, since different conventional etching apparatuses are respectively used in each step for forming patterns on the semiconductor wafer, that is, since one etching apparatus is used only to remove one foreign material, it is impossible to use one etching apparatus to remove various materials.

[0023] As shown in FIG. 9, the conventional dry etching device used for forming fine circuit patterns of the semiconductor chip forms an electric field between a flat-shaped first electrode 300 and a flat-shaped second electrode 300' in a reactive gas atmosphere, and generates plasma into the upper surface of the semiconductor wafer 100, thereby etching a deposited layer on the upper surface 100a of the semiconductor wafer 100 and forming a fine pattern 103a. Herein, the deposited layer on the edge of the semiconductor wafer 100 is removed. Reference number 400 denotes an RF (radio frequency) generator and reference number 500 denotes a matching network.

[0024] In the conventional dry etching device, the semiconductor wafer 100 is mounted on one electrode 300' and etched, thereby not etching the side surface 100b and the lower surface 100c of the semiconductor wafer 100. Therefore, the deposited layer on the side surface 100b and the lower surface 100c of the semiconductor wafer cannot be removed.

DISCLOSURE OF THE INVENTION

[0025] Therefore, the present invention has been made in view of the above problems, and it is an object of the present invention to provide an electrode for dry etching a semiconductor wafer using plasma, which can effectively remove foreign materials deposited on the lower and the sides surfaces as well as the upper surface of the edge of the semiconductor wafer without causing damage to the wafer.

[0026] In accordance with the present invention, the above and other objects can be accomplished by the provision of an electrode for dry etching a semiconductor wafer. The electrode comprises a first electrode and a second electrode for removing foreign materials from the edge of the semiconductor wafer using plasma. The first electrode includes a first flat plate and a ring-shaped first protrusion corresponding to one surface of the edge of a semiconductor wafer, and the second electrode includes a second flat plate and a ring-shaped second protrusion corresponding to the other surface of the edge of the semiconductor wafer. Herein, the first protrusion and the second protrusion are the same size.

[0027] Preferably, an insulation layer may be deposited on or an insulating material may be attached to an inner area of the upper surface of the first electrode, which is inside of the first protrusion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0029] FIG. 1 is a partial cross-sectional view of an electrode for dry etching a semiconductor wafer in accordance with the present invention;

[0030] FIG. 2 is a schematic view illustrating the etching of the upper and the side surfaces of a semiconductor wafer using the electrode of the present invention;

[0031] FIG. 3 is a schematic view illustrating the etching of the lower and the side surfaces of the semiconductor wafer using the electrode of the present invention;

[0032] FIG. 4 is a cross-sectional view of a dry etching device provided with the electrode of the present invention;

[0033] FIG. 5 is a side view of semiconductor wafer, on which multiple layers are deposited;

[0034] FIG. 6 is a schematic view illustrating the attachment of foreign materials on the semiconductor wafer by equipment.

[0035] FIGS. 7a to 7e are cross-sectional views illustrating a process for removing a nitride layer using a conventional wet etching;

[0036] FIGS. 8a to 8e are cross-sectional views illustrating a process for removing a poly-silicon layer using a conventional dry etching; and

[0037] FIG. 9 is a schematic view illustrating the etching of a semiconductor wafer using a conventional electrode.

BEST MODE FOR CARRYING OUT THE INVENTION

[0038] FIG. 1 is a partial cross-sectional view of an electrode for dry etching a semiconductor wafer in accordance with the present invention. The electrode of the present invention comprises a pair of electrodes, i.e., a first electrode 10 and a second electrode 20. The first electrode 10 and the second electrode 20 are means for generating plasma for removing foreign materials deposited and accumulated on the edge of the semiconductor wafer.

[0039] Herein, the first electrode 10 is used as an anode and the second electrode 20 is used as a cathode. However, the first electrode 10 may be used as a cathode and the second electrode 20 may be used as an anode.

[0040] The same as the conventional electrode, the first electrode 10 is shaped as a flat circle. A ring-shaped first protrusion 10a is formed on the bottom surface of the first electrode 10. A gas inlet hole 10b is formed between the first protrusion 10a and the circumference of the first electrode 10. The gas inlet hole 10b serves to introduce a reactive gas for generating plasma into a vacuum chamber (not shown), in which the first electrode 10 and the second electrode 20 are formed.

[0041] The second electrode 20 is also shaped as a flat circle having the same diameter of that of the first electrode 10. An opening 20a is formed on the center of the second electrode 20 and a ring-shaped second protrusion 20b having the same dimension as that of the first protrusion 10a is formed between the opening 20a and the circumference of the second electrode 20.

[0042] A flat portion of the outside of the first protrusion 10a of the first electrode 10 and a flat portion of the outside of the second protrusion 20b of the second electrode 20 are referred to as a first flat portion 10c and a second flat portion 20c.

[0043] An insulation layer or an insulator 11 is deposited on or attached to an inner area of the bottom surface of the first protrusion 10a. The attached insulating material 11 serves to prevent an electric field or an electromagnetic field from being formed between the first electrode 10 and the second electrode 20, when a RF power is supplied between

the first electrode **10** and the second electrode **20**. Polyimide, Teflon, silicon, quartz, or ceramic may be used as the insulator **11**.

[0044] FIGS. 2 and 3 illustrate the etching of a semiconductor wafer using the electrode of the present invention. Hereinafter, with reference to FIGS. 2 and 3, an interaction between the first and the second electrodes **10**, **20** of the present invention and the semiconductor wafer **30** is described.

[0045] As shown in FIG. 2, the semiconductor wafer **30** is interposed between the first electrode **10** as the anode and the second electrode **20** as the cathode by an electrostatic chuck **40**. The electrostatic chuck **40** is installed at a lowering position via the opening **20a** of the second electrode **20**, thereby bringing the lower surface **30c** of the edge of the semiconductor wafer **30** into contact with the upper surface of the second protrusion **20b** of the second electrode **20**.

[0046] A reactive gas is introduced via the gas inlet hole **10b** of the first electrode **10** and power is supplied from the RF generator **50** to the second electrode **20**, thereby forming an electric field or an electromagnetic field through the first protrusion **10a** and the first flat portion **10c** of the first electrode **10** and the second protrusion **20b** and the second flat portion **20c** of the second electrode **20**. Then, two types of plasma with different intensity are generated by the reactive gas between the first protrusion **10a** and the second protrusion **20b** and between the first flat portion **10c** and the second flat portion **20c**.

[0047] Herein, plasma is formed along width of the first protrusion **10a** and the second protrusion **20b**. The width of the first protrusion **10a** and the second protrusion **20b** corresponds to the width B of the edge of the semiconductor wafer **30** to be etched. Therefore, an area A of the semiconductor wafer **30**, in which fine circuit pattern **31** is formed, is not affected by this plasma. The side surface **30b** of the semiconductor wafer **30** is etched by plasma C formed between the first flat portion **10c** and the second flat portion **20c**.

[0048] Since the lower surface **30c** of the semiconductor wafer **30** is in contact with the upper surface of the second protrusion **20b** of the second electrode **20**, the etching is mainly performed on the upper surface **30a** and the side surface **30b** of the semiconductor wafer **30** by RIB Reactive Ion Etching).

[0049] Further, since the insulating material **11** attached to the inner area of the first electrode **10**, an electric field or an electromagnetic field is not formed in the area A, thereby preventing plasma from being generated on the area A and improving the efficiency of the etching.

[0050] Herein, reference number **60** denotes a matching network.

[0051] As shown in FIG. 3, the electrostatic chuck **40** is elevated via the opening **20a** of the second electrode **20**, thereby bringing the upper surface **30a** of the edge of the semiconductor wafer **30** into contact with the upper surface of the first protrusion **10a** of the first electrode **10**. Then, the reactive gas is introduced via the gas inlet hole **10b** of the first electrode **10** and the power is supplied from the RF generator **50**, thereby generating plasma between the first

protrusion **10a** and the second protrusion **20b**. Herein, the etching is mainly performed on the lower surface **30c** and the side surface **30b** of the semiconductor wafer **30** by plasma, thereby removing the foreign materials deposited on the area B.

[0052] FIG. 4 is a cross-sectional view of a vacuum chamber **70**, in which the electrode of the present invention is installed. The vacuum chamber **70** comprises a blow pipe **71** for introducing a reactive gas for generating plasma into the first electrode **10** and the second electrode **20**, a port **70a** for entering the semiconductor wafer **30**, an outlet **70b** for exhausting the gas after the etching of the semiconductor wafer **30**, and the electrostatic chuck **40** for moving the semiconductor wafer **30** upward and downward.

[0053] The semiconductor wafer **30** is entered into the vacuum chamber **70** via the port **70a** and mounted on the electrostatic chuck **40**. Under a reactive gas atmosphere, the RF generator **50** supplies a voltage via the second electrode **20**. At this time, the upper surface of the central portion of the semiconductor wafer **30** is protected by the insulating material **11** of the first electrode **10**, and plasma is generated between the first protrusion **10a** and the second protrusion **20b** and between the first flat portion **10c** and the second flat portion **20c**. Then, the upper, the lower, and the side surfaces **30a**, **30c**, and **30b** of the edge of the semiconductor wafer **30** are etched through the aforementioned process.

[0054] During the etching process, the same as the conventional case, the foreign materials removed from the semiconductor wafer **30** and the reactive gas are pumped out via the outlet **70b**.

[0055] Hereinafter, Table 1 illustrates the reactive gases used in the dry etching of the edge of the semiconductor wafer using the electrode of the present invention and the foreign materials removed using the corresponding reactive gas.

TABLE 1

Material	Reactive Gas
Organic ARC (SiON)	CF ₄ , SF ₆
Inorganic ARC (C _x Si _y)	CF ₄ , O ₂
Oxide layer (SiO ₂)	CF ₄ , CHF ₃ , C ₄ F ₈ , C ₂ F ₆ , Ar, O ₂ , CH ₂ F ₂
Nitride layer (Si ₃ N ₄)	CF ₄ , SF ₆ , CHF ₃ , Ar, O ₂
Poly-silicon (Si)	HBr, Cl ₂ , CCl ₄ , SF ₆ , O ₂
Tungsten silicide (WSi _x)	SF ₆ , Cl ₂
Tungsten (W)	SF ₆ , CF ₄ , Ar, O ₂
Aluminum (Al)	Cl ₂ , CCl ₄ , BCl ₃
Copper (Cu)	Cl ₂
Tantalum oxide (TaO ₂)	SF ₆ , Cl ₂ , CF ₄
Tantalum (TaON)	SF ₆ , Cl ₂ , CF ₄
Titanium (Ti)	CF ₄ , SF ₆
Titanium silicide (TiSi _x)	SF ₆ , CF ₄ , O ₂
SOG, [R _x SiO _y SiO ₂] _n , H(SiO _{3/2}) _n	SF ₆ , CF ₄ , O ₂

[0056] As described above, the conventional etching device has been used to remove only one type of materials, i.e., a wet etching device for removing the nitride layer or a dry etching device for forming a fine circuit pattern on a semiconductor wafer. Therefore, the process for etching the semiconductor wafer is very complex and each step of the process requires a corresponding etching device.

[0057] Further, with the structure of the electrode of the conventional etching device, foreign materials deposited on

the upper surface and the side surface of the edge of the semiconductor wafer can be removed. However, foreign materials deposited on the lower surface of the edge of the semiconductor wafer cannot be removed.

[0058] However, the electrode of the present invention is used to remove all foreign materials shown in Table 1 by sequentially supplying appropriate reactive gases corresponding to each material without additional equipment, thereby simplifying the whole process.

[0059] Moreover, portions other than the upper, the side and the lower surfaces of the edge of the semiconductor wafer are not affected by plasma, thereby effectively etching the edge of the semiconductor wafer and not damaging the fine circuit pattern formed on the center of the semiconductor wafer.

[0060] Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

INDUSTRIAL APPLICABILITY

[0061] As apparent from the above description, the present invention provides a an electrode for dry etching a semi-

conductor wafer, which removes foreign materials deposited on the upper, the side and the lower surfaces of the edge of the semiconductor wafer, without additional equipment or step, thereby simplifying the whole process, reducing the process cost, and improving the yield, the quality of the semiconductor wafer, and its productivity.

1. An electrode for dry etching a wafer, said electrode comprising a first electrode and a second electrode for removing foreign materials from the edge of the wafer by plasma, said first electrode including a first flat plate and a ring-shaped first protrusion corresponding to one surface of the edge of a wafer, and said second electrode including a second flat plate and a ring-shaped second protrusion corresponding to the other surface of the edge of the wafer, wherein said first protrusion and said second protrusion are the same size.

2. The electrode for dry etching a wafer as set forth in claim 1, wherein an insulation layer is deposited on or an insulating material is attached to an inner area of the upper surface of the first electrode, which is inside of the first protrusion.

* * * * *