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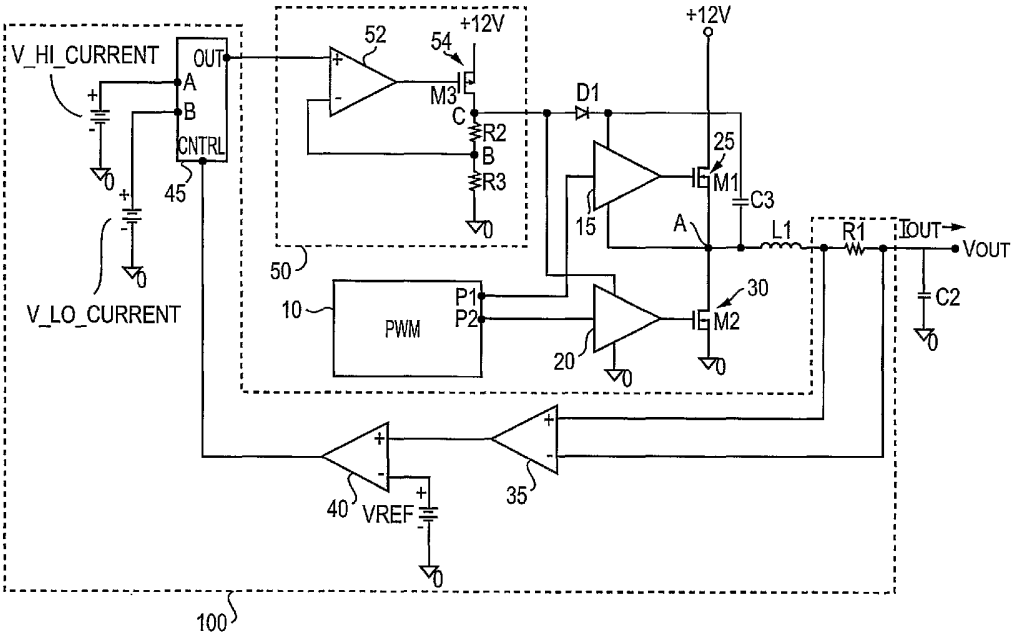
(54) **Title:** ADAPTIVE GATE DRIVE VOLTAGE CIRCUIT



(57) **Abstract:** A circuit and method for reducing losses in a DC/DC converter by optimizing gate drive voltage. The circuit and method detect a change in the output load, or more specifically the output current, and adjust the gate voltage accordingly; in other words, providing adaptive gate drive voltage. In response to a reduction of output current, the invention reduces the gate voltage so as to reduce both conduction and switching losses in the semiconductor switching devices in the output stage.

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ADAPTIVE GATE DRIVE VOLTAGE CIRCUIT

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present application is based upon and claims priority of U.S. Provisional Application Serial No. 60/603,814 filed August 23, 2004, incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a DC/DC converter, and more particularly to a DC/DC converter including a circuit for driving the gates in the output stage adaptively as a function of output current.

Related Art

[0003] DC/DC converter designs today are supporting very high output currents of greater than 100A. A key challenge at this power level is to reduce power loss to keep system efficiency as high as possible, given other system constraints such as board area, cost, etc. One technique that has been used to improve efficiency in these systems is to adjust the gate drive voltage to minimize the combination of switching loss and conduction loss in the converter.

[0004] A known DC/DC power output stage is shown schematically in Fig. 1. As seen, the output stage comprises a pair of power MOSFETs designated CTRL FET and SYNC FET connected in a totem-pole configuration with the source of CTRL FET and the drain of SYNC FET connected together at a node "A". The drain of CTRL FET is connected to a high voltage supply and the source of SYNC FET is grounded. The CTRL FET is driven with a voltage V_{GATE} and a current I_{GATE} and supplies an output current I_{OUT} at a voltage V_{OUT}. Filter elements L_{OUT} and C_{OUT} are also shown.

[0005] In this circuit, the switching loss, the gate drive loss, and the conduction loss in CTRL FET are given by the following expressions:

(1) Switching loss = $V_{GATE} \bullet I_{OUT} \bullet F_{SWX} \bullet \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$

(2) Gate drive loss = $V_{GATE} \bullet Qg \bullet F_{SWX}$

(3) Conduction loss = $I^2_{OUT} \bullet R_{DSON}$

wherein:

F_{SWX} = switching frequency,

Qg = total charge,

Q_{GS} = gate-source charge,

Q_{GD} = gate-drain charge, and

R_{DSON} is a function of V_{GATE}.

[0006] Conduction losses can be reduced by increasing the gate drive voltage, albeit with diminishing returns.

[0007] Fig. 2 is a graph showing total power loss vs. gate drive voltage at 120A load in a typical converter. As seen, the converter has an optimal gate drive voltage for this current level, where the total power loss reaches a minimum.

[0008] However, this known technique of tuning the gate drive voltage to minimize power loss only works well at one load current and is typically set at the maximum output load. In applications where the load current can drop to a very low percentage of full load current, the conduction power loss also decreases rapidly, but the switching power loss still burdens the converter, effectively reducing the overall system efficiency in this lighter load condition. Effectively, the optimal gate drive voltage level which minimizes power loss has changed due to the decreased load current.

SUMMARY OF THE INVENTION

[0009] The present invention provides a practical circuit and method that make it possible to reduce losses by optimizing gate drive voltage.

[0010] More specifically, the circuit and method detect a change in the output load, or more specifically the output current, and adjusts the gate voltage accordingly; in other words, providing adaptive gate drive voltage. In response to a reduction of output current, the invention reduces the gate voltage so as to reduce gate drive, conduction and switching losses in the semiconductor switching devices in the output stage.

[0011] The circuitry can be added to a standard DC/DC converter system, for example, to adaptively adjust gate drive voltage. The conventional circuitry includes a PWM control IC, gate drivers, power MOSFETs, output filter, and a linear regulator to provide the gate drive voltage. The invention, in addition, senses output current information and uses that information to adjust the gate drive voltage.

[0012] The invention thereby provides several advantages. For example, efficiency is improved at light loads while maintaining switching frequency, preventing unwanted noise due to hysteretic mode behavior. Also, an optimized gate drive voltage can be automatically generated for all output current conditions, effectively reducing power loss.

[0013] Other features and advantages of the present invention will become apparent from the following description of embodiments of invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a schematic diagram of a conventional DC/DC converter output stage;

[0015] Fig. 2 is a graph showing total power loss vs. gate drive voltage in typical DC/DC converters; and

[0016] Fig. 3 is a schematic diagram of a DC/DC converter according to an embodiment of the invention.

[0017] Fig. 4 is a schematic diagram of a DC/DC converter according to a second embodiment of the invention.

[0018] Fig. 5 is a schematic diagram of a DC/DC converter according to a third embodiment of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0019] A DC/DC converter having an adaptive gate drive voltage circuit 100 is shown in Figure 3. The converter comprises a PWM controller 10 with outputs P1, P2 for controlling the high side gate driver 15 and the low side gate driver 20. The driver 15 drives an N-channel power MOSFET M1 (25) and the driver 20 drives a N-channel power MOSFET M2 (30). The MOSFETs M1 and M2 are connected in a totem-pole arrangement, delivering the output of the converter at a node A therebetween. Also shown are a bootstrap diode D1, a bootstrap capacitor C3, a filtering inductor L1, and a filtering capacitor C2.

[0020] The foregoing components and their operation are conventional and will be well known to those conversant with this art.

[0021] The output current from the node A is sensed in this example by a sense resistor R1 in series with the output inductor. The voltage developed across this resistor is sensed by an amplifier 35. The output of this amplifier is a voltage proportional to the output current.

[0022] Those having skill in this art will know of other current sensing and feedback techniques, besides those just described, that may be used with the present invention.

[0023] In the example of Figure 3, the output of the current sense amplifier 35 is compared with a reference voltage V_{REF} by a comparator 40. The reference voltage V_{REF} sets a threshold between a "heavy-load" and a "light-load" condition. If

the output current is a "heavy load", the output of the comparator is high. The comparator gives a low output if the output current is a "light load".

[0024] The output of the voltage comparator 40 is sent to the control pin CNTRL of the 2:1 multiplexer 45, which determines which of two reference voltages is sent to the linear regulator 50. Refer to the table below:

COMPARATOR OUTPUT (CNTRL PIN)	MUX OUTPUT (OUT PIN)
HIGH	V_HI_CURRENT
LOW	V_LO_CURRENT

[0025] The linear regulator 50 comprises an amplifier 52 which drives a p-channel MOSFET M3 (54) to control the current from a 12VDC supply through a voltage divider R2, R3. The amplifier receives at its non-inverting input the selected reference voltage V_HI_CURRENT or V_LO_CURRENT from the multiplexer 45. It receives at its inverting input a feedback signal from a node "B" between R2 and R3. A voltage at a node "C" between M3 and R2 is the selected drive voltage to be supplied to the drivers 15, 20 for driving the MOSFETs M1, M2, respectively.

[0026] The linear regulator thus provides a gate voltage that is a function of the output current. Typically, the gate voltage is in the range of (6.5V - 8V) for high output currents and it is 4V - 5V for "light-load" currents. These voltages give optimal gate drive efficiency for both load conditions.

[0027] There are many ways to sense output current and there are many methods for adjusting a reference or feedback voltage. Although there are two reference voltages in this example, three or more could be used. For example, multiple comparators could be used for sensing multiple current set points. See Fig. 4, in which the feedback voltage from amplifier 35 is compared against three thresholds V_{REF}, V_{REF2} and V_{REF3} by comparators 40, 41 and 42, whose outputs will indicate whether the feedback voltage is above, below or between the three threshold voltages. The outputs from comparators 40, 41 and 42 are provided to inputs of a

multiplexer 46 which is thereby controlled to select one of four control voltages V-ITHRESH1 through V-ITHRESH4, which are representative of the four voltage ranges above, below and between the thresholds V_{REF}, V_{REF2} and V_{REF3}. The selected control voltage is then supplied to the amplifier 52 of the linear regulator 50.

[0028] In another alternative, a linear amplifier 36 having gain-setting components giving the amplifier a predetermined gain characteristic is used to track the output current, rather than the comparators and mulitplexer in Figs. 3 and 4. In the embodiment of Fig. 5, the feedback voltage from the amplifier 36 is added to a reference voltage V_{REF} by a summer 47, and the summed output is then applied directly to the amplifier 52. By these means, the gate drive voltage is reduced in response to a reduction in I_{OUT}, to reduce gate drive and switching losses, or increased when I_{OUT} increases, so as to reduce conduction losses, to reach an optimum drive voltage.

[0029] Thus, although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention is not limited by the specific disclosure herein.

WHAT IS CLAIMED IS:

1. A DC/DC converter comprising:

at least one switching device responsive to a drive signal having a drive voltage level, for receiving DC input power and delivering DC output current to an output circuit of said converter;

a driver for supplying said drive signal to said switching device; and

an adaptive drive voltage circuit which senses said DC output current, and in response thereto, sets said drive voltage level to be supplied by said driver to said switching device.

2. The DC/DC converter of claim 1, wherein said adaptive drive voltage circuit, in response to a reduction of output current, reduces said drive voltage level so as to reduce losses in said switching device.

3. The DC/DC converter of claim 2, wherein said adaptive drive voltage circuit defines at least one current threshold, and selects one of at least two predetermined drive voltage levels, in response to whether said output current is above or below said threshold.

4. The DC/DC converter of claim 2, wherein said adaptive drive voltage circuit defines a first plurality of current thresholds, and selects one of a second plurality of predetermined drive voltage levels in response to whether said output current is above, below or between said first plurality of current thresholds.

5. The DC/DC converter of claim 2, wherein said adaptive drive voltage circuit generates a variable drive voltage level in response to variations in said DC output current.

6. A method of controlling a DC/DC converter, said converter comprising:

at least one switching device responsive to a drive signal having a drive voltage level, for receiving DC input power and delivering DC output current to an output circuit of said converter; and a driver for supplying said drive signal to said switching device;

said method comprising the steps of:

sensing said DC output current, and

in response thereto, setting said drive voltage level to be supplied by said driver to said switching device.

7. The method of claim 6, wherein said adaptive drive voltage circuit, in response to a reduction of output current, reduces said drive voltage level so as to reduce losses in said switching device.

8. The method of claim 7, wherein said adaptive drive voltage circuit defines at least one current threshold, and selects one of at least two predetermined drive voltage levels, in response to whether said output current is above or below said threshold.

9. The method of claim 7, wherein said adaptive drive voltage circuit defines a first plurality of current thresholds, and selects one of a second plurality of predetermined drive voltage levels in response to whether said output current is above, below or between said first plurality of current thresholds.

10. The method of claim 7, wherein said adaptive drive voltage circuit generates a variable drive voltage level in response to variations in said DC output current.

11. A DC/DC converter comprising:

a pair of semiconductor switching devices for receiving DC input power and delivering DC output current to an output circuit of said converter connected to said pair of semiconductor switching devices;

a pair of drivers, each for supplying a respective gate drive signal to a corresponding gate of one of said switching devices, said gate drive signals having a gate drive voltage level; and

an adaptive drive voltage circuit which senses said DC output current, and in response thereto, sets said gate drive voltage level of said gate drive signals to be supplied by said drivers to said switching devices.

12. The converter of claim 11, wherein said pair of semiconductor switching devices are connected in a totem-pole arrangement and said output circuit is connected to a junction point between said pair of semiconductor switching devices.

13. The converter of claim 11, comprising setting circuitry which responds to a reduction of said output current by reducing said gate drive voltage level, thereby reducing losses in said switching devices.

14. The converter of claim 13, wherein said reduction of said gate drive voltage level results in a reduction of switching losses and gate drive losses.

15. The converter of claim 13, wherein said setting circuitry defines at least one current threshold, and selects one of at least two predetermined gate drive voltage levels, in response to whether said output current is above or below said threshold.

16. The converter of claim 13, wherein said setting circuitry defines a first plurality of current thresholds, and selects one of a second plurality of predetermined

drive voltage levels in response to whether said output current is above, below or between said first plurality of current thresholds.

17. The converter of claim 13, wherein said setting circuitry generates a variable drive voltage level in response to variations in said DC output current.

18. The converter of claim 13, wherein said setting circuitry selects one of at least two reference voltages corresponding to said gate drive voltage level.

19. The converter of claim 18, wherein said setting circuitry comprises a multiplexer responsive to said output current and connected to said at least two reference voltages, and delivers one of said at least two reference voltages for controlling said gate drive voltage level.

20. The converter of claim 19, wherein said multiplexer delivers said reference voltage to a linear regulator, which generates said gate drive voltage level in response thereto.

21. The converter of claim 13, wherein said setting circuitry increases said gate drive voltage level in response to an increase in said output current, thereby reducing conduction losses in said switching devices.

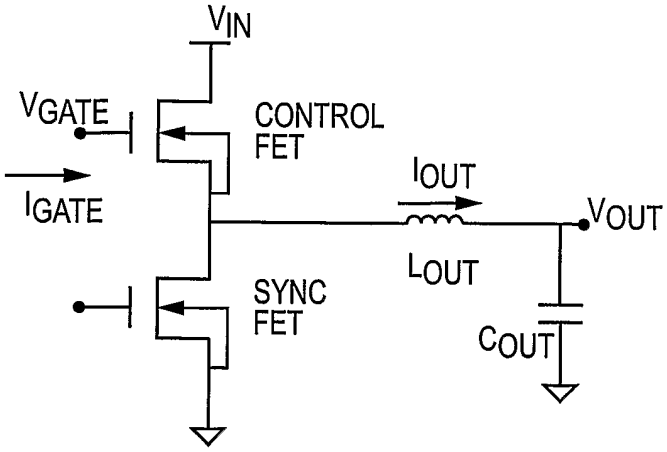


FIG.1
PRIOR ART

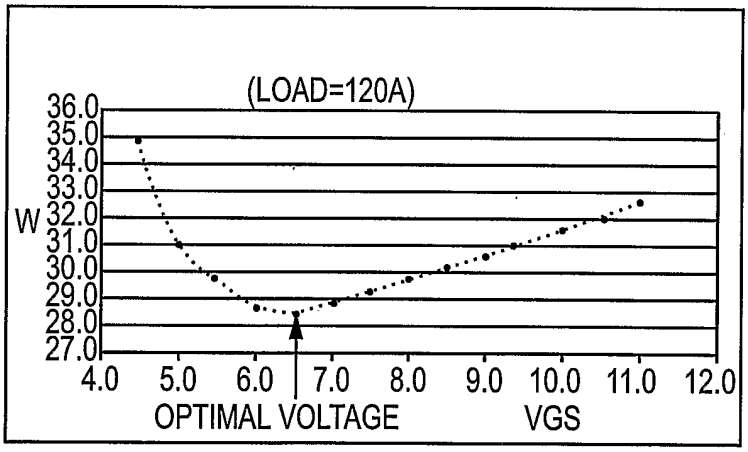


FIG. 2
PRIOR ART

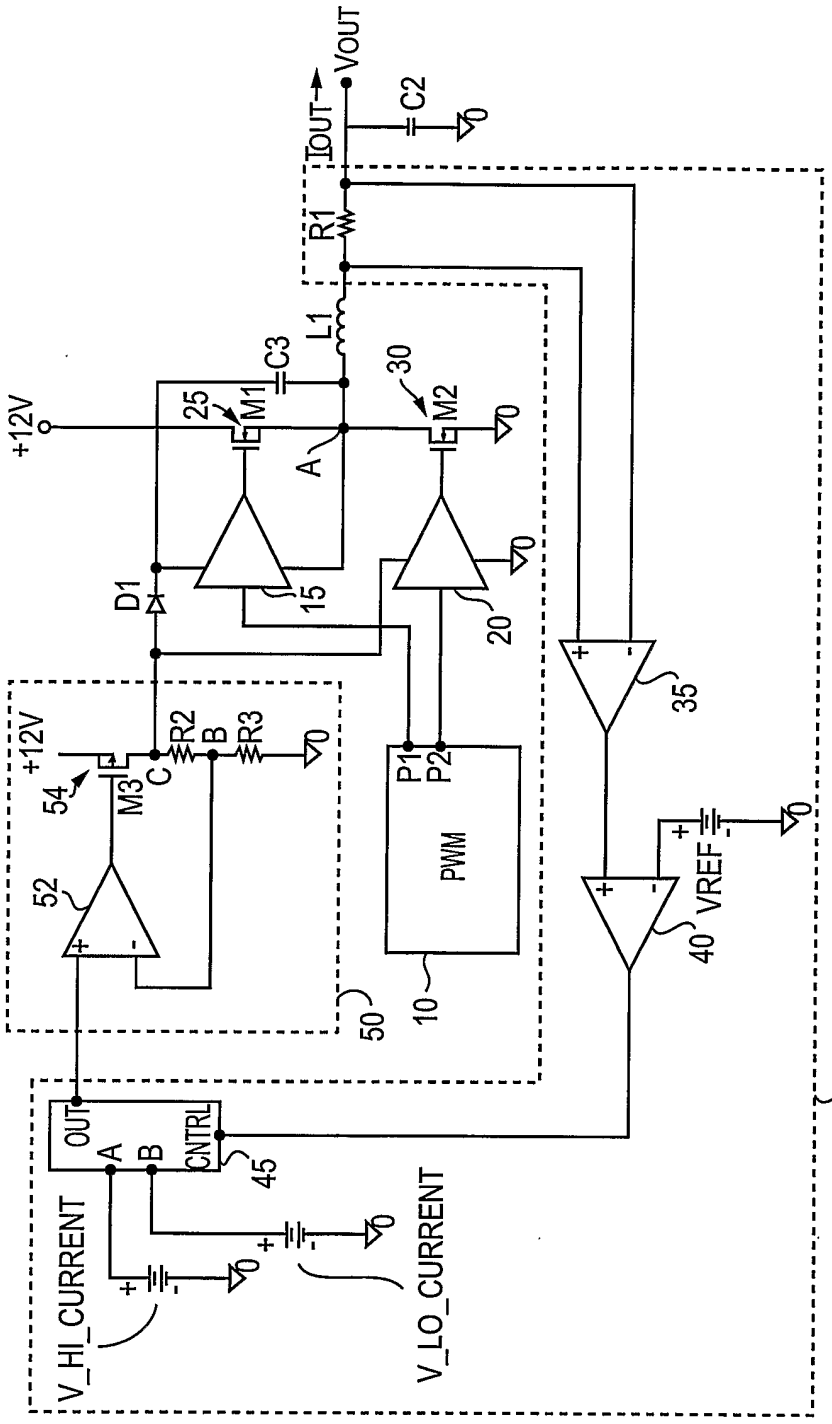
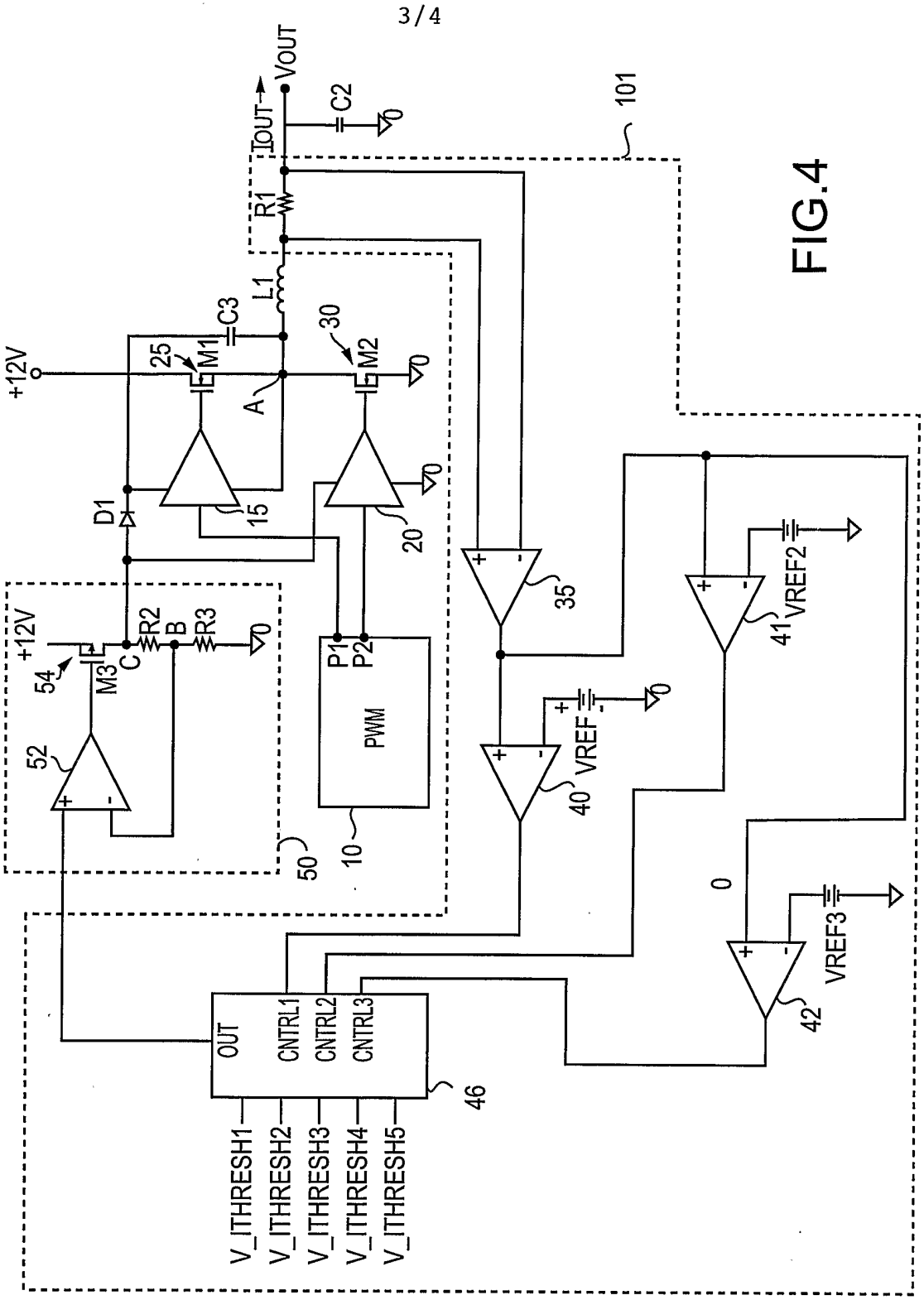

VOUT
IOUT
C2
R1
L1
C3
+12V
25
M1
30
M2
A
D1
15
20
35
+12V
54
M3
C
R2
B
R3
52
P1
P2
PWM
10
50
VREF
40
OUT
A
B
CNTRL
45
V_HI_CURRENT
V_LO_CURRENT
100

FIG.3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IOUT
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R1
L1
C3
M1
M2
25
30
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A
D1
15
20
101
35
41
VREF2
VREF
40
0
VREF3
42
+12V
54
M3
C
R2
B
R3
52
50
10
P1
P2
PWM
OUT
CNTRL1
CNTRL2
CNTRL3
46
V_ITHRESH1
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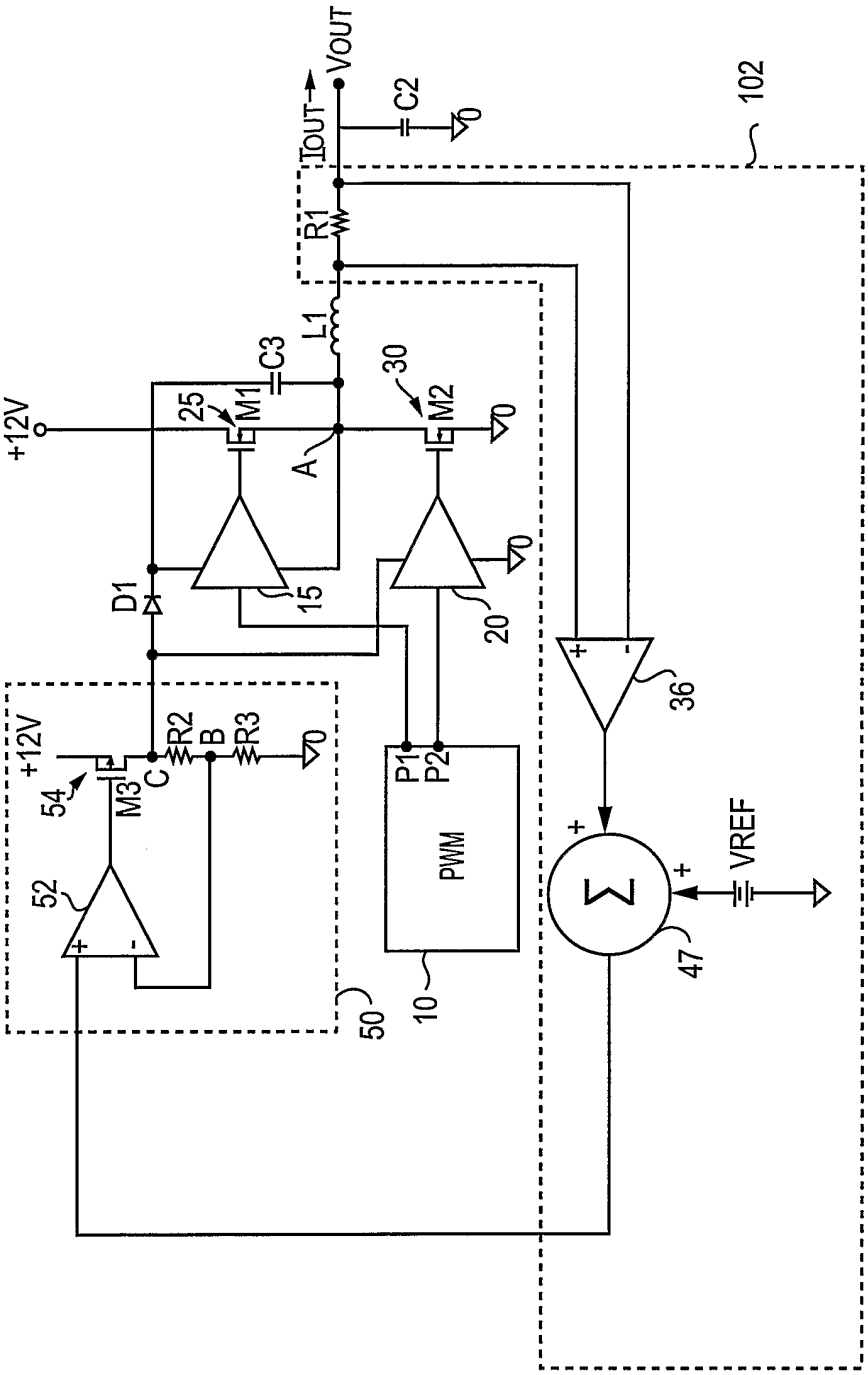
V_ITHRESH3
V_ITHRESH4
V_ITHRESH5

FIG.4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R3
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54
M3
C
P1
P2
PWM
36
52
VREF
47
50
10

FIG.5