

MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))

TRANSISTORS WITH NON-VERTICAL GATES

TECHNICAL FIELD

[0001] This disclosure generally relates to transistors, and more particularly to transistors.

5 BACKGROUND

[0002] Transistors can refer to semiconductor devices used to amplify or switch electronic signals and electrical power. Transistors can be composed of semiconductor material usually with at least three terminals for connection to an external circuit. The metal oxide semiconductor field-effect transistor (MOSFET) can refer to a type of transistor, for example, a type of field-effect transistor (FET). In one embodiment, a MOSFET can have an insulated gate, whose voltage can determine the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals.

BRIEF DESCRIPTION OF THE FIGURES

15 [0003] Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, and wherein:

[0004] FIG. 1 shows a diagram of a transistor having a vertical gate.

[0005] FIG. 2A shows a first diagram of the transistor having a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

20 [0006] FIG. 2B shows a second diagram of a transistor having a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0007] FIG. 2C shows a diagram of an enlarged portion of the transistor having a non-vertical gate of FIG. 2B, in accordance with example embodiments of the disclosure.

25 [0008] FIG. 3A shows a plot of the electric field for a transistor comprising a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0009] FIG. 3B shows a plot of an electrical field for a transistor comprising a vertical gate.

[0010] FIG. 4 shows a plot of the electrical field of transistors having vertical gates and non-vertical gates in accordance with one or more example embodiments of the disclosure.

[0011] FIG. 5 shows a diagram of a partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0012] FIG. 6 shows a diagram of another partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0013] FIG. 7 shows a diagram of another partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0014] FIG. 8 shows a diagram of another partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0015] FIG. 9 shows a diagram of a partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0016] FIG. 10 shows a diagram of another partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0017] FIG. 11 shows a diagram of another partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0018] FIG. 12A shows a diagram of another partial structure of a transistor for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0019] FIG. 12B shows a diagram of an enlarged portion of the transistor of FIG. 12A,
5 in accordance with example embodiments of the disclosure.

[0020] FIG. 13 shows a diagram of an example flowchart that describes the fabrication of transistor having a non-vertical gate, in accordance with example embodiments of the disclosure.

[0021] FIG. 14 shows a diagram of an example system, in accordance with example
10 embodiments of the disclosure.

DETAILED DESCRIPTION

[0022] Embodiments of the disclosure are described more fully hereinafter with reference to the accompanying drawings, in which example embodiments of the disclosure are shown. This disclosure may, however, be embodied in many different forms and
15 should not be construed as limited to the example embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. Like numbers refer to like, but not necessarily the same or identical, elements throughout.

[0023] The following embodiments are described in sufficient detail to enable at least
20 those skilled in the art to understand and use the disclosure. It is to be understood that other embodiments would be evident based on the present disclosure and that process, mechanical, material, dimensional, process equipment, and parametric changes may be made without departing from the scope of the present disclosure.

[0024] In the following description, numerous specific details are given to provide a
25 thorough understanding of various embodiments of the disclosure. However, it will be apparent that the disclosure may be practiced without these specific details. In order to avoid obscuring the present disclosure, some well-known system configurations and process steps may not be disclosed in full detail. Likewise, the drawings showing embodiments of the disclosure are semi-diagrammatic and not to scale and, particularly,

some of the dimensions are for the clarity of presentation and may be exaggerated in the drawings. In addition, where multiple embodiments are disclosed and described as having some features in common, for clarity and ease of illustration, description, and comprehension thereof, similar and like features will ordinarily be described with like
5 reference numerals even if the features are not identical.

[0025] The term “horizontal” as used herein may be defined as a direction parallel to a plane or surface (for example, surface of a substrate), regardless of its orientation. The term “vertical,” as used herein, may refer to a direction orthogonal to the horizontal direction as just described. Terms, such as “on,” “above,” “below,” “bottom,” “top,”
10 “side” (as in “sidewall”), “higher,” “lower,” “upper,” “over,” and “under,” may be referenced with respect to a horizontal plane, where the horizontal plane can include an x-y plane, a x-z plane, or a y-z plane, as the case may be. The term “processing” as used herein includes deposition of material or photoresist, patterning, exposure, development, etching, cleaning, ablating, polishing, and/or removal of the material or photoresist as
15 required in formation a described structure.

[0026] Transistors can refer to semiconductor devices used to amplify or switch electronic signals and electrical power. Transistors can be composed of semiconductor material usually with at least three terminals for connection to an external circuit. The metal oxide semiconductor field-effect transistor (MOSFET) can refer to a type of field-
20 effect transistor (FET). In one embodiment, a MOSFET can have an insulated gate, whose voltage can determine the conductivity of the device. The ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals.

[0027] Transistors (such as MOSFETs) may have a vertical gates, which can mean
25 that the gate of the transistor can have portions having corners that are approximately 90°. Due to such sharp corners at the gate edge and/or corner (about 90°), the electric field can be relatively strong and concentrated at the gate edge and/or corner (as compared with other regions of the gate and/or transistor), potentially leading to large tunneling leakage current in the device. In one embodiment, in order to reduce the electric field at the gate
30 edge and/or portions having corners of a transistor, (for example, a MOSFET device), a non-vertical gate comprising a curved or wide angle gate can be formed. Compared to

transistors (for example, MOSFETs) having vertical gates, transistors having a non-vertical gate including a curved or wide angle gate can have a smoother spatial distribution of the electric field and a reduction of the electric field at the drain side of the gate edge.

[0028] Further, in Transistors (such as MOSFETs) having a vertical gate, electric field crowding on the drain side of the gate edge and/or corner can cause large band to band tunneling (BTBT) leakage and/or gate-induced drain leakage (GIDL) parasitics, reducing device performance. GIDL can be caused by high field effect in the drain junction of MOS transistors. For example, in an NMOS transistor, when the gate is biased at zero or negative voltage and the drain are biased at the supply voltage level, there can be an increase of effects like avalanche multiplication and band-to-band tunneling. Minority carriers underneath the gate can be swept to the substrate, completing the GIDL path.

[0029] In one embodiment, using the non-vertical gates having a curved or wide angle gate can reduce the electric field crowding on the drain side of the gate edge and/or corner and thereby reduce these above mentioned leakage currents. In one embodiment, the non-vertical gate can be generated by one or more etching steps (for example, isotropic etching steps) of an underlying channel during the fabrication of a transistor having the non-vertical gate. In one embodiment, the non-vertical gate can be generated by one or more directional etching steps that may expose various crystallographic facets having predetermined orientations of a source and/or drain associated with the transistor. For example, the orientation of a crystallographic facet of the source and/or drain can have Miller indices of (111). In one embodiment, the source or the drain of the transistor can include an n-doped InGaAs material. In another embodiment, the channel of the transistor comprises an InGaAs material.

[0030] In one embodiment, the disclosure can be used in connection with InGaAs or GaN high-electron-mobility transistor (HEMT) technology. In another embodiment, the disclosure can be used in connection with dynamic random-access memory (DRAM) structures. In one embodiment, the disclosure can be used in connection with logic transistors. In another embodiment, the disclosure can be used in connection with Ge/InGaAs alternative channels, for example, because high mobility channels may have smaller band gap energies.

[0031] FIG. 1 shows a diagram of a transistor 100 having a vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the transistor 100 can include a substrate 102. In another embodiment, the substrate can include a silicon substrate. In one embodiment, the substrate 102 can refer to a solid
5 (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 102 can include a silicon substrate. In one embodiment, the substrate 102 can include a p-doped silicon substrate. In one embodiment, the substrate 102 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and
10 germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 102 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0032] In one embodiment, the transistor 100 can include a buffer layer 104. In one
15 embodiment, the buffer layer 104 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 104 can include a shallow trench isolation (STI) layer. In one embodiment, the buffer layer 104 can include portion, such as portion, that may be proximate to a trench (not fully shown but represented by phantom lines 113), which can be formed in the buffer layer 104. In one
20 embodiment, the STI layer can provide field isolation regions that isolate one channel and/or fin from other channels and/or fins (not shown), for example, other channels and/or fins on adjacent device(s). In one embodiment, the buffer layer 104 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 104 can include an interlayer dielectric (ILD), such as silicon dioxide. In
25 one embodiment, the buffer layer 104 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 104 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the
30 thickness of the buffer layer 104 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 104 can be deposited using physical vapor deposition

(PVD), chemical vapor deposition (CVD), molecular beam epitaxy (MBE), metal organic chemical vapor deposition (MOCVD), and/or atomic layer deposition (ALD), and the like.

[0033] In an embodiment, the transistor 100 can include a source 106. In another embodiment, the source 106 can include an n doped Indian Gallium Arsenide layer. In one
5 embodiment, the source 106 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 106 can be fabricated using MBE. In another embodiment, the source 106 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 106 can include
10 silicon, germanium, indium gallium arsenide (InGaAs), silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can
15 include generating electron vacancies in the source 106. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 106 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 106 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another
20 embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 106 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 106 can be approximately 1 nanometer to approximately 100 nm thick (y dimension), with example thicknesses of approximately 10 nm to approximately 50 nm thick (y dimension). In one embodiment,
25 the source 106 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0034] In one embodiment, the transistor 100 can include a drain 107. In another embodiment, the drain can include an N doped Indian Gallium Arsenide material. In one embodiment, the drain 107 can be deposited using a mask. In one embodiment, the drain
30 107 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 107 can be fabricated using MBE. In another embodiment, the drain 107 can include can include doped or undoped black phosphorous, titanium,

tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 107. In one embodiment, the drain 107 can include silicon, germanium, indium gallium arsenide (InGaAs), silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain can include gettering materials. In one embodiment, the gettering materials can getter sulfur.

10 In one embodiment, the drain can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 107 can have a thickness of approximately 1 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 10 nm to approximately 50 nm (in the x or y dimensions). In one embodiment, the drain 107 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0035] In one embodiment, the transistor 100 can include a source contact 108. In one embodiment, the source contact 108 can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The source contact 108 can include any alloys of such materials. In one embodiment, the source contact 108 can have a thickness of approximately 2 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the source contact

20 25 108 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0036] In another embodiment, the transistor 100 can include a drain contract 110. In one embodiment, the drain contact 110 can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The drain contact 110 can include any alloys of such materials. In one embodiment, the drain contract 110 can have a thickness of approximately 2 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 5 nm to approximately 20

30

nm (in the x or y dimensions). In one embodiment, the drain contact 110 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0037] In one embodiment, the transistor 100 can include a channel 112. In another embodiment, the channel 112 can include an Indian Gallium Arsenide material. In one embodiment, the device can further include a channel 112. In one embodiment, the channel 112 can include silicon. In another embodiment, the channel 112 can include intrinsic silicon. In one embodiment, the channel 112 can be deposited using MBE. In another embodiment, the channel 112 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 112 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 112 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 112 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0038] In one embodiment, the transistor 100 can include a gate 114, for example, a vertical gate 114, which can mean that the gate of the transistor can have portions having corners that are approximately 90°. Due to the sharp corner at the gate edge and/or corner (about 90°), the electric field can be strong and concentrated at the gate edge and/or corner, potentially leading to large tunneling leakage current in the device. In another embodiment, the gate 114 can include a metal. In another embodiment, the gate 114 can include a transition metal. In one embodiment, the gate 114 can be used to tune the threshold voltage of the device. In one embodiment, gate 114 can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the gate 114 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the gate 114 can have a width of approximately 5 nm to approximately 150 nm (x-dimension). In

another embodiment, the gate 114 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0039] In another embodiment, the transistor 100 can include a gate material 116. In one embodiment, the gate material 116 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 116 can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 116. In one embodiment, the gate material 116 can include hydrogenated boron nitride (HBN).
10 In one embodiment, the gate material 116 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 116 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 116 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

15 [0040] In one embodiment, the transistor 100 can include a spacer 118. In another embodiment, spacer 118 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the spacer 118 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like. In one embodiment, the spacer 118
20 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the spacer 118 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0041] FIG. 2A shows a diagram of the transistor 200 having a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment,
25 the transistor 200 can include a wide-angle region 230. In one embodiment, the wide-angle region 230 can be generated by an etching step applied on the channel 212. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet
30 etching process can include, for example, any suitable chemicals for the removal of the portion of the channel 212. In a later step, the gate 214 and the gate material 216 can be

deposited on the channel 212 including the wide-angle region 230, thereby providing a non-vertical gate 214.

[0042] In one embodiment, the transistor 200 can include a substrate 202. In another embodiment, the substrate can include a silicon substrate. In one embodiment, the substrate 202 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 202 can include a silicon substrate. In one embodiment, the substrate 202 can include a p-doped silicon substrate. In one embodiment, the substrate 202 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 202 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0043] In one embodiment, the transistor 200 can include a buffer layer 204, for example, proximate to the substrate 202. In one embodiment, the buffer layer 204 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 204 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 204 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 204 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 204 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene, BCB), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 204 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 204 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 204 can be deposited using PVD, CVD and/or ALD, and the like.

[0044] In an embodiment, the transistor 200 can include a source 206, for example, proximate to the buffer layer 204. In another embodiment, the source 206 can include an n doped Indian Gallium Arsenide layer. In one embodiment, the source 206 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 206 can be fabricated using MBE. In another embodiment, the source 206 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 206 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 206. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 206 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 206 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 206 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 206 can be approximately 1 nanometer to approximately 100 nm thick, with example thicknesses of approximately 10 nm to approximately 50 nm thick. In one embodiment, the source 206 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0045] In one embodiment, the transistor 200 can include a drain 207, for example, proximate to the buffer layer 204. In another embodiment, the drain can include an N doped Indian Gallium Arsenide material. In one embodiment, the drain 207 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 207 can be fabricated using MBE. In another embodiment, the drain 207 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron

vacancies in the drain 207. In one embodiment, the drain 207 can include silicon, germanium, indium gallium arsenide (InGaAs), silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 207 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 207 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0046] In one embodiment, the transistor 200 can include a source contact 208, for example, proximate to the source 206. In one embodiment, the source contact 208 can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The source contact 208 can include any alloys of such materials.

[0047] In another embodiment, the transistor 200 can include a drain contract 210, for example, proximate to the drain 207. In one embodiment, the drain contact 210 can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The drain contact 210 can include any alloys of such materials.

[0048] In one embodiment, the transistor 200 can include a channel 212, for example, proximate to the buffer layer 204, source 206, and/or drain 207. In another embodiment, the channel 212 can include an Indian Gallium Arsenide material. In one embodiment, the device can further include a channel 212. In one embodiment, the channel 206 can include silicon. In another embodiment, the channel 212 can include intrinsic silicon. In one embodiment, the channel 212 can be deposited using MBE. In another embodiment, the

channel 212 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 212 can include silicon, germanium, indium gallium arsenide (InGaAs), silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), gallium nitride (GaN), amorphous
5 semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 212 can be approximately 0.5 nm to approximately 200 nm long
10 (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 212 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

15 **[0049]** In one embodiment, the transistor 200 can include a gate 214, for example, proximate to the source 206 and/or drain 207. In another embodiment, the gate 214 can include a metal. In another embodiment, the gate 214 can include a transition metal. In one embodiment, the gate 214 can be used to tune the threshold voltage of the device. In one embodiment, gate 214 can include titanium nitride, cobalt, tungsten and/or platinum.
20 In one embodiment, the gate 214 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the gate 214 can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the gate 214 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

25 **[0050]** In another embodiment, the transistor 200 can include a gate material 216, for example, proximate to the source 206 and/or drain 207. In one embodiment, the gate material 216 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 216
30 can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 216. In one embodiment, the gate material 216 can include hydrogenated boron nitride (HBN). In one embodiment, the gate

material can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 216 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 216 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

5 [0051] In one embodiment, the transistor 200 can include a spacer 218. In another embodiment, spacer 218 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the oxide can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

10 [0052] FIG. 2B shows a diagram of a transistor 201 having a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0053] In another embodiment, the transistor 201 can include a second wide-angle area 234 for a second gate associated with the transistor 201. In one embodiment, the second wide-angle region 234 can be generated by an etching step applied on the channel
15 212. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the channel 212. In a later step, a second gate 214 and a second gate
20 material 222 can be deposited on the channel 212 including the wide-angle region 234, thereby providing a non-vertical gate 220.

[0054] In one embodiment, the transistor 201 can include a second gate 220, for example, proximate to the buffer layer 204. In another embodiment, the gate 220 can include a metal. In another embodiment, the gate 220 can include a transition metal. In
25 one embodiment, the gate 220 can be used to tune the threshold voltage of the device. In one embodiment, gate 220 can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the gate 220 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the gate 220 can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment,
30 the gate 220 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0055] In one embodiment, the transistor 201 can include a second gate material 222, for example, proximate to the buffer layer 204. In one embodiment, the gate material 222 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 222 can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 222. In one embodiment, the gate material 222 can include hydrogenated boron nitride (HBN). In one embodiment, the gate material can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 222 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 222 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0056] In one embodiment, the transistor 200 can include a wide-angle area 230. In one embodiment, the wide-angle region 230 can be generated by an etching step applied on the channel 212. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the channel 212. In a later step, the gate 214 and the gate material 216 can be deposited on the channel 212 including the wide-angle region 230, thereby providing a non-vertical gate 214.

[0057] In one embodiment, the transistor 200 can include a substrate 202. In another embodiment, the substrate can include a silicon substrate. In one embodiment, the substrate 202 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 202 can include a silicon substrate. In one embodiment, the substrate 202 can include a p-doped silicon substrate. In one embodiment, the substrate 202 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 202 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0058] In one embodiment, the transistor 200 can include a buffer layer 204 for example, proximate to the substrate 202. In one embodiment, the buffer layer 204 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 204 can include a shallow trench isolation (STI) layer.

5 In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 204 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 204 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer

10 204 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 204 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the

15 buffer layer 204 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 204 can be deposited using PVD, CVD and/or ALD, and the like.

[0059] In an embodiment, the transistor 200 can include a source 206, for example, proximate to the buffer layer 204. In another embodiment, the source 206 can include an

20 doped Indian Gallium Arsenide layer. In one embodiment, the source 206 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 206 can be fabricated using MBE. In another embodiment, the source 206 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like.

25 In one embodiment, the source 206 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs,

30 and the like. In one embodiment, the doping can include generating electron vacancies in the source 206. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 206

can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 206 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 206 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 206 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 206 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

10 [0060] In one embodiment, the transistor 200 can include a drain 207, for example, proximate to the buffer layer 204. In another embodiment, the drain can include an N doped Indian Gallium Arsenide material. In one embodiment, the drain 207 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 207 can be fabricated using MBE. In another embodiment, the drain 207 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 207. In one embodiment, the drain 207 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain can include gettering materials. In one embodiment, the gettering materials can getter sulfur.

25 In one embodiment, the drain can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 207 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 207 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source

30

206 and drain 207 can include the same material, except that the source 207 can be treated to remove some of the sulfur and/or selenium.

[0061] In one embodiment, the transistor 200 can include a source contact 208 for example, proximate to the source 206. In one embodiment, the source contact 208 can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The source contact 108 can include any alloys of such materials.

[0062] In another embodiment, the transistor 200 can include a drain contract 210 for example, proximate to the drain 207. In one embodiment, the drain contact 210 can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The drain contact 210 can include any alloys of such materials.

[0063] In one embodiment, the transistor 200 can include a channel 212, for example, proximate to the source 206 and/or drain 207. In another embodiment, the channel 212 can include an Indian Gallium Arsenide material. In one embodiment, the device can further include a channel 212. In one embodiment, the channel 206 can include silicon. In another embodiment, the channel 212 can include intrinsic silicon. In one embodiment, the channel 212 can be deposited using MBE. In another embodiment, the channel 212 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 212 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 212 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 212 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0064] In one embodiment, the transistor 200 can include a gate 214, for example, proximate to the source 206 and/or drain 207. In another embodiment, the gate 214 can include a metal. In another embodiment, the gate 214 can include a transition metal. In one embodiment, the gate 214 can be used to tune the threshold voltage of the device. In one embodiment, gate 214 can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the gate 214 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the gate 214 can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the gate 214 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0065] In another embodiment, the transistor 200 can include a gate material 216, for example, proximate to the source 206 and/or drain 207. In one embodiment, the gate material 216 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 216 can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 216. In one embodiment, the gate material 216 can include hydrogenated boron nitride (HBN). In one embodiment, the gate material can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 216 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 216 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0066] In one embodiment, the transistor 200 can include a spacer 218, for example, proximate to the source 206 and/or drain 207. In another embodiment, spacer 218 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the oxide can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0067] FIG. 2C shows a diagram 203 of an enlarged portion of the transistor having a non-vertical gate of FIG. 2B, in accordance with example embodiments of the disclosure. In one embodiment, FIG. 2C shows a first portion 240 of the gate 214 and/or gate

dielectric 216, a connecting portion 242 of the gate 214 and/or gate dielectric 216, and a second portion 244 of the gate 214 and/or gate dielectric 216. In one embodiment, the first portion 240 of the gate 214 and/or gate dielectric 216 can have at least a portion including one or more planar side walls. Similarly, in another embodiment, the second portion 244
5 of the gate 214 and/or gate dielectric 216 can have at least a portion including one or more planar bottom walls. In one embodiment, the connecting portion 242 can have at least an arcuate and/or curved portion. In one embodiment, the connecting portion 242 can have more than one angle, for example, more than one obtuse angle, such as angle 243. In one embodiment, the more than angle can have an angle of greater than about ninety degrees.
10 In one embodiment, the connecting portion 242 can be generated by an etching process, as described further herein. In one embodiment, the connecting portion 242 can have a radius of curvature that is finite. In one embodiment, the connecting portion 242 can have cross-section having a well-defined derivative at all points along the cross-section of the connecting portion 242. For example, if the connecting portion 242 were to have a sharp
15 corner (with an interior angle of less than or equal to ninety degrees), the derivative may be undefined at least one point along the cross-section of the connecting portion 242. In one embodiment, the channel 212 can have a first portion 246 and/or a second portion 248, where the first portion 246 and/or second portion 248 can mechanically connect to and/or mate with a corresponding section, for example, a first portion of the connecting portions
20 242.

[0068] FIG. 3A shows a contour plot 300 of an electric field for a transistor comprising a non-vertical gate 302, in accordance with one or more example embodiments of the disclosure. In one embodiment, a map of the electric field strength can be represented by the map 303 of the electric field. In one embodiment, the map 303 can
25 have a normalized intensity of between 20 and approximately 134 units. In one embodiment, a gate corner 313 is shown in the plot 300 of the electrical field for a transistor comprising a non-vertical gate 302. The intensity of the electrical field (as represented by the contour plot of the electrical field near the gate corner 313) can have a smaller area of high intensity (for example, an intensity of 11.2 units and above), as
30 compared, for example, to a similar area of the gate corner 315 of the contour plot 301 of an electric field for a transistor comprising a vertical gate 305. In one embodiment, this reduction of the electrical field strength at the gate corner 313 can be due to the reduction

of the angle in the corner 313 for the non-vertical gate corner 313 as compared to the perpendicular angle of the corner 315 of plot 301 of an electric field for a transistor comprising a vertical gate 305.

[0069] FIG. 3B shows a plot 301 of an electrical field for a transistor comprising a vertical gate 305 in accordance with one or more example embodiments of the disclosure. In one embodiment, a map of the electric field strength can be represented by the map 303 of the electric field. In one embodiment, the map 303 can have a normalized intensity of between 20 and approximately 134 units. In one embodiment, the gate corner 315 is shown for the plot 301 of the electrical field for a transistor comprising a non-vertical gate 305. The intensity of the electrical field (as represented by the contour plot of the electrical field near the gate corner 315) can have a larger area of high intensity (for example, an intensity of 11.2 units and above), as compared, for example, to a similar area of the gate corner 313 of the contour plot 300 of an electric field for a transistor comprising a non-vertical gate 302. In one embodiment, this reduction of the electrical field strength at the gate corner 313 can be due to the reduction of the angle in the corner 313 for the non-vertical gate corner 313 as compared to the perpendicular angle of the corner 315 of plot 301 of an electric field for a transistor comprising a vertical gate 305.

[0070] FIG. 4 shows a plot 400 of the electrical field of transistors having vertical gates and non-vertical gates in accordance with one or more example embodiments of the disclosure. In one embodiment, the plot 400 comprises an x-axis 402 that represents the distance in a given dimension, for example, the x dimension of FIG. 1 and/or FIG. 2, in normalized units. In one embodiment, the plot 400 comprises a y-axis 404 that represents the electric field strength, in normalized units. In one embodiment, the plot 400 can represent a comparison of the electric field over a horizontal cut line running through the peak electric field locations of the plot 300 of FIG. 3. In another embodiment, the plot 400 shows a curve 408 representing an electrical field strength for a transistor including a vertical gate, for example, as shown and described in connection with FIG. 1. In one embodiment, the plot 400 shows a curve 410 representing the electric field strength for a transistor including a non-vertical gate, as shown and described in connection with FIGS. 2A-2B. In one embodiment, the integral of the curve 408 (representing transistors having a vertical gate) and 410 (representing transistors having a non-vertical gate) can be taken to have an indication of the relative electrical field strength for the transistors having a

vertical gate and a non-vertical gate, respectively. As is shown in FIG. 4, transistors having a non-vertical gate, that is, transistors represented by the curve 410 show a smaller area under the curve and, therefore, a total electric field that is lower than transistors having a vertical gate as is represented by the curve 408. In another embodiment, the transistors represented by the curve 410 have similar peak electric field to the transistors represented by the curve 408, but has a smaller high field regions. In one embodiment, to the first order, the BTBT and/or GIDL current should be proportional to the area of high field regions, so on the transistors represented by the curve 410 can have lower BTBT and/or GIDL current.

10 [0071] FIG. 5 shows a diagram of a partial structure of a transistor 500 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the transistor 500 can include a substrate 502. In one embodiment, the substrate 502 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres.

15 In another embodiment, the substrate 502 can include a silicon substrate. In one embodiment, the substrate 502 can include a p-doped silicon substrate. In one embodiment, the substrate 502 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 502 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

20

[0072] In another embodiment, the transistor 500 can include a buffer layer 504. In one embodiment, the buffer layer 504 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 504 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 504 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 504 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 504 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials,

25

30

and/or spin-on-glass. In one embodiment, the buffer layer 504 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 504 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 504 can be deposited using PVD, CVD and/or ALD, and the like.

[0073] In one embodiment, the transistor 500 can include a source 506. In another embodiment, the source 506 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the source 506 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 506 can be fabricated using MBE. In another embodiment, the source 506 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 506 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 506. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 506 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 506 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 506 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 506 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 506 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0074] In one embodiment, the transistor 500 can include a drain 507. In another embodiment, the drain 507 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the device 500 can include a drain 507. In one embodiment, the drain 208 can be deposited using a mask. In one embodiment, the drain 507 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 507 can be fabricated using MBE. In another embodiment, the drain 507 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 507. In one embodiment, the drain 507 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 507 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 507 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 506 and drain 507 can include the same material, except that the source 507 can be treated to remove some of the sulfur and/or selenium.

[0075] In one embodiment, the transistor 500 can include a channel 508. In another embodiment, the channel 508 can include an Indian Gallium Arsenide material. In one embodiment, the channel 508 can include silicon. In another embodiment, the channel 508 can include intrinsic silicon. In one embodiment, the channel 508 can be deposited using MBE. In another embodiment, the channel 508 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the

channel 508 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 508 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 508 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0076] In an embodiment, the transistor 500 can include a dummy gate 510. In another embodiment, the dummy gate 510 can include a polysilicon material. In one embodiment, the dummy gate 510 can serve as a temporary placeholder for the eventual deposition of a gate and/or gate dielectric, to be further described below.

[0077] In one embodiment, the transistor 500 can include spacer 512. In another embodiment, spacer 512 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the oxide can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0078] FIG. 6 shows a diagram of a partial structure of a transistor 600 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the transistor 600 can include a first recess 614. In another embodiment, the transistor 600 can include a second recess 616.

[0079] In one embodiment, recess 614 and/or 616 that can be generated by the removal of the dummy gate 510 as shown and described in connection with FIG. 5. In one embodiment, the removal of the portion of the dummy gate 510 can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example,

a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the dummy gate 510.

[0080] In one embodiment, the transistor 600 can include a substrate 602. In one embodiment, the substrate 602 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 602 can include a silicon substrate. In one embodiment, the substrate 602 can include a p-doped silicon substrate. In one embodiment, the substrate 602 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 602 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0081] In another embodiment, the transistor 600 can include a buffer layer 604. In one embodiment, the buffer layer 604 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 604 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 604 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 604 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 604 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 604 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 604 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 604 can be deposited using PVD, CVD and/or ALD, and the like.

[0082] In one embodiment, the transistor 600 can include a source 606. In another embodiment, the source 606 can include an N doped Indian Gallium Arsenide layer

material. In one embodiment, the source 606 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 606 can be fabricated using MBE. In another embodiment, the source 606 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 606 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 606. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 606 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 606 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 606 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 606 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 606 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0083] In one embodiment, the transistor 600 can include a drain 607. In another embodiment, the drain 607 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the drain 607 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 607 can be fabricated using MBE. In another embodiment, the drain 607 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 607. In one embodiment, the drain 607 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium

nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain 607 can include gettering materials. In one embodiment, the
5 gettering materials can getter sulfur. In one embodiment, the drain 607 can be doped with oxygen vacancies if the source 606 comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain 607 comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 607 can have a thickness of
10 approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 607 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 606 and drain 607 can include the same material, except that the source 607 can be treated to remove some of the sulfur
15 and/or selenium.

[0084] In one embodiment, the transistor 600 can include a channel 608. In another embodiment, the channel 608 can include an Indian Gallium Arsenide material. In one embodiment, the channel 608 can include silicon. In another embodiment, the channel 608 can include intrinsic silicon. In one embodiment, the channel 608 can be deposited
20 using MBE. In another embodiment, the channel 608 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 608 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO),
25 amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 608 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately
30 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one

embodiment, the channel 608 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0085] In one embodiment, the transistor 600 can include spacer 612. In another embodiment, spacer 612 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the oxide can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0086] FIG. 7 shows a diagram of a partial structure of a transistor 700 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

[0087] In one embodiment, the transistor 700 can include a wide angle region 718 for a top gate or a second gate. In one embodiment, the wide-angle region 718 can be generated by an etching step applied on the channel 708. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the channel 708. In a later step, a gate and the gate material can be deposited on the channel 708 including the wide-angle region 718, thereby providing a non-vertical gate.

[0088] In one embodiment, the transistor 700 can include a second wide angle region 720 for a bottom gate or a second gate. In one embodiment, the second wide-angle region 720 can be generated by an etching step applied on the channel 708. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the channel 708. In a later step, a gate and the gate material can be deposited on the channel 708 including the second wide-angle region 720, thereby providing a non-vertical gate.

[0089] In one embodiment, recess 714 that can be generated by the removal of the dummy gate 510 as shown and described in connection with FIG. 5. In one embodiment, the removal of the portion of the dummy gate 510 can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch.
5 dummy gate 510. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of dummy gate 510. For example, for a dummy gate 510 comprising gallium arsenide, an acid based wet etch may be used.

[0090] In one embodiment, the transistor 700 can include a substrate 702. In one
10 embodiment, the substrate 702 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 702 can include a silicon substrate. In one embodiment, the substrate 702 can include a p-doped silicon substrate. In one embodiment, the substrate 702 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum
15 oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 702 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0091] In another embodiment, the transistor 700 can include a buffer layer 704. In
20 one embodiment, the buffer layer 704 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 704 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 704 can
25 include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 704 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 704 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 704 can include a low
30 permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 704 can be approximately 10 nm to

approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 704 can be deposited using PVD, CVD and/or ALD, and the like.

[0092] In one embodiment, the transistor 700 can include a source 706. In another embodiment, the source 706 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the source 706 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 706 can be fabricated using MBE. In another embodiment, the source 706 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 606 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 706. In one embodiment, the source 706 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 706 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 706 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 706 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 706 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 706 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0093] In one embodiment, the transistor 600 can include a drain 607. In another embodiment, the drain 707 can include an n-doped Indian Gallium Arsenide layer material. In one embodiment, the drain 707 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 707 can be fabricated using MBE. In another embodiment, the drain 707 can include can include

doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 707. In one embodiment, the drain 707 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain 707 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain 707 can be doped with oxygen vacancies if the source 706 comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain 707 comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 707 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 707 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 706 and drain 707 can include the same material, except that the source 707 can be treated to remove some of the sulfur and/or selenium.

[0094] In one embodiment, the transistor 700 can include a channel 708. In another embodiment, the channel 708 can include an Indian Gallium Arsenide material. In one embodiment, the channel 708 can include silicon. In another embodiment, the channel 708 can include intrinsic silicon. In one embodiment, the channel 708 can be deposited using MBE. In another embodiment, the channel 708 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 708 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another

embodiment, the channel 708 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one
5 embodiment, the channel 708 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0095] In one embodiment, the transistor 700 can include spacer 712. In another embodiment, spacer 712 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon
10 dioxide (SiO_2), or a low-K material. In one embodiment, the spacer 712 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0096] FIG. 8 shows a diagram of a partial structure of a transistor 800 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure.

15 [0097] In one embodiment, the transistor 800 can include a gate material 824 for a top gate, that can be deposited into the recesses similar to recesses 614 and 616 having wide angle regions 718 and 720 as shown and described in connection with FIGs. 6 and 7. In one embodiment, the transistor 800 can include a gate material 826 for a bottom gate, that can be deposited into the recesses similar to recesses 614 and 616 having wide angle
20 regions 718 and 720 as shown and described in connection with FIGs. 6 and 7.

[0098] In one embodiment, the gate material 824 and/or 830 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 824 and/or 830 can include silicon
25 oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 824 and/or 830. In one embodiment, the gate material 824 and/or 830 can include hydrogenated boron nitride (HBN). In one embodiment, the gate material 824 and/or 830 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 824 and/or 830 can have a width of 0.5
30 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 824

and/or 830 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0099] In one embodiment, the transistor 800 can include a gate 826 for a top gate that can be deposited into the recesses similar to recesses 614 and 616 having wide angle regions 718 and 720 as shown and described in connection with FIGs. 6 and 7. In one
5 embodiment, the transistor 800 can include a gate 828 for a bottom gate that can be deposited into the recesses similar to recesses 614 and 616 having wide angle regions 718 and 720 as shown and described in connection with FIGs. 6 and 7. In another embodiment, the gate 826 and 828 can include a metal. In another embodiment, the gate 826 and 828
10 can include a transition metal. In one embodiment, the gate 826 and 828 can be used to tune the threshold voltage of the device. In one embodiment, gate 826 and 828 can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the gate 826 and 828 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one
15 embodiment, the gate 826 and 828 can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the gate 826 and 828 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0100] In one embodiment, the transistor 800 can include a source contact 832. In one embodiment, the transistor 800 can include a drain contact 834. In one embodiment, the source contact 832 and/or the drain contact 834 can include a metal. In one embodiment,
20 the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The source contact 832 and/or the drain contact 834 can include any alloys of such materials. In one embodiment, the source contact 832 and/or the drain contact 834 can have a thickness of approximately 2 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 5 nm to approximately 20 nm (in
25 the x or y dimensions). In one embodiment, the source contact 832 and/or the drain contact 834 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0101] In one embodiment, the transistor 800 can include a wide angle region 818 for a top gate or a second gate. In one embodiment, the transistor 800 can include a wide angle region 820 for a bottom gate or a second gate. In one embodiment, the wide-angle region 818 can be generated by an etching step applied on the channel 808. In one
30 embodiment, the etching process can include, for example, a dry etch. In one embodiment,

the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the channel 808. In a later step, a gate and the gate material can be deposited on the channel 808 including the wide-angle region 818, thereby providing a non-vertical gate.

[0102] In one embodiment, the transistor 800 can include a substrate 802. In one embodiment, the substrate 802 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 802 can include a silicon substrate. In one embodiment, the substrate 802 can include a p-doped silicon substrate. In one embodiment, the substrate 802 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 802 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0103] In another embodiment, the transistor 800 can include a buffer layer 804. In one embodiment, the buffer layer 804 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 804 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 804 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 804 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 804 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 804 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 804 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 20 nm to

approximately 100 nm. In one embodiment, the buffer layer 804 can be deposited using PVD, CVD and/or ALD, and the like.

[0104] In one embodiment, the transistor 800 can include a source 806. In another embodiment, the source 806 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the source 806 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 806 can be fabricated using MBE. In another embodiment, the source 806 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 806 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 806. In one embodiment, the source 806 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 806 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 806 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 806 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 806 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 806 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0105] In one embodiment, the transistor 800 can include a drain 807. In another embodiment, the drain 807 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the drain 807 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 807 can be fabricated using MBE. In another embodiment, the drain 807 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium

nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 807. In one embodiment, the drain 807 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain 807 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain 807 can be doped with oxygen vacancies if the source 806 comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain 807 comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 807 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 807 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 806 and drain 807 can include the same material, except that the source 807 can be treated to remove some of the sulfur and/or selenium.

[0106] In one embodiment, the transistor 800 can include a channel 808. In another embodiment, the channel 508 can include an Indian Gallium Arsenide material. In one embodiment, the channel 808 can include silicon. In another embodiment, the channel 808 can include intrinsic silicon. In one embodiment, the channel 808 can be deposited using MBE. In another embodiment, the channel 808 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 808 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 808 can be approximately 0.5 nm to approximately 200 nm long

(in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 808 can be deposited using PVD, CVD, MOCVD, MBE, and/or
5 ALD, and the like.

[0107] In one embodiment, the transistor 800 can include spacer 812. In another embodiment, spacer 812 can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the spacer 812 can be deposited
10 using PVD, CVD, MOCVD, and/or ALD, and the like.

[0108] FIG. 9 shows a diagram of a partial structure of a transistor 900 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the transistor 900 can include a substrate 902. In one embodiment, the substrate 902 can refer to a solid (usually planar) substance onto
15 which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 902 can include a silicon substrate. In one embodiment, the substrate 902 can include a p-doped silicon substrate. In one embodiment, the substrate 902 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or
20 indium phosphide (InP), and the like. In one embodiment, the substrate 902 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0109] In another embodiment, the transistor 900 can include a buffer 904. In one
25 embodiment, the buffer layer 904 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 904 can include a STI layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device.

[0110] In one embodiment, the buffer layer 904 can include an oxide layer (e.g.,
30 silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 904 can include an interlayer dielectric (ILD), such as silicon dioxide. In one

embodiment, the buffer layer 904 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene, BCB), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 904 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k)
5 lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 904 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 904 can be deposited using PVD, CVD and/or ALD, and the like.

[0111] In one embodiment, the transistor 900 can include a source 906. In another
10 embodiment, the source 906 can include an N doped Indian Gallium Arsenide material. In one embodiment, the source 906 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 906 can be fabricated using MBE. In another embodiment, the source 906 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride,
15 hafnium, copper, gadolinium, and the like. In one embodiment, the source 906 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline
20 silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 906. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 906 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 906 can be doped with oxygen
25 vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 906 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 906 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of
30 approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 906 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0112] In one embodiment, the transistor 900 can include a drain 907. In another embodiment, the drain 907 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the drain 907 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 907 can be fabricated using MBE. In another embodiment, the drain 907 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 907. In one embodiment, the drain 907 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain 907 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain can be doped with oxygen vacancies if the source 907 comprises an oxide or a multi-material system. In another embodiment, the source 907 can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 907 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 907 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 906 and drain 907 can include the same material, except that the source 907 can be treated to remove some of the sulfur and/or selenium.

[0113] In one embodiment, the transistor 900 can include a dielectric 908. In another embodiment, dielectric 908 can include an oxide. In another embodiment, the dielectric 908 can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the dielectric 908 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0114] In one embodiment, the transistor 900 can include an angular region 909 in the source 906 and/or the drain 907. In one embodiment, the angular region 909 can be

generated by the removal of a portion of the source 906 and/or the drain 907, which can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the source 906 and/or the drain 907.

[0115] In one embodiment, the transistor can include a channel 910. In another embodiment, the channel 910 can include an Indian Gallium Arsenide material. In one embodiment, the channel 910 can include silicon. In another embodiment, the channel 910 can include intrinsic silicon. In one embodiment, the channel 910 can be deposited using MBE. In another embodiment, the channel 910 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 910 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 910 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 910 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0116] In an embodiment, the transistor 900 can include a dummy gate 912. In another embodiment, the dummy gate 912 can include a polysilicon material. In another embodiment, dummy gate 912 can include an oxide. In another embodiment, the dummy gate 912 can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the dummy gate 912 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like. In one embodiment, the dummy gate 912 can serve as a placeholder for the deposition (at a later step) of a gate and a gate material, to be discussed below.

[0117] FIG. 10 shows a diagram of a partial structure of a transistor 1000 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the transistor 1000 can include a first recess 1014 for the deposition of a top gate in a future step. In another embodiment, the transistor 1000 can include a second recess 1016 for the deposition of a bottom gate. In one embodiment, the first recess 1014 can be generated by the removal of the portion of the dummy gate 912. In one embodiment, the second recess 1016 can be generated by the removal of a portion of the buffer layer 904. In one embodiment, the removal of the portion of the dummy gate 912 or the buffer layer 904 can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the dummy gate 912 or the buffer layer 904.

[0118] In one embodiment, the transistor 1000 can include a substrate 1002. In one embodiment, the substrate 1002 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 1002 can include a silicon substrate. In one embodiment, the substrate 1002 can include a p-doped silicon substrate. In one embodiment, the substrate 1002 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 1002 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0119] In another embodiment, the transistor 1000 can include a buffer 1004. In one embodiment, the buffer layer 1004 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 1004 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 1004 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the

buffer layer 1004 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 1004 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 1004 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer 1004 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 1004 can be deposited using PVD, CVD and/or ALD, and the like.

[0120] In one embodiment, the transistor 1000 can include a source 1006. In another embodiment, the source 1006 can include an N doped Indian Gallium Arsenide material. In one embodiment, the source 1006 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 1006 can be fabricated using MBE. In another embodiment, the source 1006 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 1006 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 1006. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 1006 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 1006 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 1006 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 1006 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm

thick (y dimension). In one embodiment, the source 1006 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0121] In one embodiment, the transistor 1000 can include a drain 1007. In another embodiment, the drain 1007 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the drain 1007 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 1007 can be fabricated using MBE. In another embodiment, the drain 1007 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 1007. In one embodiment, the drain 1007 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain 1007 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source 1006 can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 1007 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 1007 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 1006 and drain 1007 can include the same material, except that the source 1006 can be treated to remove some of the sulfur and/or selenium.

[0122] In one embodiment, the transistor 1000 can include a dielectric 1008. In another embodiment, dielectric 1008 can include an oxide. In another embodiment, the dielectric 1008 can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the dielectric 1008 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0123] In one embodiment, the transistor 1000 can include an angular region 1009 in the source 1006 and/or the drain 1007. In one embodiment, the angular region 1009 can be generated by the removal of a portion of the source 1006 and/or the drain 1007, which can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the source 1006 and/or the drain 1007.

10 [0124] In one embodiment, the transistor can include a channel 1010. In another embodiment, the channel 1010 can include an Indian Gallium Arsenide material. In one embodiment, the channel 1010 can include silicon. In another embodiment, the channel 1010 can include intrinsic silicon. In one embodiment, the channel 1010 can be deposited using MBE. In another embodiment, the channel 1010 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 1010 can include silicon, germanium, indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 1010 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 1010 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0125] FIG. 11 shows a diagram of a partial structure of a transistor 1100 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the transistor 1100 can include a recess 1116 for the top gate that can be similar to the recess 1114 except that it is expanded to expose a portion of the source 1120 and a portion of the drain 1124 that can include a crystallographic facet of the source 1106 and/or the drain 1107.

[0126] In one embodiment, the recess 1116 can be generated by the removal of the portion of the recess 1014. In one embodiment, the removal of the portion of the portion of the recess 1014 can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the recess 1014.

[0127] In one embodiment, the transistor 1100 can include a substrate 1102. In one embodiment, the substrate 1102 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 1102 can include a silicon substrate. In one embodiment, the substrate 1102 can include a p-doped silicon substrate. In one embodiment, the substrate 1102 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 1102 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0128] In another embodiment, the transistor 1100 can include a buffer 1104. In one embodiment, the buffer layer 1104 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 1104 can include a shallow trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 1104 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 1104 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer 1104 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 104 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide. In one embodiment, the

thickness of the buffer layer 1104 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 1104 can be deposited using PVD, CVD and/or ALD, and the like.

5 **[0129]** In one embodiment, the transistor 1100 can include a source 1106. In another embodiment, the source 1106 can include an N doped Indian Gallium Arsenide material. In one embodiment, the source 1106 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 1106 can be fabricated using MBE. In another embodiment, the source 1106 can include doped or
10 undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 1106 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO),
15 amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 1106. In one embodiment, source 1106 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 1106 can be doped,
20 for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 1106 can be doped with oxygen vacancies if the source 1106 comprises an oxide or a multi-material system. In another embodiment, the source 1106 can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 1106 comprises a non-oxide a single-material semiconductor. In another
25 embodiment, the source 1106 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 1106 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

30 **[0130]** In one embodiment, the transistor 1100 can include a drain 1107. In another embodiment, the drain 1107 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the drain 1107 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 1107 can be

fabricated using MBE. In another embodiment, the drain 1107 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 1107. In one
5 embodiment, the drain 1107 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the
10 like. In one embodiment, the drain 1107 can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain 1107 can be doped with oxygen vacancies if the source 1106 comprises an oxide or a multi-material system. In another embodiment, the source 1106 can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain
15 comprises a non-oxide a single-material semiconductor. In one embodiment, the drain 1107 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 1107 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source
20 1106 and drain 1107 can include the same material, except that the source 1106 can be treated to remove some of the sulfur and/or selenium.

[0131] In one embodiment, the transistor 1100 can include a dielectric 1108. In another embodiment, dielectric 1108 can include an oxide. In another embodiment, the dielectric 1108 can include an interlayer dielectric (ILD) material. In another embodiment,
25 ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the dielectric 1108 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0132] In one embodiment, the transistor 1100 can include an angular region 1120 and/or an angular region 1124 in the source 1106 and/or the drain 1107. In one embodiment, the angular region 1120 can be generated by the removal of a portion of the
30 source 1106 and/or the drain 1107, which can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-

based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the source 1106 and/or the drain 1107.

[0133] In one embodiment, the transistor 1100 can include a channel 1110. In another embodiment, the channel 1110 can include an Indian Gallium Arsenide material. In one embodiment, the channel 1106 can include silicon. In another embodiment, the channel 1106 can include intrinsic silicon. In one embodiment, the channel 1106 can be deposited using MBE. In another embodiment, the channel 1106 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 1106 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 1106 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 1106 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0134] FIG. 12 shows a diagram of a partial structure of a transistor 1200 for the fabrication of a non-vertical gate, in accordance with one or more example embodiments of the disclosure. In one embodiment, the diagram 1200 can include a top gate 1228. In another embodiment, the top gate 1228 can include a metal. In another embodiment, the top gate 1228 can include a transition metal. In one embodiment, the top gate 1228 can be used to tune the threshold voltage of the device. In one embodiment, top gate 1228 can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the top gate 1228 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the top gate 1228 can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the top gate 1228 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0135] In one embodiment, the transistor 1200 can include a gate material 1226 for the top gate 1228, for example, proximate to the source 1206 and/or drain 1207. In one embodiment, the gate material 1226 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 1226 can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 1226. In one embodiment, the gate material 1226 can include hydrogenated boron nitride (HBN). In one embodiment, the gate material can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 1226 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 1226 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0136] In another embodiment, the transistor 1200 can include a bottom gate 1232, for example, proximate to the source 1206 and/or drain 1207. In another embodiment, the bottom gate 1232 can include a metal. In another embodiment, the bottom gate 1232 can include a transition metal. In one embodiment, the bottom gate 1232 can be used to tune the threshold voltage of the device. In one embodiment, bottom gate 1232 can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the bottom gate 1232 can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the bottom gate 1232 can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the bottom gate 1232 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0137] In one embodiment, the transistor 1200 can include a gate material 1230 for the bottom gate 1232, for example, proximate to the buffer layer 1204, and/or source 1206 and/or drain 1207. In one embodiment, the gate material 1230 can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material 1230 can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material 1230. In one embodiment, the gate material 1230 can include hydrogenated boron nitride (HBN). In one embodiment, the gate material can be deposited using PVD,

CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material 1230 can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material 1230 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

5 **[0138]** In one embodiment, the transistor 1200 can include a substrate 1202. In one embodiment, the substrate 1202 can refer to a solid (usually planar) substance onto which a layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate 1202 can include a silicon substrate. In one embodiment, the substrate 1202 can include a p-doped silicon substrate. In one
10 embodiment, the substrate 1202 can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like. In one embodiment, the substrate 1202 can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs),
15 or any combination thereof).

[0139] In another embodiment, the transistor 1200 can include a buffer 1204, for example, proximate to the buffer 1204. In one embodiment, the buffer layer 1204 can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer 1204 can include a shallow trench isolation (STI) layer.
20 In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer 1204 can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer 1204 can include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the
25 buffer layer 1204 may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene (BCB)), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer 1204 can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the permittivity of silicon dioxide.

30 **[0140]** In one embodiment, the thickness of the buffer layer 1204 can be approximately 10 nm to approximately 200 nm, with an example thicknesses of

approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer 1204 can be deposited using PVD, CVD and/or ALD, and the like.

[0141] In one embodiment, the transistor 1200 can include a source 1206, for example, proximate to the buffer layer 1204. In another embodiment, the source 1206 can include an N doped Indian Gallium Arsenide material. In one embodiment, the source 1206 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source 1206 can be fabricated using MBE. In another embodiment, the source 1206 can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source 1204 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source 1206. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source 1206 can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source 1206 can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source 1206 comprises a non-oxide a single-material semiconductor. In another embodiment, the source 1206 can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source 1206 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0142] In one embodiment, the transistor 1200 can include a drain 1207, proximate to the buffer layer 1204. In another embodiment, the drain 1207 can include an N doped Indian Gallium Arsenide layer material. In one embodiment, the device 1200 can include a drain 1207. In one embodiment, the drain 1207 can be deposited using a mask. In one embodiment, the drain 1207 can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain 1207 can be fabricated using

MBE. In another embodiment, the drain 1207 can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include generating electron vacancies in the drain 1207. In one embodiment, the drain
5 1207 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment,
10 the drain can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain 1207 can be doped with oxygen vacancies if the source 1206 comprises an oxide or a multi-material system. In another embodiment, the source 1206 can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain 1207 comprises a non-oxide a single-material
15 semiconductor. In one embodiment, the drain 1207 can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the drain 1207 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source 1206 and drain 1207 can include the
20 same material, except that the source 1206 can be treated to remove some of the sulfur and/or selenium.

[0143] In one embodiment, the transistor 1100 can include a dielectric 1208, proximate to the source 1206 and/or the drain 1207. In another embodiment, dielectric 1208 can include an oxide. In another embodiment, the dielectric 1208 can include an
25 interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the dielectric 1208 can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

[0144] In one embodiment, the transistor 1200 can include an angular region 1220 and/or an angular region 1224 in the source 1206 and/or the drain 1207. In one
30 embodiment, the angular region 1220 can be generated by the removal of a portion of the source 1206 and/or the drain 1207, which can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. In one

embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the portion of the source 1206 and/or the drain 1207.

5 **[0145]** In one embodiment, the transistor can include a channel 1210, for example, proximate to the source 1206 and/or the drain 1207. In another embodiment, the channel 1210 can include an Indian Gallium Arsenide material. In one embodiment, the device can further include a channel 1210. In one embodiment, the channel 1210 can include silicon. In another embodiment, the channel 1210 can include intrinsic silicon. In one 1210, the channel 1210 can be deposited using MBE. In another embodiment, the channel 1210 can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel 1210 can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), 15 indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel 1210 can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80 nm long (in the y-dimension). In one 20 embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel 1210 can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0146] FIG. 12B shows a diagram 1201 of an enlarged portion of the transistor of FIG. 25 12A, in accordance with example embodiments of the disclosure. In one embodiment, FIG. 12B shows a first portion 1240 of the gate 1228 and/or gate dielectric 1226, a connecting portion of the gate 1228 and/or gate dielectric 1226, and a second portion of the gate 1228 and/or gate dielectric 1226. In one embodiment, the first portion of the gate 1228 and/or gate dielectric 1226 can have at least a portion including one or more planar side walls. Similarly, in another embodiment, the second portion of the gate 1228 and/or 30 gate dielectric 1226 can have at least a portion including one or more planar bottom walls. In one embodiment, the connecting portion 1242 can have more than one angle, for

example, more than one obtuse angle. For example, although two angles 1243 and 1245 are shown in FIG. 12B, there can be three, four, or more angles having the same or different angle measurements. In one embodiment, the more than angle can have an angle of greater than about ninety degrees. In one embodiment, the connecting portion 1242 can
5 be generated by an etching process, as described further herein.

[0147] FIG. 13 shows a diagram of an example flowchart that describes the fabrication of transistor (for example, a MOSFET) having a non-vertical gate, in accordance with example embodiments of the disclosure. In block 1302, a substrate can be provided. In one embodiment, the substrate can refer to a solid (usually planar) substance onto which a
10 layer of another substance is applied, and to which that second substance adheres. In another embodiment, the substrate can include a silicon substrate. In one embodiment, the substrate can include a p-doped silicon substrate. In one embodiment, the substrate can be a thin slice of material such as silicon, silicon oxide, silicon dioxide, aluminum oxide, sapphire, an alloy of silicon and germanium, and/or indium phosphide (InP), and the like.
15 In one embodiment, the substrate can include a semiconductor material (e.g., monocrystalline silicon, germanium, silicon germanium, SiGe, and/or a III-V materials based material (e.g., gallium arsenide, GaAs), or any combination thereof).

[0148] In block 1304, a buffer layer can be provided on the substrate. In one embodiment, the buffer layer can include any material suitable to insulate adjacent devices and prevent current leakage. In one embodiment, the buffer layer can include a shallow
20 trench isolation (STI) layer. In one embodiment, the STI layer can provide field isolation regions that isolate one fin from other fins (not shown), for example, other fins on adjacent device. In one embodiment, the buffer layer can include an oxide layer (e.g., silicon dioxide), or any other electrically insulating layer. In one embodiment, the buffer layer can
25 include an interlayer dielectric (ILD), such as silicon dioxide. In one embodiment, the buffer layer may include polyimide, epoxy, photodefinable materials (for example, benzocyclobutene, BCB), WPR-series materials, and/or spin-on-glass. In one embodiment, the buffer layer can include a low permittivity (low-k) ILD layer. In one embodiment, low-k can refer to dielectrics having a dielectric constant (permittivity k) lower than the
30 permittivity of silicon dioxide. In one embodiment, the thickness of the buffer layer can be approximately 10 nm to approximately 200 nm, with an example thicknesses of

approximately 50 nm to approximately 100 nm. In one embodiment, the buffer layer can be deposited using PVD, CVD and/or ALD, and the like.

[0149] In block 1306, a source can be provided and be disposed on the buffer layer. In another embodiment, the source can include an n doped Indian Gallium Arsenide layer. In one embodiment, the source can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the source can be fabricated using MBE. In another embodiment, the source can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the source can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the doping can include generating electron vacancies in the source. In one embodiment, source can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the source can be doped, for example, by creating vacancies of sulfur and selenium. In one embodiment, the source can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the source comprises a non-oxide a single-material semiconductor. In another embodiment, the source can be approximately 1 nanometer to approximately 75 nm thick (y dimension), with example thicknesses of approximately 20 nm to approximately 30 nm thick (y dimension). In one embodiment, the source can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

[0150] In block 1308, a drain can be provided and be disposed on the buffer layer. In another embodiment, the drain can include an N doped Indian Gallium Arsenide material. In one embodiment, the drain can include silicon. In another embodiment, the silicon material may be n-doped. In another embodiment, the drain can be fabricated using MBE. In another embodiment, the drain can include can include doped or undoped black phosphorous, titanium, tantalum, cobalt, molybdenum, titanium nitride, tantalum nitride, hafnium, copper, gadolinium, and the like. In one embodiment, the doping can include

generating electron vacancies in the drain. In one embodiment, the drain can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the drain can include gettering materials. In one embodiment, the gettering materials can getter sulfur. In one embodiment, the drain can be doped with oxygen vacancies if the source comprises an oxide or a multi-material system. In another embodiment, the source can be doped with phosphorous, boron, aluminum, tin, hafnium, titanium, copper, indium, and/or arsenic if the drain comprises a non-oxide a single-material semiconductor. In one embodiment, the drain can have a thickness of approximately 0.5 nm to approximately 100 nm (in the x or y dimensions), with example thicknesses of approximately 0.5 nm to approximately 20 nm (in the x or y dimensions). In one embodiment, the can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the source and drain can include the same material, except that the source can be treated to remove some of the sulfur and/or selenium.

[0151] In block 1310, a channel can be provided and be disposed on the buffer layer. In another embodiment, the channel can include an Indian Gallium Arsenide material. In one embodiment, the device can further include a channel. In one embodiment, the channel can include silicon. In another embodiment, the channel can include intrinsic silicon. In one embodiment, the channel can be deposited using MBE. In another embodiment, the channel can include black phosphorous, amorphous silicon, germanium, carbon nanotube, and the like. In one embodiment, the channel can include silicon, germanium, silicon germanium (SiGe), indium phosphide (InP), indium arsenide (InAs), indium gallium arsenide (InGaAs), gallium nitride (GaN), amorphous semiconductors such as zinc oxide (ZnO), indium gallium zinc oxide (IGZO), amorphous silicon (a-Si), amorphous germanium (a-Ge), polycrystalline germanium, polycrystalline silicon, and/or polycrystalline InGaAs, and the like. In one embodiment, the channel width can depend on the technology used to generate the transistor. In another embodiment, the channel can be approximately 0.5 nm to approximately 200 nm long (in the y-dimension), with example thicknesses of approximately 60 nm to approximately 80

nm long (in the y-dimension). In one embodiment, the channel width can be approximately 200 nm down to approximately 5 nm (in the x-dimension). In one embodiment, the channel can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like.

5 **[0152]** In block 1312, a sacrificial gate material and one or more spacers can be provided and be disposed on the channel. In one embodiment, the sacrificial gate material can also be referred to as a dummy gate. In another embodiment, the dummy gate can include a polysilicon material. In one embodiment, the dummy gate can serve as a temporary placeholder for the eventual deposition of a gate and/or gate dielectric, to be
10 further described below.

[0153] In another embodiment, spacer can include an oxide. In one embodiment, the oxide can include an interlayer dielectric (ILD) material. In another embodiment, ILD can include silicon dioxide (SiO₂), or a low-K material. In one embodiment, the oxide can be deposited using PVD, CVD, MOCVD, and/or ALD, and the like.

15 **[0154]** In block 1314, the sacrificial gate material and a portion of the buffer layer can be removed. In one embodiment, a first recess can be generated by the removal of the portion of the dummy gate. In one embodiment, a second recess can be generated by the removal of a portion of the buffer layer. In one embodiment, the removal of the portion of the dummy gate or the buffer layer can be performed using an etching process. In one
20 embodiment, the etching process can include, for example, a dry etch. In one embodiment, the dry etch can include, for example, a plasma-based and/or a mechanical-based etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of the dummy gate or the buffer layer.

25 **[0155]** In block 1316, a first portion of a first side of the channel can be removed to generate a first recess having a first corner proximate to the source, and a second corner proximate to the drain, wherein the first corner or the second corner has the interior angle greater than about ninety degrees. In one embodiment, the removal of the portion of the first portion of a first side of the channel can be performed using an etching process. In
30 one embodiment, the etching process can include, for example, a dry etch. In one embodiment, the etching process can include, for example, a wet etch. The wet etching

process can include, for example, any suitable chemicals for the removal of the first portion of a first side of the channel.

[0156] In block 1318, a second portion of a second side of the channel can be removed to generate a second recess having a third corner proximate to the source, and a fourth corner proximate to the drain, wherein the third corner or the fourth corner has the interior angle greater than about ninety degrees. In one embodiment, the removal of the second side of the channel can be performed using an etching process. In one embodiment, the etching process can include, for example, a dry etch. dummy gate. In one embodiment, the etching process can include, for example, a wet etch. The wet etching process can include, for example, any suitable chemicals for the removal of dummy gate.

[0157] In block 1320, a first gate material can be deposited in the first recess. In one embodiment, the gate material can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material. In one embodiment, the gate material can include hydrogenated boron nitride (HBN). In one embodiment, the gate material can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material can have a width of 0.5 nm to approximately 20 nm (x-dimension). In another embodiment, the gate material can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0158] In block 1322, a second gate material can be deposited in the second recess. In one embodiment, the gate material can include a high-K dielectric material. In another embodiment, the high-K material, for example, hafnium oxide, tantalum oxide, titanium oxide, aluminum oxide, silicon dioxide, silicon nitride and the like. In another embodiment, the gate material can include silicon oxide, which may not be a high-K material. In one embodiment, an electroglass (EG) can be used as the gate material. In one embodiment, the gate material can include hydrogenated boron nitride (HBN). In one embodiment, the gate material can be deposited using PVD, CVD, MOCVD, MBE, and/or ALD, and the like. In one embodiment, the gate material can have a width of 0.5 nm to

approximately 20 nm (x-dimension). In another embodiment, the gate material can have a thickness of approximately 0.5 nm to approximately 100 nm (in the y dimension).

[0159] In block 1324, a first gate can be deposited on the first gate material. In another embodiment, the gate can include a metal. In another embodiment, the gate can include a transition metal. In one embodiment, the gate can be used to tune the threshold voltage of the device. In one embodiment, gate can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the gate can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the gate can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the gate can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0160] In block 1326, a second gate can be deposited on the second gate material. In another embodiment, the gate can include a metal. In another embodiment, the gate can include a transition metal. In one embodiment, the gate can be used to tune the threshold voltage of the device. In one embodiment, gate can include titanium nitride, cobalt, tungsten and/or platinum. In one embodiment, the gate can be deposited using PVD, CVD, MOCVD, MBE and/or ALD, and the like. In one embodiment, the gate can have a width of approximately 10 nm to approximately 150 nm (x-dimension). In another embodiment, the gate 214 can have a length of approximately 10 nm to approximately 150 nm (y-dimension).

[0161] In block 1328, a source contact can be deposited on the source. In one embodiment, the source contact can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The source contact can include any alloys of such materials.

[0162] In block 1330, a drain contact can be deposited on the drain. In one embodiment, the drain contact can include a metal. In one embodiment, the metal can include gold, copper, silver, aluminum, zinc, tin, platinum, and any of the like. The drain contact can include any alloys of such materials.

[0163] FIG. 14 depicts an example of a system 1400 according to one or more embodiments of the disclosure. In one embodiment, system 1400 includes, but is not

limited to, a desktop computer, a laptop computer, a netbook, a tablet, a notebook computer, a personal digital assistant (PDA), a server, a workstation, a cellular telephone, a mobile computing device, a smart phone, an Internet appliance or any other type of computing device. In some embodiments, system 1400 can include a system on a chip (SOC) system.

[0164] In one embodiment, system 1400 includes multiple processors including processor 1410 and processor N 1405, where processor N 1405 has logic similar or identical to the logic of processor 1410. In one embodiment, processor 1410 has one or more processing cores (represented here by processing core 1 1412 and processing core N 1412N, where 1412N represents the Nth processor core inside processor 1410, where N is a positive integer). More processing cores can be present (but not depicted in the diagram of FIG. 14). In some embodiments, processing core 1412 includes, but is not limited to, pre-fetch logic to fetch instructions, decode logic to decode the instructions, execution logic to execute instructions, a combination thereof, or the like. In some embodiments, processor 1410 has a cache memory 1416 to cache instructions and/or data for system 1400. Cache memory 1416 may be organized into a hierarchical structure including one or more levels of cache memory.

[0165] In some embodiments, processor 1410 includes a memory controller (MC) 1414, which is configured to perform functions that enable the processor 1410 to access and communicate with memory 1430 that includes a volatile memory 1432 and/or a non-volatile memory 1434. In some embodiments, processor 1410 can be coupled with memory 1430 and chipset 1420. Processor 1410 may also be coupled to a wireless antenna 1478 to communicate with any device configured to transmit and/or receive wireless signals. In one embodiment, the wireless antenna 1478 operates in accordance with, but is not limited to, the IEEE 1402.11 standard and its related family, Home Plug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMax, or any form of wireless communication protocol.

[0166] In some embodiments, volatile memory 1432 includes, but is not limited to, Synchronous Dynamic Random Access Memory (SDRAM), Dynamic Random Access Memory (DRAM), RAMBUS Dynamic Random Access Memory (RDRAM), and/or any other type of random access memory device. Non-volatile memory 1434 includes, but is

not limited to, flash memory, phase change memory (PCM), read-only memory (ROM), electrically erasable programmable read-only memory (EEPROM), or any other type of non-volatile memory device.

5 [0167] Memory device 1430 stores information and instructions to be executed by processor 1410. In one embodiment, memory 1430 may also store temporary variables or other intermediate information while processor 1410 is executing instructions. In the illustrated embodiment, chipset 1420 connects with processor 1410 via Point-to-Point (PtP or P-P) interface 1417 and P-P interface 1422. Chipset 1420 enables processor 1410 to connect to other elements in system 1400. In some embodiments of the disclosure, P-P
10 interface 1417 and P-P interface 1422 can operate in accordance with a PtP communication protocol, such as the Intel® QuickPath Interconnect (QPI) or the like. In other embodiments, a different interconnect may be used.

[0168] In some embodiments, chipset 1420 can be configured to communicate with processor 1410, the processor N 1405, display device 1440, and other devices 1472, 1476,
15 1474, 1460, 1462, 1464, 1466, 1477, etc. Chipset 1420 may also be coupled to the wireless antenna 1478 to communicate with any device configured to transmit and/or receive wireless signals.

[0169] Chipset 1420 connects to display device 1440 via interface 1426. Display 1440 may be, for example, a liquid crystal display (LCD), a plasma display, cathode ray tube
20 (CRT) display, or any other form of visual display device. In some embodiments of the disclosure, processor 1410 and chipset 1420 are integrated into a single SOC. In addition, chipset 1420 connects to bus 1450 and/or bus 1455 that interconnect various elements 1474, 1460, 1462, 1464, and 1466. Bus 1450 and bus 1455 may be interconnected via a bus bridge 1472. In one embodiment, chipset 1420 couples with a non-volatile memory
25 1460, a mass storage device(s) 1462, a keyboard/mouse 1464, and a network interface 1466 via interface 1424 and/or 1404, smart TV 1476, consumer electronics 1477, etc.

[0170] In one embodiment, mass storage device(s) 1462 can include, but not be limited to, a solid state drive, a hard disk drive, a universal serial bus flash memory drive, or any other form of computer data storage medium. In one embodiment, network
30 interface 1466 is implemented by any type of well-known network interface standard including, but not limited to, an Ethernet interface, a universal serial bus (USB) interface,

a Peripheral Component Interconnect (PCI) Express interface, a wireless interface and/or any other suitable type of interface. In one embodiment, the wireless interface operates in accordance with, but is not limited to, the IEEE 802.11 standard and its related family, Home Plug AV (HPAV), Ultra Wide Band (UWB), Bluetooth, WiMax, or any form of
5 wireless communication protocol.

[0171] While the modules shown in FIG. 7 are depicted as separate blocks within the system 1400, the functions performed by some of these blocks may be integrated within a single semiconductor circuit or may be implemented using two or more separate integrated circuits. For example, although cache memory 1416 is depicted as a separate block within
10 processor 1410, cache memory 1416 or selected elements thereof can be incorporated into processor core 1412.

[0172] It is noted that the system 1400 described herein may be any suitable type of microelectronics packaging and configurations thereof, including, for example, system in a package (SiP), system on a package (SOP), package on package (PoP), interposer
15 package, 3D stacked package, etc. Further, any suitable type of microelectronic components may be provided in the semiconductor packages, as described herein. For example, microcontrollers, microprocessors, baseband processors, digital signal processors, memory dies, field gate arrays, logic gate dies, passive component dies, MEMSs, surface mount devices, application specific integrated circuits, baseband
20 processors, amplifiers, filters, combinations thereof, or the like may be packaged in the semiconductor packages, as disclosed herein. The semiconductor packages (for example, the semiconductor packages described in connection with any of FIGS. 1-6), as disclosed herein, may be provided in any variety of electronic device including consumer, industrial, military, communications, infrastructural, and/or other electronic devices.

[0173] In various embodiments, the devices, as described herein, may be used in connection with one or more processors. The one or more processors may include, without limitation, a central processing unit (CPU), a digital signal processor(s) (DSP), a reduced instruction set computer (RISC), a complex instruction set computer (CISC), a microprocessor, a microcontroller, a field programmable gate array (FPGA), or any
25 combination thereof. The processors may also include one or more application specific integrated circuits (ASICs) or application specific standard products (ASSPs) for handling
30

specific data processing functions or tasks. In certain embodiments, the processors may be based on an Intel® Architecture system and the one or more processors and any chipset included in an electronic device may be from a family of Intel® processors and chipsets, such as the Intel® Atom® processor(s) family or Intel-64 processors (for example, Sandy Bridge®, Ivy Bridge®, Haswell®, Broadwell®, Skylake®, etc.).

[0174] Additionally or alternatively, the devices, as described herein, may be used in connection with one or more additional memory chips. The memory may include one or more volatile and/or non-volatile memory devices including, but not limited to, magnetic storage devices, read-only memory (ROM), random access memory (RAM), dynamic RAM (DRAM), static RAM (SRAM), synchronous dynamic RAM (SDRAM), double data rate (DDR) SDRAM (DDR-SDRAM), RAM-BUS DRAM (RDRAM), flash memory devices, electrically erasable programmable read-only memory (EEPROM), non-volatile RAM (NVRAM), universal serial bus (USB) removable memory, or combinations thereof.

[0175] In example embodiments, the electronic device in which the disclosed devices are used and/or provided may be a computing device. Such a computing device may house one or more boards on which the devices may be disposed. The board may include a number of components including, but not limited to, a processor and/or at least one communication chip. The processor may be physically and electrically connected to the board through, for example, electrical connections of the devices. The computing device may further include a plurality of communication chips. For instance, a first communication chip may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth, and a second communication chip may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, and others. In various example embodiments, the computing device may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, combinations thereof, or the like. In further example embodiments, the computing device may be any other electronic device that processes data.

[0176] Example 1 is a transistor device, comprising: a substrate; a buffer layer disposed on the substrate; a source disposed on the buffer layer; a drain disposed on the buffer layer;

5 a channel disposed on the buffer layer; a first gate disposed on the channel between the source and the drain, wherein the first gate has a first connecting portion connecting a first side edge of the first gate proximate to the source and a lower edge proximate the channel, and a second connecting portion connecting a second side edge of the first gate proximate to the drain and the lower edge proximate the channel, and wherein at least one of the first connecting portion or the second connecting portion comprises more than one angle. In
10 example 2, the device of example 1 can optionally include a second gate, wherein the second gate has a third connecting portion connecting a first side edge of the second gate proximate to the source and an upper edge proximate the channel, and a second connecting portion connecting a second side edge of the second gate proximate to the drain and the upper edge proximate the channel, and wherein at least one of the first connecting portion
15 or the second connecting portion comprises more than one angle. In example 3, the device of any one of examples 1 or 2 can optionally include a channel having a first connecting portion connecting a first side edge of the channel gate proximate to the source and an upper edge of the channel, and a second connecting portion connecting a second side edge of the channel proximate to the drain and the upper edge of the channel, and wherein at
20 least one of the first connecting portion or the second connecting portion comprises more than one angle. In example 4, the device of any one of examples 1-3 can optionally include a channel having a first connecting portion connecting a first side edge of the channel gate proximate to the source and an lower edge of the channel, and a second connecting portion connecting a second side edge of the channel proximate to the drain
25 and the lower edge of the channel, and wherein at least one of the first connecting portion or the second connecting portion comprises more than one angle. In example 5, the device of any one of examples 1-4 can optionally include a source comprising a material having a first crystallographic face of a first orientation proximate to the first connecting portion of the gate. In example 6, the device of any one of examples 1-5 can optionally include a
30 drain comprising a material having a second crystallographic facet of a second orientation proximate to the first connecting portion of the gate. In example 7, the device of example 5 can optionally include a first orientation of the first crystallographic face having Miller indices of (111). In example 8, the device of example 6 can optionally include a second

orientation of the second crystallographic facet having Miller indices of (111). In example 9, the device of any one of examples 1-8 can optionally include a source or the drain comprising an n-doped InGaAs material. In example 10, the device of any one of examples 1-9 can optionally include a channel comprising an InGaAs material. In example 11, the device of any one of examples 1-10 can optionally include a gate material comprising a high-k dielectric material.

[0177] Example 12 is a method for fabricating a transistor device, the method comprising: providing a substrate; providing a buffer layer disposed on the substrate; providing a source disposed on the buffer layer; providing a drain disposed on the buffer layer; providing a channel disposed on the buffer layer; providing a sacrificial gate material and one or more spacers disposed on the channel; removing the sacrificial gate material and a portion of the buffer layer; removing a first portion of a first side of the channel to generate a first recess having a first connecting portion proximate to the source, and a second connecting portion proximate to the drain, wherein the first connecting portion or the second connecting portion comprises more than one angle; removing a second portion of a second side of the channel to generate a second recess having a third connecting portion proximate to the source, and a fourth connecting portion proximate to the drain, wherein the third connecting portion or the fourth connecting portion comprises more than one angle; depositing a first gate material in the first recess; depositing a second gate material in the second recess; depositing a first gate on the first gate material; depositing a second gate on the second gate material; depositing a source contact on the source; and depositing a drain contact on the drain. In example 13, the method of example 12 can optionally include removing the first portion of the first side of the channel comprising removing the first portion of the first side of the channel using an isotropic etch process. In example 14, the method of example 12 or 13 can optionally include removing the second portion of the second side of the channel comprising removing the second portion of the second side of the channel using an isotropic etch process. In example 15, the method of example 12-14 can optionally include providing the source or providing the drain comprising providing an n-doped InGaAs material. In example 16, the method of example 12-15 can optionally include providing the channel comprising providing an InGaAs material. In example 17, the method of example 12-16 can optionally

include depositing the first gate material comprising depositing a high-k dielectric material.

[0178] Example 18 is a method for fabricating a transistor device, the method comprising: providing a substrate; providing a buffer layer disposed on the substrate; providing a source disposed on the buffer layer, the source having a first crystallographic facet of a first orientation; providing a drain disposed on the buffer layer, the drain having a second crystallographic facet of a second orientation; providing a channel disposed on the buffer layer; providing a sacrificial gate material disposed on the channel; providing an interlayer dielectric layer disposed on the source and the drain; removing the sacrificial gate material to produce a first recess and a portion of the buffer layer to produce a second recess; removing a portion of the interlayer dielectric layer to produce a third recess; depositing a first gate material and a first gate metal in the second recess; and depositing a second gate material and a second gate metal in the third recess. In example 19, the method of claim 18 can optionally include a first orientation of the first crystallographic facet having Miller indices of (111). In example 20, the method of any one of claims 18 or 19 can optionally include a second orientation of the second crystallographic facet having Miller indices of (111). In example 21, the method of any one of 18-20 can optionally include providing the source or providing the drain comprising providing an n-doped InGaAs material. In example 22, the method of any one of 18-21 can optionally include providing the channel comprising providing an InGaAs material. In example 23, the method of any one of 18-22 can optionally include providing the gate material comprises providing a high-k dielectric material.

[0179] Example 24 is a system comprising: a transistor device, comprising: a substrate; a buffer layer disposed on the substrate; a source disposed on the buffer layer; a drain disposed on the buffer layer; a channel disposed on the buffer layer; a first gate disposed on the channel between the source and the drain, wherein the first gate has a first connecting portion connecting a first side edge of the first gate proximate to the source and a lower edge proximate the channel, and a second connecting portion connecting a second side edge of the first gate proximate to the drain and the lower edge proximate the channel, and wherein at least one of the first connecting portion or the second connecting portion comprises more than one angle. In example 25, the system of example 24 can optionally include a second gate, wherein the second gate has a third connecting portion connecting a

first side edge of the second gate proximate to the source and an upper edge proximate the channel, and a second connecting portion connecting a second side edge of the second gate proximate to the drain and the upper edge proximate the channel, and wherein at least one of the first connecting portion or the second connecting portion comprises more than one angle. In example 26, the system of any one of examples 24 or 25 can optionally include a channel having a first connecting portion connecting a first side edge of the channel gate proximate to the source and an upper edge of the channel, and a second connecting portion connecting a second side edge of the channel proximate to the drain and the upper edge of the channel, and wherein at least one of the first connecting portion or the second connecting portion comprises more than one angle. In example 27, the system of any one of examples 24-26 can optionally include a channel having a first connecting portion connecting a first side edge of the channel gate proximate to the source and an lower edge of the channel, and a second connecting portion connecting a second side edge of the channel proximate to the drain and the lower edge of the channel, and wherein at least one of the first connecting portion or the second connecting portion comprises more than one angle. In example 28, the system of any one of examples 24-27 can optionally include a source comprising a material having a first crystallographic face of a first orientation proximate to the first connecting portion of the gate. In example 29, the system of any one of examples 24-28 can optionally include a drain comprising a material having a second crystallographic facet of a second orientation proximate to the first connecting portion of the gate. In example 30, the system of example 28 can optionally include a first orientation of the first crystallographic face having Miller indices of (111). In example 31, the system of example 29 can optionally include a second orientation of the second crystallographic facet having Miller indices of (111). In example 32, the system of any one of examples 24-31 can optionally include a source or the drain comprising an n-doped InGaAs material. In example 33, the system of any one of examples 24-32 can optionally include a channel comprising an InGaAs material. In example 34, the system of any one of examples 24-33 can optionally include a gate material comprising a high-k dielectric material.

[0180] Various features, aspects, and embodiments have been described herein. The features, aspects, and embodiments are susceptible to combination with one another as well as to variation and modification, as will be understood by those having skill in the art.

The present disclosure should, therefore, be considered to encompass such combinations, variations, and modifications.

5 [0181] The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims. Other modifications, variations, and alternatives are also possible. Accordingly, the claims are intended to cover all such equivalents.

10 [0182] While the disclosure includes various embodiments, including at least a best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, the disclosure is intended to embrace all such alternatives, modifications, and variations, which fall within the scope of the included claims. All matters disclosed herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-
15 limiting sense.

[0183] This written description uses examples to disclose certain embodiments of the disclosure, including the best mode, and also to enable any person skilled in the art to practice certain embodiments of the disclosure, including making and using any apparatus, devices or systems and performing any incorporated methods and processes. The
20 patentable scope of certain embodiments of the disclosure is defined in the claims, and may include other examples that occur to those skilled in the art. Such other examples are intended to be within the scope of the claims if they have structural elements that do not differ from the literal language of the claims, or if they include equivalent structural elements with insubstantial differences from the literal language of the claims.

25

CLAIMS

What is claimed is:

1. A transistor device, comprising:
 - a substrate;
 - 5 a buffer layer on the substrate;
 - a source on the buffer layer;
 - a drain on the buffer layer;
 - a channel on the buffer layer;
 - a gate on the channel between the source and the drain, wherein the gate includes,
 - 10 a first connecting portion connecting a first side edge of the gate proximate to the source and a lower edge proximate the channel, and
 - a second connecting portion connecting a second side edge of the gate proximate to the drain and the lower edge proximate the channel,
 - wherein at least one of the first connecting portion or the second connecting
 - 15 portion comprises more than one angle.
2. The device of claim 1, wherein the gate is a first gate, the device further comprising a second gate, wherein the second gate includes,
 - a third connecting portion connecting a first side edge of the second gate
 - 20 proximate to the source and an upper edge proximate the channel, and
 - a fourth connecting portion connecting a second side edge of the second gate proximate to the drain and the upper edge proximate the channel,
 - wherein at least one of the third connecting portion or the fourth connecting
 - 25 portion comprises more than one angle.
3. The device of claim 2 wherein the channel includes,
 - a seventh connecting portion connecting a first side edge of the channel
 - gate proximate to the source and an lower edge of the channel, and
 - a eight connecting portion connecting a second side edge of the channel
 - 30 proximate to the drain and the lower edge of the channel,
 - wherein at least one of the seventh connecting portion or the eight
 - connecting portion comprises more than one angle.

4. The device of claim 1, wherein the channel includes,
a fifth connecting portion connecting a first side edge of the channel gate proximate to the source and an upper edge of the channel, and
5 a sixth connecting portion connecting a second side edge of the channel proximate to the drain and the upper edge of the channel,
wherein at least one of the fifth connecting portion or the sixth connecting portion comprises more than one angle.
- 10 5. The device of claim 1, wherein the source comprises a material having a first crystallographic face of a first orientation proximate to the first connecting portion of the gate.
6. The device of claim 5, wherein the first orientation of the first crystallographic facet has
15 Miller indices of (111).
7. The device of claim 1, wherein the drain comprises a material having a second crystallographic facet of a second orientation proximate to the first connecting portion of the gate.
20
8. The device of claim 6, wherein second orientation of the second crystallographic facet has Miller indices of (111).
9. The device of claim 1, wherein the source or the drain comprises an n-doped InGaAs
25 material.
10. The device of claim 1, wherein the channel comprises an InGaAs material.
11. The device of claim 1, wherein the gate material comprises a high-k dielectric
30 material.
12. A method for fabricating a transistor device, the method comprising:
providing a substrate;

- providing a buffer layer disposed on the substrate;
providing a source disposed on the buffer layer;
providing a drain disposed on the buffer layer;
providing a channel disposed on the buffer layer;
5 providing a sacrificial gate material and one or more spacers disposed on the channel;
removing the sacrificial gate material and a portion of the buffer layer;
removing a first portion of a first side of the channel to form a first recess having a first connecting portion proximate to the source and a second connecting portion
10 proximate to the drain, wherein the first connecting portion or the second connecting portion comprises more than one angle;
removing a second portion of a second side of the channel to form a second recess having a third connecting portion proximate to the source, and a fourth connecting portion proximate to the drain, wherein the third connecting portion or the fourth connecting
15 portion comprises more than one angle;
depositing a first gate material in the first recess;
depositing a second gate material in the second recess;
depositing a first gate on the first gate material;
depositing a second gate on the second gate material;
20 depositing a source contact on the source; and
depositing a drain contact on the drain.

13. The method of claim 12, wherein removing the first portion of the first side of the channel comprises removing the first portion of the first side of the channel using an
25 isotropic etch process.

14. The method of claim 12, wherein removing the second portion of the second side of the channel comprising removing the second portion of the second side of the channel
using an isotropic etch process.

30 15. The method of claim 12, wherein providing the source or providing the drain comprises providing an n-doped InGaAs material.

16. The method of claim 12, wherein providing the channel comprises providing an InGaAs material.

17. The method of claim 12, wherein depositing the first gate material comprises
5 depositing a high-k dielectric material.

18. A method for fabricating a transistor device, the method comprising:
providing a substrate;
providing a buffer layer disposed on the substrate;
10 providing a source disposed on the buffer layer, the source having a first
crystallographic facet of a first orientation;
providing a drain disposed on the buffer layer, the drain having a second
crystallographic facet of a second orientation;
providing a channel disposed on the buffer layer;
15 providing a sacrificial gate material disposed on the channel;
providing an interlayer dielectric layer disposed on the source and the drain;
removing the sacrificial gate material to form a first recess and a portion of the
buffer layer to form a second recess;
removing a portion of the interlayer dielectric layer to form a third recess;
20 depositing a first gate metal in the second recess; and
depositing a second gate material and a second gate metal in the third recess.

19. The method of claim 18, wherein the first orientation of the first crystallographic facet
has Miller indices of (111).
25

20. The method of claim 18, wherein second orientation of the second crystallographic
facet has Miller indices of (111).

21. The method of claim 18, wherein providing the source or providing the drain
30 comprises providing an n-doped InGaAs material.

22. The method of claim 18, wherein providing the channel comprises providing an
InGaAs material.

23. The method of claim 18, wherein providing the gate material comprises providing a high-k dielectric material.

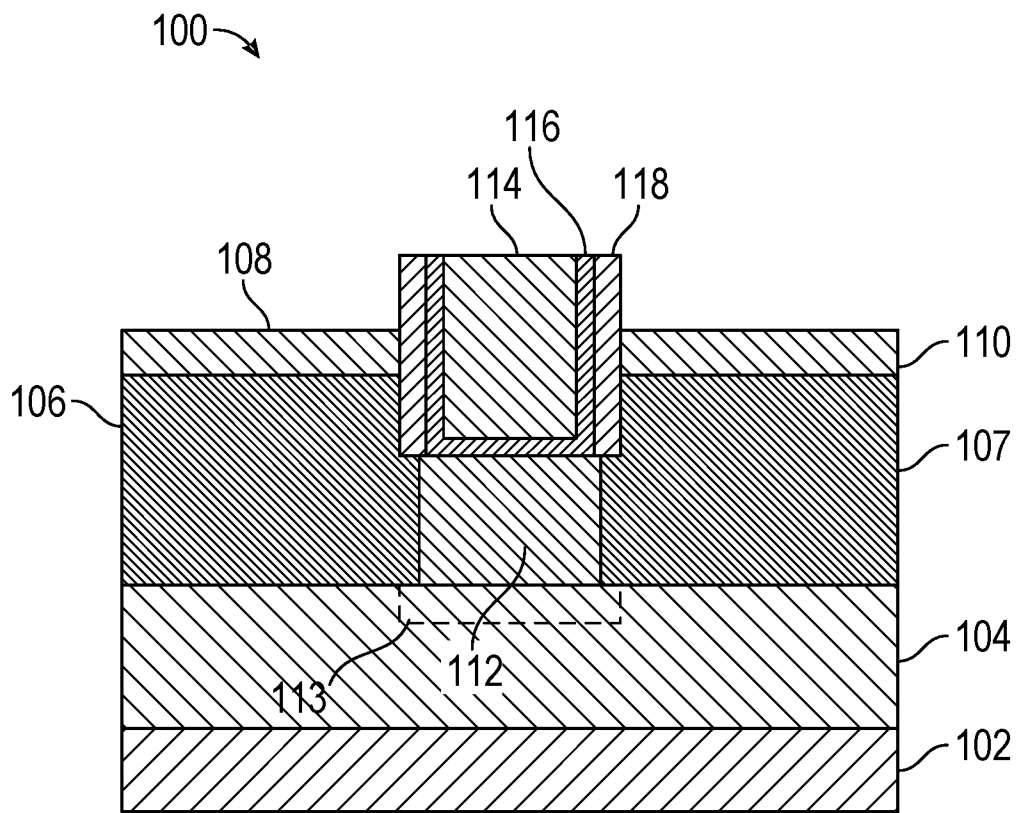
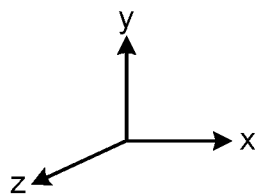


FIG. 1



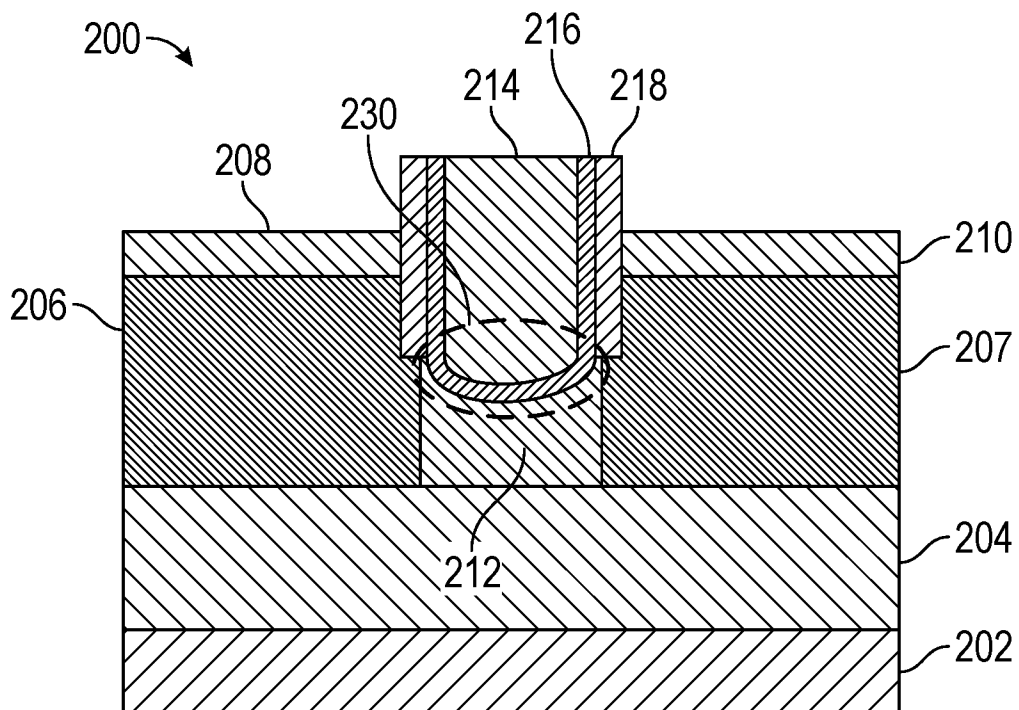


FIG. 2A

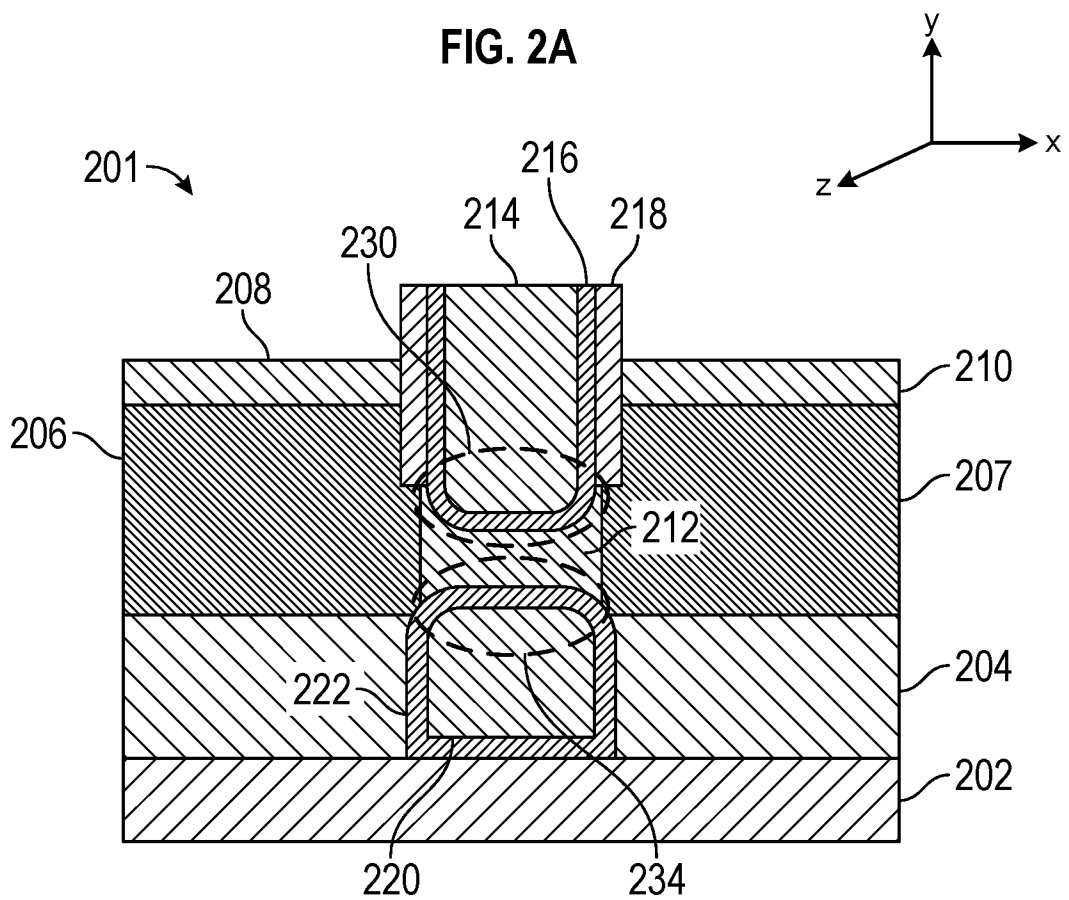


FIG. 2B

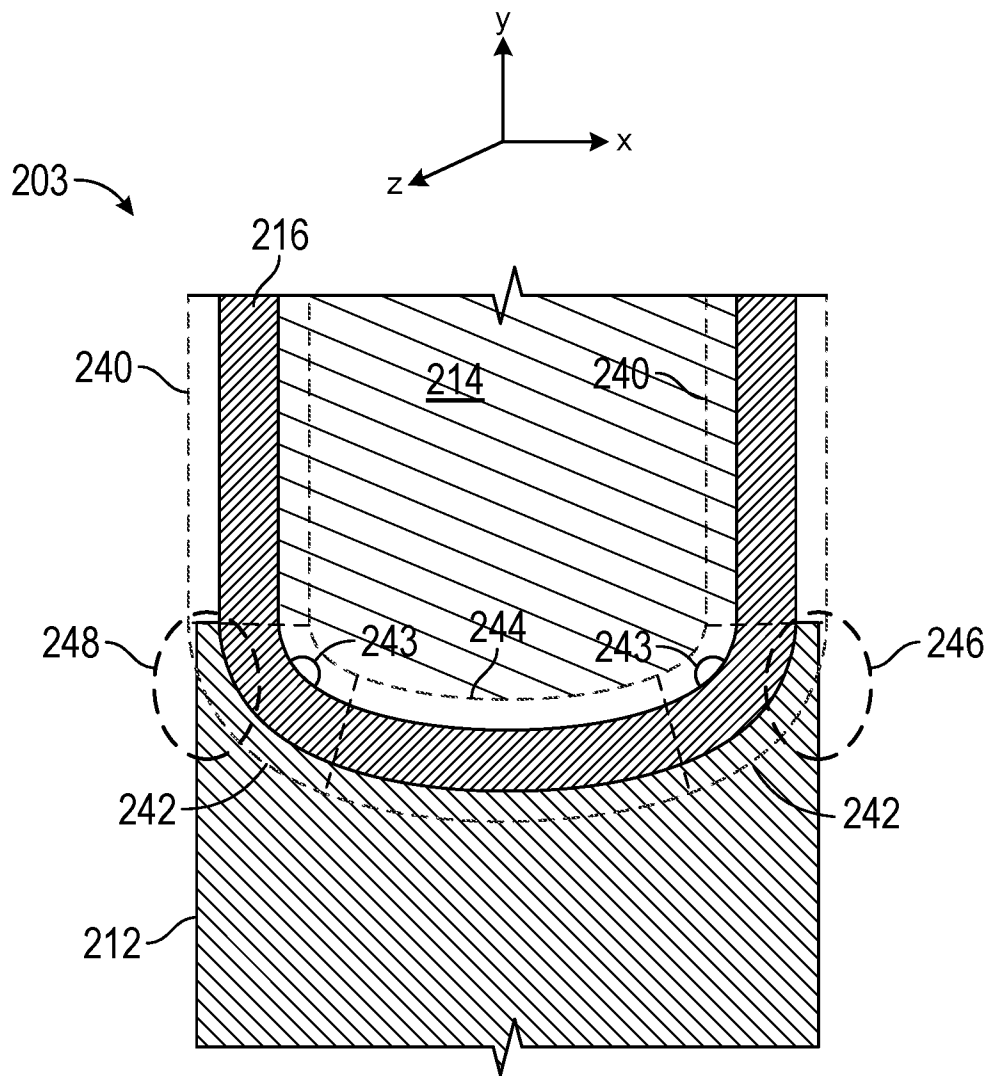


FIG. 2C

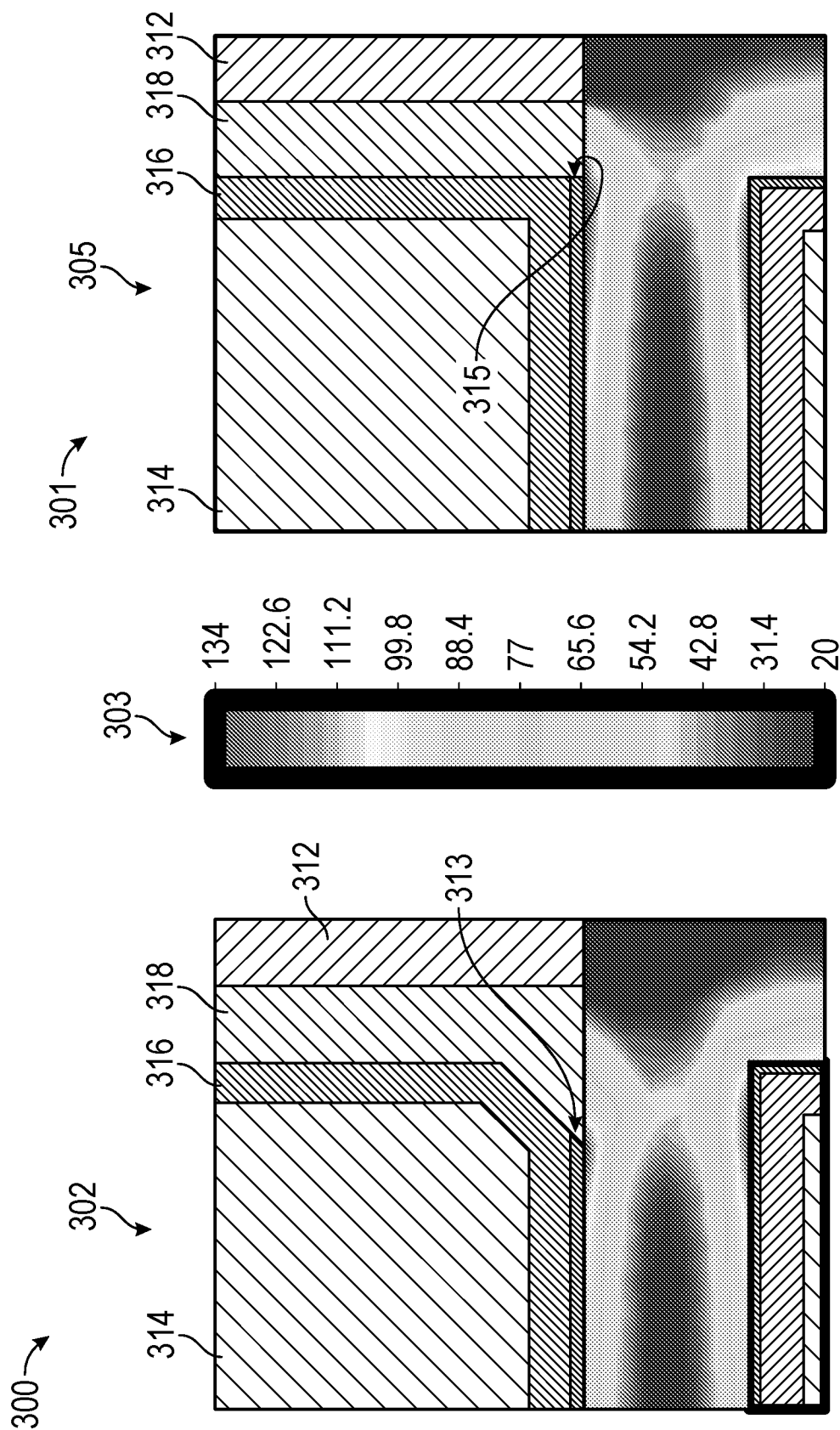


FIG. 3B

FIG. 3A

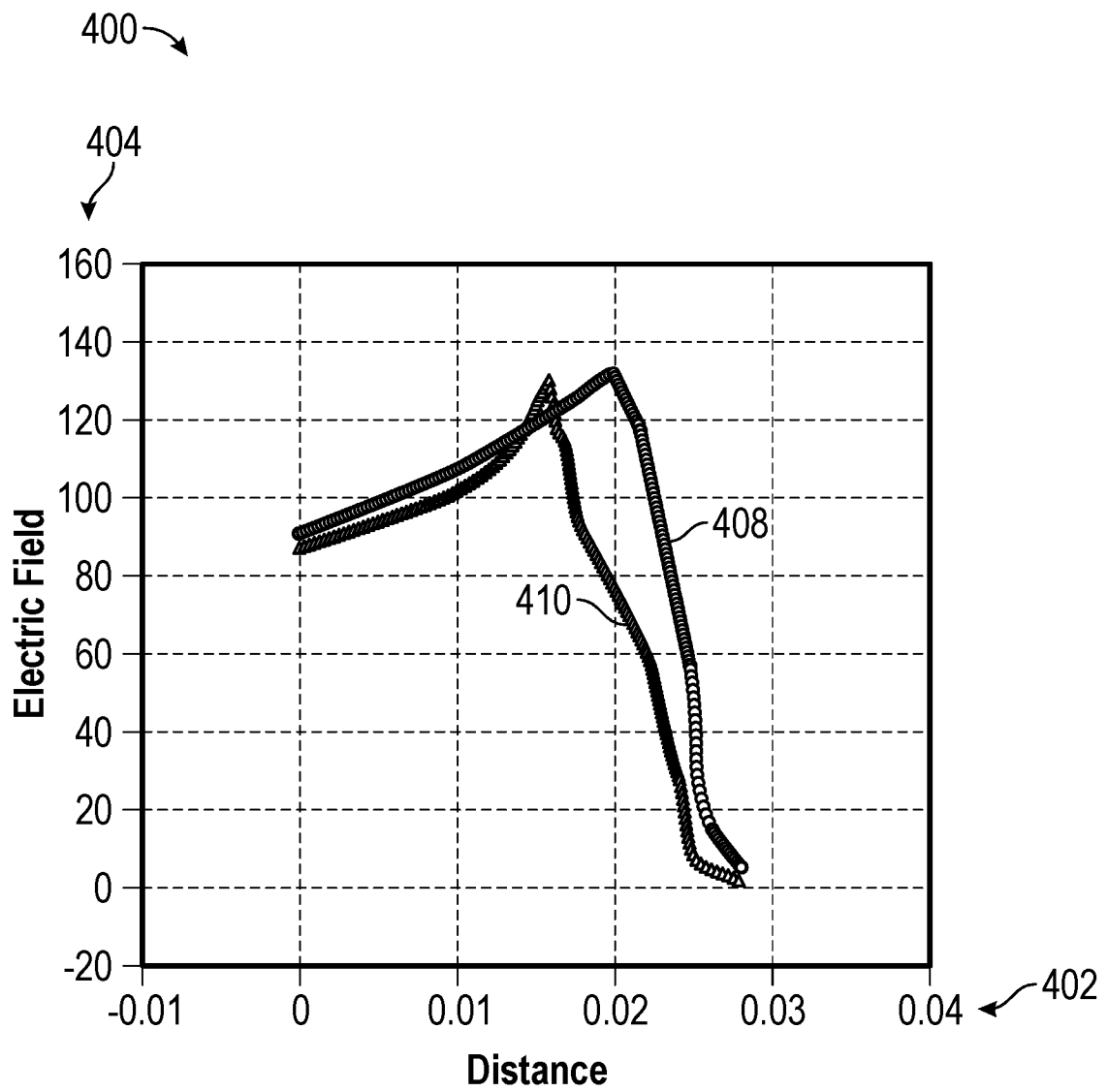


FIG. 4

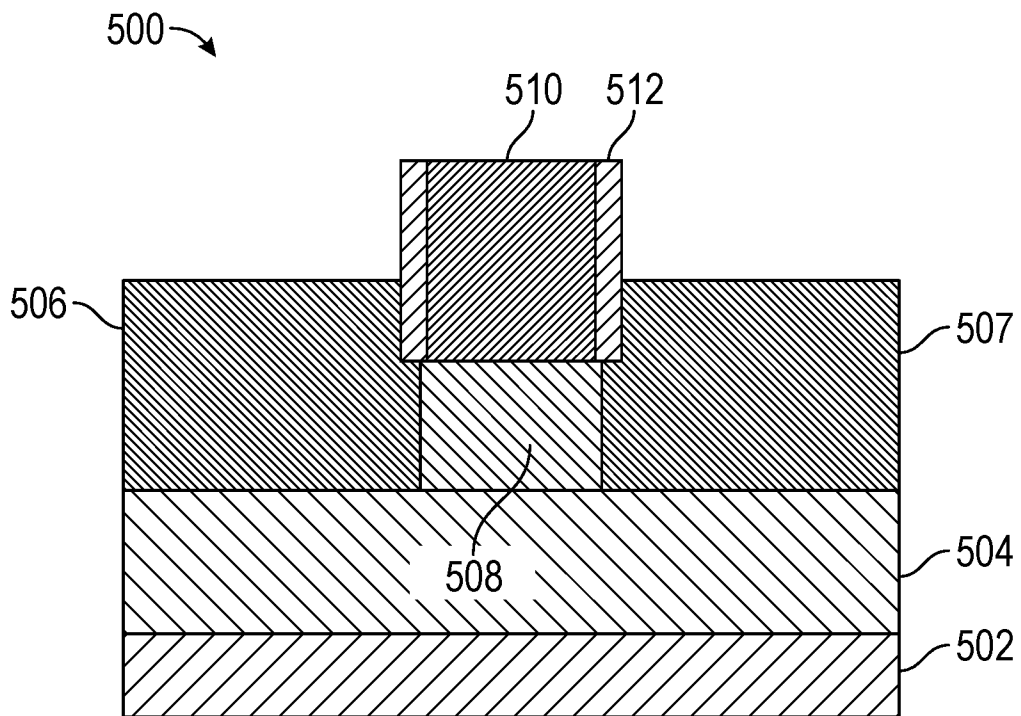


FIG. 5

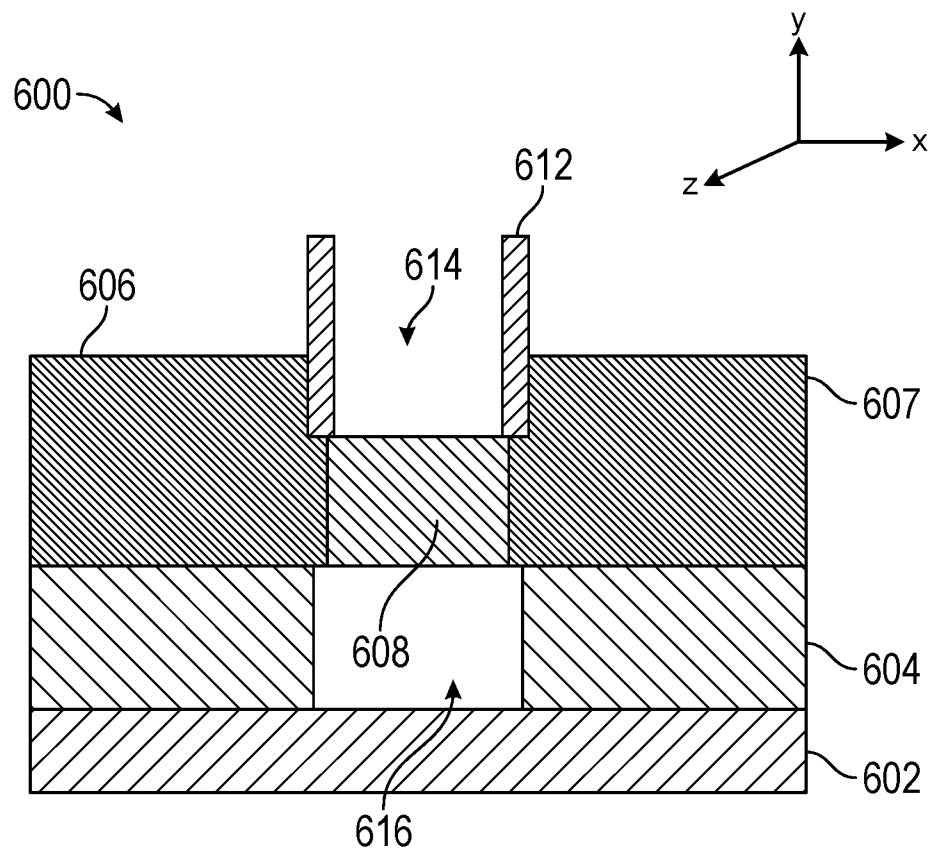


FIG. 6

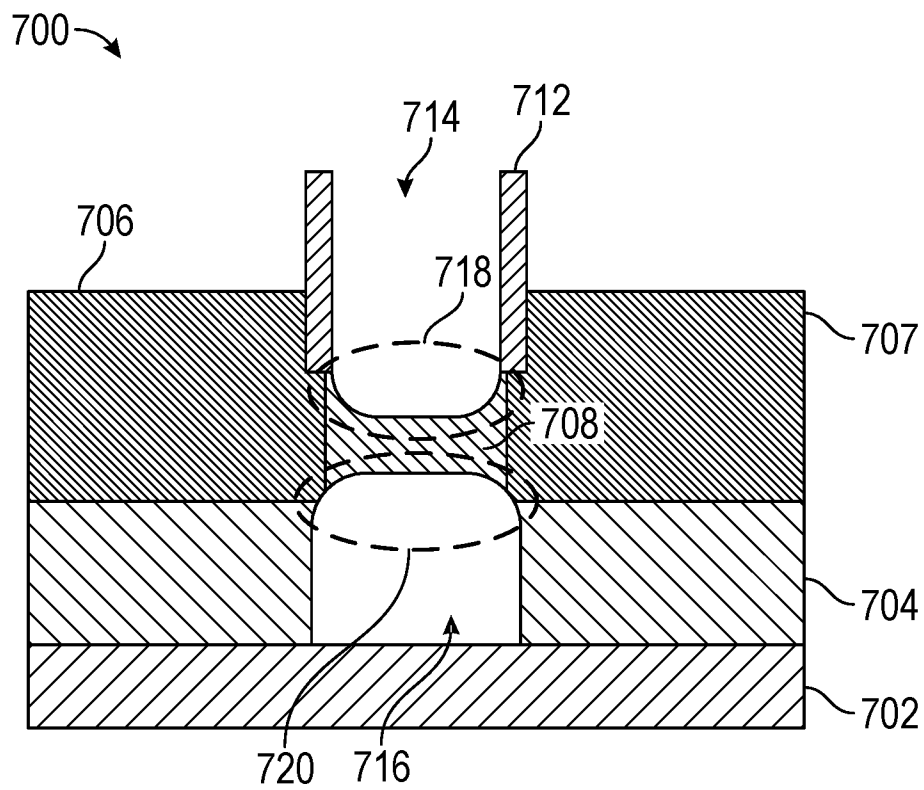


FIG. 7

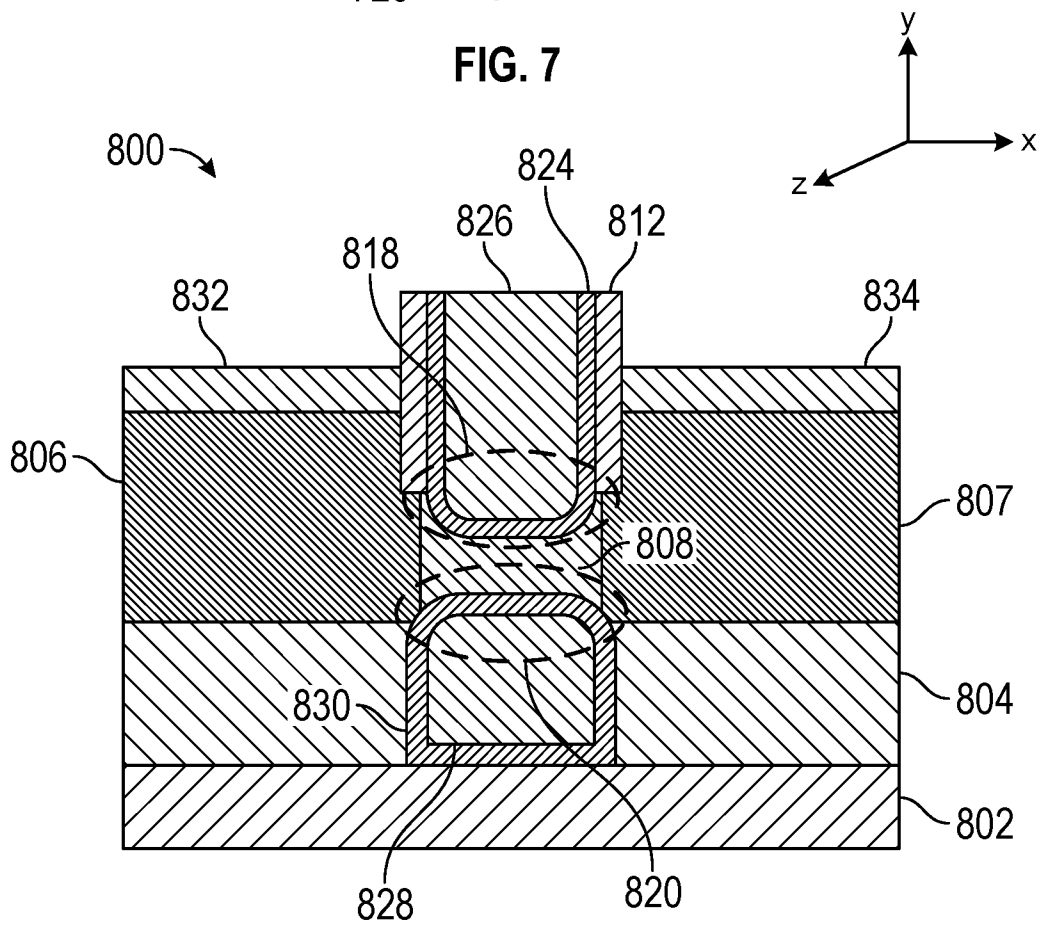


FIG. 8

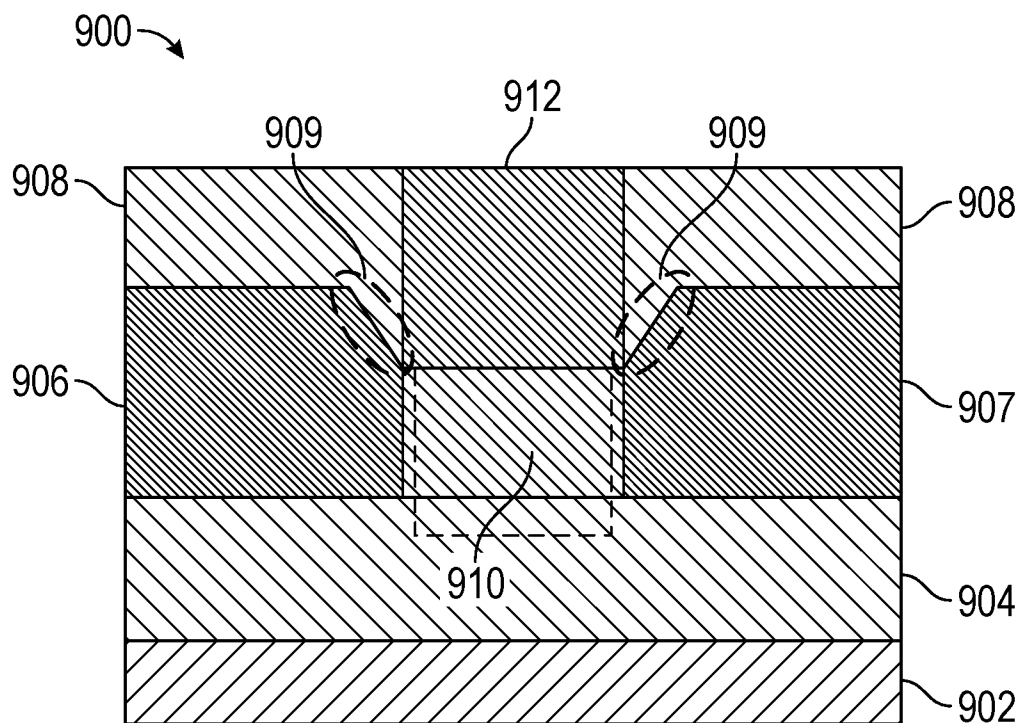


FIG. 9

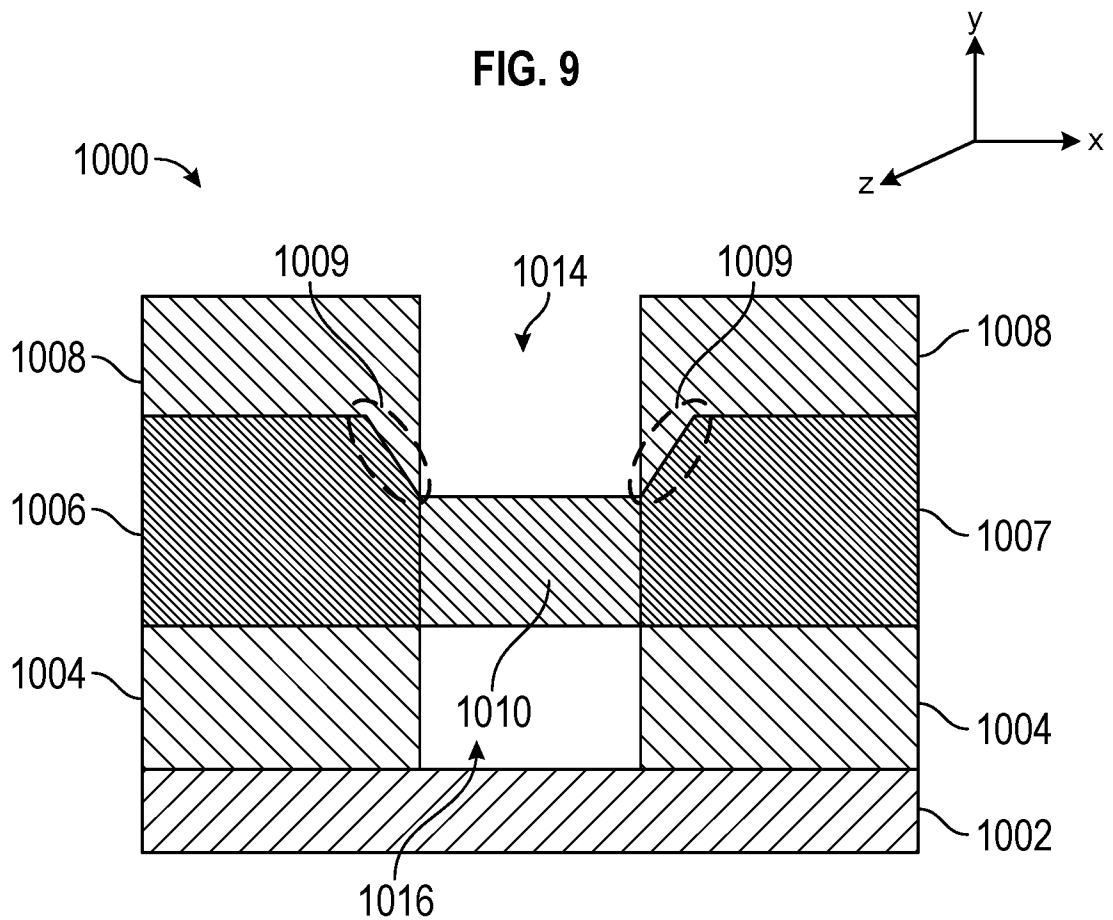


FIG. 10

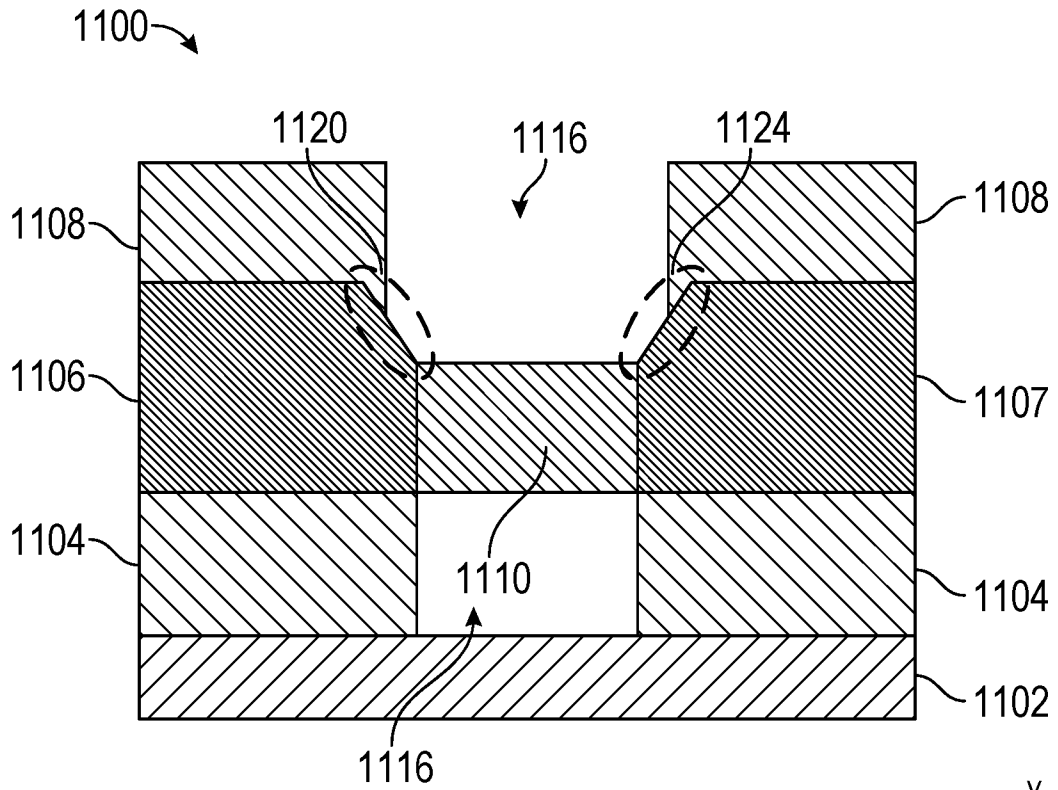


FIG. 11

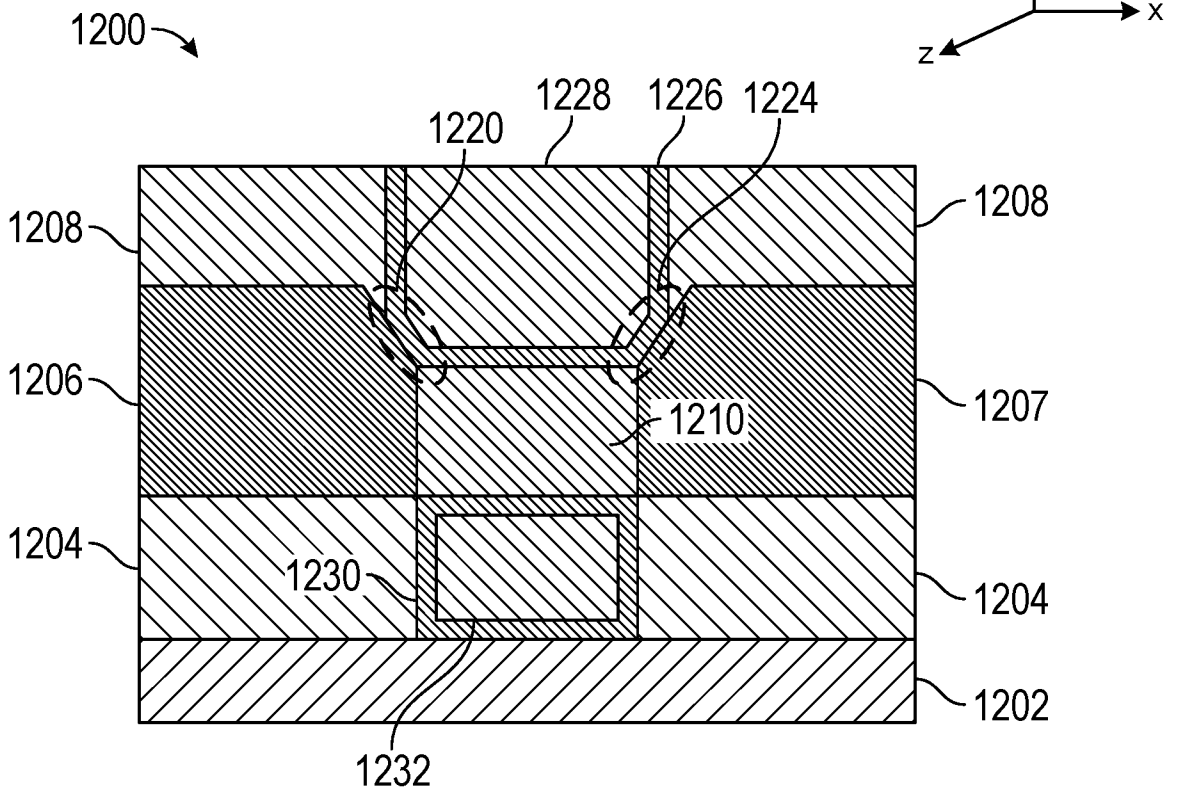


FIG. 12A

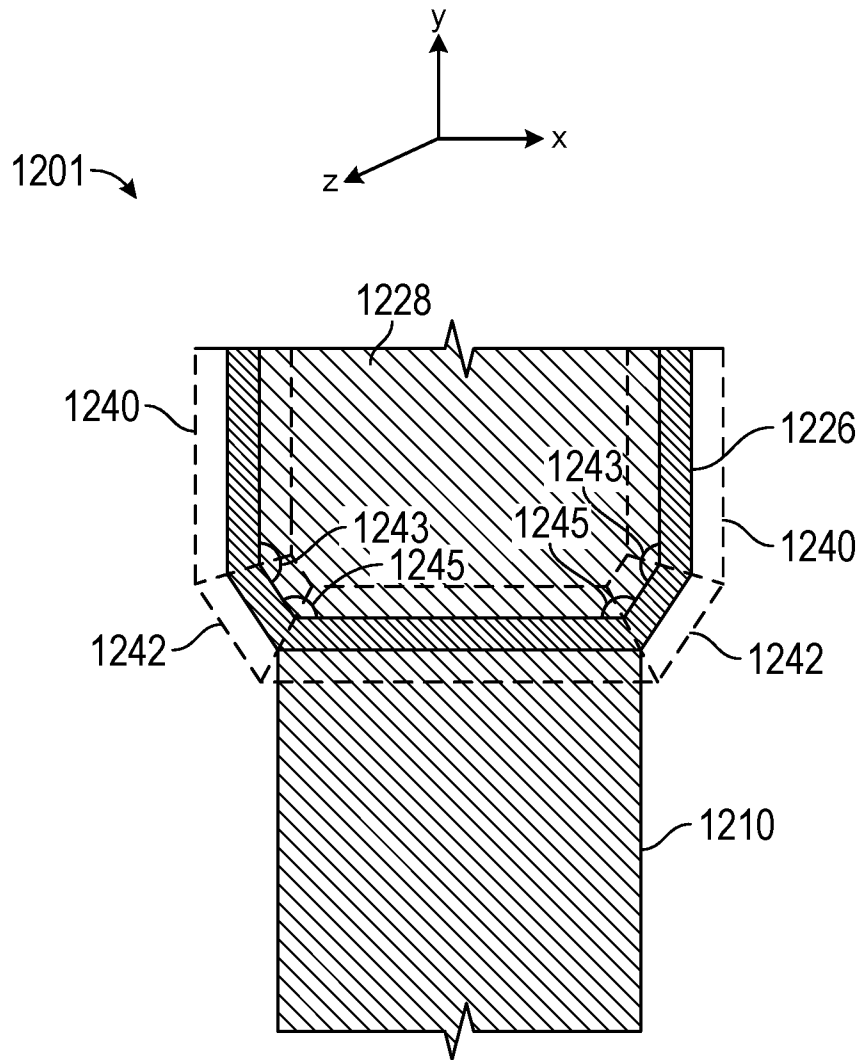


FIG. 12B

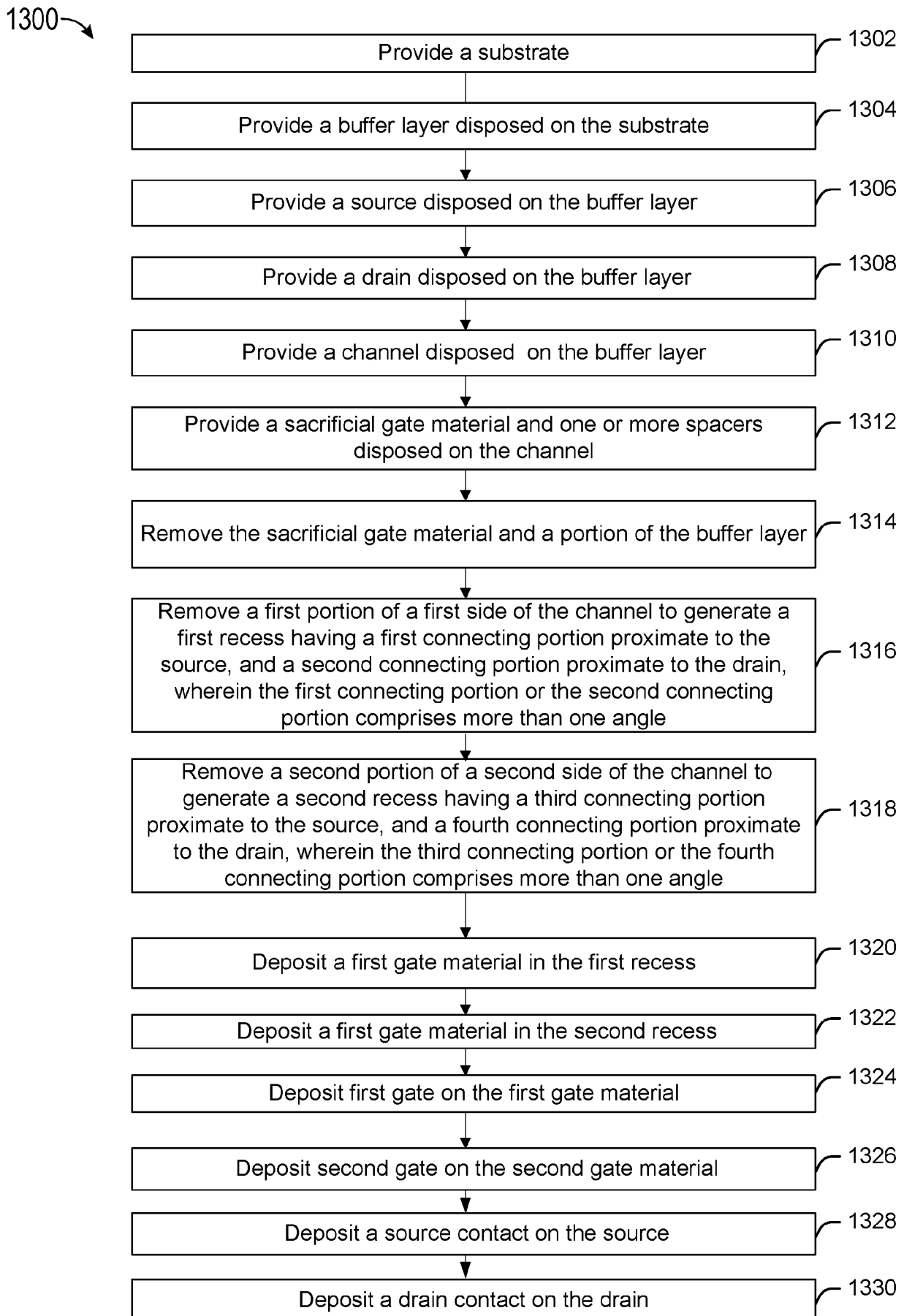


FIG. 13

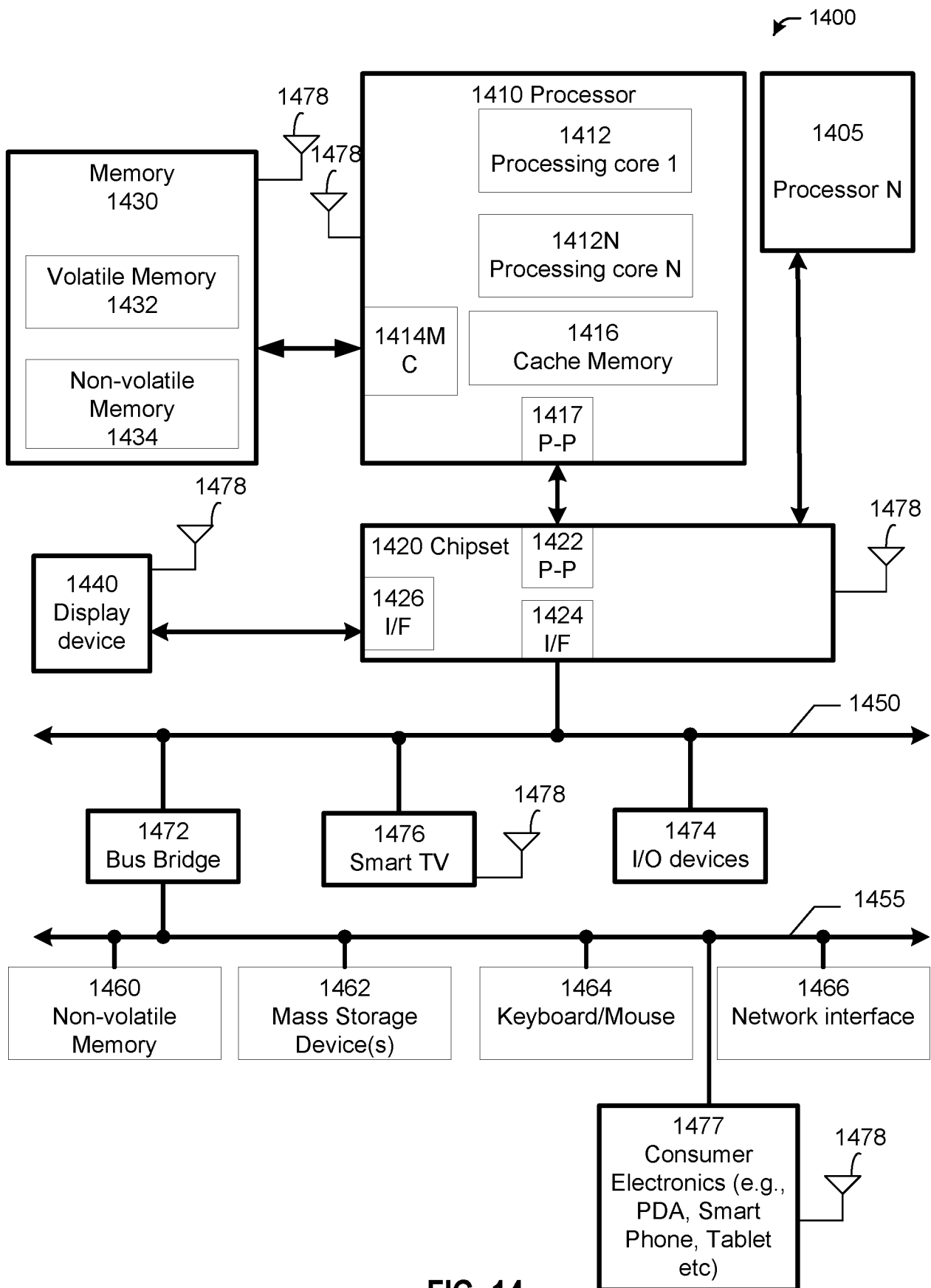


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/025610**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/423(2006.01)i, H01L 21/28(2006.01)i, H01L 29/66(2006.01)i, H01L 29/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/423; H01L 29/778; H01L 21/36; H01J 19/28; H01L 29/78; H01L 21/338; H01J 21/06; H01L 29/16; H01L 29/161; H01L 29/812; H01L 21/28; H01L 29/66; H01L 29/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, vertical, gate, buffer, source, drain, channel, angle, recess, facet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0181549 A1 (JEFFREY B. JOHNSON et al.) 19 July 2012 See paragraphs 16-21, claims 1-20 and figures 1-7.	1-23
A	US 2015-0279607 A1 (SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION) 01 October 2015 See paragraphs 73-133, claims 1-20 and figures 1A-17B.	1-23
A	US 2009-0267078 A1 (UMESH MISHRA et al.) 29 October 2009 See paragraphs 34-64 and figures 2-7.	1-23
A	US 2014-0117379 A1 (HYUNDAI MOTOR COMPANY) 01 May 2014 See paragraphs 29-48 and figures 1-9.	1-23
A	JP 2000-138235 A (KYOCERA CORP.) 16 May 2000 See paragraphs 17-23 and figure 1.	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 December 2017 (27.12.2017)

Date of mailing of the international search report

27 December 2017 (27.12.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

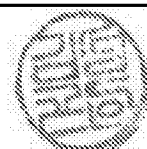


Facsimile No. +82-42-481-8578

Authorized officer

KIM, Sung Gon

Telephone No. +82-42-481-8746



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/025610

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0181549 A1	19/07/2012	CN 103314434 A CN 103314434 B DE 112012000510 B4 DE 112012000510 T5 GB 2500848 A GB 2500848 B JP 2014-506726 A US 2013-0140636 A1 US 8361847 B2 US 8921939 B2 WO 2012-099808 A1	18/09/2013 20/01/2016 18/06/2014 05/12/2013 02/10/2013 22/10/2014 17/03/2014 06/06/2013 29/01/2013 30/12/2014 26/07/2012
US 2015-0279607 A1	01/10/2015	CN 104979388 A US 9715987 B2	14/10/2015 25/07/2017
US 2009-0267078 A1	29/10/2009	CN 102017160 A CN 102017160 B TW 201010076 A TW I509794 B US 2013-0316502 A1 US 2014-0361309 A1 US 2016-0071951 A1 US 2016-0359030 A1 US 8519438 B2 US 8841702 B2 US 9196716 B2 US 9437708 B2 WO 2009-132039 A2 WO 2009-132039 A3	13/04/2011 08/05/2013 01/03/2010 21/11/2015 28/11/2013 11/12/2014 10/03/2016 08/12/2016 27/08/2013 23/09/2014 24/11/2015 06/09/2016 29/10/2009 25/02/2010
US 2014-0117379 A1	01/05/2014	CN 103811350 A DE 102012113217 A1 KR 10-1382328 B1	21/05/2014 08/05/2014 08/04/2014
JP 2000-138235 A	16/05/2000	JP 3488833 B2	19/01/2004