(71) **Applicants and**
(72) **Inventors: RAJAN, Suresh, Natarajan** [US/US]; 3284 Isadora Drive, San Jose, CA 95132 (US). **SMITH, Michael, John, Sebastian** [US/US]; 825 Ilima Court, Palo Alto, CA 94306 (US). **SCHAKEL, Keith, R.** [US/US]; 6238 Running Springs Rd., San Jose, CA 95135 (US). **WANG, David, T.** [US/US]; 1039 Coleman Rd. Apt. 6302, San Jose, CA 95123 (US). **WEBER, Frederick, Daniel** [US/US]; 1137 Settle Ave., San Jose, CA 95125 (US).

(74) **Agents: KOTAB, Dominic, M.** et al; Zilka-Kotab, PC, P.O. Box 721 120, San Jose, California 95172-1 120 (US).

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(54) **Title:** MEMORY CIRCUIT SYSTEM AND METHOD
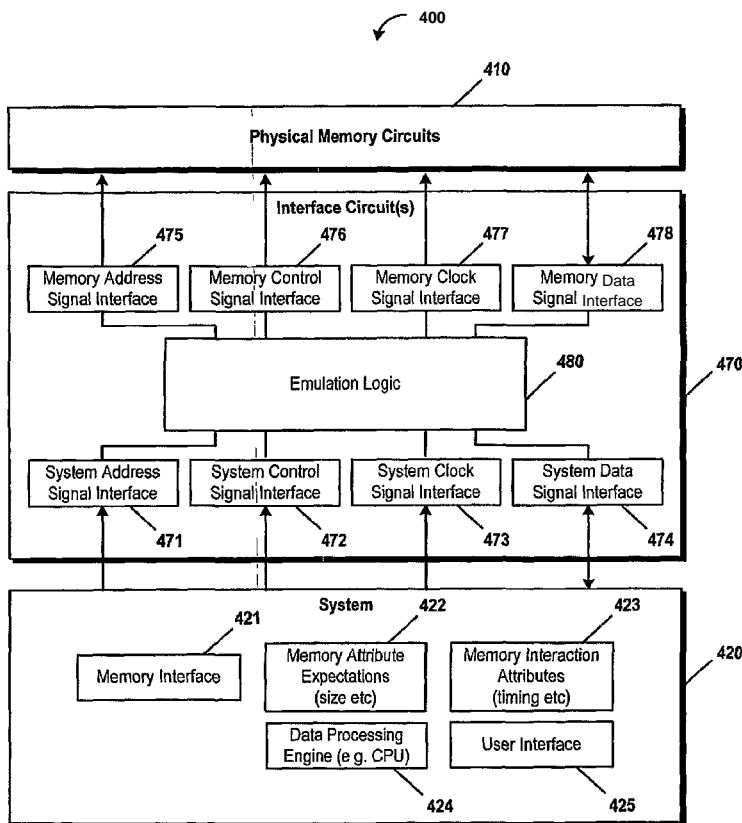
(57) **Abstract:** A memory circuit system and method are provided. In one embodiment, an interface circuit is capable of communication with a plurality of memory circuits and a system. In use, the interface circuit is operable to interface the memory circuits and the system for reducing command scheduling constraints of the memory circuits. In another embodiment, an interface circuit is capable of communication with a plurality of memory circuits and a system. In use, the interface circuit is operable to translate an address associated with a command communicated between the system and the memory circuits. In yet another embodiment, at least one memory stack comprises a plurality of DRAM integrated circuits. Further, a buffer circuit, coupled to a host system, is utilized for interfacing the memory stack to the host system for transforming one or more physical parameters between the DRAM integrated circuits and the host system. In still yet another embodiment, at least one memory stack comprises a plurality of DRAM integrated circuits. Further, an interface circuit, coupled to a host system, is utilized for interfacing the memory stack to the host system so to operate the memory stack as a single DRAM integrated circuit.

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