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(54) IMPROVEMENTS IN OR RELATING TO CIRCUIT ARRANGEMENTS INCLUDING I²L GATES

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to circuit arrangements including I²L gates.

I²L gates (integrated injection logic) are known. The cut-off frequency of I²L gates can be controlled over many orders of magnitude by the current consumption of the gates. In known circuits the problem of operating the gates with mutually different currents is overcome by means of a differing geometry of the I²L gates, and by integrating series resistances.

One object of the present invention consists in providing an arrangement for supplying a first group of I²L gates with a first current, and a second group of I²L gates with a different current, in which I²L gates arranged on a chip can be supplied by one single, external voltage supply.

The invention consists in a circuit arrangement including first and second groups of I²L gates, wherein a first injector path is connected to an external supply voltage source, wherein this first injector path is connected to the injectors of the I²L gates in said first group, wherein the first injector path is connected to the injecting emitter of a CHIL gate, wherein the first input of this CHIL gate is connected to a second injector path, and wherein this second injector path is connected to the injectors of the I²L gates in said second group.

An advantage of the invention consists in that it obviates the need for the groups of I²L gates which are to be supplied with mutually different currents to possess mutually different geometries, and that no integration of series resistances is necessary.

The invention will now be described with reference to the drawings, in which:—

Figure 1 is a schematic circuit diagram of an exemplary arrangement according to the invention, in which I²L gates having a low current consumption are supplied via the current-hogging input of a CHIL gate;

Figure 2 is a plan view of an exemplary arrangement of the embodiment shown in Figure 1; and

Figure 3 schematically illustrates a cross-section through a CHIL gate of the Figure 1 embodiment.

By using so-called CHIL gates (current-hogging-injection-logic) as intermediate gates, individual circuit components can be supplied with differing currents. In this case a group of I²L gates in circuit components having a low current consumption are connected by their injectors, via an injector path, to the current-hogging-input of a CHIL gate. Current amplifier stages provided with CHIL input gates facilitate the transfer of signals into circuit components having a higher current consumption. The publication "IEEE Journal of Solid-State Circuits", Vol. SC—10, No. 5, October, 1975, pages 348 to 352 describes CHIL gates and their function.

Figure 1 schematically illustrates the circuit diagram of an exemplary arrangement comprising two groups of I²L gates. For example, individual I²L gates 1 and 2 constitute a first group and gates 4 and 5 constitute a second group. The inputs of these gates are referenced 11, 21, 41 and 51, the gate outputs are referenced 12 to 14, 22 to 24, 42 to 44 and 52 to 54, and the injectors of these gates are referenced 15, 25, 45 and 55.

The I²L gates 1, 2, 4 and 5, which are known *per se*, consist, for example, of lateral pnp-transistors 16, 26, 46 and 56, and of vertical npn-transistors 17, 27, 47 and 57 having multiple collectors.

In Figure 1 the injectors 15 and 25 of the I²L gates 1 and 2 are connected to one another via the injector path 61. The

injectors of the I^2L gates 4 and 5 are connected to one another via the injector path 62. In respect of the I^2L gates 1 and 2 which are directly connected to the injector path 61, to which the external voltage supply V_s is connected, the current per gate 1, 2 amounts to I_v, assuming that a width 19 (Figure 2) of the gates 1 and 2 corresponds to one length unit. The injector path 61 is connected to the injecting emitter 35 of a CHIL gate 3. CHIL gates of this type are described, for example, in "IEEE Journal of Solid-State Circuits", Vol. SC—10, No. 5 October 1975. The CHIL gate 3 possesses the injecting emitter 35, at least two inputs 31 and 36, and outputs 32 to 34. Figure 3 schematically illustrates a cross-section through a CHIL gate of this type. Details in Figure 3 which have already been described in association with Figure 1 bear corresponding references.

In the following we shall briefly describe the function of the CHIL gate 3, which consists, for example, of the lateral pnp-transistor 37 and the vertical npn-transistor 39. The injecting emitter 35 is supplied with a current via the injector path 61. As a result, minority carriers emanating from said emitter are injected into the epitaxial layer 101. If the diffusion length of these minority carriers is considerably greater than the distance between the injector diffusion zone 35 and the input diffusion zone 36, most of these minority charge carriers will reach the input diffusion zone 36, and supply the latter, and the associated injector path 62, with current. When the input diffusion zone 36 and the associated injector path 62 have become charged, minority charge carriers flow out therefrom to the base diffusion zone 38 and to further interlying input diffusion zones. The output diffusion zones 32 to 34 are arranged in the diffusion zone 38. These output diffusion zones represent multiple-collectors of the vertical transistor 39. The zone 10 represents the emitter of the vertical transistor 39 and the base terminal of the lateral transistor 37.

The input 36 of the CHIL-arrangement 3 is connected to the injector path 62 which, for example, is connected to the injectors 45 and 55 of the I^2L gates 4 and 5. Here this input 36 of the CHIL gate 3 feeds the injector path 62 with current. Assuming that n gates are connected to the injector path 62, for the current for gate we have

$$I_v' = \frac{A.Iv}{n},$$

if the width of the gates again corresponds to one length unit. In the above formula, A represents the coupling factor which corresponds approximately to the current amplification of the lateral pnp transistor 37 of the CHIL gate 3 between the injector 35 and the input 36. Here saturation effects are negligible. The base of the lateral pnp transistor 37 is connected to earth. I_v' is the current flowing through the injector path 61 in respect of each gate. By varying the width of the gate 3 and the number n of the connected gates, it is possible to vary the current I_v'.

By providing a series connection of such couplings, it is advantageously possible to set up current differences of several orders of magnitude.

Figure 2 is a plan view of the arrangement corresponding to Figure 1. Details of Figure 2 which have already been described in association with Figures 1 and 3 bear the corresponding references.

The arrangement corresponding to the invention is advantageously arranged in a n^+– doped silicon layer 10 and n-conducting, epitaxial layers 101 arranged thereupon.

Our co-pending United Kingdom Patent Application No. 22712/77 of even date, (Specification No. 1577192) refers to other I^2L amplifier stage circuits.

WHAT WE CLAIM IS:—

1. A circuit arrangement including first and second groups of I^2L gates, wherein a first injector path is connected to an external supply voltage source, wherein this first injector path is connected to the injectors of the I^2L gates in said first group, wherein the first injector path is connected to the injecting emitter of a CHIL gate, wherein the first input of this CHIL gate is connected to a second injector path, and wherein this second injector path is connected to the injectors of the I^2L gates in said second group.

2. An arrangement as claimed in Claim 1, wherein the second injector path is connected to the injecting emitter of a further CHIL gate, wherein the first input of said further CHIL gate is connected to a further injector path, and wherein the further injector path is connected to the injectors of a third group of I^2L gates.

3. An arrangement, as claimed in Claim 1 or Claim 2, wherein the CHIL gate, or each of said CHIL gates, consists of a lateral pnp transistor and a vertical npn transistor.

4. An arrangement as claimed in any preceding Claim, wherein each of the I^2L gates consists of a lateral pnp transistor and a vertical npn transistor.

5. An arrangement as claimed in any

preceding Claim, formed in a n+ doped silicon layer, and a n– conducting, epitaxial layer arranged thereupon.

6. A circuit arrangement substantially as described with reference to Figures 1, 2 and 3.

For the Applicants
G. F. REDFERN & CO.,
Marlborough Lodge,
14 Farncombe Road,
Worthing,
BN11 2BT.

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1577191 COMPLETE SPECIFICATION

2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

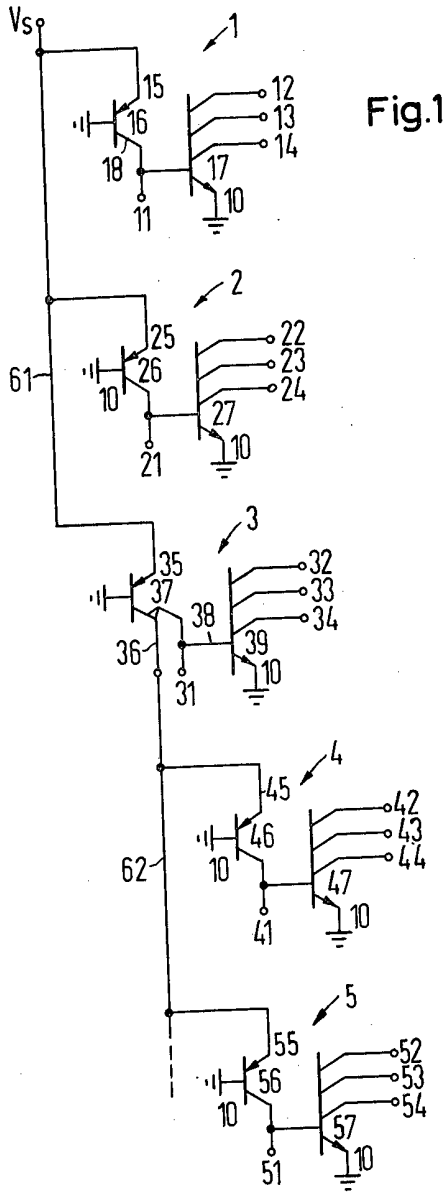

Fig.1

Fig.2

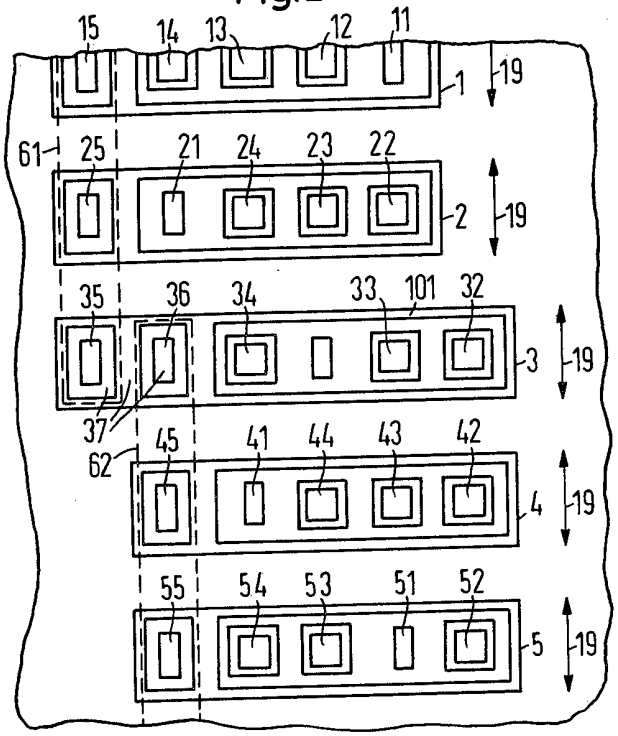
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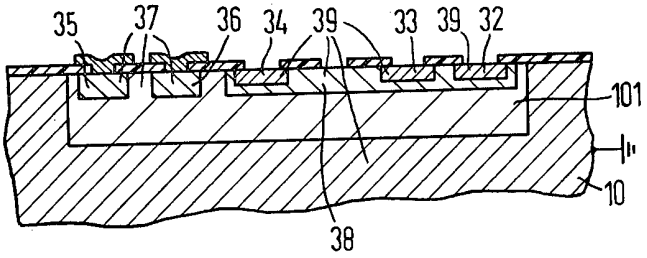
Fig.3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