



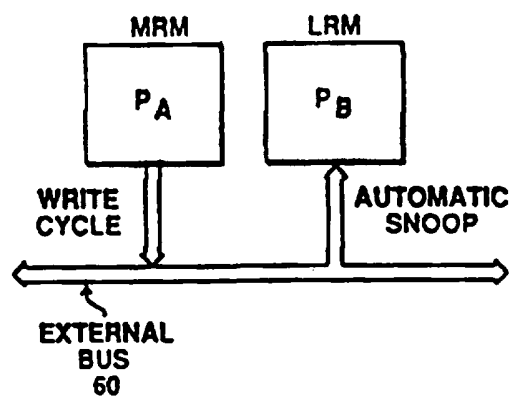
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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<p>(21) International Application Number: PCT/US95/16601</p> <p>(22) International Filing Date: 20 December 1995 (20.12.95)</p> <p>(30) Priority Data: 08/363,735                      23 December 1994 (23.12.94)      US</p> <p>(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).</p> <p>(72) Inventors: CARMEAN, Douglas, M.; 14815 S.W. Bonnie Brae, Beaverton, OR 97007 (US). CRAWFORD, John; 2754 Glorietta Circle, Santa Clara, CA 95051 (US).</p> <p>(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor &amp; Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).</p>		<p>(81) Designated States: AL, AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).</p> <p><b>Published</b> <i>With international search report.</i></p>

(54) Title: A CACHE COHERENT MULTIPROCESSING COMPUTER SYSTEM WITH REDUCED POWER OPERATING FEATURES

## (57) Abstract

A multiprocessing system maintains cache coherency during a reduced power mode of operation. The multiprocessing system has a first processor and a second processor (20) coupled to the external bus (60) to perform data transactions with the main memory. During the reduced power mode of operation, the internal clock signal (ICLK) of the second processor (20) is decoupled from a portion of the internal logic of the second processor (20) while the internal clock signal (CLK) remains coupled to a portion of the internal logic of the second processor (20) that is used to monitor and respond to the traffic on the external bus (60) to maintain cache coherency. During the reduced power mode of operation, the second processor (20) continues to perform snoop and write back processes to maintain a cache coherent multiprocessor system.



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**A CACHE COHERENT MULTIPROCESSING COMPUTER  
SYSTEM  
WITH REDUCED POWER OPERATING FEATURES**

**FIELD OF THE INVENTION**

The present invention relates generally to the field of microprocessor-based computer systems; more particularly, to multiprocessor computer systems which include features for regulating power consumption.

**BACKGROUND OF THE INVENTION**

Advances in semiconductor processing technology have made it possible to compact the feature sizes of integrated circuits to allow more transistors to be fabricated on a single semiconductor substrate. For example, the most sophisticated microprocessors being manufactured today typically comprise a single integrated circuit (IC) made up of several million transistors. Although these astounding technological advances have made it possible to dramatically increase the performance and data handling capabilities of today's modern computer systems, these advances have come at the cost of increased power consumption. Increased power consumption, of course, means that there is more heat that must be dissipated from the IC.

Because excessive power consumption and heat dissipation is now a critical problem facing computer designers, various power-saving techniques have evolved for minimizing power supply current levels within computer systems. Many of these techniques adopt the strategy of powering down the microprocessor when not in use to conserve power. This approach, however, is not without drawbacks.

By way of example, a problem arises in multiprocessor (MP) computer systems which employ two or more processors that cooperate to complete system tasks. If one microprocessor has been powered-down (e.g., because its current tasks have been completed or it is

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otherwise inactive) another microprocessor in the system may continue to perform data transactions on the system bus. The problem is that some the bus transactions may attempt to read/write data stored in a modified state in a powered-down or otherwise inactive microprocessor. Unless there exists some mechanism for monitoring bus activity and updating shared memory locations, data coherency will be lost. Therefore, MP computer systems have a need for a mechanism which makes inactive processors both aware and responsive to bus activity that may attempt to access stale data.

As will be seen, the present invention provides a multiprocessing computer system in which individual processors monitor bus traffic to maintain cache coherency while operating in a reduced power mode. In accordance with the present invention, an inactive or powered-down processor responds to certain bus transactions by writing back modified data to the system bus in a reduced power mode of operation. In addition, the invention functions without latency or intervention from the operating system. Thus, the invention provides a totally transparent way of interacting with an external bus while minimizing power consumption.

**SUMMARY OF THE INVENTION**

A multiprocessor computer system is described as including a bus coupled to a main memory and also to first and second processors. The first and second processors are coupled to the bus for performing data transactions with the main memory. The second processor has a bus unit coupled to the bus, a local cache with an associated tag array, a phase-locked loop (PLL) for generating a clock signal, and a means for reducing a power consumption by decoupling the clock signal from a portion of the internal logic of the second microprocessor while the bus unit, PLL and associated tag array remain coupled to the clock signal. The bus unit of the second microprocessor further includes a means for snooping the bus when in a reduced power mode of operation and means for signaling to the first microprocessor that a write cycle on the bus by the first microprocessor is to a modified cache line in the local cache of the second microprocessor.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be understood more fully from the detailed description which follows and from the accompanying drawings, which, however, should not be taken to limit the invention to the specific embodiments shown, but rather are for explanation and understanding only.

**Figure 1** is a generalized block diagram of a microprocessor operating in accordance with the present invention.

**Figure 2** is a diagram showing state transitions for the clock control architecture utilized in one embodiment of the present invention.

**Figure 3** is a timing diagram illustrating the operation of one aspect of the present invention.

**Figures 4A - 4D** are a set of diagrams illustrating various exemplary operations performed in one embodiment of the present invention.

**Figure 5** illustrates a test register which includes bits allowing software to disable certain features in accordance with the present invention.

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## DETAILED DESCRIPTION

The present invention is a multiprocessor computer system for maintaining cache coherency while minimizing power consumption. In the following description, numerous specific details are set forth, such as particular signals, protocol, device types, etc., to provide a thorough understanding of the present invention. It should be understood, however, that these specific details need not be used to practice the present invention. In other instances, well known structures, circuit blocks, and architectures have not been shown in detail to avoid unnecessarily obscuring the present invention.

Figure 1 is a block diagram of a microprocessor 20 which incorporates various features of the present invention. In one embodiment, processor 20 comprises an improvement of the commercially-available Pentium™ processor manufactured by Intel Corporation of Santa Clara, California. Although the present invention will be described in conjunction with the embodiment of Figure 1, it should be understood that the broad concept of the present invention is applicable to many different types of computer systems -- covering microprocessors that are compatible with the Pentium processor, or which utilize different data processor architectures.

Microprocessor 20 includes a phase-locked loop (PLL) circuit 30 that provides an internal clock signal (ICLK) coupled along line 46 to the various functional unit blocks of the integrated circuit. For example, the ICLK signal present on line 46 is shown in Figure 1 coupled to a majority of the internal logic of the IC, including instruction cache 25, data cache 26, control ROM 21, and the internal logic which comprises the integer unit 22 and floating point (FP) unit 23 of the processor. The ICLK signal is also coupled to a portion of the interrupt logic unit 29. Instruction cache 25, data cache 26 and bus unit 40 are each coupled to a 64-bit data bus 42 and 32-bit address bus 43.

In addition to the ICLK signal, PLL circuit 30 also provides a second clock signal (CLK) that is coupled along line 45 to the tag comparison arrays of instruction cache 25 and data cache 26. The CLK

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signal on line 45 is also coupled to a portion of interrupt logic unit 29 and bus unit 40. (The distinction between the ICLK and CLK clock signals is discussed in more detail below.) During normal operation microprocessor 20 operates with a clock (i.e., ICLK and CLK) frequency of approximately 100 MHz. Variations of processor 20 may also support a variety of core/bus ratios. For instance, in alternative implementations bus frequencies of 50 MHz and 60 MHz are supported.

In one embodiment, bus unit 40 and interrupt logic unit 29 include logic circuitry enabling microprocessor 20 to be utilized in a MP system. By way of example, bus cycles issued and received by bus unit 40, as well as interrupt signals received and provided by interrupt logic unit 29, are compatible with the well-known Pentium™ processor. Microprocessor 20 also includes logic that maintains cache consistency and which arbitrates for an external bus.

In one embodiment, microprocessor 20 also includes power management features which allow the processor to enter a reduced power dissipation state (i.e., a HALT or STANDBY mode of operation). When functioning in a normal mode of operation at peak power, microprocessor 20 may dissipate as much as 10 watts; in a HALT or STANDBY mode of operation, as little as 700 milliwatts of power is consumed. One of the ways in which microprocessor 20 implements power management functions, as well as operating system independent functions, is by a system management mode of operation. System management mode (SMM) consists of an interrupt (SMI), an alternative address space and an instruction (SRET). The system management interrupt causes a system management interrupt request to be latched within logic unit 29. When the latch SMI# is recognized on an instruction boundary, microprocessor 20 enters SMM.

With continuing reference to Figure 1, in one implementation microprocessor 20 includes an external pin (labeled STPCLK#) and associated circuitry that can be used to regulate the power of the microprocessor. The STPCLK# pin is disclosed more fully in co-pending application entitled, "Method And Apparatus For Asynchronously Stopping The Clock In A Processor", Serial No. 07/970,576, filed

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11/3/92, herein incorporated by reference, and which application is assigned to the assignee of the present invention. The STPCLK# pin provides a level-sensitive SMI that places the processor in a low-power STANDBY state. In accordance with the present invention, microprocessor 20 responds to both private (i.e., ADS#) and external snoop (i.e., EADS#) requests while in a STANDBY mode of operation.

Processor 20 also supports a mechanism referred to as AUTO\_HALT that places the processor in a reduced power mode of operation every time a HALT instruction is executed. Microprocessor 20 responds to all stop break events including private snoops and inter-processor interrupt events that are generated while the processor is in a reduced power state (without the STPCLK# pin asserted).

When microprocessor 20 functions in a normal mode of operation both clock lines 46 (ICLK) and 45 (CLK) are enabled such that the internal core clock signal is provided to all units of the integrated circuit. When the processor enters a low-power or STANDBY state as a result of the assertion of either the STPCLK# pin or the execution of a HALT instruction, the internal clock signal (ICLK) on line 46 is disabled. It should be understood, however, that disabling line 46 does not alter the continuous functioning of PLL circuit 30. In other words, PLL 30 continues to generate an internal core CLK frequency on line 45 coupled to certain portions of microprocessor 20. The portions of microprocessor 20 which remain operational (i.e., activated by CLK) include PLL 30, the tag comparison arrays of cache units 25 and 26, a portion of interrupt logic unit 29 and bus unit 40. In accordance with the present invention, providing power to the selected portions of microprocessor 20 allows the processor to monitor and respond to external bus traffic for the purpose of maintaining cache coherency in MP systems. That is, bus arbitration and cache coherency mechanisms are intentionally kept active in a reduced power mode of operation.

Referring now to Figure 2, there is shown a state diagram illustrating certain key features of one embodiment of the present invention. In normal operating conditions, state 51, microprocessor 20 is active executing instructions. This represents the processor's full power

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state in which both the ICLK and CLK signals are coupled to all portions of the IC's internal logic.

The STOP\_GRANT state, represented by block 53, can be entered by asserting the external STPCLK# pin of microprocessor 20. In the STOP\_GRANT state the integrated circuit operates in a reduced power consumption mode wherein most of the internal functional units of the processor are deactivated (i.e., ICLK off). On the other hand, bus unit 40, the tag arrays of caches 25 and 26, PLL 30 and portions of the interrupt logic unit 29 remain active. Once the STOP\_GRANT bus cycle has been placed on the bus and the BRDY# signal is returned, the processor is in the STOP\_GRANT state. Practitioners in the art understand the BRDY# signal to indicate that the external system has presented valid data on the data pins in response to a read, or that the external system (e.g., main memory, other processor, etc.) has accepted the processor data in response to a write request. In one embodiment, the processor returns to the normal execution state approximately ten clock periods after STPCLK# has been deasserted. A RESET also brings the processor out of the STOP\_GRANT state, returning it to the normal state.

Processor 20 recognizes inputs to bus unit 40 for maintaining cache coherency (e.g., invalidation's and external snoops) by monitoring bus traffic when in a reduced power mode of operation. For example, while in the STOP\_GRANT state, the processor latches transitions on external interrupt signals (e.g., SMI#, NMI, INTR, FLUSH#, R/S# and INIT). All of these interrupts are taken after the de-assertion of STPCLK#; that is, upon re-entering the normal state.

The AUTO\_HALT state, denoted by block 50 in Figure 2, is entered whenever the HALT instruction is executed. In AUTO\_HALT state the internal clock (ICLK) is decoupled from a majority of the internal logic while the continuous clock signal CLK keeps selected functional units of the chip operational. Upon the occurrence of the INTR, NMI, SMI#, RESET or INIT, the processor transitions back to the normal operating state, i.e., state 51. As explained earlier, the AUTO\_HALT state results in a significant reduction in power

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consumption by stopping the clock signal to most of the internal logic of the processor. The bus unit 40, PLL 30, tag arrays, and interrupt logic remains active to support snoops and to allow fast restart. Any external interrupt causes the processor to exit AUTO\_HALT state 50 and return to normal operating state 51. When operating in AUTO\_HALT state 50, the assertion of a FLUSH# signal (active low) causes the flush event to be latched and acted upon as illustrated by block 55. For the embodiment described, the FLUSH# signal forces the processor to write-back all modified lines in data cache 26 and invalidate its internal caches. A FLUSH acknowledge special signal is then generated by the processor indicating completion of the write-back and invalidation operations.

Assertion of the R/S# input (active low) causes the processor to stop normal execution and place it in an IDLE state. Figure 2 illustrates a R/S# event causing a transition from AUTO\_HALT state 50 to enter PROBE\_MODE state 56. The R/S# pin is provided for use with debugging of the processor in conjunction with a special debug port. A high-to-low transition of the R/S# pin interrupts the processor and causes it to stop execution at the next instruction boundary. De-assertion of the R/S# pin causes a transition from PROBE\_MODE state 56 back to AUTO\_HALT state 50.

Figure 2 also includes state 52 which represents the snooping ability of the processor when operating in a reduced power mode, as would be the case following the assertion of the STPCLK# pin or the execution of a HALT instruction. Even though power dissipation is reduced in either of these two states, the processor continues to drive bus signals via unit 40, and the processor's internal machine state is preserved. Both private and inter-processor snoops are supported for both cache invalidation and write-back cycles. Power consumption increases for a short period if the snoop requires a write-back cycle to be run. In accordance with the present invention snoops are handled completely by hardware without the need for microcode intervention.

In both the STOP\_GRANT and AUTO\_HALT states, microprocessor 20 supports snoops -- including private and inter-

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processor snoops -- by keeping the cache units tag comparison logic enabled by CLK. This is illustrated in Figure 1, wherein the CLK signal on line 45 is coupled to the tag comparison logic of caches 25 and 26. On the other hand, the ICLK signal is disabled to the data array portions of the caches to minimize power consumption. When a snoop occurs, the MESI (i.e., Modified, Exclusive, Shared, Invalid) cache protocol bits are updated when the need arises. Portions of the processor (e.g., at least the data cache, associated cache control logic, and buses between the data cache and bus interface) other than the tag arrays are awakened only if a write-back cycle is required. In an alternative embodiment, more aggressive power saving may be achieved by disabling the tag comparison logic in certain situations, e.g., all the cache entries are invalid, or to power down the tag arrays until a snoopable transaction has been detected then provide a slightly increased power state to allow the tags to perform the snoop operation.

Note that Figures 1-4 illustrate only one exemplary embodiment of the present invention; however, more complex implementations are possible to provide a variety of power saving techniques involving a variety of different clocking schemes. The same is true with respect to the particular protocol employed once snooping has been performed. For instance, instead of having the first processor write back the data on the system bus, the first processor might absorb the write and keep the dirty line. Thus, practitioners in the art will appreciate the many different ways that the present invention may be implemented.

Figure 3 illustrates a timing diagram showing the latency between a STPCLK# request and the STOP\_GRANT bus cycle. Note that for the illustrative embodiment, there is a delay of approximately ten clocks between the STPCLK# request and the STOP\_GRANT bus cycle. This latency is dependent upon the current instruction, the amount of data in the CPU write buffers, and system memory performance.

Data cache 26 of processor 20 utilizes the MESI protocol to enforce cache consistency. A line in the data cache can be in the Modified, Exclusive, Shared or Invalid state, whereas a line in instruction cache 25 can be either in the Valid or Invalid state. The

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present invention is directed to situations which can arise wherein two or more processors share common data in a computer system. The local caches of the processors may attempt to cache data whenever possible. In one embodiment of processor 20, a private cache coherency mechanism is included to guarantee data consistency between processors. If any data is cached in one of the processors and another processor attempts to access the data, the processor containing the data notifies the requesting processor that it has cached the data. The state of the cache line and the processor containing the data will change depending upon the current state, and the type of request that the other processor has made.

In accordance with the present invention, the basic coherency mechanism requires that the processor not running a cycle and which does not own a bus (herein referred to as the least-recent bus master, or LRM) snoop all MRM bus activity (MRM referring to the most-recent bus master that owns the bus). The MRM processor running a bus cycle then watches the LRM processor for an indication that the data is contained in the LRM cache.

To better appreciate the operation of the present invention, consider the example arbitration interface exchange represented in Figures 4A - 4D. First, assume that processor PB operating in a reduced power mode or is idle on external bus 60. This would be the case if processor PB were in the AUTO\_HALT or STOP\_GRANT states. Also assume that processor PA in the computer system just ran a write cycle on external bus 60. Furthermore, assume that the write cycle on the bus is to a line that is in the modified (M) state in processor PB. This is the situation depicted in Figure 4A. Because both the bus unit and the internal interrupt and snoop logic remains active in processor PB-- despite the fact that most of the other internal logic is powered down -- processor PB automatically snoops external bus 60 to monitor the write cycle started by processor PA

Figure 4B shows processor PB indicating to processor PA that the write transaction has hit a Modified state cache line. This is done by asserting the PHITM# signal coupled to processor PA. Processor PB

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also asserts a private arbitration pin, BPBREQ#, to indicate that processor PB has generated a bus request (in this example, it is assumed that processor PA currently owns external bus 60). Note that a HITM# signal is also coupled to bus 60 to inhibit another bus master from accessing the data until after the line has been completely written back. Processor PA then completes the write cycle on external bus 60 as if processor PB did not exist.

The external snoop happens just as the write cycle completes on bus 60, but before processor PB has had a chance to write the modified data back to system memory. Figure 4B illustrates processor PB asserting the HITM# signal to inform the system that the snoop address is cached in the dual processor pair and is in a Modified state. The external snoop in this example hits the same line that caused the PHITM# signal to be asserted.

In Figure 4C, an arbitration exchange has occurred on external bus 60 and processor PB now owns the bus. At this point, processor PB writes back the M state line. From the viewpoint of the computer system, it appears as if a single processor was completing the snoop transaction. Note that in Figure 4C, two private arbitration pins coupled between the two processors are utilized to indicate that bus ownership has been granted to processor PB (or that processor PA requests ownership back after completion of the writeback operation).

Finally, in Figure 4D processor PA reruns the original write cycle after processor PB has granted the bus back to processor PA. It is important to recognize that processor PB has remained in a reduced power consumption mode of operation throughout the entire snoop and writeback processes represented by Figures 4A - 4D. This is a key feature of the present invention since it provides a considerable advantage in computer systems limited by power consumption requirements, but yet having a need for cache coherency.

With reference now to Figure 5, there is shown a specialized test register 12 which includes bits to allow software to disable certain features of microprocessor 20. For example, the AUTO\_HALT feature may be disabled to setting bit 6 in register 12 to a "1". In this setting, the

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execution of a HALT instruction does not disable the internal clock (ICLK) to any of the functional units of the processor. In one embodiment, the AUTO\_HALT feature is enabled by default, i.e., bit 6 in register 12 is set to a "0" after RESET.

Other features which are controlled by software via test register 12 include advanced programmable interrupt controlling (APIC) for multiprocessor systems. In one embodiment of the present invention the processor incorporates an advanced processor SMI controller that supports interrupts in a complex, multiprocessor environment, as well as interrupts in a simple uniprocessor environment. The local interrupt controller module communicates with an I/O APIC module (such as part no. 8259A manufactured by Intel Corporation) over a 3-wire serial bus. When bit 4 of register 12 is set to a "1", the APIC feature is completely disabled. This means that the APIC circuitry cannot send or receive any interprocessor interrupts. Reads or writes to the APIC register space are sent through to the external bus. Dual processor arbitration hardware may also be disabled when bit 5 of register 12 is set. When this bit is set to a "1", the private dual processor features (e.g., PHIT#, PHITM#, PBREQ#, and PBGRNT# pins) are disabled as soon as the processor becomes the most recent bus master (MRM). If this bit is subsequently set to "0", then the DP features are re-enabled. Other features, which may be enabled/disabled by register 12, include SMM entry and exit messages (bit 7), and fast execution tracing messages (bit 8).

**CLAIMS**

What is claimed is:

1. A multiprocessor computer system comprising:
  - a bus;
  - a main memory coupled to the bus;
  - a first processor coupled to the bus for performing data transactions with the main memory;
  - a second processor having a bus unit coupled to the bus, a local cache with an associated tag array, a phase-locked loop (PLL) for generating a clock signal, and a means for reducing a power consumption by decoupling the clock signal from a portion of the internal logic of the second microprocessor while the bus unit, PLL and associated tag array remain coupled to the clock signal;
  - the bus unit of the second microprocessor further including means for snooping the bus when in a reduced power mode of operation and means for signaling to the first microprocessor that a write cycle on the bus by the first microprocessor is to a modified cache line in the local cache of the second microprocessor.
  
2. The multiprocessor computer system of claim 1 wherein the second microprocessor further comprises means for writing back the modified cache line to the main memory on the bus following completion of the write cycle of the second microprocessor.
  
3. The multiprocessor computer system of claim 2 wherein the first microprocessor further comprises means responsive to the signaling means of the first microprocessor for regenerating the write cycle after the second microprocessor completes write-back of the modified cache line.

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4. The multiprocessor computer system of claim 1 wherein the decoupling means comprises a microcoded halt instruction.
  
5. The multiprocessor computer system of claim 1 wherein the decoupling means comprises an external pin which, when asserted, causes decoupling of the clock signal from the portion of internal logic.
  
6. A multiprocessor computer system comprising:
  - an external bus;
  - first and second microprocessors coupled to the external bus;
  - an arbitration mechanism which allows the first and second microprocessor to arbitrate for ownership of the external bus;
  - an interrupt control unit coupled to the first and second microprocessors for controlling inter-processor interrupts;wherein the first microprocessor includes an instruction means for halting the clock signal to a majority of the internal logic while still providing the clock signal to at least a bus unit and tag array of a data cache, causing the first microprocessor to operate in a reduced power mode;
  - the first microprocessor also including a register having a first bit, the register being read/written by software such that when the first bit is set the reduced power mode is disabled from operation.
  
7. The multiprocessor computer system of claim 6 wherein the register further includes a second bit which, when set, disables the arbitration mechanism.

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8. The multiprocessor computer system of claim 7 wherein the register further includes a third bit which, when set, disables the interrupt control unit.

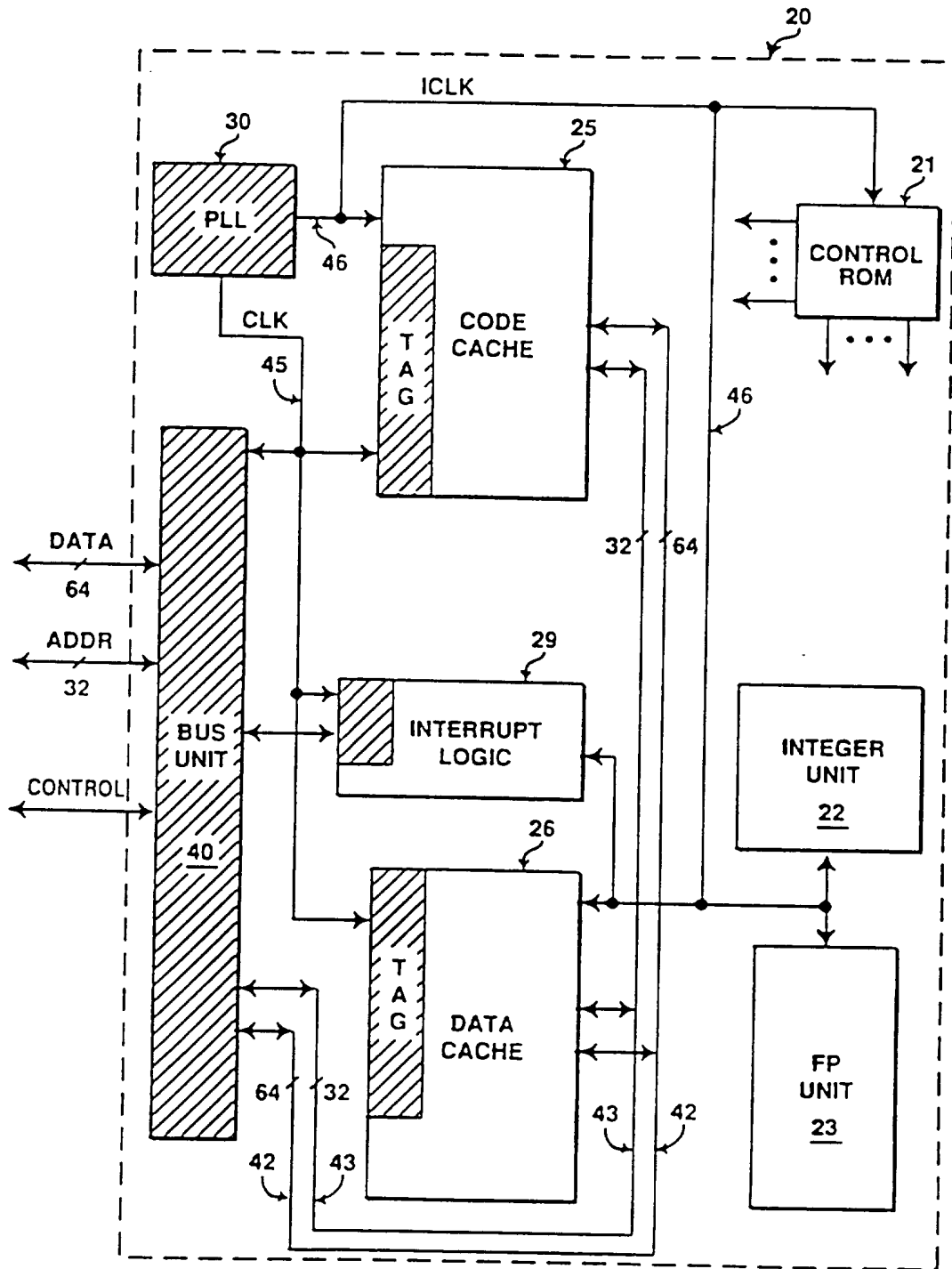


FIGURE 1

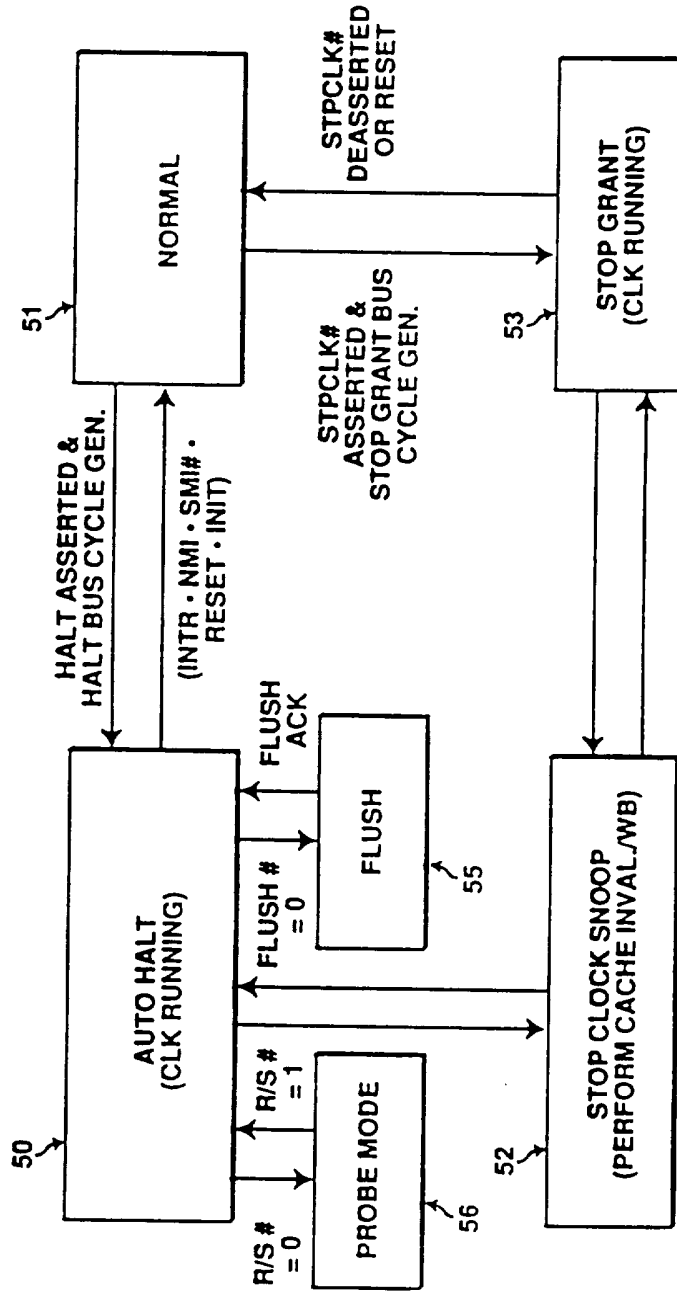


FIGURE 2

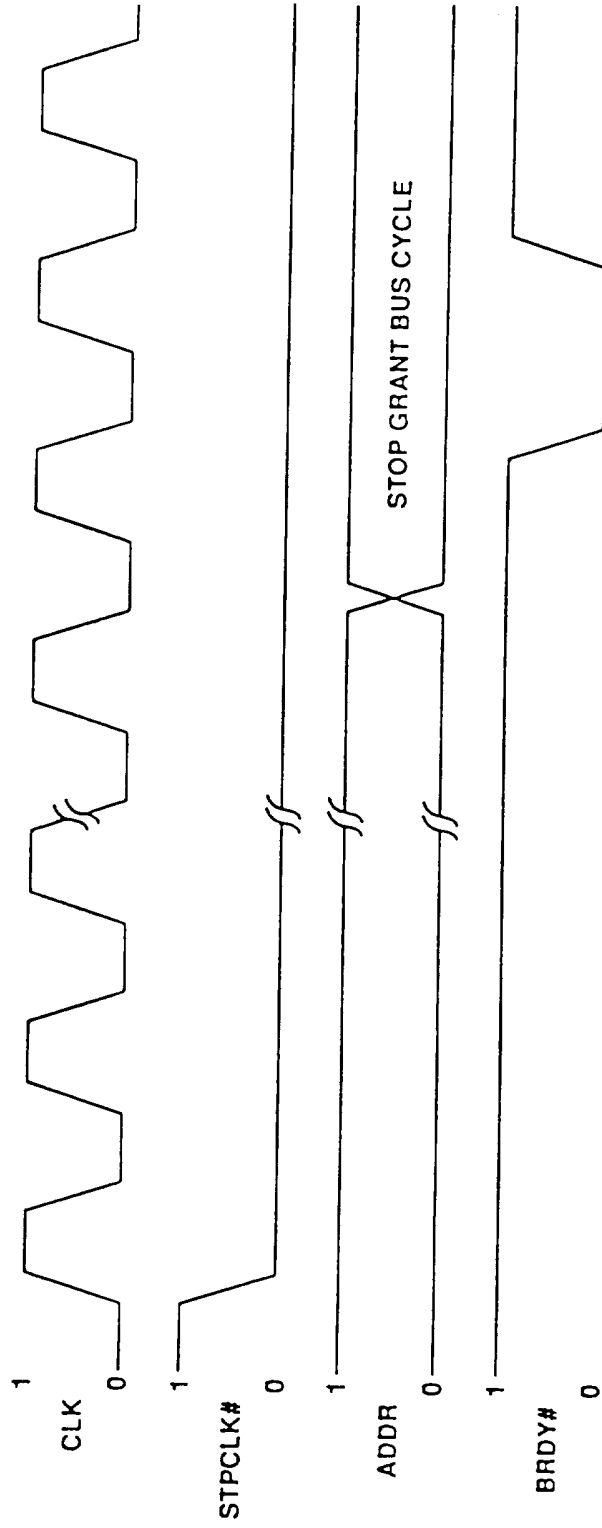


FIGURE 3

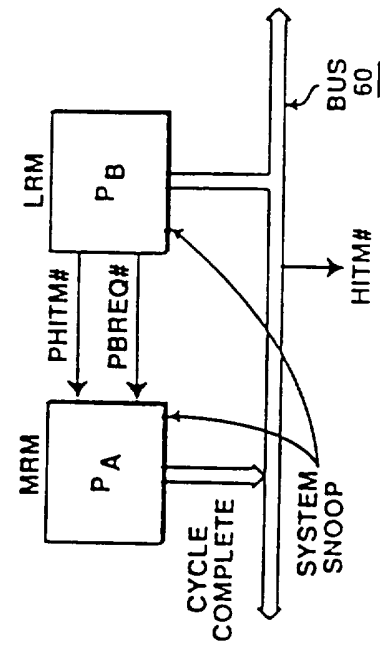


FIGURE 4b

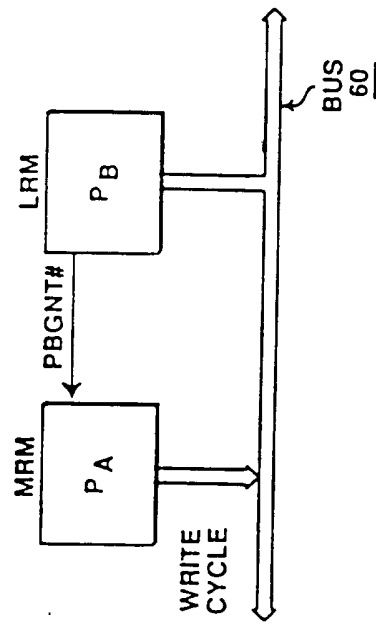


FIGURE 4d

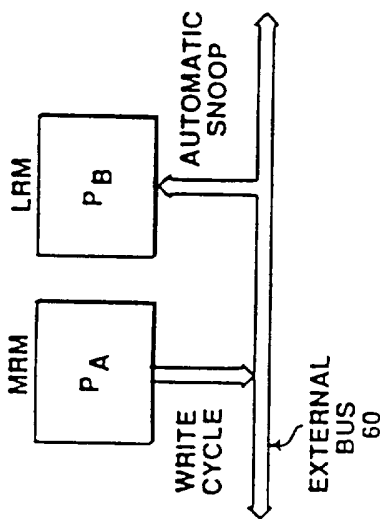


FIGURE 4a

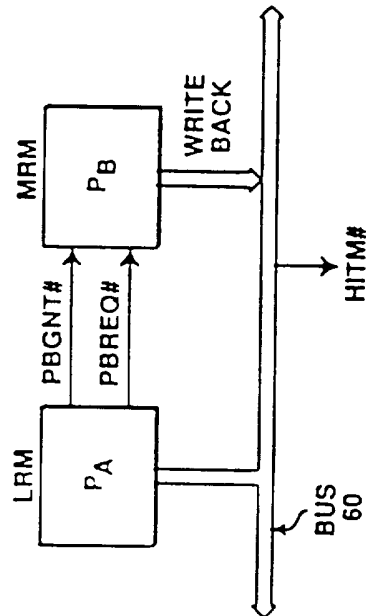


FIGURE 4c

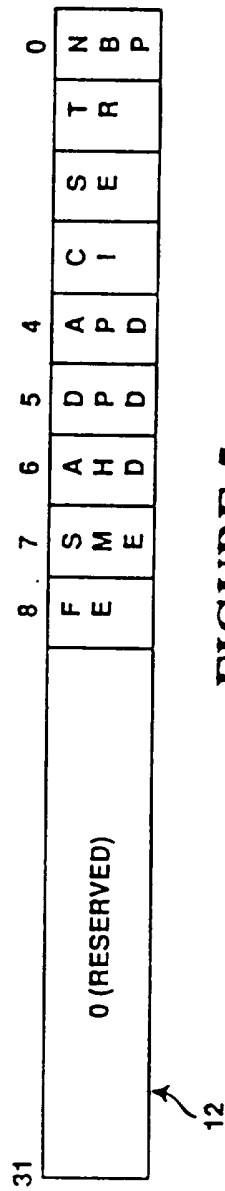


FIGURE 5

**INTERNATIONAL SEARCH REPORT**

Int...national application No.  
PCT/US95/16601

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) :G06F 1/32, 12/00, 13/00  
US CL :395/468, 750; 364/707; 365/226, 227

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/468, 750; 364/707; 365/226, 227

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS: multiprocess? or multi(w)process?, processor#, cache#, cache coherency, (low or reduced) power mode#, snoop?, write back or write-back

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,228,136 (SHIMIZU ET AL.) 13 July 1993, Fig. 1 and col. 2, line 62 - col. 3, line 48.	1-8
Y	US, A, 5,167,024 (SMITH ET AL.) 24 November 1992, Fig. 1 and col. 3, lines 13-56.	1-8
Y	US, A, 5,297,269 (DONALDSON ET AL.) 22 March 1994, Fig. 1 and col. 4, lines 5-62.	1-8
Y	US, A, 5,303,362 (BUTTS, JR. ET AL.) 12 April 1994, Fig. 1 and col. 4, line 57 - col. 6, line 6.	1-8
Y	US, A, 5,119,485 (LEDBETTER, JR. ET AL.) 02 June 1992, Fig. 1 and col. 3, line 65 - col. 4, line 32.	1-8

Further documents are listed in the continuation of Box C.  See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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*O* document referring to an oral disclosure, use, exhibition or other means	
*P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

02 APRIL 1996

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**INTERNATIONAL SEARCH REPORT**International application No.  
PCT/US95/16601**C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,287,525 (LUM ET AL.) 15 February 1994, col. 1, lines 39-55.	1-8
Y	US, A, 5,313,591 (AVERILL) 17 May 1994, Fig. 1 and col. 2, lines 40-51.	1-8