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(71) Applicant and
(72) Inventor: **BOGDAN, John, W.** [CA/CA]; 1210 Major Street, Ottawa, Ontario K2C 2S2 (CA).

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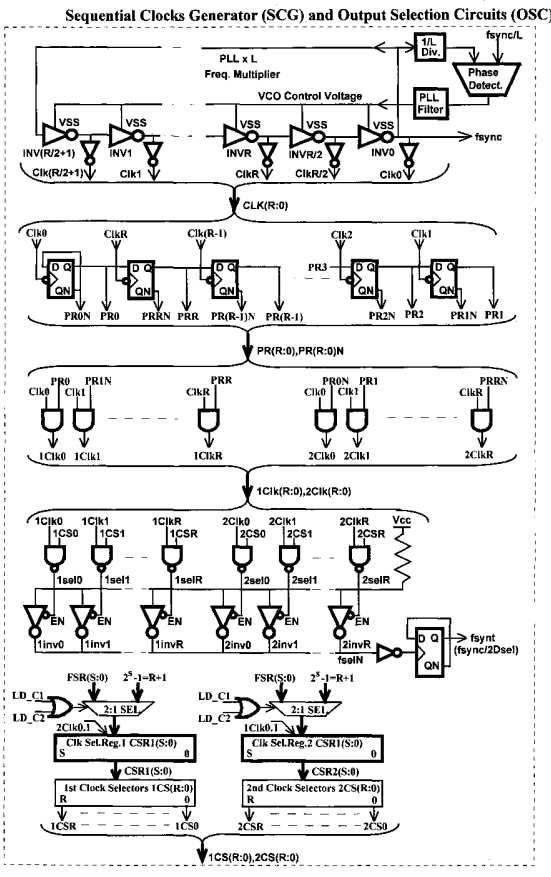
(54) **Title:** UNIVERSAL HETERODYNE TIMING SYSTEM



(57) **Abstract:** An inexpensive SOC providing programmable Heterodyne Timing System (HTS) for synthesizing output clock with indefinite frequency resolution from reference clocks of any frequency. The output clock has very low jitter independent of reference clock quality while output clock phase is controlled with resolution matching single gate delays. HTS allows frequency multiplications in continous range exceeding 50 000 which enables use of local oscillator below 32kHz for implementing free of phase transients programmable synthesis of GHz clocks.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Universal Heterodyne Timing System

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed: to a Heterodyne Timing System (HTS) implemented as an inexpensive SOC using low frequency and low cost local oscillator which may have frequency as low as 30kHz. The HTS enables fully programmable frequency and phase synthesis applicable in all communication systems and industrial control systems. In particular the HTS can implement universal synchronization functions for vast majority of communication systems.

The HTS provides integration of digital PLLs (DPLLs) an analog PLLs (APLLs) into an SOC hybrid PLL (HPLL).

The HTS includes invention of a Phase Synthesizer (PS) which can generate any even most irregular waveform having frequences ranging up to 1/2 of maximum clock frequency of used IC technology. The PS provides phase resolution matching single gate delay when producing waveform of any fully programmable shape and is free of any unpredictable transients.

Background Art

Prior art synchronization systems use frequency synthesizers introducing 10 times greater phase steps than this inventions phase synthesizer PS.

Said prior art frequency synthesizers are based on a direct digital frequency synthesis (DDFS) method, which modifies average frequency of an output clock by periodical removals of entire clock pulses from a uniform stream of fundamental clocks.

For economical and technical reasons their fundamental frequency is significantly lower than maximum clock frequency of IC process. Therefore their phase steps and resulting jitter are 10 times greater than those of said phase synthesizer using phase steps matching gate propagation delay.

Furthermore prior art frequency synthesizers produce unknown phase transients during their normal frequency switching operations.

Background art for this invention phase synthesizers is represented by the following documents:

D1 (US 5,257,294 invented by Fried at al);

D2 (US 6,046,644 invented by Pitot at al);

D3 (US 5,602, 884 invented by Kenny at al);

D4 (PCT/CA02/01873 invented by Bogdan).

Presently known frequency synthesizers have relatively high phase jitter levels, and provide limited resolution and accuracy of generated frequencies.

In addition to that, said present frequency synthesizers, including fractional synthesizers, do not allow phase control functions which would cover transitional phase conditions during frequency switching operations.

Therefore said frequency synthesizers can only provide a carrier frequency for data transmitters, but cannot implement an actual carrier phase or a frequency modulation with transmitted data.

Said deficiencies of the present frequency synthesizers degrade their performances in IF generation for data receivers as well, because they impair synthesizers ability to maintain an accurate locking to the received signal carrier frequency and phase.

On the other hand synthesized clock generators, which are designed for network synchronization systems, provide only limited ranges of frequency and phase modulations.

These limitations of said synthesized clock generators, make them less useful for data transmitters and/or receivers and complicate their applications in network synchronization systems as well.

There was a need for a phase/frequency synthesizer which will further reduce cost and improve performances of data transmitters, data receivers and synchronization systems: by generating very wide ranges of frequencies with very wide phase modulation ranges, by improving frequency and phase generation accuracy while reducing phase jitter, and by simplifying circuits used for said applications.

While D4 is unique in providing high resolution of phase/frequency synthesis, its phase modification steps are limited to <1/4 of minimum clock cycle of IC technology and steps

frequencies are limited by micro-controller cycle time.

The above D4 deficiencies are eliminated by this invention phase synthesizer enabling unlimited phase modification steps and extending steps frequencies up to ¼ of maximum clock frequency.

Background art for this invention network synchronizers is represented by the following documents:

D3 (US 5,602, 884 invented by Kenny at al);

D4 (PCT/CA02/01873 invented by Bogdan).

Prior art clock synchronization systems require expensive local oscillators, expensive external off-chip analog components, and expensive IC technologies suitable for mixed mode operations; in order to provide highly stable and low jitter synchronization clocks required in industrial control systems and in communication networks.

State of art network synchronizers represented by D3, D4 require use of a multiplication of a local reference clock for producing synchronizer output clocks.

Since feasible multiplication factors can not be risen too high without compromising stability margins, a very accurate local reference clock must provide a relatively high clock frequency and the higher frequency increases the cost and the complexity of said local oscillator.

In addition to that: since said local clock multiplications can provide only a fixed set of multiplication factors, current synchronizers require specific local reference frequencies and it limits a choice of local oscillators.

Temperature stable crystal oscillators are major cost contributors exceeding 2/3 of total costs of synchronization systems. However in prior art; low cost highly stable crystal cuts can not be used, since their oscillation frequencies are to low to be transformed into a stable low jitter clock.

Furthermore, universal synchronization system shall be able to lock to wide variety of external reference frequencies which may differ from one application to another. Therefore in order to accommodate very wide ranges of input frequencies belonging to different frequency domains, current synchronizers have to provide multiple inputs which are designated for specific frequencies of reference clocks.

Similarly current universal synchronization systems are using multiple different outputs to provide different frequencies required for different application areas.

SUMMARY OF THE INVENTION

Purpose of the invention

It is an object of the present invention to provide a Phase Synthesizer (PS) for generating a waveform for a telecommunication transmitter or receiver and for a universal synchronization system, which shall provide listed below advantages over existing fractional synthesizers:

- lower phase jitter levels,
- significantly higher resolution and better accuracy of frequency generation,
- complete control of phase transients during phase/frequency switching operations,
- one order higher frequency of phase & frequency modulation,
- very wide ranges of frequency & phase adjustments.

It is other object of the HTS invention to create novel configuration fully utilizing mutually complementing advantages of APLL and DPLL by combining them into a hybrid PLL (HPLL).

It is still other object of the present invention to provide a Heterodyne Timing System for a variety of telecommunication systems, which is based on said PS and provides listed below advantages over current universal synchronization systems:

- can use inexpensive very low frequency local oscillators providing any clock frequency,
- enables using the same single input for accepting external reference clocks having a wide variety of different frequencies,
- is able to use the same re-programmable output to provide different output frequencies for a variety of applications,
- simplifies circuits and lowers cost of a universal synchronizer for use in variety of telecommunication systems with wide ranges of data rates, including wireless, optical, or wireline transmission systems.

The HTS defined by this invention is unique, as it allows: multiplication of said very low frequency clocks by factors as high as 50 000 while maintaining very low jiiter.
Furthermore this major advantage is combined with indefinite flexibility and precision in setting frequency of output clocks generated without any unpredicted phase transients.

These major contributions over prior art make the HPLL conclusively superior alternative to prior art PLLs in many major areas including analog, SOC, signal processing, and frequency control products where combining high multiplication with low jitter is a major bottleneck.

Digital Wave Synthesis from Multi Sub-Clocks (DWS MSC)

Accordingly the invention provides DWS MSC as a new timing method and circuit for programming and selecting a phase and a frequency of a synthesized clock.
The DWS MSC method comprises programmable phase modifications which are defined below:
Phase increases of the synthesized clock are provided; by adding whole clock periods and/or fractional sub-clock delays, obtained from serially connected delay elements which the reference clock is propagated through, to a present phase obtained from a counter of reference clock periods and/or a present fractional sub-clock delay.
Phase decreases of the synthesized clock are provided; by subtracting whole clock periods and/or fractional sub-clock delays, obtained from serially connected delay elements which the reference clock is propagated through, from a present phase obtained from a counter of clock periods and/or a present fractional sub-clock delay.

The DWS MSC method provides one order better phase adjustment resolution than the commonly used DDFS method; because the DWS MSC can modify phase with time intervals specified in fractions of clock cycle, instead of inserting or eliminating whole clock cycles from a synthesized clock.
Therefore, the phase hits and resulting jitter are reduced by around 10 times compared to the DDFS method.
The DWS MSC method provides phase & frequency adjustment ranges, which are by many orders wider than for the DPFS method invented in D4.
The DWS MSC invention provides an implementation of programmable algorithms for synthesizing a very wide range of low and high frequency wave-forms.

The DWS MSC invention comprises; a 1-P phase generator, a synchronous sequential phase processor (SSPP) for real time processing and selection of a phase of out-coming wave-form, and a programmable computing unit (PCU) for controlling SSPP operations and supporting

signal synthesis algorithms.

Said 1-P phase generator is an extension of a 1bit odd/even phase generator to p bits enabling 2^p=P phases to be generated from every reference sub-clock, as it is defined below.

The odd/even phase generator provides splitting of reference sub-clocks, generated by outputs of a reference propagation circuit built with serially connected gates which a reference clock is propagated through, into odd phase sub-clocks which begin during odd cycles of the reference clock and even phase sub-clocks which begin during odd cycles of the reference clock, wherein the odd/even phase selector comprises:

said reference propagation circuit connected to the reference clock;

serially connected flip-flops, wherein a clock input of a first flip-flop is connected to the reference clock and a data input of a first flip-flop is connected to an inverted output of the first flip-flop while a clock input of any other Nth flip-flop is connected to an (N-1) output of the reference propagation circuit and a data input of the N flip-flop is connected to an output of the (N-1) flip-flop;

connected to the serially connected flip-flops an odd/even selector generating the odd sub-clocks which begin during every odd reference clock cycle and the even sub-clocks which begin during every even reference clock cycle, wherein the output of the 1st flip-flop is used to select odd and even reference clocks while the output of the Nth flip-flop is used to select odd and even reference sub-clocks from the (N-1) output of the reference propagation circuit.

The odd/even phase generator is extended into the 1-P phase generator splitting the reference sub-clocks into 1-P phase sub-clocks which begin during the corresponding 1-P cycles of the reference clock, wherein the 1-P phase selector further comprises:

a parallel 1-P sub-clock counter built as an extension to the first flip-flop working as 1-2 counter wherein the whole 1-P sub-clock counter is clocked by the first reference sub-clock, wherein an output of the 1-P sub-clock counter represents a 1-P phase number of the first sub-clock;

2-N parallel multi-bit buffers built as extensions to the original 2-N flip-flops working as 1 bit buffers wherein the whole 1-P sub-clock counter is clocked by the 2nd reference sub-clock into the first multi-bit buffer which is clocked by the 3rd reference sub-clock into

the 2nd multi-bit buffer and the content of the 1-P counter is similarly propagated into all next buffers until the Nth sub-clock loads the N-2 buffer into the N-1 buffer, wherein the 1st buffer defines a phase number minus 1 for the 2nd reference sub-clock and next buffers define similarly phase numbers for their corresponding reference sub-clocks until the N-1 buffer defines a phase number minus (N-1) for the Nth reference sub-clock.

1-P phase selectors built as extensions to the corresponding odd/even selectors wherein a first 1-P selector is connected to the 1-P sub-clock counter and selects a phase, of the first reference sub-clock, defined by the 1-P sub-clock counter while every next N-K+1 phase selector is connected to its N-K buffer and to its N-K+1 reference sub-clock ($0<K<N$), wherein every next N-K+1 phase selector generates phases, of its N-K+1 sub-clock, defined by its buffer content plus (N-K).

The 1-P phase generator can use both solutions defined below:
using rising edges of the reference sub-clocks for clocking the 1-P sub-clock counter and the 2-P buffers while negative pulses of the reference sub-clocks are used for activating outputs of the 1-P selectors generating the 1-P phase sub-clocks;
or using rising edges of the reference sub-clocks for clocking the 1-P sub-clock counter and the 2-P buffers while negative pulses of the reference sub-clocks are used for activating outputs of the 1-P selectors generating the 1-P phase sub-clocks.

Furthermore the 1-P phase generator can use the serially connected gates of the reference propagation circuit, which are connected into a ring oscillator controlled by a PLL circuit or are connected into a delay line control by a delay locked loop (DLL) circuit or are connected into an open ended delay line.

Furthermore this 1-P phase generator invention includes extending the remaining 2-N flip-flops with parallel sub-clock counters, the same as the parallel sub-clock counter extending the 1st flip-flop, instead of using the defined above 2-P multi-bit buffers. The use of the 2-P parallel counters requires adding preset means for all the 1-P counters, in order to maintain the same or predictably shifted content in all the 1-N parallel counters. Continues maintaining of said predictability of all the parallel counters content is necessary for generating predictable sequences of multiphase sub-clocks.

Said SSPP invention comprises a selection of one of multi sub-clocks for providing an edge of out-coming synthesized signal, where said sub-clocks are generated by the outputs of serially connected gates which an SSPP reference clock is propagated through.

The SSPP comprises calculating a binary positioning of a next edge of the out-coming wave-form versus a previous wave edge, which represents a number of reference clock cycles combined with a number of reference clock fractional delays which correspond to a particular sub-clock phase delay versus the reference clock.

Furthermore the SSPP comprises selective enabling of a particular sub-clock, which provides the calculated phase step between the previous and the current wave-form edges.

The SSPP further comprises a synchronous sequential processing (SSP) of incoming signal by using multiple serially connected processing stages with every stage being fed by data from the previous stage which are clocked-in by a clock which is synchronous with the reference clock.

Since every consecutive stage is driven by a clock which is synchronous to the same reference clock, all the stages are driven by clocks which are mutually synchronous but may have some constant phase displacements versus each other.

The synchronous sequential processor (SSP) multiplies processing speed by splitting complex signal processing operation into a sequence of singular micro-cycles, wherein:

every consecutive micro-cycle of the complex operation is performed by a separate logical or arithmetical processing stage during a corresponding consecutive time slot synchronous with a reference clock providing a fundamental timing for a synthesized wave-form;

serially connected sequential stages are connected to a programmable control unit (PCU), wherein the sequential stages are clocked by reference sub-clocks generated by a reference propagation circuit built with serially connected gates which the reference clock is propagated through;

whereby inputs from the PCU are processed into a phase delay between a next edge of the synthesized wave-form versus a previous edge and a position of the next edge is calculated by adding the phase delay to a position of the previous edge, wherein the positions of wave-form edges are provided by a last of the sequential stages and said positions are expressed as numbers identifying reference sub-clocks needed for generating said wave-form edges.

The above defined SSP can be implemented by processing said inputs from the PCU into a phase modification step which is added to a period of the reference clock in order to calculate the phase delay.

Furthermore this invention includes the SSP circuit upgraded into a parallel multiphase processor (PMP) by extending the time slot allowed for the micro-cycles of the synchronous sequential processor by a factor of P, wherein:

2-P stages are added to the original sequential stage and every one of the resulting 1-P parallel multiphase stages is clocked with a corresponding 1-P phase sub-clock, wherein such 1-P phase sub-clock begins during the corresponding to that phase 1-P cycle of the reference clock and has a cycle which is P times longer than the reference clock cycle;

whereby consecutive 1-P parallel multiphase stages have processing cycles overlapping by 1 cycle of the reference clock wherein every 1-P parallel processing stage has P times longer cycle time equal to the cycle time of the corresponding 1-P phase sub-clock used for timing that stage.

The parallel multiphase processor further comprises:

a parallel processing phase 2-P built with plurality of 2-P parallel multiphase stages which are connected serially and are driven by the phase sub-clocks belonging to the same 2-P phase.

The SSPP invention comprises the use of the parallel multiphase processing for synthesizing a target wave-form by assigning consecutive parallel phases for the processing of a synthesized signal phase using signal modulation data provided by a programmable control unit (PCU) or by any other source.

Consequently the SSPP invention comprises using 1 to N parallel phases which are assigned for processing incoming signal data with clocks corresponding to-reference clock periods number 1 to N, as it is further described below:

- circuits of phase1 process edge skews or phase skews or other incoming signal data with a clock which corresponds to the reference clock period number 1;
- circuits of phase2 process edge skews or phase skews or other incoming signal data with a clock which corresponds to the reference clock period number 2;

- finally circuits of phaseN process edge skews or phase skews or other incoming signal data with a clock which corresponds to the reference clock period number N.

Said parallel multiphase processing allows N times longer processing and/or sub-clocks selection times for said multiphase stages, compared with a single phase solution.

The above mentioned sub-clock selecting methods further include:

- using falling edges of said sub-clocks for driving clock selectors which select parallel processing phases during which positive sub-clocks are enabled to perform said synthesized wave-form timing, or using rising edges of said sub-clocks for driving selectors which select parallel processing phases during which negative sub-clocks are enabled to perform said synthesized wave-form timing;
- using serially connected clock selectors for enabling consecutive sub-clocks during said processing phases, in order to assure that the enabled sub-clocks will occur within a selected processing phase and to enable selection of a sub-clock specified by a number contained in a fraction selection register of a particular processing phase.

The SSPP invention includes using said serially connected gates:

- as being an open ended delay line;
- or being connected into a ring oscillator which can be controlled in a PLL configuration;
- or being connected into a delay line which can be controlled in a delay locked loop (DLL) configuration.

Every said sub-clock phase delay versus the reference clock phase amounts to a fraction of a reference clock period which is defined by a content of a fraction selection register which is assigned for a particular processing phase and is driven by the SSPP.

The SSPP invention includes a parallel stage processing of an incoming signal by providing multiple processing stages which are driven by the same clock which is applied simultaneously to inputs of output registers of all the parallel stages.

The SSPP further comprises:

- a merging of processing phases which occurs if multiple parallel processing phases are merged into a smaller number of parallel phases or into a single processing phase, when passing from a one processing stage to a next processing stage;
- a splitting of processing phases which occurs if one processing phase is split into

multiple processing phases or multiple processing stages are split into even more processing stages, when passing from a one processing stage to a next processing stage.

The SSPP invention includes using the 1-P phase generator defined above to generate SSPP clocks which drive said parallel phases and said sequential stages, and to generate selector switching signals for said merging and splitting of processing phases.

The SSPP invention includes time sharing of said parallel phases: which is based on assigning a task of processing of a next wave-form edge timing to a next available parallel processing phase.

The SSPP comprises a timing control (TC) circuit, which uses decoding of reference clock counters and/or other wave edge decoding and said SSPP clocks, for performing said time sharing phase assignments and for further control of operations of an already assigned phase.

The SSPP comprises passing outputs of a one parallel phase to a next parallel phase, in order to use said passed outputs for processing conducted by a following stage of the next parallel phase.
The outputs passing is performed: by re-timing output register bits of the one phase by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase.

The SSPP further comprises all the possible combinations of the above defined: parallel multiphase processing, parallel stage processing, synchronous sequential processing, merging of processing phases, splitting of processing phases, and outputs passing.

The SSPP invention includes processing stage configurations using selectors, arithmometers, and output registers, which are arranged as it is defined below:

- input selectors select constant values or outputs of previous stages or outputs of parallel stages or an output of the same stage to provide arithmometer inputs, and arithmometer output is clocked-in to an output register by a clock which is synchronous to the reference clock;
- multiple arithmometers are fed with constant values or outputs of previous stages or

outputs of parallel stages or an output of the same stage, and an output selector selects an arithmometer output to be clocked-in to an output register by a clock synchronous to the reference clock;

- the above defined configuration as being supplemented by using an output of an output selector of a parallel processing stage for controlling functions of other output selector.

The SSPP invention comprises:
using switching signals of said input selectors for producing pulses which clock data into output registers of previous stages;
using switching signals of said output selectors for producing pulses which clock data into output registers of previous stages;

The SSPP invention also comprises:
using results obtained in earlier stages for controlling later stages operations,
and using results obtained in the later stages for controlling the earlier stages operations.

Proper arrangements of said parallel and sequential combinations and said stages configurations provide real time processing capabilities for very wide ranges of signal frequencies and enable a wide coverage of very diversified application areas.

The DWS MSC invention comprises two different methods for accommodating a phase skew between the reference clock and a required carrier clock frequency of the transmitted signal, and both methods allow elimination of ambiguities and errors in encoding of output signal data patterns. Said two methods are further defined below:

- a source of the reference clock provides frequency or phase alignment with the timing of the data which are being encoded and sent out in the synthesized output wave-form;
- phase skews between the reference clock and the timing of the destined for transmission data are digitally measured and translated into implemented by the SSPP phase adjustments of the synthesized signal which provide required carrier frequency of the transmitted output signal;
- both above mentioned methods include measurements of phase or frequency deviations of the destined for transmission data versus the reference clock, and using said measurements results to assure required carrier frequency of the synthesized signal.

Furthermore the DWS MSC method comprises phase modulations of the synthesized wave-form by adding or subtracting a number of reference clock periods and/or a number of fractional delays to a phase of any edge of the synthesized wave-form.
Said adding or subtracting of a number of reference clock periods is further referred to as a periodical adjustment, and said adding or subtracting of fractional delays is further called a fractional adjustment.

The DWS MSC method allows synthesizing of any waveform by modulating a phase of the reference clock with periodical and/or fractional adjustments of any size.

Phase Synthesizer (PS)

The invention also includes the Phase Synthesizer (PS) for carrying out the DWS MSC method; as it is further explained below and is shown in FIG.1, FIG.1A, FIG.2, and FIG.3. The Timing Diagram of the PS is shown in the FIG.5.

Said phase synthesizer provides programmable modifications of a phase of a synthesized clock by unlimited number of gate delays per a modification step with step resolution matching single gate delay at steps frequencies ranging from 0 to 1/2 of maximum clock frequency, wherein:

a delay control circuit is connected to a programmable control unit (PCU) wherein the delay control circuit defines size and frequency of phase delay modifications of the synthesized clock versus a reference clock, the delay control circuit also having a terminal connected to reference sub-clocks generated by a reference propagation circuit or connected to odd/even sub-clocks generated by an odd/even phase selector;

the reference clock is connected to the reference propagation circuit consisting of serially connected gates wherein outputs of the gates generate the reference sub-clocks providing variety of phase delays versus the reference clock;

the reference sub-clocks are connected to an odd/even phase selector which splits the reference sub-clocks by generating separate odd sub-clocks and even sub-clocks, wherein the odd sub-clocks begin during odd cycles of the reference clock and the even sub-clocks begin during even cycles of the reference clock;

a clock selection register is loaded by the odd sub-clocks and by the even sub-clocks with the outputs of the delay control circuit, wherein the odd sub-clocks or the even sub-clocks beginning during an earlier cycle of the reference clock download outputs of the delay control circuit which select the even sub-clocks or the odd sub-clocks beginning during a later cycle of the reference clock for providing the synthesized clock;

an output selector is connected to the output of the clock selection register and to the outputs of the odd/even phase selector, wherein the output selector uses inputs from the clock selection register for selecting output of the odd/even phase selector which is passed through the output selector for providing the synthesized clock.

The above defined PS can use the odd/even phase generator or the 1-P phase generator, which have been already defined above.

The PS can use the delay control circuit implemented with the parallel multiphase processor (PMP) which has been already defined above.

The PS invention comprises 2 different implementation methods, which are explained below.

The first PS implementation method is based on moving a synthesized clock selection point from a delay line which propagates a reference clock (see the FIG.1); wherein:
said phase increases are provided by moving said selection point of the synthesized clock from the reference clock propagation circuit, in a way which adds gate delays to a present delay obtained from the propagation circuit;
said phase decreases are provided by moving said selection point of the synthesized clock from the reference clock propagation circuit, in a way which subtracts gate delays from a present delay obtained from the propagation circuit;
The first PS implementation method is conceptually presented in FIG.1 & FIG.3, and its principles of operations are explained below.
The PLL x L Freq. Multiplier produces the series of sub-clocks Clk0, ClkR - Clk1.
The sub-clock Clk0 keeps clocking in a reversed output of its own selector PR0.
The sub-clocks CLkR-Clk1 keep clocking in outputs of the previous selectors PR0, PRR - PR2 into their own selectors PRR-PR1.
Since the selector PR0 is being reversed by every Clk0, every selector in the PR0, PRR -

PR1 chain is being reversed as well by a falling edge of its own sub-clock Clk0, ClkR - Clk1, and every selector in the chain represents reversal of its predecessor which is delayed by a single sub-clock fractional delay.

Consequently the PR0, PR1N - PRR select sub-clocks Clk0, Clk1 - ClkR during any odd processing phase, and their reversals PR0N, PR1 - PRRN select sub-clocks Clk0, Clk1 - ClkR during any even processing phase.

The odd/even processing phase has been named phase1/phase2, and their sub-clocks are named 1Clk0,1Clk1-1ClkR/2Clk0,2Clk1-2ClkR accordingly.

Since said phase1/phase2 sub-clocks are used to run a phase synthesis processing in separate designated for phase1/phase2 phase processing stages which work in parallel, a time available for performing single stage operations is doubled (see also the FIG.3 for more comprehensive presentation of said parallel processing).

Furthermore, the Clock Selection Register 1 (CSR1) can be reloaded at the beginning of the phase2 by the 2Clk0 and its decoders shall be ready to select a glitch free phase1 sub-clock which is defined by any binary content of the CSR1.

Similarly the CSR2 is reloaded by the 1Clk0, in order to select a single glitch free sub-clock belonging to the phase2.

The second PS implementation method is based on adjusting alignment between an exit point of the synthesized clock from the reference propagation circuit versus an input reference clock; in a way which adds gate delays for phase increases, and subtracts gate delays for phase decreases.

The second method is presented in FIG.1A, and its differences versus the FIG.1 are explained below.

The moving exit point from the driven by Fsync/2Dsel phase locked delay line is used as a return clock for the PLL x 2Dsel multiplier, instead of using a fixed output of the INV0 to be the PLL return clock.

The fixed output of the INV0 is divided by the programmable frequency divider (PFD) in order to provide the synthesized clock Fsynt, instead of the moving synthesized clock selection point.

The first method exit point alignments, introduce phase jumps which cause synthesized clock jitter. The second method configuration shown in Fig.1A, filters out Fsynt jitter frequencies which are higher than a bandwidth of the multiplier's PLL.

While any of the two PS implementation methods is shown above using a particular type of a reference clock propagation circuit, the PS invention comprises using all the listed below reference clock propagation circuits by any of the two methods:
an open ended delay line built with serially connected logical gates or other delay elements;
a ring oscillator built with serially connected logical gates or other delay elements, which have propagation delays controlled in a PLL configuration;
a delay line built with serially connected logical gates or other delay elements, which have propagation delays controlled in a Delay Locked Loop (DLL) configuration.

It shall be noticed that further splitting to more than 2 parallel phases is actually easier than the splitting to the original 2 processing phases; because while one of the phases is active, its earlier sub-clocks can be used to trigger flip-flops which can segregate sub-clocks which belong to multiple other phases and can be used to drive the other parallel phases. Consequently using this approach; allows increasing parallel stages processing times to multiples of reference clock periods, and provides implementation of said DWS MSC multiple phase processing which has been introduced in the previous section.

Said selection of a sub-clock for synthesized clock timing, can be physically implemented in two different ways:
by using phase producing gates from 1inv0 to 1invR and from 1inv0 to 1invR, as having 3state outputs with enable inputs EN, one of which is enabled by one of the outputs of the sub-clock selection gates from 1sel0 to 1selR and from 2sel0 to 2selR;
or by using the sub-clock selection gates which have all their outputs connected into a common collector configuration (instead of having them followed by the 3state gates), in order to allow a currently active output of one of the sub-clock selection gates to produce a phase of the synthesized clock FselN.

The PS invention comprises fractional adjustments of synthesized clock phase for providing high resolution phase modifications by fractional parts of a reference clock period.
The PS invention comprises combined periodical and fractional adjustments of synthesized clock phase, which use counters of reference clock periods for generating counter end (CE) signals when a periodical part of a phase adjustment is expired.

The PS invention further comprises using said counter end signals for generation of control signals which assign and/or synchronize consecutive parallel processing phases for processing consecutive combined or fractional phase adjustments of the synthesized clock.

The PS invention comprises:

- Using a basic periodical adjustment and a basic fractional adjustment for providing a basic phase step, which can remain the same for multiple edges of the synthesized clock.
- Using a modulating periodical adjustment and a modulating fractional adjustment, which can be different for every specific edge of the synthesized clock.
- Using said DWS MSC and SSPP methods for processing of said basic periodical adjustments, basic fractional adjustments, modulating periodical adjustments and modulating fractional adjustments for calculating periodical and fractional parts of combined adjustments.
- Processing of said calculated combined adjustment with a positioning of a synthesized clock previous edge for calculating a periodical and a fractional part of the next edge position of the synthesized clock.

Heterodyne Timing System

The invention further includes an universal network synchronizer named Heterodyne Timing System (HTS) which is completely integrated into a single chip (see also FIG.4, and FIG.4A).

The programmable HTS is not limited to discrete sets of input/output frequencies but accepts a local reference clock of any frequency and accepts an external reference clock of any frequency while providing any required frequency of an HTS output clock and very low phase transients during any switching of reference clocks, wherein the HTS comprises:

a micro-controller (MC) for implementing a programmable phase transfer function (PTF) between a phase of the HTS output clock and a phase of a second reference clock, wherein the micro-controller controls operations of the phase synthesizer (PS) defined above, the micro-controller has a terminal for a first phase error;

the PS connected to the micro-controller while the reference clock input of the PS is connected to the HTS output clock, wherein the synthesized clock of the PS is connected

to a return input of an analog PLL (APLL);

the APLL having its reference input connected to the HTS output clock or to an APLL output clock while the return input of the APLL is connected to the synthesized clock, wherein an APLL output clock drives the HTS output clock;

a first digital phase detector (1DPD) receiving the second reference clock and the local reference clock or receiving the second reference clock and the synthesized clock or receiving the second reference clock and the HTS output clock, wherein the digital 1DPD produces the first phase error connected back to the micro-controller;

wherein said micro-controller uses its internal micro-operations for implementing filter functions of an on chip digital PLL (DPLL) by processing said first phase error into the micro-controller output driving the PS into producing the synthesized clock providing compliance of the APLL output clock and the HTS output clock with the phase transfer function defined by the PTF.

The HTS invention includes reference selection means for alternative use of one of multiple connected reference clocks for producing the HTS output clock, the HTS further comprises:

a reference selector connected to multiple external reference clocks and controlled by the micro-controller, wherein the micro-controller selects one of the multiple reference clocks for being connected to the 1DPD which is read by the MC and used by MC subroutines for controlling the HTS output clock;

activity monitors for the external reference clocks for producing active/non-active output signals connected to the micro-controller;

wherein the activity monitors output signals are read and processed by the microprocessor which is producing reference selection signals connected to the reference selectors.

The HTS further includes means supporting a VCXO jiitter filter for HTS applications which are extremely jitter sensitive, the HTS comprises:

an analog phase detector (APD) having a reference input connected to the HTS output clock or to the APLL output clock while a return input of the APD is connected to an output clock of the VCXO jitter filter, wherein an output of the APD is used to drive a remaining circuit of the VCXO jitter filter.

The HTS further comprises:

an output phase locked loop (OUT-PLL) referenced by the APLL output clock and producing a fundamental output clock, wherein the OUT-PLL has a return input connected to HTS output clock;

an output clock generator (OCG) connected to the fundamental output clock, the OCG produces a plurality of the HTS output clocks (F_{OUT}) wherein one of the HTS output clocks is connected back to the return input of the OUT_PLL.

The HTS further includes an analog phase locked loop mode (APLL mode) of operation using a first reference clock (f_{R1}) as an external reference source which the HTS output clock is phase locked to, the HTS comprises:

a reference selector connected to the APLL output clock and to the first reference clock or to the HTS output clock and to the first reference clock wherein the reference selector is controlled by the MC and an output of the reference selector is connected to the APLL reference input, wherein the MC selects the first reference clock for the APLL mode while the MC selects the HTS output clock or the APLL output clock for the DPLL mode;

whereby during the APLL mode the HTS output is phase locked to the first reference clock wherein the PS is driven by a constant MC output maintaining a fixed frequency relation between the HTS output and the first reference clock.

The HTS further includes reference selection means for alternative use of one of multiple connected reference clocks for producing the HTS output clock, the HTS further comprises:

a first reference selector providing the first reference clock f_{R1} selected from a first set of reference clocks, the first reference selector connected to the first set of reference clocks and controlled by the micro-controller, wherein the micro-controller selects one of the first set clocks for being used for referencing the HTS output clock;

a second reference selector providing the second reference clock f_{R2} selected from a second set of reference clocks, the second reference selector connected to the second set of reference clocks and controlled by the micro-controller, wherein the micro-controller selects one of the second set clocks for being used for referencing the HTS output clock;

activity monitors, for the first set clocks and for the second set clocks, for producing

active/non-active output signals connected to the micro-controller;

wherein the activity monitors output signals are read and processed by the microprocessor producing reference selection signals connected to the first reference selector and to the second reference selector.

The HTS further comprises:

interface circuits, for communication with an external control processor, connected to the external control processor and to the micro-controller;

wherein the interface circuits and the micro-controller enable the external control processor to read information about statuses of the activity monitors and to select an external reference clock or the local reference clock for referencing the HTS output clock.

Furthermore the interface circuits and the micro-controller enable the external control processor to perform switching of mode of operation of the HTS between the APLL mode and the DPLL mode.

The HTS micro-controller is provisioned to perform operations listed below:

reading information about statuses of the activity monitors and selecting an external reference clock or the local reference clock for referencing the HTS output clock;

switching mode of operation of the HTS between the APLL mode and the DPLL mode.

Furthermore the HTS is provisioned to perform a master/slave mode switching for maintaining phase alignment between an active HTS unit and a backup HTS unit installed in a back-plane for protection switching, the HTS comprises:

a master/slave subroutine reading activity monitor of a reference clock provided by a mate HTS unit and reading internal status of the own HTS unit;

wherein the master/slave subroutine performs switching to the master mode by selecting other reference clock than the mate's reference clock when the mate's reference clock becomes inactive or performs switching to the slave mode by selecting the mate's reference clock when the mate's reference clock is detected active during a power-up initialization of the own HTS unit.

The HTS invention comprises using a programmable phase synthesizer to produce an Analog PLL return clock, which can be reprogrammed to match a frequency of a reference clock of said Analog PLL.

Furthermore the HTS invention comprises:

applying an output clock of the APLL to a reference input of the APLL;

using the return clock synthesizer for inserting phase deviations between the APLL return clock and the output clock applied to the APLL reference input;

using the inserted phase deviations for implementing required phase and frequency transfer functions between the APLL output clock and other HTS reference clocks;

implementing digital PLL (DPLL) algorithms for providing the required phase and frequency transfer functions.

Still furthermore the HTS invention comprises:

using digital phase detectors (DPDs) for measuring phase errors between the APLL output clock and said other HTS reference clocks;

using a programmable control unit (PCU) for processing the measured phase errors and producing control codes for the return clock synthesizer, which implement pre-programmed phase and frequency transfer functions between the APLL output clock and said other HTS reference clocks.

The HTS comprises:

Said analog phase locked loop (APLL) for producing the output clock F-out1 which can be locked to the first reference signal F_r1, unless the APLL is driven by the digital phase locked loop (DPLL);

Said DPLL can provide locking to the second reference F_r2, or to a local oscillator f_lo, or to a frequency source f_fs (which can be a GPS clock).

For producing an APLL return clock, the HTS uses a programmable clock synthesizer which can be re-programmed to synthesize a return clock which can match any frequency of said APLL reference signal F_r1.

Very high accuracy and very wide adjustment ranges of the PS allows it to be used in said heterodyne configuration (where it is named RET_CS), in which synthesized by the RET_CS return clock is applied to the return input of the OUT_PLL Phase Detector named APD.

A first/second set of reference signals is named F_r1 / F_r2 and their single representatives are named f_r1 / f_r2 accordingly, throughout this document.

The HTS invention further comprises two different configurations which are explained below.

The first HTS configuration implements the APLL using voltage controlled cristal oscillator (VCXO) which is driven by and on-chip analog phase detector (APD) through an external (out of chip) Loop Filter (see FIG.4).

The first HTS configuration comprises circuits and functions which are listed below:

a return clock synthesizer (RET_CS) for generating a clock adjusted to a frequency of the first reference signal;

a first digital phase detector (DPD1) for comparing a phase of a synchronizer output clock from said APLL with a phase of the second reference clock, for producing a first phase error;

a second digital phase detector (DPD2) for comparing a phase of the output clock from said APLL with a phase of the local oscillator clock, for producing a second phase error;

a third digital phase detector (DPD3) for comparing a phase of the output clock from said APLL with a phase of the frequency source clock, for producing a third phase error;

a programmable control unit (PCU) for driving said synthesized clock generator, based on the first phase error and the second phase error and in accordance with a preprogrammed phase transfer function (PTF);

the analog phase lock loop (APLL) for generating said synchronizer output clock;

a programmable reference selector (RFS) for said APLL, for providing reference switching which allows the APLL to be driven by said synthesized clock or by one of the multiple first reference signals F_r1;

programmable frequency dividers for a reference signal and for return signal of said APLL, for providing programmable bandwidth adjustments of the APLL;

a programmable DPLL reference selector (DRS) for selecting one of the multiple available reference signals F_r2 for said DPLL, which allows switching between using different DPLL reference clocks;

programmable frequency dividers in the output clock generator (OCG) which can be reprogrammed by the PCU, in order to allow utilizing a single pin of F_out1 for providing multiple different output clock frequencies;

activity monitoring circuits for synchronizer input clocks and output clocks;

frequency monitoring circuits for synchronizer reference clocks;

status control circuits for switching synchronizer modes of operation and active reference clocks, based on an analysis of said activity and frequency monitoring circuits;

phase transfer control circuits for providing a required phase transfer function between an active reference clock and synchronizer output clocks;

a serial interface which allows the status control circuits and the phase transfer control circuits to be monitored and reprogrammed by an external controller;

a parallel interface which allows the status control circuits and the phase transfer control circuits to be monitored and reprogrammed by an external controller;

automatic reference switching functions including hold-over and free-run switching, which are performed by the status control circuits and are based on monitoring a status of the activity and frequency monitoring circuits;

a master/slave switching circuit which allows a pair of integrated synchronizers to work in a master/slave configuration having a slave synchronizer being phase locked to a mate clock which is generated by a mate master synchronizer;

a re-timing circuit in an output clock generator (OCG) which adjusts all the rising edges of the output clocks F_out1 of said slave synchronizer with the rising edge of the frame signal fr_mate from said mate master synchronizer;

a second clock synthesizer configured as output clock synthesizer (OUT_CS) for providing a second set of synchronizer output clocks F_out2 which can belong to a different frequency domain than the first set of output clocks F_out1.

The above listed status control circuits and phase transfer control circuits can be implemented as separate on-chip control units or with a single on-chip PCU.

The first synchronizer configuration is carried out by an HTS configuration which is based on the DWS MSC, the PS, the DPD1, the DPD2 and the DPD3.

As it is shown in FIG.4, the first configuration allows the integration of all the circuits and the functions of the integrated synchronizer, with the exception of the VCXO and eventually the Loop Filter; into a single CMOS ASIC.

HTS's APLL mode of operation is described below.

One of the first reference clocks F_r1 is selected to be applied to the APLL reference input and the return clock synthesizer (RET_CS) is switched by the PCU into producing the APLL

return clock which is matching said selected first reference clock.

The implementation of a DPLL mode is explained below.

The APLL output clock f_filter is applied to the APLL reference input and the return clock synthesizer (RET_CS) is switched by the PCU into producing the APLL return clock which is matching said output clock f_filter.

The DPD1 measures a phase error between the output clock multiplication f_samp and the second reference clock derivative fr_r2 , and the DPD2 measures a phase error between the f_samp and the local clock derivative fr_lo.

The PCU reads the above phase errors and uses them to calculate new contents of the RET_CS's periodical adjustment buffers and the fractional adjustment buffers needed for inserting phase deviations required for providing a phase transfer function (PTF), between the output clock f_filter and the second reference clock F_r2, which is already preprogrammed in the PCU.

The second synchronizer configuration (see FIG.4A) allows the complete integration of the DPLL, the APLL, and all the other circuits of the integrated synchronizer into a single CMOS ASIC.

The second synchronizer configuration comprises the same circuits and functions as the listed above for the first configuration, with the exceptions which are specified below.

The Analog PLL is based on the on-chip phase locked loop cell OUT_PLL, instead of requiring said external VCXO which becomes an optional component attached only for jiiter sensitive applications.

Consequently; both the APLL reference clock and the APLL return clock are applied directly to the OUT_PLL reference input and to the OUT_PLL return input, instead of driving said VCXO based PLL.

Therefore instead of the VCXO output f_filter; one of the synchronizer's output clocks F_out1 is driving the RET_CS, and is applied to the APLL reference input during a DPLL mode of operation

The invention includes providing slave mode implementation which replaces the external F_r1 clock with the mate HTS output clock f_mate, in order to drive the above described APLL configuration. The slave mode allows maintaining phase alignment between active and reserve HTS units, for the purpose of avoiding phase hits when protection switching

reverts to using clocks from the reserve HTS unit.

The invention includes using the above mentioned method of slave HTS phase alignment for both the first and for the second synchronizer configurations as well.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Phase Synthesizer (PS) Block Diagrams and Circuits Description

The above mentioned first PS implementation is selected for the preferred embodiment, and it is shown in the FIG.1, FIG.2, FIG.3 and FIG.5.

The PS invention comprises wave timing definition, which includes two major components downloaded to the PS from the PCU:

basic less frequently changed phase adjustments, which can include both periodical adjustments and fractional adjustments, define more stable components of wave-form phase;

high frequency phase modulations, which can include both the periodical adjustments and the fractional adjustments, allow every leading edge phase and/or every falling edge phase to be modulated with a different modulation factor.

Said phase modulations are downloaded to the PS simultaneously in batches containing multiple different modulation factors, where every said batch refers to a series of consecutive wave edges.

The PS has internal selection circuits, which select and use consecutive modulation factors for modulating phases of consecutive edges.

In order to allow higher wave generation frequencies, 2 parallel processing circuits are implemented which use consecutive phase1 / phase2 circuits for synthesizing phases of consecutive odd/even edges.

As it is shown in the FIG.3, said basic phase adjustments are loaded to the Periodical Number Buffer (PNB) and to the Fractional Number Buffer (FNB); where they remain unchanged until PS internal Modulations Counter (MC) reaches MC = 0 condition.

On the other hand, said modulation factors M1, M2 - M6, M7 are shifted left, by one factor for every new edge, in the Phase Modulation Buffers (PMB1/PMB2) for providing

consecutive modulation factor needed for a next edge in the left end of the PMB1/PMB2.

Such updated modulation factor is then added to the basic phase adjustments and resulting modulated phase adjustments are downloaded into the Periodical Number Registers (PNR1/PNR2) and into the Fractional Number Registers (FNR1/FNR2).

In order to synthesize an actual position of a new edge of the synthesized waveform; said downloaded modulated phase adjustments need to be added to a current edge position, and the results of said addition are downloaded into the Periods Counters (PC1 or PC2) and into the Fractional Selection Register (FSR)

The Sequential Clocks Generator (SCG) and Output Selection Circuits (OSC) are shown in the FIG.1 and have been already explained in the previous section "Phase Synthesizer (PS)".

The Clock Selection Register 1/2 (CSR1/CSR2) specifies a sub-clock which will be selected in a forthcoming Phase2/Phase1 cycle of the reference clock fsync.
In order to remain settled during a whole next cycle of the fsync, the CSR1/CSR2 registers are loaded by the early sub-clocks of the present Phase2/Phase1 cycle of the fsync.
The CSR1/CSR2 are loaded:
with a current content of the Fractional Selection Register (FSR) (shown in FIG.3), if the LD_C1 or LD_C2 (Load Counter 1 or Load Counter2) signal indicates that an end period of the present phase adjustment is indicated by the C2E or C1E (Counter 2 End or Counter 1 End) accordingly (see FIG2 and FIG.3);
with the binary value 2^S-1=R+1 which exceeds ranges of the 1st Clock Selector (1CS) and the 2nd Clock Selector (2CS) and results in none of selectors outputs being activated and none of sub-clocks being selected during a following phase cycle.

The Timing Control (TC) circuits are shown in FIG.2, the resulting Timing Diagram of Phase Synthesizer (TDPS) is shown in FIG.5, and TC operations are explained below.

The LD_C1 signal enables loading of the Period Counter 1 (PC1) with a number of periods which the previous stages of the Synchronous Sequential phase Processor (SSPP) have calculated for the current phase adjustment.

Said download deactivates/activates the C1E signal if a downloaded value is (bigger than 1) / (equal to 1) accordingly. When said downloaded value is bigger than 1, the C1EN = 1 enables decreasing the PC1 content by 1 at every leading edge of the Clk1.1 until the PC1 = 1 condition is achieved and is detected by the PC1-OVF Detector which signals it with the C1E = 1 signal.

It shall be noticed that: when a fractional part of a phase adjustment calculated in said FSR reaches or exceeds a whole period of the fsync, the overflow bit FSR(OVF) = 1 is activated and switches the PC1=1-OVF DETECTOR from said 1 detection mode to a 0 detection mode which prolongs current phase adjustment by 1 fsync period.

The phase 2 control circuit is driven by the C1E and by the LD_C1, and controls phase 2 operations with signals LD_C2, LD_RE2, LD_BU2; as it is further explained below:

- The first C1E activation period generates the LD_C2 signal, and is followed by setting the LDR2_FF which terminates the LD_C2.
- The LD_C2 signal; enables loading of PC2 with a periods number for the next phase adjustment, enables loading of the FSR with a fractional adjustment for the next phase adjustment, and enables a downloading of the FSR to the CSR1 or to the CSR2.
- The LDR2_FF = 1 generates the leading edge of the LD_RE2 signal.
- The LD_RE2 signal clocks in; a new modified fractional adjustment to the Fractional Number Register 2 (FNR2), and a new modified periodical adjustment to the Periodical Number Register 2 (PNR2).
- When the period number loaded by the LD_C2 is counted down to its end by the PC2, the C2E signal activates the LD_C1 similarly as the C1E has activated the LD_C2.
- The LD_C1 =1 resets both the C1E and the LDR2_FF in the next cycle;
- The LDR2_FF = 0 generates the leading edge of the LD_BU2 signal.
- The LD_BU2 signal clocks in; a previous PMB2 content shifted left by S+1 bits, or a new PM[M6,M4,M2,M0] content from the PCU when the Modulations Counter (MC) is decoded as MC=0.

The phase 1 control circuit is similarly driven by the C2E and by the LD_C2; and similarly generates the LD_C1, LD_RE1, LD_BU1 signals for controlling phase1 operations.

The only differences in the phase 1 versus phase 2 operations, are specified below:

- The LD_BU1 signal clocks in a decreased by 1 value to the MC which is the modulo 4 counter.
- The DECODER MC=0 generates the MC=0 signal which selects provided by the PCU; the Periodical Number (PN) / the Fractional Number (FN) / the Phase Modifications (PM) to be loaded into the Periodical Number Buffer (PNB / the Fractional Number Buffer / the Phase Modifications Buffer 1(PMB1) by the leading edge of the LD_BU1.
- The DECODER MC=1 generates the MC=1_INT interrupt signal to the PCU, which informs the PCU that all the above mentioned phase adjustment parameters have been already stored in the PS buffers and can be replaced by new phase adjustment parameters.

Heterodyne Timing System (HTS)

FIG.4 shows HTS configuration according to the preferred embodiment.
The HTS configuration integrates both Digital PLLs (DPLLs) and Analog PLLs (APLLs) into a single CMOS ASIC, with the exception of the external VCXO which provides a stable clock (f_filter) having very low phase jitter.

Said APLL mode of the HTS configuration is described below.
The Reference Selector (RFS) is programmed by the PCU to select one of the first reference clocks F_r1. The selected f_r1 reference clock is applied to the reference input of the Analog Phase Detector (APD) which drives the Loop Filter of the VCXO which provides the stable low jitter output f_filter.
The f_filter; drives the Output Clock PLL (OUT_PLL), and is connected to the fsync/L input of the Return Clock Synthesizer (RET_CS) which is implemented with the PS embodiment described in the previous section.
The RET_CS synthesizes the fsynt1 clock, which is connected to the APD return input.
It shall be noticed that very wide ranges of the RET_CS frequency adjustments, enable the PCU to tune the RET_CS to any frequency which the selected first reference clock f_r1 may have.
Said OUT_PLL generates output clock f_out which drives the first Output Clocks Generator 1 (OCG1) which provides all the major HTS output clocks F-out1.
Since the OCG1 consists of frequency dividers having very tightly controlled and well

matched propagation delays, all the F_out1 clocks are phase aligned with the f_out and between themselves.

The DPLL mode of the HTS configuration is described below.

The f_filter signal is programmed to be selected by the RFS for the APD reference signal, and the RET_CS provides the APD return signal which is synthesized from the same f_filter signal.

One of the second reference clocks (F_r2) is selected by the programmable Digital Reference Selector (DRS) and is divided by the Digital Reference Divider (DRD) for providing the second reference frame (fr_r2), which is connected to the Digital Phase Detector 1 (DPD1).

Local oscillator fixed output f_lo is divided by the programmable 1/N Divider for providing a local oscillator frame fr_lo, which is connected to the Digital Phase Detector 2 (DPD2).

A stable frequency source (like GPS clock) can provide f_fs fixed output which is divided by the programmable 1/M Divider for providing a frequency source frame fr_fs, which is connected to the Digital Phase Detector 3 (DPD3).

Every phase detector DPD1/DPD2/DPD3 shall use the high frequency sampling clock f_samp for accurate digital measurements of phase deviations of the frame fr-r2/fr_lo/fr_fs versus the f_samp phase.

Said sampling clock f_samp is generated by the Frequency Multiplier FMxR from the OUT_PLL output clock f_out. Since the F_out1 output clocks are phase aligned with the OUT_PLL ouput clock f_out, and the sampling clock f_sampl is phase aligned with the f_out as well; the f-sampl is phase aligned with the HTS output clocks F_out1.

The DPD1 measures a phase error between the sampling clock f_samp and the fr_r2, as $\Delta\phi 1 = \phi\_f\_samp - \phi\_fr\_r2$.

The DPD2 measures a phase error between the sampling clock f_samp and the fr_lo, as $\Delta\phi 2 = \phi\_f\_samp - \phi\_fr\_lo$.

The DPD3 measures a phase error between the sampling clock f_samp and the fr_fs, as $\Delta\phi 3 = \phi\_f\_samp - \phi\_fr\_fs$.

The PCU reads the measured phase errors and uses the RET_CS to introduce digital phase differences between the APD reference input and the APD return input which will drive the VCXO based PLL for providing required phase transfer functions between the f_filter signal and the f_r2 signals. Since the f_filter drives the OUT_PLL which has much higher BW than the VCXO PLL and the OUT_PLL determines phase of the F_out1, the F-out1 phase will

provide the same phase transfer function as the f_filter.

Based on the measurements of $\Delta\phi 1$ and $\Delta\phi 2$, the PCU calculates said Periodical Numbers (PN), Fractional Numbers (FN) and Phase Modifications (PM) which need to be provided to the Return Clock Synthesizer (RET_CS); in order to achieve a preprogrammed transfer function between the HTS output clocks and the selected DPLL reference clock f_r2.

For more demanding applications the measurements of the $\Delta\phi 3$ can be read by the PCU as well and can be used to drive additional higher level Digital PLL which shall have a BW by several orders lower than the previously described lower level DPLL.

Said higher level DPLL will be usually referenced by the GPS signal connected via the f_fs input, and will be destined to provide very stable frequency reference for said lower level DPLL.

HTS free-run and hold-over modes use the above described DPLL mode configuration, as it is described below.

In the free-run mode; the PCU uses the phase error measurements for calculating phase differences which need to be inserted via the RET_CS for providing F_out1 locking to the local oscillator frequency f_lo.

In the hold-over mode; the PCU inserts phase differences via the RET_CS which cause the F_out1 clocks to maintain its last frequency displacement versus the f_lo.

The HTS configuration includes generation of the second set of output clocks F_out2 which maintains the same phase transfer functions as the F_out1, but can belong to a totally different frequency domain.

The F_out2 are provided by the second Output Clocks Generator (OCG2), which is driven by the Output Clocks Synthesizer (OUT_CS) which is referenced by the f_filter clock. The OUT_CS uses identical phase synthesizer circuits as the RET_CS.

CLAIMS

While the invention has been described with reference to particular example embodiments, further modifications and improvements which will occur to those skilled in the art, may be made within the purview of the appended claims, without departing from the scope of the invention in its broader aspect.

Numerous modification and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

What is claimed is:

1. An odd/even phase selector for splitting reference sub-clocks, generated by outputs of a reference propagation circuit built with serially connected gates which a reference clock is propagated through, into odd phase sub-clocks which begin during odd cycles of the reference clock and even phase sub-clocks which begin during odd cycles of the reference clock, wherein the odd/even phase selector comprises:

serially connected flip-flops, wherein a clock input of a first flip-flop is connected to the reference clock and a data input of a first flip-flop is connected to an inverted output of the first flip-flop while a clock input of any other Nth flip-flop is connected to an (N-1) output of the reference propagation circuit and a data input of the N flip-flop is connected to an output of the (N-1) flip-flop;

connected to the serially connected flip-flops an odd/even selector generating the odd sub-clocks which begin during every odd reference clock cycle and the even sub-clocks which begin during every even reference clock cycle, wherein the output of the 1st flip-flop is used to select odd and even reference clocks while the output of the Nth flip-flop is used to select odd and even reference sub-clocks from the (N-1) output of the reference propagation circuit.

2. The circuit of claim 1 with the odd/even phase selector extended to a 1-P phase selector for splitting the reference sub-clocks into 1-P phase sub-clocks which begin during the corresponding 1-P cycles of the reference clock, the 1-P phase selector further comprising:

a parallel 1-P sub-clock counter built as an extension to the corresponding serially connected

flip-flop, wherein the whole 1-P sub-clock counter is clocked by the reference sub-clock driving the original serially connected flip-flop wherein an output of the 1-P sub-clock counter represents a 1-P phase number of the clocking sub-clock;

a 1-P selector built as an extension to the corresponding odd/even selector bit, wherein the 1-P selector is connected to the 1-P sub-clock counter and to the corresponding reference sub-clock wherein outputs of the 1-P selector generate the 1-P phases of the corresponding reference sub-clock;

whereby all needed 1-P phases are generated for any one of the reference sub-clocks by extending the corresponding serially connected flip-flop with the 1-P sub-clock counter and extending the corresponding odd/even selector bit with the 1-P selector generating the needed 1-P phases of the reference sub-clock.

3. The circuit of claim 2, wherein:

rising edges of the reference sub-clocks are used to clock the 1-P sub-clock counters;

negative pulses of the reference sub-clocks are used for activating outputs of the 1-P selectors generating the 1-P phase sub-clocks.

4. The circuit of claim 2, wherein:

falling edges of the reference sub-clocks are used to clock the 1-P sub-clock counters;

positive pulses of the reference sub-clocks are used for activating outputs of the 1-P selectors generating the 1-P phase sub-clocks.

5. The circuit of claim 2, wherein:

the serially connected gates of the reference propagation circuit, are connected into a ring oscillator controlled by a PLL circuit or are connected into a delay line control by a delay locked loop (DLL) circuit or are connected into an open ended delay line.

6. A synchronous sequential processor (SSP) for multiplying processing speed by splitting complex signal processing operation into a sequence of singular micro-cycles, wherein:

every consecutive micro-cycle of the complex operation is performed by a separate logical or arithmetical processing stage during a corresponding consecutive time slot synchronous with a reference clock providing a fundamental timing for a synthesized wave-form;

serially connected sequential stages are connected to a programmable control unit (PCU),

wherein the sequential stages are clocked by reference sub-clocks generated by a reference propagation circuit built with serially connected gates which the reference clock is propagated through;

whereby inputs from the PCU are processed into a phase delay between a next edge of the synthesized wave-form versus a previous edge and a position of the next edge is calculated by adding the phase delay to a position of the previous edge, wherein the positions of wave-form edges are provided by a last of the sequential stages and said positions are expressed as numbers identifying reference sub-clocks needed for generating said wave-form edges.

7. The circuit claimed in claim 6, wherein:

inputs from the PCU are processed into a phase modification step further added to a period of the reference clock, in order to calculate the phase delay.

8. The circuit claimed in claim 6 upgraded into a parallel multiphase processor (PMP) by extending the time slot allowed for the micro-cycles of the synchronous sequential processor by a factor of P, wherein:

2-P stages are added to the original sequential stage and every one of the resulting 1-P parallel multiphase stages is clocked with a corresponding 1-P phase sub-clock, wherein such 1-P phase sub-clock begins during the corresponding to that phase 1-P cycle of the reference clock and has a cycle which is P times longer than the reference clock cycle;

whereby consecutive 1-P parallel multiphase stages have processing cycles overlapping by 1 cycle of the reference clock wherein every 1-P parallel processing stage has P times longer cycle time equal to the cycle time of the corresponding 1-P phase sub-clock used for timing that stage.

9. The parallel multiphase processor of claim 8, further comprising:

a parallel processing phase 2-P built with plurality of 2-P parallel multiphase stages which are connected serially and are driven by the phase sub-clocks belonging to the same 2-P phase.

10. The parallel multiphase processor of claim 9, further comprising:

a timing control circuit (TC) for performing time sharing assignments of a wave-form

synthesis tasks between the parallel processing phases based on decoding of reference clock counters or PCU outputs or feedback signals from next sequential stages.

11. The parallel multiphase processor of claim 9, further comprising:

inter-phase circuits for a transmittal of an output of a previous parallel multiphase stage to an input of a later parallel multiphase stage.

12. The circuit of the claim 11, wherein:

the transmittal is performed by re-timing the output of the earlier parallel multiphase stage by clocking that output into the input of the later parallel multiphase stage with the same phase sub-clock which drives all the rest of the later parallel multiphase stage.

13. The circuit of the claim 8, wherein:

the sequential processing stage or the parallel multiphase stage use an input selector, wherein the input selector selects a constant value or an output of the previous sequential stage or an output of the previous parallel multiphase stage or an output of the same stage;

the input selector is connected to an arithmometer and that arithmometer output is clocked into an output register of the sequential processing stage by one of the reference sub-clocks.

14. The circuit of the claim 13, wherein:

the input selector produces enabling signal for generating pulses which clock data into the output register of the earlier sequential stage or into the output register of the later sequential stage.

15. The circuit of the claim 13, wherein:

the output register of the earlier sequential stage is used for controlling operations of the later sequential stage or the output register of the later sequential stage is used for controlling operations of the earlier sequential stage.

16. A phase synthesizer providing programmable modifications of a phase of a synthesized clock by unlimited number of gate delays per a modification step with step resolution

matching single gate delay at steps frequencies ranging from 0 to 1/2 of maximum clock frequency, wherein:

a delay control circuit is connected to a programmable control unit (PCU) wherein the delay control circuit defines size and frequency of phase delay modifications of the synthesized clock versus a reference clock, the delay control circuit also having a terminal connected to reference sub-clocks generated by a reference propagation circuit or connected to odd/even sub-clocks generated by an odd/even phase selector;

the reference clock is connected to the reference propagation circuit consisting of serially connected gates wherein outputs of the gates generate the reference sub-clocks providing variety of phase delays versus the reference clock;

the reference sub-clocks are connected to an odd/even phase selector which splits the reference sub-clocks by generating separate odd sub-clocks and even sub-clocks, wherein the odd sub-clocks begin during odd cycles of the reference clock and the even sub-clocks begin during even cycles of the reference clock;

a clock selection register is loaded by the odd sub-clocks and by the even sub-clocks with the outputs of the delay control circuit, wherein the odd sub-clocks or the even sub-clocks beginning during an earlier cycle of the reference clock download outputs of the delay control circuit which select the even sub-clocks or the odd sub-clocks beginning during a later cycle of the reference clock for providing the synthesized clock;

an output selector is connected to the output of the clock selection register and to the outputs of the odd/even phase selector, wherein the output selector uses inputs from the clock selection register for selecting output of the odd/even phase selector which is passed through the output selector for providing the synthesized clock.

17. The circuit of claim 16, wherein the odd/even phase selector further comprises:

serially connected flip-flops, wherein a clock input of a first flip-flop is connected to the reference clock and a data input of a first flip-flop is connected to an inverted output of the first flip-flop while a clock input of any other Nth flip-flop is connected to an (N-1) output of the reference propagation circuit and a data input of the N flip-flop is connected to an output of the (N-1) flip-flop;

connected to the serially connected flip-flops an odd/even selector generating the odd sub-clocks which begin during every odd reference clock cycle and the even sub-clocks which begin during every even reference clock cycle, wherein the output of the 1st flip-

flop is used to select odd and even reference clocks while the output of the Nth flip-flop is used to select odd and even reference sub-clocks from the (N-1) output of the reference propagation circuit.

18. The circuit of claim 17 with the odd/even phase selector extended to a 1-P phase selector for splitting the reference sub-clocks into 1-P phase sub-clocks which begin during the corresponding 1-P cycles of the reference clock, the 1-P phase selector further comprising:

a parallel 1-P sub-clock counter built as an extension to the corresponding serially connected flip-flop, wherein the whole 1-P sub-clock counter is clocked by the reference sub-clock driving the original serially connected flip-flop wherein an output of the 1-P sub-clock counter represents a 1-P phase number of the clocking sub-clock;

a 1-P selector built as an extension to the corresponding odd/even selector, wherein the 1-P selector is connected to the 1-P sub-clock counter and to the corresponding reference sub-clock wherein outputs of the 1-P selector generate the 1-P phases of the corresponding reference sub-clock;

whereby all needed 1-P phases are generated for any one of the reference sub-clocks by extending the corresponding serially connected flip-flop with the 1-P sub-clock counter and extending the corresponding odd/even selector with the 1-P selector generating the needed 1-P phases of the reference sub-clock.

19. The circuit of claim 18, wherein:

the delay control circuit is implemented with the synchronous sequential processor of claim 6.

20. The circuit of claim 18, wherein:

the delay control circuit is implemented with the synchronous sequential processor of claim 7.

21. The circuit of claim 18, wherein:

the delay control circuit is implemented with the parallel multiphase processor of claim 8.

22. A programmable heterodyne timing system (HTS)) which is not limited to discrete sets of input/output frequencies but accepts a local reference clock of any frequency and accepts an external reference clock of any frequency while providing any required frequency of an HTS output clock and very low phase transients during any switching of reference clocks, wherein the HTS comprises:

a micro-controller (MC) for implementing a programmable phase transfer function (PTF) between a phase of the HTS output clock and a phase of a first reference clock, wherein the micro-controller controls operations of the phase synthesizer (PS) claimed in claim 16, the micro-controller has a terminal for a first phase error;

the PS connected to the micro-controller while the reference clock input of the PS is connected to the HTS output clock, wherein the synthesized clock of the PS is connected to a return input of an analog PLL (APLL);

the APLL having its reference input connected to the HTS output clock or to an APLL output clock while the return input of the APLL is connected to the synthesized clock, wherein an APLL output clock drives the HTS output clock;

a first digital phase detector (1DPD) receiving the first reference clock and the local reference clock or receiving the first reference clock and the synthesized clock or receiving the first reference clock and the HTS output clock, wherein the digital 1DPD produces the first phase error connected back to the micro-controller;

wherein said micro-controller uses its internal micro-operations for implementing filter functions of an on chip digital PLL (DPLL) by processing said first phase error into the micro-controller output driving the PS into producing the synthesized clock providing compliance of the APLL output clock and the HTS output clock with the phase transfer function defined by the PTF.

23. The circuit of claim 22 including reference selection means for alternative use of one of multiple connected reference clocks for producing the HTS output clock, the circuit of claim 22 further comprising:

a reference selector connected to multiple external reference clocks and controlled by the micro-controller, wherein the micro-controller selects one of the multiple reference clocks for being connected to the 1DPD which is read by the MC and used by MC subroutines for controlling the HTS output clock;

activity monitors for the external reference clocks for producing active/non-active output

signals connected to the micro-controller;

wherein the activity monitors output signals are read and processed by the microprocessor which is producing reference selection signals connected to the reference selectors.

24. The circuit of claim 22 including means supporting a VCXO jiitter filter for HTS applications which are extremely jitter sensitive, the circuit of claim 22 further comprising:

an analog phase detector (APD) having a reference input connected to the HTS output clock or to the APLL output clock while a return input of the APD is connected to an output clock of the VCXO jitter filter, wherein an output of the APD is used to drive a remaining circuit of the VCXO jitter filter.

25. The circuit of claim 22, further comprising:

an output clock generator (OCG) connected to the APLL output clock, wherein the OCG produces a plurality of HTS output clocks (F_{OUT}).

26. The circuit of claim 22, further comprising:

an output phase locked loop (OUT-PLL) referenced by the APLL output clock and producing the HTS output clock, wherein the OUT-PLL has a return input connected to the HTS output clock or to a frequency divider of the HTS output clock.

27. The circuit of claim 22, further comprising:

an output phase locked loop (OUT-PLL) referenced by the APLL output clock and producing a fundamental output clock, wherein the OUT-PLL has a return input connected to the HTS output clock;

an output clock generator (OCG) connected to the fundamental output clock, the OCG produces a plurality of the HTS output clocks (F_{OUT}) wherein one of the HTS output clocks is connected back to the return input of the OUT_PLL.

28. The circuit of claim 22 including an analog phase locked loop mode (APLL mode) of operation using a second reference clock (f_{R2}) as an external reference source which the HTS output clock is phase locked to, the circuit of claim 22 further comprising:

a reference selector connected to the APLL output clock and to the second reference clock or

to the HTS output clock and to the second reference clock wherein the reference selector is controlled by the MC and an output of the reference selector is connected to the APLL reference input, wherein the MC selects the second reference clock for the APLL mode while the MC selects the HTS output clock or the APLL output clock for the DPLL mode;

whereby during the APLL mode the HTS output is phase locked to the second reference clock wherein the PS is driven by a constant MC output maintaining a fixed frequency relation between the HTS output and the second reference clock.

29. The circuit of claim 28 including reference selection means for alternative use of one of multiple connected reference clocks for producing the HTS output clock, further comprising:

a first reference selector providing the first reference clock f_{R1} selected from a first set of reference clocks, the first reference selector connected to the first set of reference clocks and controlled by the micro-controller, wherein the micro-controller selects one of the first set clocks for being used for referencing the HTS output clock;

a second reference selector providing the second reference clock f_{R2} selected from a second set of reference clocks, the second reference selector connected to the second set of reference clocks and controlled by the micro-controller, wherein the micro-controller selects one of the second set clocks for being used for refrencing the HTS output clock;

activity monitors, for the first set clocks and for the second set clocks, for producing active/non-active output signals connected to the micro-controller;

wherein the activity monitors output signals are read and processed by the microprocessor producing reference selection signals connected to the first reference selector and to the second reference selector.

30. The HTS as claimed in claim 29, the HTS comprising:

interface circuits, for communication with an external control processor, connected to the external control processor and to the micro-controller;

wherein the interface circuits and the micro-controller enable the external control processor to read information about statuses of the activity monitors and to select an external reference clock or the local reference clock for referencing the HTS output clock.

31. The HTS as claimed in claim 30, wherein: the interface circuits and the micro-controller enable the external control processor to perform switching of mode of operation of the HTS between the APLL mode and the DPLL mode.

32. The HTS as claimed in claim 29, wherein: the micro-controller reads information about statuses of the activity monitors and selects an external reference clock or the local reference clock for referencing the HTS output clock.

33. The HTS as claimed in claim 29, wherein: the micro-controller performs switching of mode of operation of the HTS between the APLL mode and the DPLL mode.

34. The HTS as claimed in claim 33 wherein the MC performs a master/slave mode switching for maintaining phase alignment between an active HTS unit and a backup HTS unit installed in a back-plane for protection switching, the HTS comprising:

a master/slave subroutine reading activity monitor of a reference clock provided by a mate HTS unit and reading internal status of the own HTS unit;

wherein the master/slave subroutine performs switching to the master mode by selecting other reference clock than the mate's reference clock when the mate's reference clock becomes inactive or performs switching to the slave mode by selecting the mate's reference clock when the mate's reference clock is detected active during a power-up initialization of the own HTS unit.

FIG.1 Sequential Clocks Generator (SCG) and Output Selection Circuits (OSC)

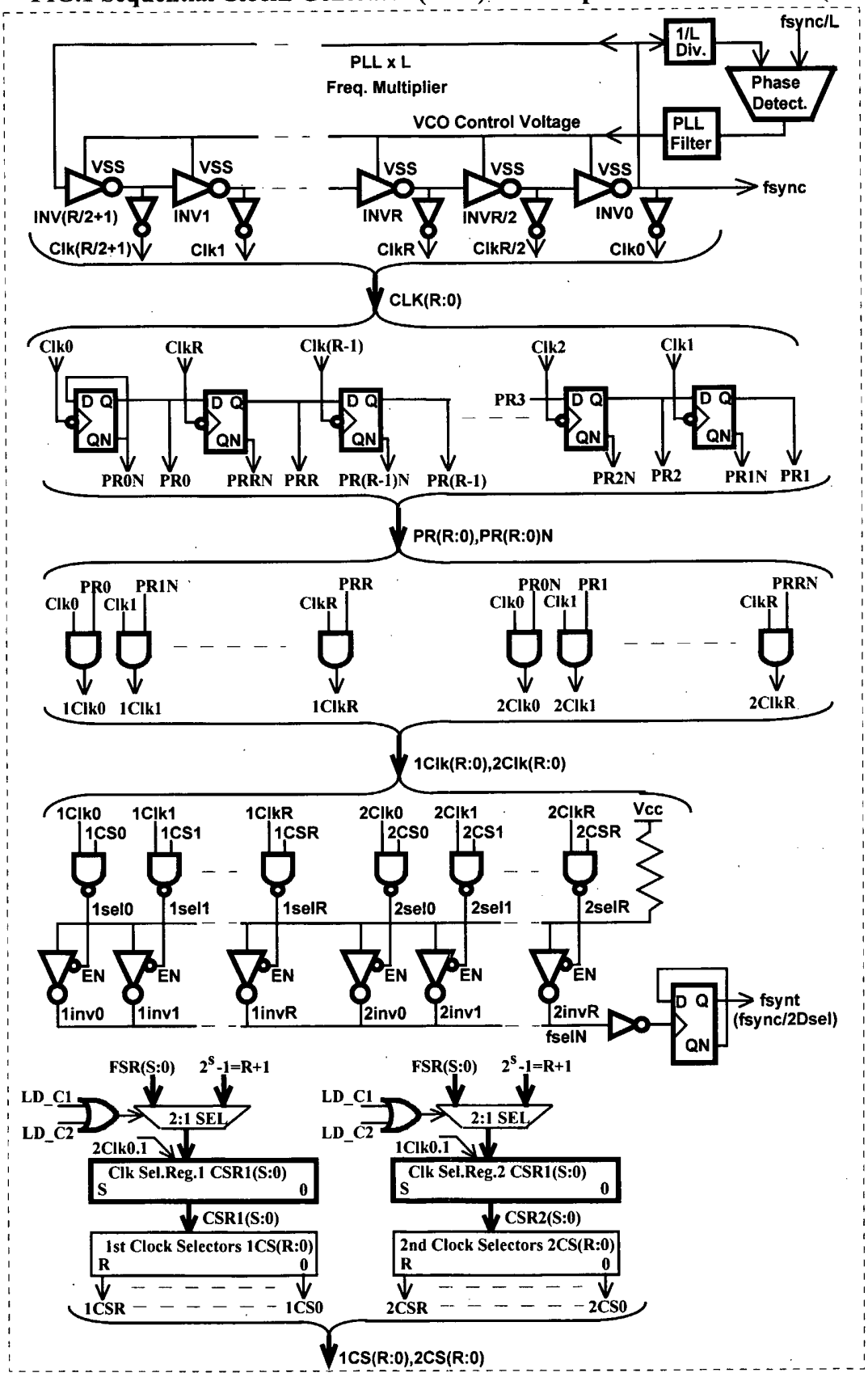


FIG.1A Sequential Clocks Generator (SCG) and Return Selection Circuits (RSC)

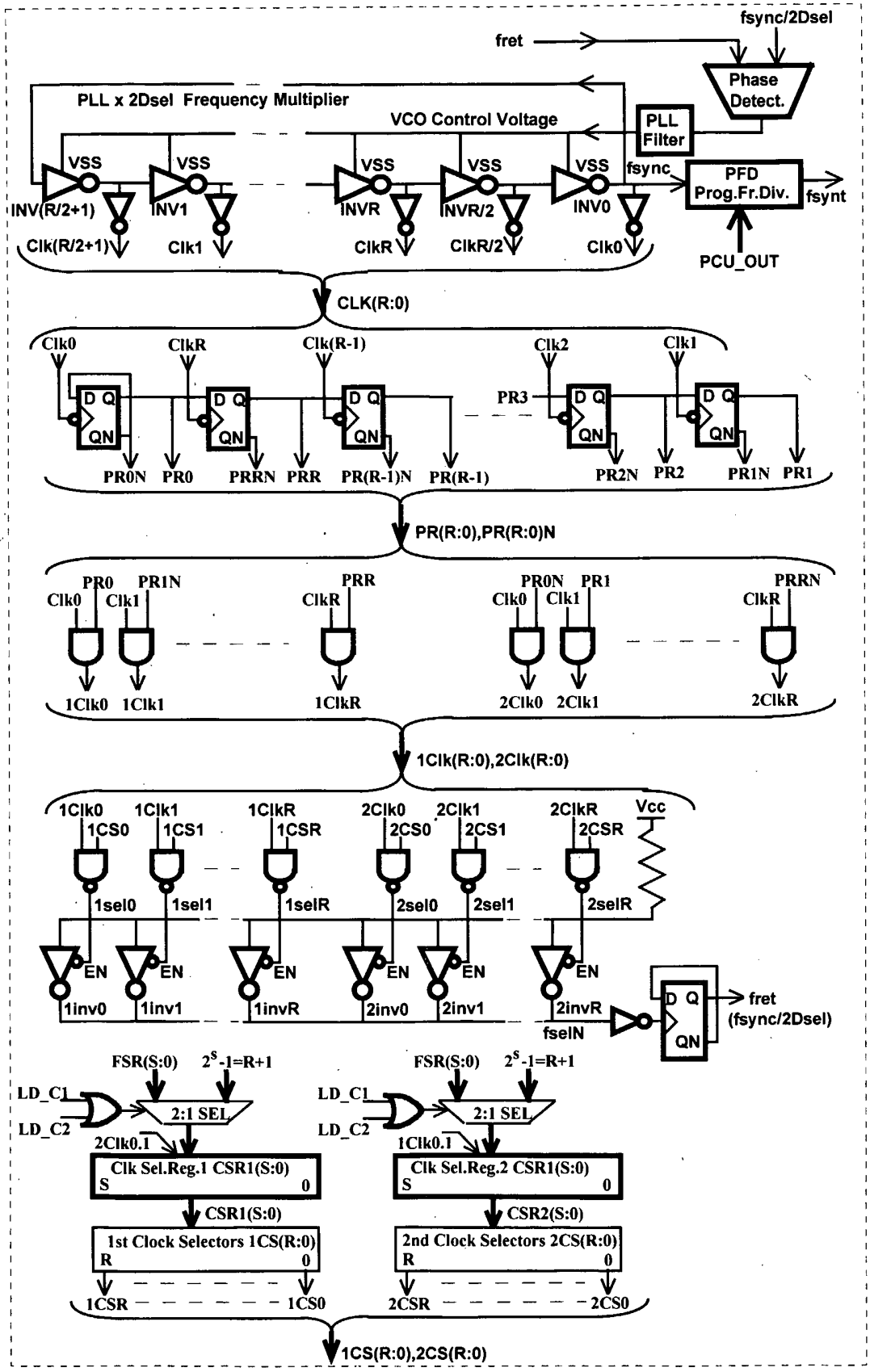


FIG.2 Timing Control (TC) and Clocks Equalization (CE)

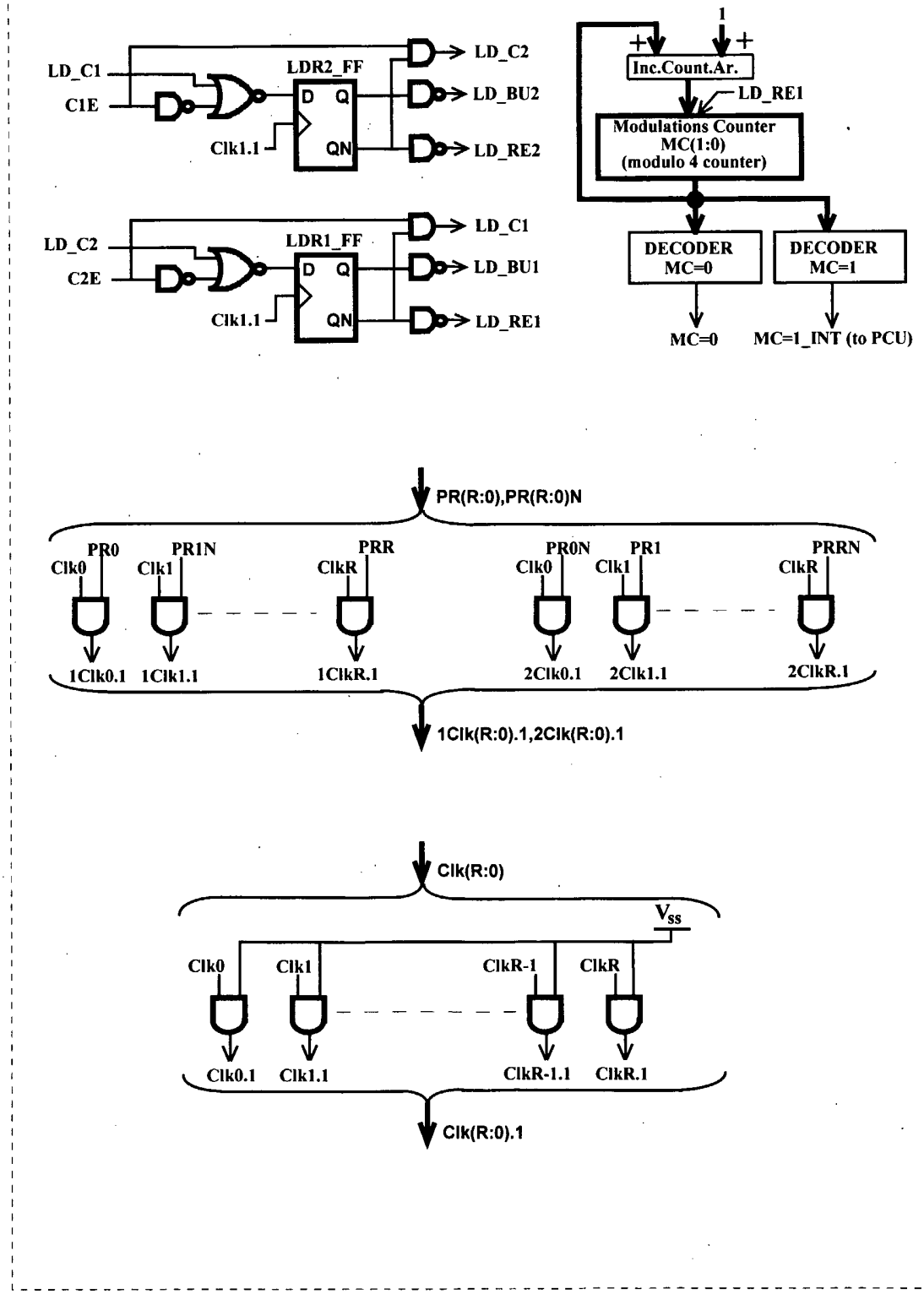


FIG.3 Synchronous Sequential Phase Processor (SSPP)

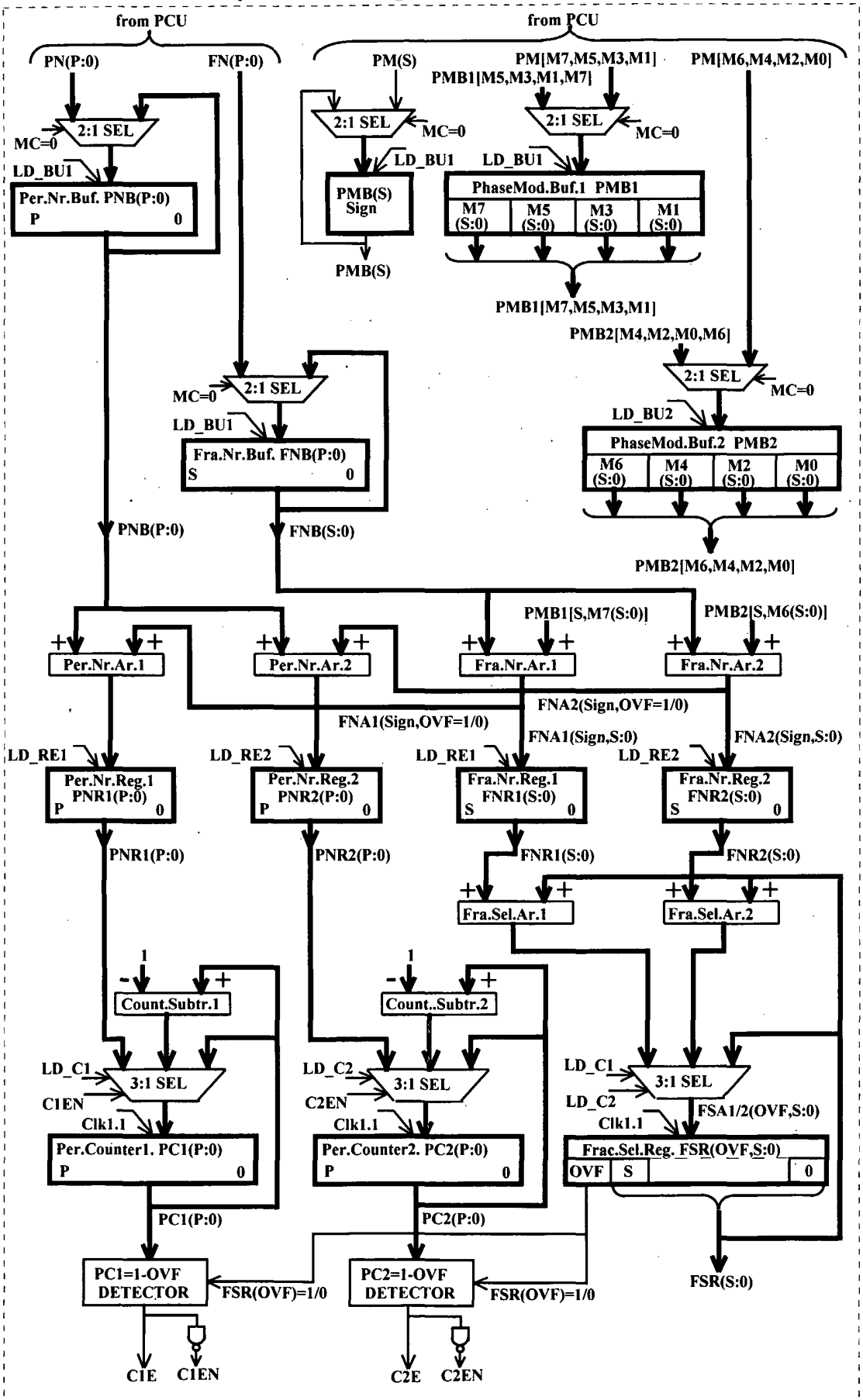


FIG.4 Heterodyne Timing System with Inherent VCXO Filter

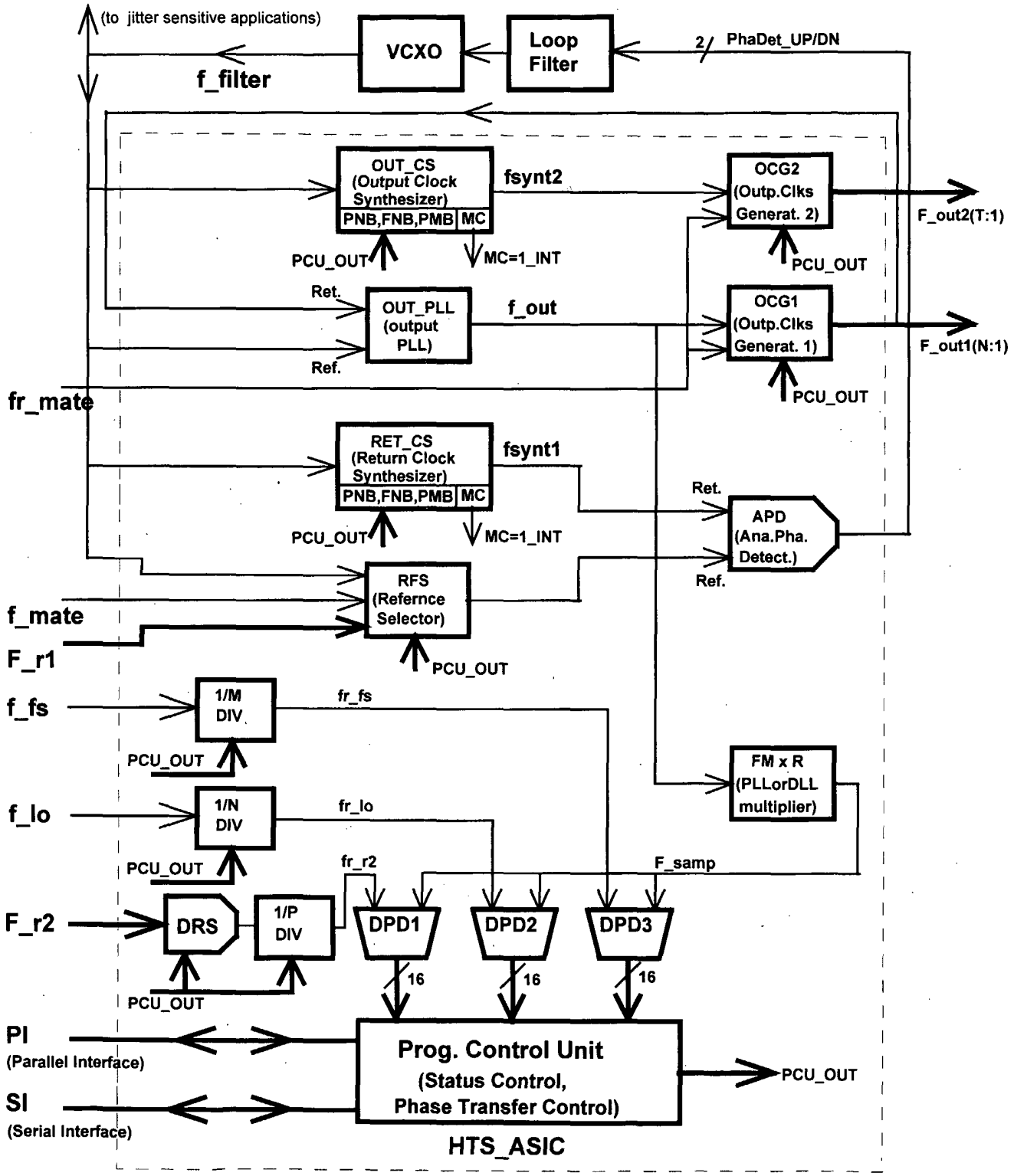


FIG.4A Heterodyne Timing System with Optional VCXO Filter

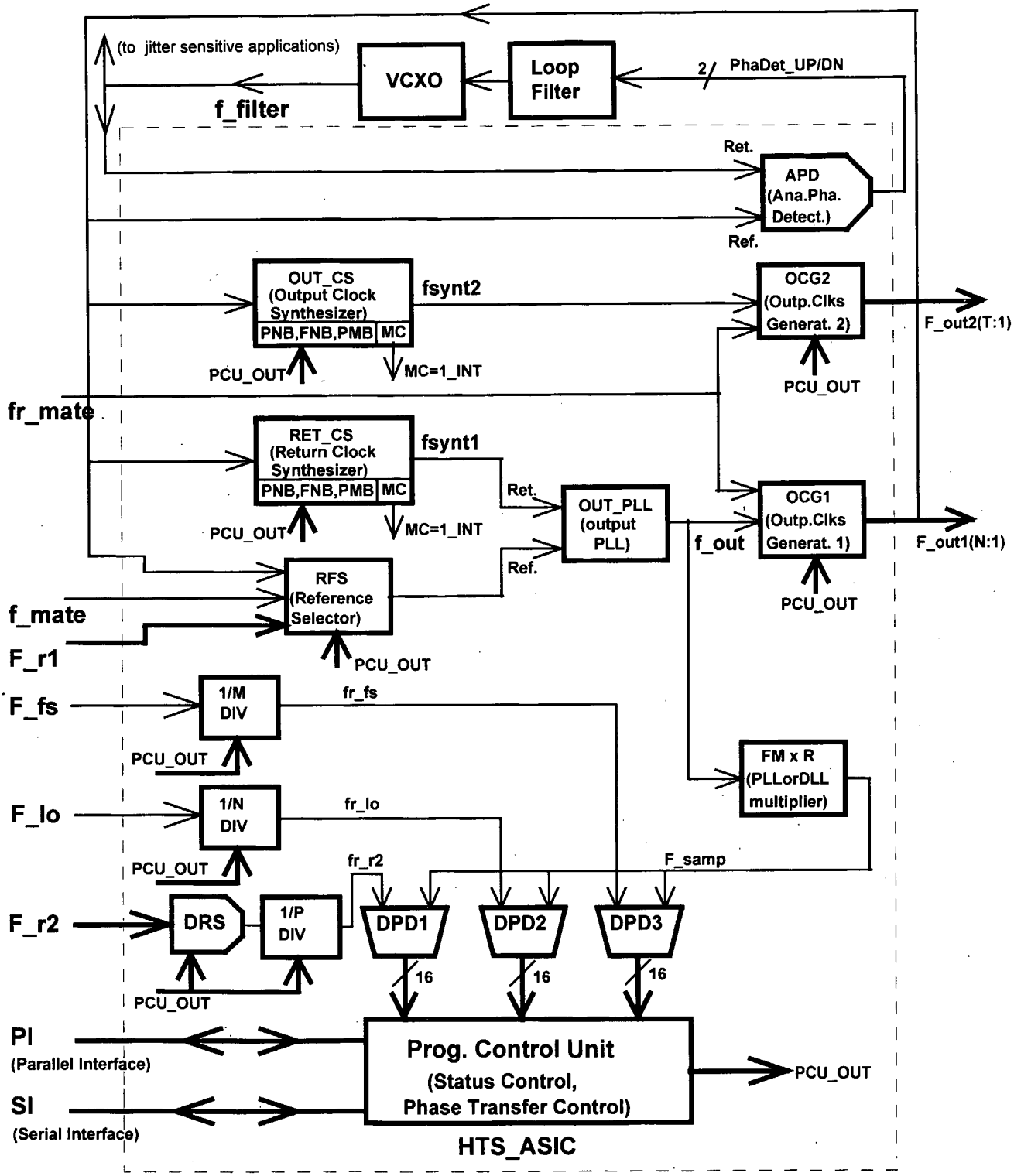
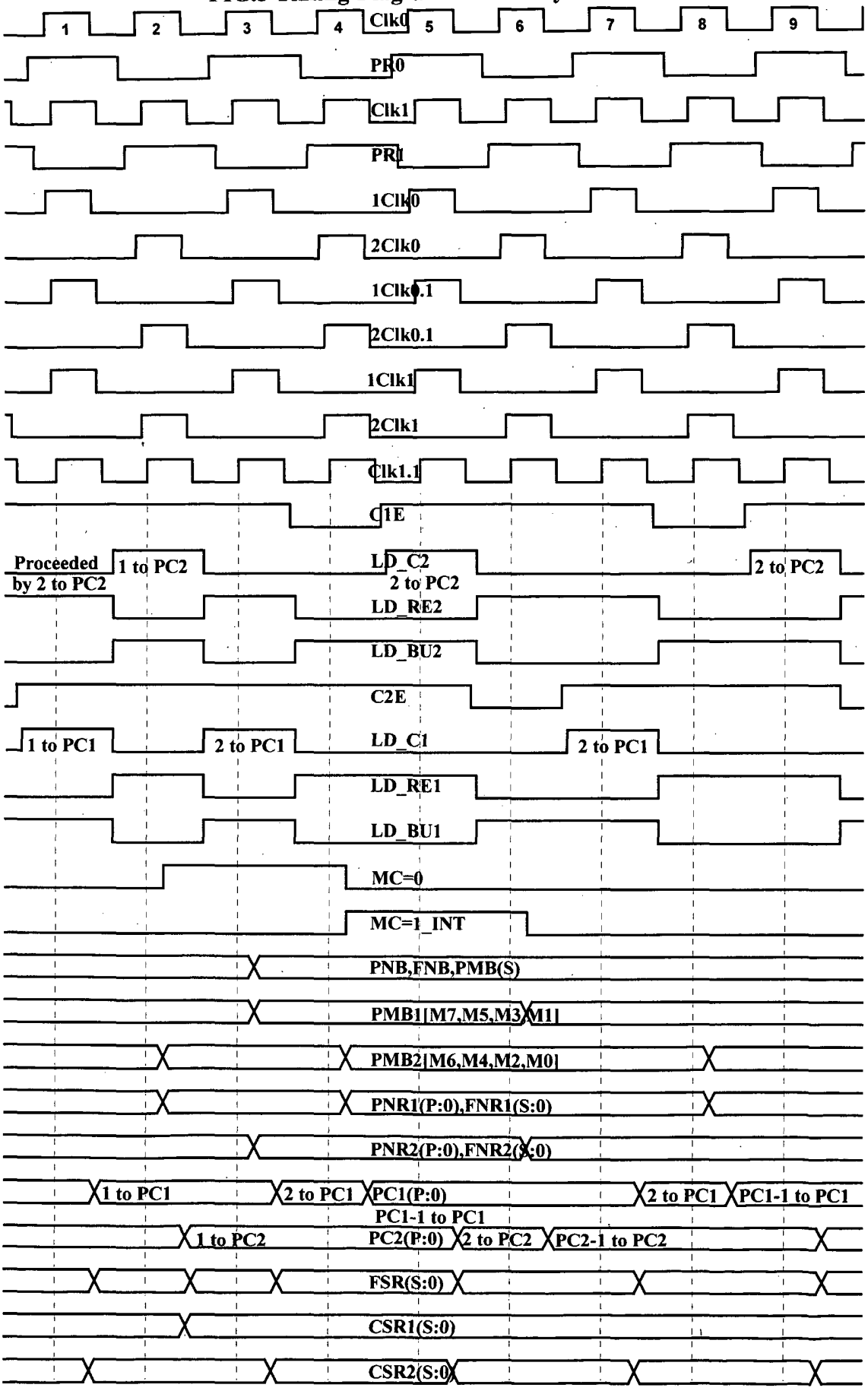


FIG.5 Timing Diagram of Phase Synthesizer



INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2005/000995

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7): H03L 7/06, G06F 1/04, H03L 7/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(7): HO3L 7/06, GO6F 1/04, HO3L 7/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Delphion, Canadian Patent Database, USPTO, (Keywords: heterodyne timing system, universal synchronization, hybrid pll, phase synthesizer, frequency synthesizer, phase selector, odd and even and phase selector)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	US 2005/0007203 (Chen) 13 January 2005 (13-01-2005) (abstract, paragraph[0009], [0011], [0024])	1-34
A	US 5,485,490 (Leung et al.) 16 January 1996 (16-01-1996) (abstract, column 3, lines 57-67 - column 4, lines 1-2)	1-34
A	WO 2004/002052 A1 (Bogdan) 31 December 2003 (31-12-2003) (whole document)	1-34

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 October 2005 (14-10-2005)	2 November 2005 (02-11-2005)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001(819)953-2476	Camran Syed (819) 934-4550

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of the first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons :

1. [ ] Claim Nos. :
because they relate to subject matter not required to be searched by this Authority, namely :

2. [ ] Claim Nos. :
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically :

3. [ ] Claim Nos. :
because they are dependant claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows :

Group A: **Claims 1-5** disclose an odd/even phase selector, the selector comprising a reference propagation circuit, and serially connected flip-flops configured in a particular way as to generate odd sub-clocks beginning every odd reference clock cycle and even sub-clocks beginning every even reference clock cycle.

Group B: **Claims 6-15** disclose a synchronous sequential processor (SSP) enabled to multiply processing speeds by splitting complex signal processing operations into singular micro-cycles.

Group C: **Claims 16-21** disclose a phase synthesizer capable of enabling programmable modifications to the phase of a synthesized clock.

Group D: **Claims 22-34** disclose a heterodyne timing system (HTS) capable of receiving a local reference clock of any frequency and an external clock of any frequency, and producing any required frequency for the HTS output clock.

1. [ ] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [X] As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claim Nos. :

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim Nos. :

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

[ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

[ ] No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/CA2005/000995

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US2005/0007203	13-01-2005	NA	NA
US5485490	16-01-1996	USRE38482E E1	30-03-2004
		US5596610 A	21-01-1997
		US5799051 A	25-08-1998
WO2004002052	31-12-2003	AU2003245142 A1	06-01-2004
		CA2389969 A1	25-12-2003
		EP1518346 A1	30-03-2005