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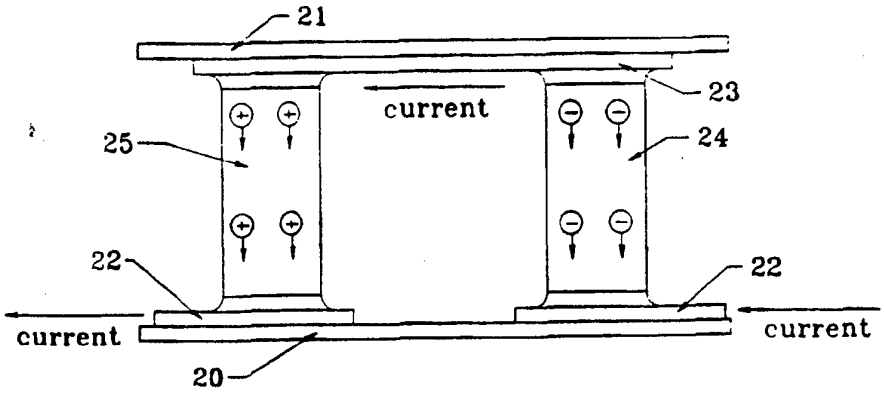

(57) Abstract

An apparatus and method of manufacturing a thermoelectric module is provided. A first electrically conductive pattern (22) is defined on a first substrate (20) and a second electrically conductive pattern (23) is defined on a second substrate (21). Alternating bars (54, 55) of a first thermoelectric material and a second thermoelectric material are arranged parallel to each other. The bars are fixed into place on the first conductive pattern by an effective thermal and electrical connection with the conductive pattern. One such connection means is soldering. Then the bars are separated into elements (64, 65). The second substrate is positioned over the elements and fixed to the elements to complete the manufacture of the TEM.

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AN IMPROVED METHOD OF MANUFACTURE AND RESULTING THERMOELECTRIC MODULE

BACKGROUND OF THE INVENTION

The present invention is related to solid-state electronic heat pumps, known as thermoelectric modules (TEMs), and to their manufacture. More particularly, the present invention is related to an improved manufacturing method so that TEMs can be manufactured at lower cost. The resulting TEM is also improved and can operate at high performance and efficiency.

A thermoelectric module is typically formed by an electrical circuit of elements of alternating types of thermoelectric materials, which are connected in series. Each thermoelectric material element has two sides, one side connected to a higher voltage than the other side, when the module is in operation. Physically the thermoelectric material elements are arranged so that the hot sides of thermoelectric material elements define one side of the TEM and the cold sides of the elements define the other side of the TEM.

Operationally, as current is driven through the TEM, the electronic carriers in the thermoelectric material elements carry thermal energy from one direction to the other. In other words, the TEM is a heat pump which transfers heat by electric current. There are no moving parts, as in the case of a mechanical heat pump.

Present TEM manufacturing methods require skilled technicians to arrange the thermoelectric material elements during manufacture. To replace this manual assembly, other methods have been attempted, including automation, robots, and mechanical spacing aids, without much success.

Besides high manufacturing costs, a problem with these conventionally manufactured TEMs has been that the operating point of maximum cooling power is substantially different from the operating point of maximum coefficient of performance. That is, at maximum cooling, the TEM does not operate at peak efficiency. The result is that, for a particular application which limits the number of TEMs, a large, expensive power supply is required to drive the TEMs at high power and low efficiency. Alternatively, where the constraint on the number of TEMs is removed, a less expensive power supply can drive an increased number of TEMs at lower power and higher efficiency. Neither alternative is satisfactory. In one case, increased costs go toward the power supply. In the other case, the increased costs go toward the additional TEMs, which occupy more space.

Efforts to overcome this problem appear to be directed toward the development of new thermoelectric materials which have higher maximums in cooling power or coefficient of performance. In contrast, a TEM manufactured with present thermoelectric materials increases its cooling power so that a much greater cooling power according to the present invention is reached around the maximum coefficient of performance. As new thermoelectric materials are developed, a TEM with the improved performance according to the present invention should also be correspondingly improved.

The present invention permits for a superior arrangement of such elements without skilled technicians.

SUMMARY OF THE INVENTION

For such improvement, the present invention provides for a method of manufacturing a thermoelectric module. A first electrically conductive pattern is defined on a first substrate and a second electrically

conductive pattern is defined on a second substrate. Alternating bars of a first thermoelectric material and a second thermoelectric material are arranged parallel to each other. The bars are fixed into place on the first conductive pattern by an effective thermal and electrical connection with the conductive pattern. One such connection means is soldering. Then the bars are separated into elements. The second substrate is positioned over the elements and fixed to the elements to complete the manufacture of the TEM.

The result is an improved thermoelectric module which has a first substrate having a surface bearing a first electrically conductive pattern, a second substrate having a surface opposing said first substrate surface and bearing a second electrically conductive pattern, and an array of first and second thermoelectric material elements are arranged between the surfaces of said first and second substrates. Each first and second material element has a first side contacting the first conductive pattern and a second side contacting the second electrically conductive pattern. The first and second conductive patterns are arranged with respect to the array to form one or more electrical circuits of serially connected first and second thermoelectric material elements, with the first and second material elements alternating in the circuit. The array is arranged in alternating rows of first and second thermoelectric material elements, with each element in a row spaced apart from a neighboring element in the row by less than 0.010 inch. Thus more first and second material elements may be placed between the surfaces of the first and second substrates to form an improved thermoelectric module, with a higher cooling power at the maximum coefficient of performance.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a representative circuit of a thermoelectric module(TEM).

Fig. 2A is a bottom assembly of a TEM in the prior art; Fig. 2B is the top assembly of the TEM in Fig. 2A.

Fig. 3 is a cross-sectional view of part of combined assemblies of the TEM in Figs. 2A and 2B.

Fig. 4 is a combined representative graph which plots the current through a TEM versus its cooling power and the current versus the coefficient of performance. A prior art TEM and a TEM according to the present invention are illustrated in the graph of Fig. 4.

Fig. 5 is an arrangement of bars of thermoelectric material used in the manufacture of TEMs according to the present invention.

Fig. 6A is a bottom assembly of a TEM according to one embodiment of the present invention; Fig. 6B is the top assembly of the TEM in Fig. 6A.

Fig. 7 is a graph of the cooling power versus the thickness of the thermoelectric materials in a TEM.

Fig. 8A is a bottom assembly of a TEM according to another embodiment of the present invention; Fig. 8B is the top assembly of the TEM in Fig. 8A.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT(S)

Fig. 1 is a representative diagram of the electric circuit of a TEM. A TEM has two terminals 12 and 13, between which are connected several thermoelectric elements 10 and 11. In the TEM the elements 10 and 11 are connected in series alternately. The elements 10 are of one type of thermoelectric material and the elements 11 are of another type. Typically semiconductor material is used where one type

is doped with N-type impurities and the other type doped with P-type impurities.

The thermoelectric elements 10 and 11 are arranged in such a manner that the electronic carriers in the elements 10 and 11 work cooperatively with each other to heat or cool one side or the other of a TEM. The structure of a TEM will become apparent below. Present TEM manufacturing methods, which are virtually the same, require skilled manual labor.

In a conventional TEM, electrically conductive patterns are first placed on ceramic substrates, as shown in Figs. 2A and 2B, which respectively illustrate top and bottom assemblies of a partially completed TEM. In Fig. 2A the substrate 20 has a pattern 22. Fig. 2B more clearly illustrates the pattern 23 on the substrate 21. Ceramic alumina roughly 0.025 inch thick is commonly used for the substrates 20 and 21, and the patterns 22 and 23 are printed copper on the substrates 20 and 21. The outer dimensions of the alumina substrates are dictated by the total cooling needed. The range in substrate length in one direction is from about 0.250 inch up to about 2 inches per side. The typical length is about 1 inch.

An array of thermoelectric elements 24 and 25 is placed onto a sheet of solder (not shown) which covers one of the conductive patterns, shown as the pattern 22 on the bottom substrate 20. The elements 24 and 25 are formed from semiconducting crystal ingots, each several inches in diameter and 2-3 feet long. Each cylindrically-shaped ingot is doped with an impurity with a resulting excess of electrons (N-type material) or deficiency of electrons (P-type material). The ingots are then cut into disks and then into cube-shaped P-type elements 25 and N-type elements 24, roughly 0.100 inch on a side. These elements are positioned by highly trained

technicians with the aid of tweezers and a microscope, one at a time, on the pattern 22.

This bottom assembly is heated in an oven or on a hot plate until the sheet melts, bonding the thermoelectric elements 24 and 25 to the pattern 22.

Finally, the top assembly of the substrate 21 and pattern 23, which is also covered with a sheet of solder, shown in Fig. 2B is positioned and aligned with the assembly shown in Fig. 2A. The top and bottom assemblies are reheated to bond the two assemblies together.

A side view in Fig. 3, of part of the completed assembly, illustrates the operation of the TEM. The conductive pattern 22 on the bottom substrate 20 is attached to the bottoms of N-type unit 24 and P-type unit 25. The pattern 22 is such that the bottoms of two elements 24 and 25 are not connected. On the other hand, the conductive pattern 23 on the top substrate 21 connects the tops of the two neighboring elements 24 and 25. In operation, a current is driven through the circuit formed by the assembly. As shown, the current enters the bottom of the N-type unit 24 and exits its top. The current then travels through the pattern 23 on the top substrate 21 to enter the top of the P-type unit 25 and exits its bottom to the next N-type unit connected to the conductive pattern 22. The complete assembly forms a single, series-type circuit of alternating P-type and N-type semiconducting elements 24 and 25, as represented in Fig. 1.

The majority electronic carriers (which are also the thermal carriers) in the elements 24 and 25 travel in the same direction so that thermal energy is transferred from one substrate to the other. In Fig. 3 thermal energy is transferred by the majority carriers from the substrate 21 to the substrate 20, i.e.,

substrate 21 is cooled and substrate 20 is heated. Heat is pumped from one side of the TEM to the other. Note that if the current is reversed, then direction of travel of the majority electronic carriers is reversed and the direction of the heat transfer is also reversed.

There are several major drawbacks to this labor-intensive method. A first drawback is that the individual handling of the very fragile thermoelectric elements 24 and 25 requires that they be sufficiently large to withstand being grasped and handled. This limits the number of individual elements that can be placed in a given area.

Another drawback is that the elements 24 and 25 must be spaced a sufficient distance from one another to ensure that the array is not disturbed as new elements 24 and 25 are added and positioned on the ceramic substrate 20. This further reduces the number of elements that can be placed within a given area and limits any assembly method that is based on the individual handling of elements.

Still another drawback is that the P-type material and the N-type material appear identical to each other. Hence, an element of the wrong type can be placed in a particular position. Since the carriers now travel in the wrong direction, heat flow for this element is in the wrong direction, lowering the total net heat flow of the module.

Manual handling places a practical limit of the number of the elements 24 and 25 which can be assembled. For practical reasons, the size of the substrates cannot be increased indefinitely. As the array of elements become larger, the chances of human error increases markedly. Thus there are presently no TEMs with a total number of elements greater than about 300.

Finally, manual handling of the elements also forces the thickness of each unit to be at least 0.040 inch. Typically the elements 24 and 25 are 0.080 inch or more thick. However, as the thickness of the elements increases, the coefficient of performance (COP), explained below, attains its maximum value at lower and lower cooling powers. Conversely, with a decrease in thickness, the cooling power at maximum COP improves until parasitic effects become significant.

The present invention overcomes these drawbacks. Within the same dimension of a TEM, the number of active thermoelectric elements is increased and the thickness of the elements is optimized. The result is a significantly improved TEM which can operate with cooling power greater than that of a conventional TEM, and at maximum COP.

As stated above, the present invention does not require the development of new thermoelectric materials. Rather, the present invention improves the performance of TEMs with existing materials.

In accordance with the present invention, the semiconducting crystal cylinders are formed in the same manner as described above. The cylinders are cut into disks approximately 0.020 inch thick. The disks are then cut into bars, approximately 0.100 inch wide, and up to 3 inches long. This width is selected as a balance between the fragility of the semiconductor crystal and the desire to increase the number of elements.

The semiconductor bars are then arranged, as shown in Fig. 5, in an alternating NPNP pattern on a ceramic substrate 60, which has an electrically conductive pattern 62, shown in Fig. 6A. The pattern 62 is covered with a solder sheet. The bars 54 and 55 are soldered into place by a hot plate or an oven. A slitting saw is first used to create a well-defined,

narrow gap between the alternating bars. The bars are then separated in-situ into individual N-type elements 64 and P-type elements 65 respectively, by a slitting saw running perpendicular to the previous movements of the slitting saw. A similar technique is used to separate a semiconductor wafer into integrated circuits. Typically such saw blades are less than 0.010 inches wide. Besides a slitting saw, a cutting laser may also be used to separate the bars 54 and 55 from each other, and to separate the bars 54 and 55 into the elements 64 and 65. The assembly of separated elements 64 and 65 are shown in Fig. 6A. At this point, it may be desirable to fill the gaps with an electrically and thermally insulating material.

Then an upper ceramic substrate 61 with a electrically conductive pattern 63 complementary to the pattern 62, shown in Fig. 6B, is arranged and placed over the substrate 60 and elements 64 and 65. A sheet of solder over the pattern 63 is not shown. As described with respect to a conventional TEM, the substrates 60 and 61 are bonded together to form the completed TEM.

In the manufacturing process, the size of the bars and their close arrangement allow for greater automation. This reduces labor costs and associated errors induced when assembly is performed manually.

The TEM of the present invention has many advantages in performance. The use of a thin slitting saw greatly reduces the space between the thermoelectric elements 64 and 65. This raises the percentage of the ceramic substrates 60 and 61 which are covered by the elements 64 and 65. This percentage is related to the amount of area of a substrate which is devoted toward heat transfer. The greater the area the better the cooling performance. For small TEMs, this percentage is approximately 70%; for larger TEMs, this percentage can

exceed 90%. Additionally, the thermoelectric elements are at the optimum operational thickness.

Operational parameters for a TEM include the input power, the amount of energy used to drive the TEM; the cooling power, the amount of energy transferred by the TEM in a unit of time; and the coefficient of performance (COP), the ratio of cooling power to input power. It should be noted that the term, "cooling power," is used because many of the applications contemplated are for refrigeration by the TEM. Since a TEM may used for heating purposes, the term, "heating power," could be also used.

Fig. 4, which shows the relationships between the cooling power, P_c, and the coefficient of performance, COP, versus current, illustrates the performance of a typical present-day TEM. The data for the typical module is derived from a common, commercially available TEM. Note that the maximum cooling power, defined in Fig. 4 as P_{cmax}, occurs at a particular current, defined in Fig. 4 as I_{maxp}. Note also that the operating point for maximum cooling power is displaced laterally from the point of maximum coefficient of performance, i.e., maximum cooling is achieved at the expense of efficient power consumption.

The performance of a TEM according to the present invention having the same ceramic substrate dimensions is also shown in Fig. 4. For the same input power which produced the maximum cooling power in the present, conventional TEM, the cooling power in the inventive TEM has now been increased by over a factor of three, while occupying less volume.

This improved performance arises from the greater number of thermoelectric elements. For the present TEM, the individual elements occupy 73.5% of the TEM area, rather than the 31.1% in the typical TEM.

Also, the thickness of the elements has been reduced. The result is to significantly increase cooling power at the operation point of maximum COP.

Quantitatively, the cooling power, the amount of energy transferred in a unit of time, of a TEM is shown by the following equation:

$$P_c=sIT_c-1/2RI^2-C(T_h-T_c)$$

The equation further reduces to:

$$P_c=sIT_c-1/2(\rho h/w_1w_2)nI^2-(kw_1w_2/h)n(T_h-T_c)$$

where

P_c = heat absorbed at the cold side of the TEM

s = Seebeck coefficient, a basic property of the TEM material

I = current through the TEM

T_c = temperature of the cold side of the TEM

T_h = temperature of the hot side of the TEM

R = electrical resistance of the TEM

C = thermal conductance of TEM

ρ = the resistivity of the TEM material

h = the thickness of each thermoelectric element

w_1 = the length of the element in a first direction parallel to the substrates

w_2 = the length of the element in a second direction perpendicular to the first direction and parallel to the substrates

k = the thermal conductivity of the TEM material

n = total number of thermoelectric elements in the TEM

Thus for the same current, I, P_c is increased by increasing the number of elements, n, and decreasing the thickness of the elements, h, from the present norm of 0.080 inches. In fact, the h has been reduced to 0.020 inch, the optimum thickness in view of increased parasitic effects due to smaller thicknesses. Fig. 7 plots P_c as a function of element thickness for a constant input power.

Note that in the TEM illustrated by the partial lower assembly in Fig. 6A, the top and bottom rows of the P-type elements 65 have alternating empty spaces in the array. This allows the TEM to be manufactured according to the present invention. Nonetheless, these spaces reduce the active area used for heat transfer.

An alternative embodiment of the present invention removes these spaces. A thermoelectric element can be split into two and still retain the same performance as the original, as long as the two halves are connected in parallel. As shown in Fig. 8A, P-type half-width elements 85A are placed at the top and bottom edges where the circuit reverses direction. In the manufacturing process, half-width bars are arranged at the top and bottom of the full-size bars 54 and 55. The half-width elements 85A are separated by a slitting saw with the other elements 64 and 65. Of course, the patterns 82 and 83 are respective modifications of the patterns 62 and 63. The modified patterns 82 and 83 also connect the half-width elements 85A, besides the same connections as represented in Fig. 1.

While the above is a complete description of the preferred embodiments of the present invention, various alternative, modifications and equivalents may be used. It should be evident that the present invention is equally applicable by making appropriate modifications to the embodiments described above. Therefore, the above

description should not be taken as limiting the scope of the invention which is defined by the metes and bounds of the appended claims.

WHAT IS CLAIMED IS:

1. An improved thermoelectric module comprising:

a first substrate having a surface bearing a first electrically conductive pattern;

a second substrate having a surface opposing said first substrate surface and bearing a second electrically conductive pattern;

an array of first and second material elements between said surfaces of said first and second substrates, each first and second material element having a first side contacting said first conductive pattern and a second side contacting said second electrically conductive pattern, said first and second conductive patterns arranged with respect to said array to form an electrical circuit of said first and second material elements serially connected, said first and second material elements alternating in said circuit, said array arranged in alternating rows of first and second material elements, each element in a row spaced apart from a neighboring element in said row by less than 0.010 inch;

whereby said first and second material elements cover a larger fraction of the area of said surfaces of said first and second substrates to form an improved thermoelectric module with a larger cooling power at the maximum COP.

2. The improved thermoelectric module of claim 1 wherein each of said first and second material elements has a thickness defined as the distance between said first side and said second side, and said thickness is less than 0.050 inch.

3. The improved thermoelectric module of claim 2 wherein said thickness is approximately 0.020 inch.

4. The improved thermoelectric module of claim 1 wherein said first substrate surface has an area, and first and second material elements cover more than 50 percent of said area.

5. The improved thermoelectric module of claim 4 wherein said first and second material elements cover more than 70 percent of said area.

6. An improved thermoelectric module comprising:

a first substrate having a surface bearing a first electrically conductive pattern;

a second substrate having a surface opposing said first substrate surface and bearing a second electrically conductive pattern;

an array of first and second material elements between said surfaces of said first and second substrates, each first and second material element having a first side contacting said first conductive pattern and a second side contacting said second electrically conductive pattern, said first and second conductive patterns arranged with respect to said array to form an electrical circuit of said first and second material elements serially connected, said first and second material elements alternating in said circuit, said array arranged in alternating rows of first and second material elements, each of said first and second material elements having a thickness defined as the distance between said first side and said second side, and said thickness is less than 0.050 inch;

whereby more first and second material elements form a thermoelectric module with a larger cooling power at the maximum coefficient of performance.

7. The improved thermoelectric module of claim 6 wherein the number of said first and second material elements exceed 300.

8. The improved thermoelectric module of claim 7 wherein said thickness is approximately 0.020 inch.

9. The improved thermoelectric module of claim 8 wherein each element in a row is spaced apart from a neighboring element in said row by less than 0.010 inch.

10. A partially completed workpiece for improved thermoelectric module comprising

a first substrate having a surface bearing a first electrically conductive pattern;

a second substrate having a surface opposing said first substrate surface and bearing a second electrically conductive pattern;

an array of first and second material elements between said surfaces of said first and second substrates, each first and second material element having a first side contacting said first conductive pattern and a second side contacting said second electrically conductive pattern, said first and second conductive patterns arranged with respect to said array to form an electrical circuit of said first and second material elements serially connected, said first and second material elements alternating in said circuit, said array arranged in alternating rows of first and second material

elements, each of said first and second material elements having a thickness defined as the distance between said first side and said second side, and said thickness is less than 0.050 inch;

whereby more first and second material elements form a thermoelectric module with a larger cooling power at the maximum coefficient of performance.

11. An improved thermoelectric module comprising

a first substrate having a surface bearing a first electrically conductive pattern;

a second substrate having a surface opposing said first substrate surface and bearing a second electrically conductive pattern;

an array of first and second material elements between said surfaces of said first and second substrates, each first and second material element having a first side contacting said first conductive pattern and a second side contacting said second electrically conductive pattern, said first and second conductive patterns arranged with respect to said array to form an electrical circuit of said first and second material elements serially connected, said first and second material elements alternating in said circuit, said array arranged in alternating rows of first and second material elements, each element in a row spaced apart from a neighboring element in said row by slicing said elements apart;

whereby more first and second material elements may be placed between said surfaces of said first and second substrates to form a thermoelectric module with a larger cooling power at the maximum coefficient of performance.

12. The improved thermoelectric module of claim 11 wherein said elements are sliced apart by mechanical means.

13. The improved thermoelectric module of claim 11 wherein said elements are sliced apart by a laser.

14. The improved thermoelectric module of claim 11 wherein each of said first and second material elements has a thickness defined by the distance between said first side and said second side, and said thickness is less than 0.050 inch.

15. The improved thermoelectric module of claim 14 wherein said thickness is approximately 0.020 inch.

16. The improved thermoelectric module of claim 11 wherein said first and second material elements have a width perpendicular to said rows of said elements, and elements in the top and bottom row of said array have a width less than that of elements in said remaining rows of said array.

17. The improved thermoelectric module of claim 16 wherein said elements in said top and bottom row of said array have a width approximately one-half of that of the remaining elements.

18. A method of manufacturing an improved thermoelectric module, comprising

defining a first electrically conductive pattern on a first substrate;

defining a second electrically conductive pattern on a second substrate;

placing alternate and parallel bars of first thermoelectric material and second thermoelectric material in close proximity to each other;

connecting said bars to said first conductive pattern;

separating said bars into elements;

placing said second substrate over said elements;

connecting said elements to said second conductive pattern;

whereby an improved thermoelectric module with an increased number of elements is formed.

19. The improved thermoelectric module manufacturing method of claim 18 comprising slicing apart said elements with a saw.

20. The improved thermoelectric module manufacturing method of claim 18 comprising defining said bars with a thickness less than 0.080 inch.

21. The improved thermoelectric module manufacturing method of claim 20 comprising defining said bars with a thickness of approximately 0.020 inch.

22. The improved thermoelectric module manufacturing method of claim 18 wherein in said placing step, bars are placed at the top and bottom of said alternate and parallel bars, said top and bottom bars having a width approximately one-half that of the remaining bars.

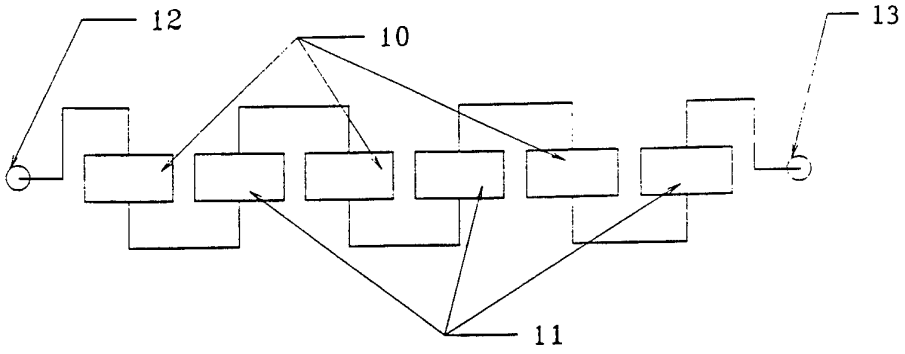


Fig. 1

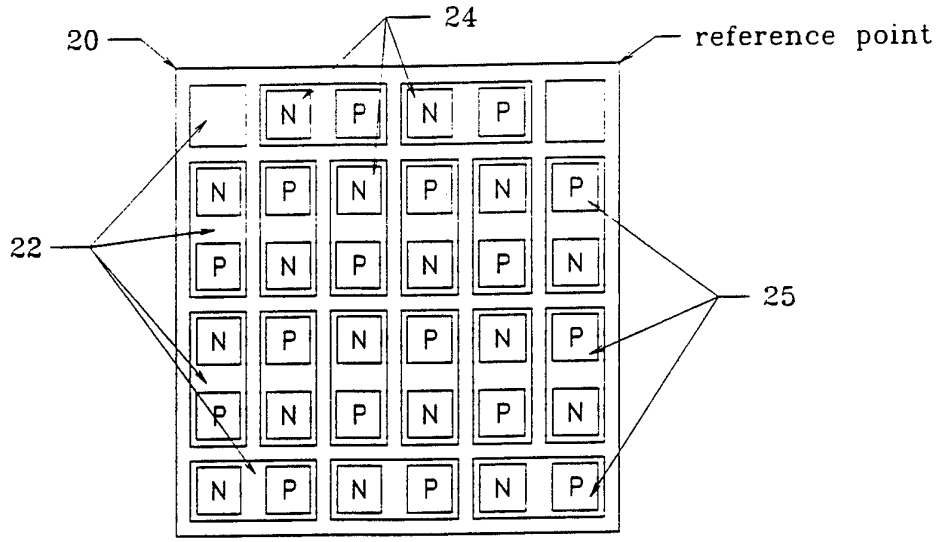


Fig. 2A

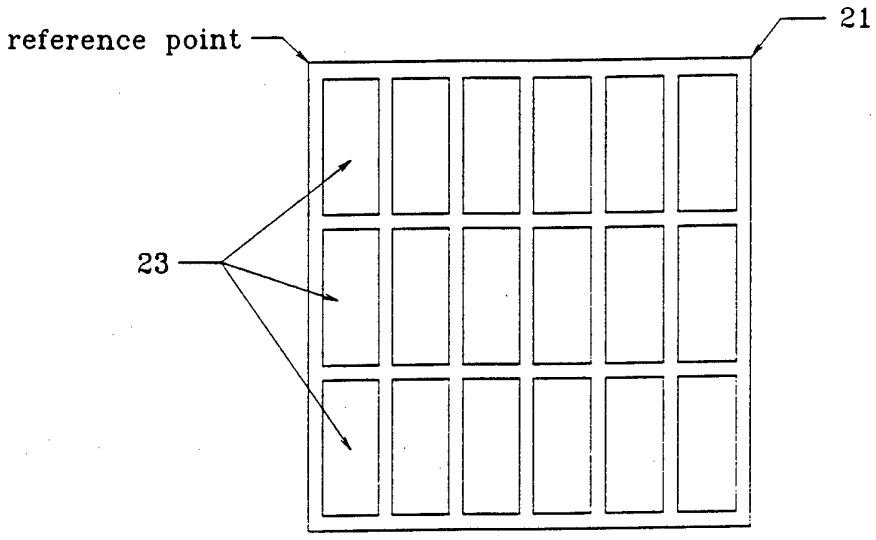


Fig. 2B

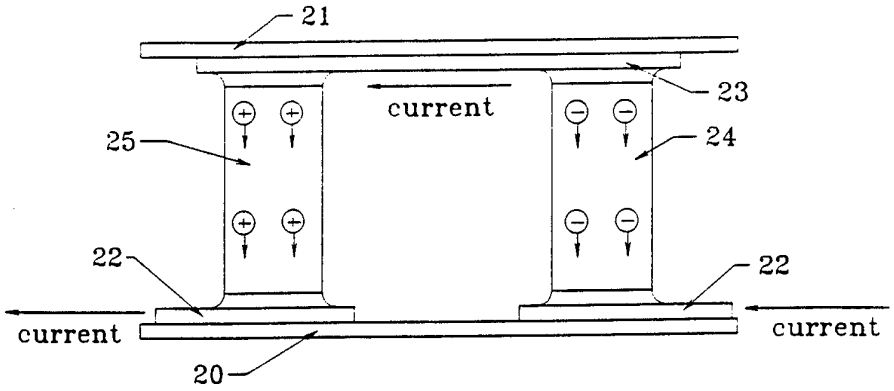
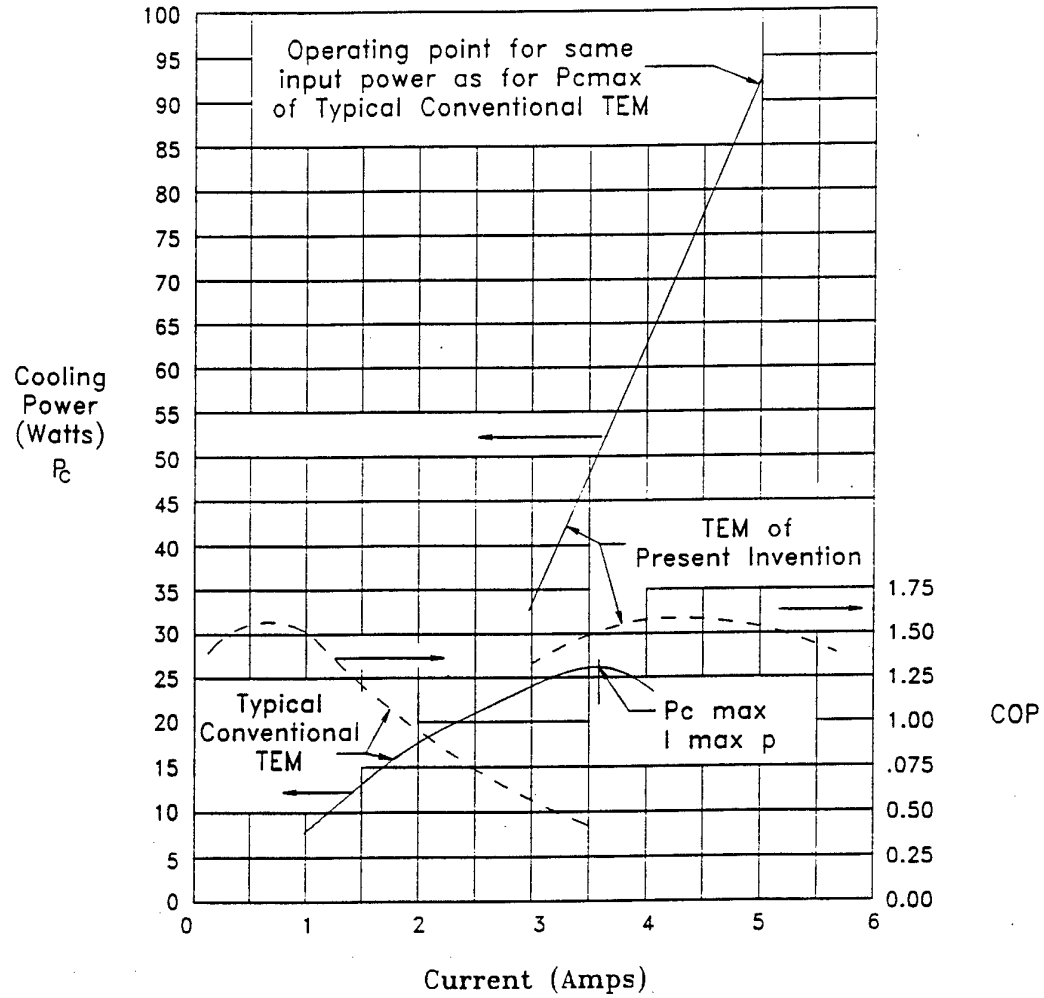

21
23
current
25
24
22
22
current
current
20

Fig. 3


Operating point for same input power as for Pcmax of Typical Conventional TEM
TEM of Present Invention
Typical Conventional TEM
Pc max
I max p
Cooling Power (Watts) Pc
COP
Current (Amps)
100
95
90
85
80
75
70
65
60
55
50
45
40
35
30
25
20
15
10
5
0
0
1
2
3
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5
6
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Fig. 4

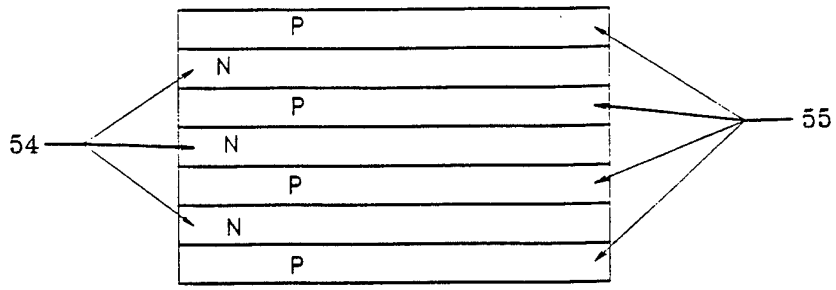

Fig. 5

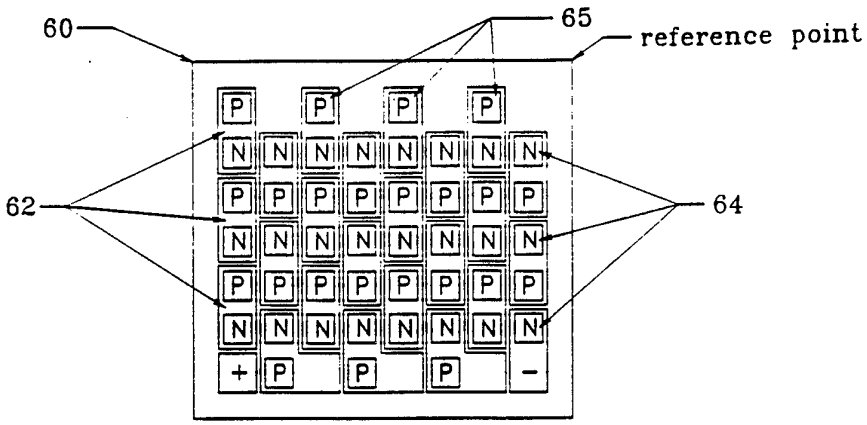

Fig. 6A

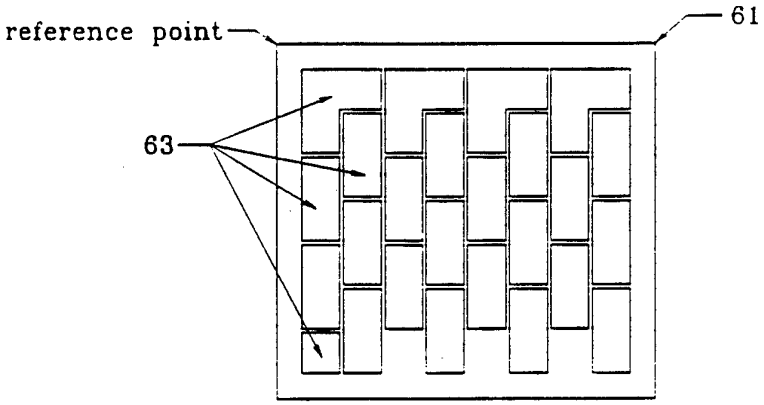

Fig. 6B

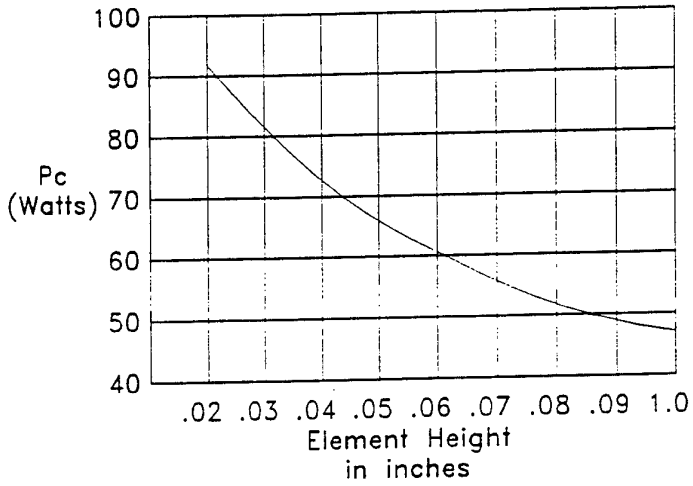

Figure 7

Pc as a Function of Element Height

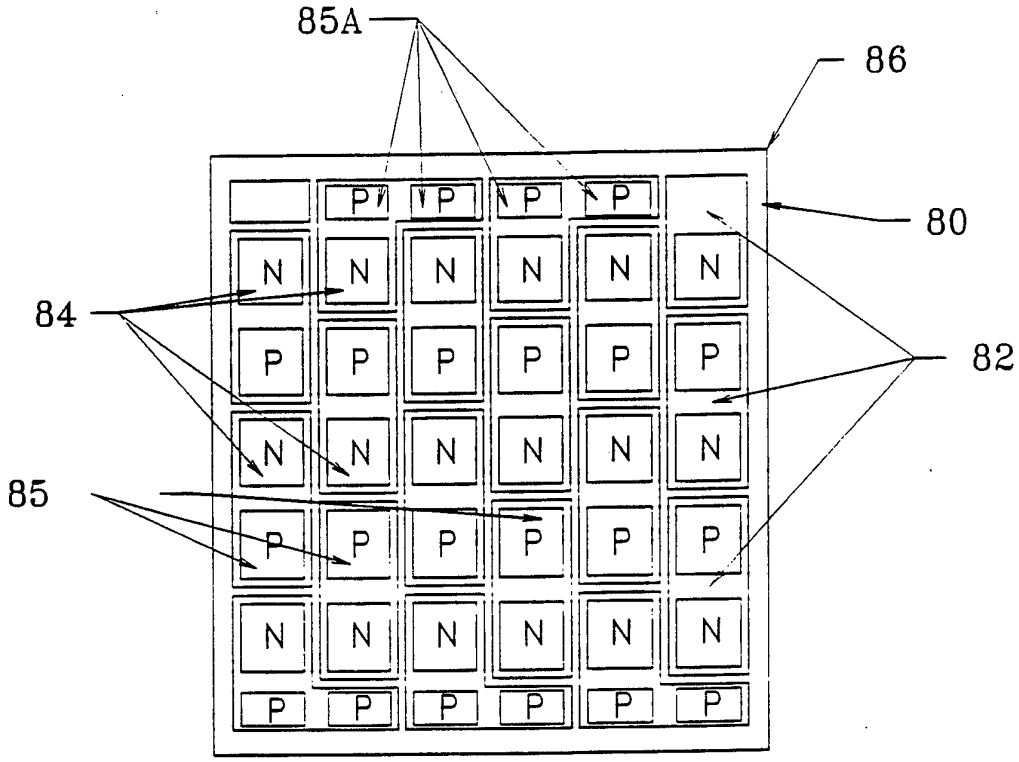

Fig. 8A

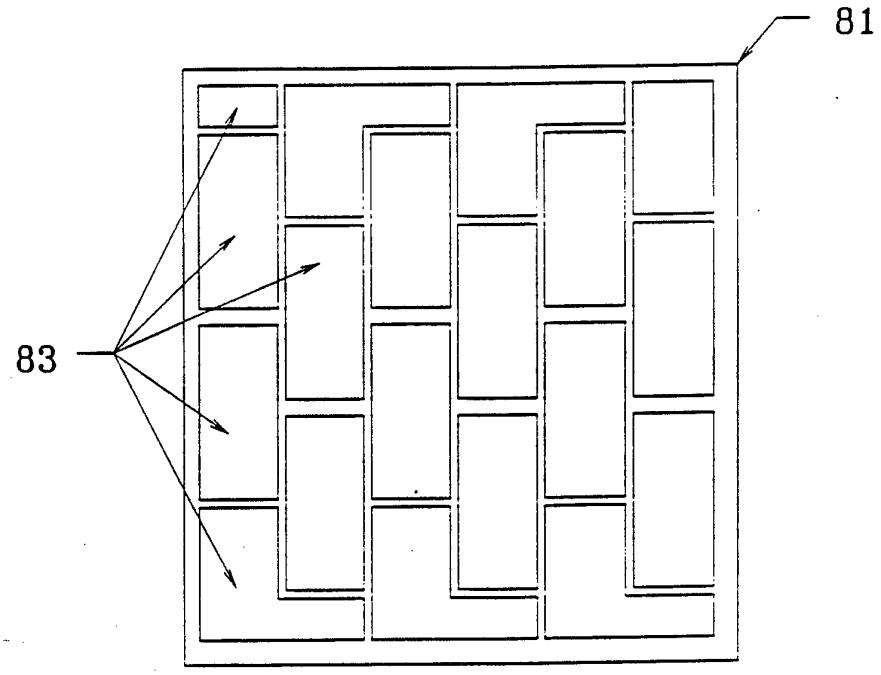

Fig. 8B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/12114

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H05K 7/20
US CL :136/203; 257/930; 361/704, 719, 784; 437/208
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US, A, 4,855,810 (GELB ET AL) 08 August 1989, see cover Figure.	1,4,6,10-13 ------- 2,3,5,7-9,14-17
X -- Y	US, A, 5,168,339 (YOKOTANI ET AL) 01 December 1992, see Figure 2.	1,4,6,10-13 ------- 2,3,5,7-9,14-17
A	US, A, 3,780,425 (PENN ET AL) 25 December 1973, see entire document.	1-22
A	US, A, 5,228,923 (HED) 20 July 1993, see entire document.	1-22
A	US, A, 5,241,828 (KAPITULNIK) 07 September 1993, see entire document.	1-22
A	DE, A 1,187,285 (HANLEIN) 18 February 1965, see entire	1-22

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 08 DECEMBER 1994	Date of mailing of the international search report 04 JAN 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer GERALD TOLIN Telephone No. (703) 308-3114

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/12114

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,343,960 (EGUCHI ET AL), 10 August 1982, see Figure 2.	18-22
Y	US, A, 4,081,895 (GERMANO ET AL) 04 April 1978, see Figure 2.	18-22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/12114

B. FIELDS SEARCHED
Minimum documentation searched
Classification System: U.S.

62/3.3, 3.3; 136/203-205, 224, 225; 165/80.3, 185; 257/470, 613, 712, 713, 930; 361/688, 704, 707, 708, 712, 718, 719, 722, 784; 437/51, 187, 208, 221, 249, 903, 965