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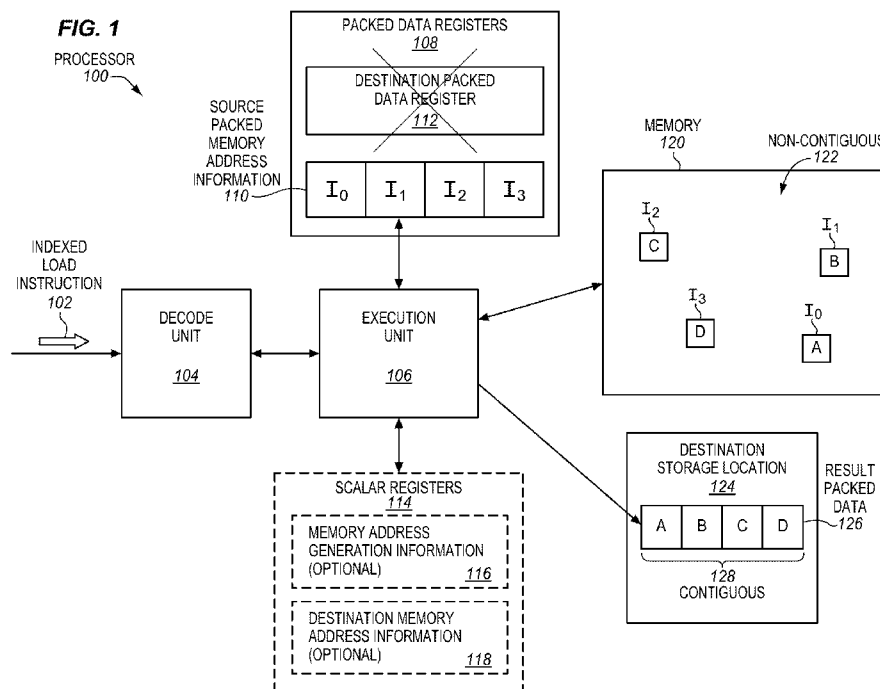
(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: HASENPLAUGH, William C.; 44 St. Botolph St. Apt. 1D, Boston, Massachusetts 02116 (US). NEWBURN, Chris J.; 8034 Renee Drive, South Beloit, Illinois 68010 (US). STEELY, Simon C., JR.; 8 Anna Louise Dr, Hudson, New Hampshire 03051 (US). SURY, Samantika S.; 11 Blueberry Lane, Westford, Massachusetts 01886 (US).

(74) Agent: VECCHIA, Brent E.; Nicholson, DeVos, Webster & Elliott, LLP, 99 Almaden Boulevard, Suite 710, San Jose, CA 95113 (US).

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(54) Title: PROCESSORS, METHODS, SYSTEMS, AND INSTRUCTIONS TO LOAD MULTIPLE DATA ELEMENTS TO DESTINATION STORAGE LOCATIONS OTHER THAN PACKED DATA REGISTERS



(57) Abstract: A processor of an aspect includes a plurality of packed data registers, and a decode unit to decode an instruction. The instruction is to indicate a packed data register of the plurality of packed data registers that is to store a source packed memory address information. The source packed memory address information is to include a plurality of memory address information data elements. An execution unit is coupled with the decode unit and the plurality of packed data registers, the execution unit, in response to the instruction, is to load a plurality of data elements from a plurality of memory addresses that are each to correspond to a different one of the plurality of memory address information data elements, and store the plurality of loaded data elements in a destination storage location. The destination storage location does not include a register of the plurality of packed data registers.



MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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A. CLASSIFICATION OF SUBJECT MATTER**G06F 9/30(2006.01)i, G06F 12/1027(2016.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
G06F 9/30; G06F 15/80; G06F 12/08; G06F 12/1027Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal), Google Search Engine & keywords: packed data registers, decode, source, destination, load, store, address, non-temporal load, cache line**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016-0019184 A1 (INTEL CORPORATION) 21 January 2016 See paragraphs [0032], [0042]-[0062], [0069]-[0077], [0083], [0258]; claims 1-2, 9; and figures 1, 3-4, 6-7.	1-9, 16-25
Y		10-15
Y	US 2009-0172359 A1 (GENE SHEN et al.) 02 July 2009 See paragraphs [0018], [0032]-[0043]; claim 16; and figures 3-5.	10-11
Y	TODD M. AUSTIN et al., 'High-Bandwidth Address Translation for Multiple-Issue Processors', In: Proceedings of the 23rd Annual International Symposium on Computer Architecture, 22 - 24 May 1996, pages 158-167. <URL: https://web.eecs.umich.edu/~taustin/papers/ISCA96-hbat.pdf > See pages 160-161.	12-13
Y	US 2014-0181482 A1 (ADVANCED MICRO DEVICES, INC.) 26 June 2014 See paragraphs [0015]-[0039], [0056]-[0058]; and figures 1, 5.	14-15
A	US 2016-0246723 A1 (INTEL CORPORATION) 25 August 2016 See paragraphs [0049]-[0095]; claims 1-13; and figures 3-8.	1-25

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

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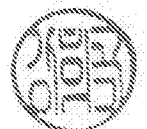
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KANG, Hee Gok

Telephone No. +82-42-481-8264



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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