(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 January 2006 (26.01.2006)

PCT

(10) International Publication Number
WO 2006/009605 A1

(51) International Patent Classification[7]: H04J 3/06

(21) International Application Number:
PCT/US2005/019115

(22) International Filing Date: 1 June 2005 (01.06.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/580,188 16 June 2004 (16.06.2004) US
60/580,189 16 June 2004 (16.06.2004) US

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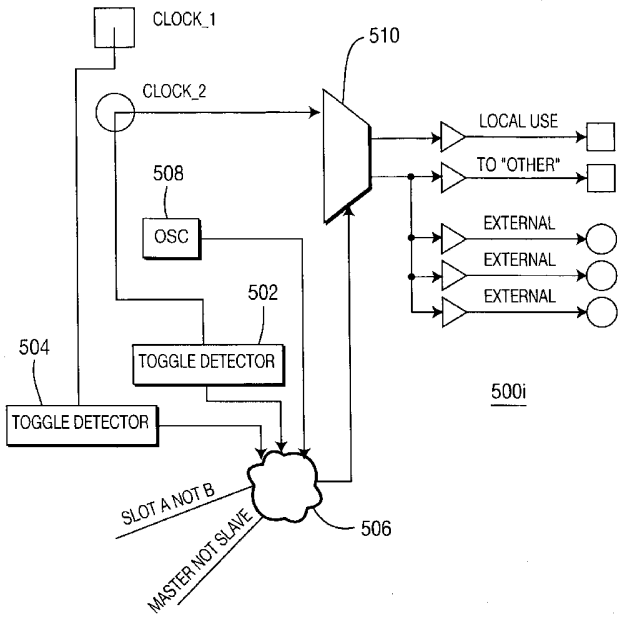
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR ROUTING ASYNCHRONOUS SIGNALS



A_NOT B	MASTER NOT SLAVE	EXTERNAL_TOGGLE	OTHER_TOGGLE	SELECTION
1	1	X	X	OSC
0	1	x	1	CLOCK_2
0	1	x	0	OSC
x	0	1	x	CLOCK_1
x	0	0	1	CLOCK_2
x	0	0	0	OSC

(57) Abstract: A router (100), for routing at least one input signal to at least one output, comprises at least one input module (4021-402x) and at least one output module (4041-404y). Each of the input and output modules includes at least one clock selector circuit (5001-500n) for selecting from among a first and second clock signal, and an oscillator signal, as a common output clock signal for the at least first router, based in part on whether at least one of the first and second clock signals has toggled. The clock selector circuit provides redundancy as well as distribution of clock signals among elements within each module.

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European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SYSTEM AND METHOD FOR ROUTING ASYNCHRONOUS SIGNALS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Serial No 60/580,188, filed on June 16, 2004, and U.S. Provisional Patent Application Serial No 60/580,189, filed on June 16, 2004, teachings of both of which are incorporated herein.

FIELD OF THE INVENTION

[0002] This invention relates to routers and more specifically to broadcast routers that route asynchronous signals.

BACKGROUND OF THE INVENTION

[0003] A router comprises a device that routes one or more signals appearing at the router input(s) to one or more outputs. Routers used in the broadcast industry typically employ at least a first router portion with a plurality of router modules (also referred to as matrix cards) coupled to at least one expansion module. The expansion module couples the first router chassis to one or more second router portion to allow further routing of signals. Many broadcast routers, and especially those that are linearly expandable, route asynchronous signals. Asynchronous signal routing by such linearly expandable routers requires an accurate clock signal throughout the entire route to preserve the integrity of routed data. For an asynchronous signal, a difference in clock frequency from one location to another can cause corruption of the signal and loss of the data represented by that signal. Even a difference in clock frequencies as small as 1 part per million (PPM) can have an undesirable effect on data. Typical examples of data corruption include repeated or dropped signal samples.

[0004] As linearly expandable routers increase in complexity, the problem of supplying an accurate and synchronized clock signal to various elements becomes more difficult. For purposes of discussion, a clock signal constitutes a signal that oscillates between

a high and a low state at defined intervals. Typical clock signals oscillate with a 50% duty cycle. However, clocks having other duty cycles are also commonly employed. Circuits using clock signals for synchronization become active upon one of the rising or falling edge of the clock signal.

[0005] A so-called, "clock multiplexer" refers to a circuit, as typically exists within a linearly expandable router, for selecting at least one clock signal from a plurality of available clock signals. The selected clock signal(s) serve to trigger other elements. When selecting among available clock signals, the output signal selected by the clock multiplexer should not include any undefined pluses. Undefined pulses occur, for example, when a selected clock signal undergoes a disruption. Such a disruption can include a missing clock signal as well as a clock signal that fails to switch states as expected. Some times, an input clock signal will remain "stuck" indefinitely at one logic state or the other. Such disruptions frequently produce undefined pulses including runt pulses, short pulses, pulses of indefinite duration, glitches, spikes and the like.

[0006] Prior art attempts to avoid undefined pulses at the output of a clock multiplexer include so-called "safe" clock multiplexers. A typical safe clock multiplexer switches from a presently selected input to a next selected input in an orderly manner. Thus, a safe multiplexer does not switch until the selected input clock signal transitions to a known state and the subsequently selected clock signal transitions to the same state as the previously selected clock signal.

[0007] However, prior art safe clock multiplexers have drawbacks. For example, when a presently selected clock signal fails to transition to a known state, a safe clock multiplexer will often lack the ability to switch to another clock signal. Prior art safe clock multiplexers have not tolerated these and other types of clock disruptions.

[0008] Thus, a need exists for a technique for providing a selected one of a set of clock signals, such as within a linearly expandable router, that overcomes the aforementioned disadvantages

SUMMARY OF THE INVENTION

Briefly in accordance with a preferred embodiment of the present principles, there is provided a method for selecting a clock signal from among at least first and second clock

signals. The method commences by detecting a failure of a first clock signal to change state and by detecting a failure of a second clock signal to change state. A selection occurs from among the first and second clock signals and an oscillator signal, based in part on whether at least one of the first and second clock signals has toggled

BRIEF DESCRIPTION Of THE DRAWINGS

[0010] FIGURE 1 illustrates a block schematic diagram of a router according to an illustrative embodiment of the present principles:

[0011] FIGURE 2 illustrates a first alternate arrangement of input and output modules for the router of FIG. 1

[0012] FIGURE 3 illustrates a second alternate arrangement of input and output modules for the router of FIG. 1;

[0013] FIGURE 4 illustrates a third alternate arrangement of input and output modules for the router of FIG. 1

[0014] FIGURE 5 illustrates a first network of clock selector circuits for use in the router of FIG. 1;

[0015] FIGURE 6 depicts a second network of clock selector circuits for use in the router of FIG. 1

[0016] FIGURE 7 depicts a block schematic diagram of an illustrative embodiment of a clock selector circuit within the networks of FIGS. 5 and 6; and

[0017] FIGURE 8 depicts a safe clock multiplexer system of for use in the selector circuit of FIG. 4.

DETAILED DESCRIPTION

[0016] FIGURE 1 depicts a block schematic of a broadcast router 100 in accordance with a preferred embodiment of the present principles. In a preferred embodiment, the router 100 comprises at least one, and preferably a plurality input modules 402_1, 402_2...402_x where x is an integer greater than zero, and at least one, and preferably, a plurality of output modules 404_1...404_y, where y is an integer. Each input module, such as input module 402_1, comprises at least one, and preferably a plurality of input cards 406_1, 406_2...406_z where z is an integer

greater than zero. Each input card has at least one, and preferably, a plurality of inputs for receiving signals for multiplexing into an output signal. Different input cards typically have different signal receiving capabilities to afford the ability to receive signals from a variety of sources. An expansion card 408 within each input module, such as module 402_1, multiplexes the output signals from the input cards 406_1-406_z into an output signal.

[0017] Each second module, such as second module 404_1, has a matrix 410 card which de-multiplexes the input signals from one or more of the input modules for delivery to at least one, and preferably a plurality of output cards 412_1, 412_2...412_p, where p is an integer greater than zero. Each output card delivers one or more output signals to one or more external devices (not shown). A control card 414 controls the matrix card 410 in response to an external control signal C to cause the matrix card to route its output signal among various of the output cards 412_1-412_p. In this way, the matrix card 410 can effectuate routing based on the external control signal C.

[0018] The router 100 of FIG. 1 has each of its input modules 402_1, 402_2...402_x coupled to each of the output modules 404_1, 402_2...404_y. Other arrangements are possible. FIGURE 2 illustrates a first alternate arrangement of input and output cards for the router 100 of FIG. 1 wherein the input and output modules are arranged to provide the same number of inputs and outputs. FIGURE 3 illustrates a second alternate arrangement of input and output modules for the router 100 of FIG. 1 in which there are more inputs than outputs. FIGURE 4 illustrates a third alternate arrangement of input and output modules for the router 100 of FIG. 1 in which there are more outputs than inputs.

[0019] The input modules 402_1-402_x and the output modules 404_1-404_y of FIG. 1 typically each include at least one of clock modules 500_1-500_n where $n \geq x + y$, with each clock module having a structure as described in greater detail with respect to FIG. 5. In practice, separate clock modules can exist in within one or more the elements within each input and output module of FIG. 1. Moreover, one or more clock module 500_1-500_n could exist as separate modular elements in the router 100, much like one of the input or output modules.

[0020] Referring to FIG. 5, the clock modules 500_1-500_n can interconnect with each other in a daisy chain fashion to yield a network 600 of clock modules. In the embodiment of FIG. 5, the clock module 500_1 supplies its clock signal to the clock module 500_2 as well as each of clock modules 500_3, 500_{i+1} and 500_{i+3}, where $i \leq n$, whereas the clock module 500_2

supplies its clock signal to each of modules 500_i, 500_{i+2} and 500_{i+4}. Each of the clock modules 500_1, 500_2...500_n also receives the clock signal from a preceding one of clock modules 500_2...500_i...500_{n-1}, respectively.

[0021] FIGURE 6 depicts an alternate arrangement of clock modules wherein the modules are arranged in first and second networks 600_1 and 600_2, with each of the networks 600_1 and 600_2 configured similarly to the clock module network 600 of FIG. 2. As seen in FIG. 6, one or more of the individual clock modules 500_1-500_n of network 600_1 provide clock signals to one or more of the clock modules 500_1-500_n of network 600_2.

[0022] FIGURE 7 depicts a block schematic diagram of an exemplary clock module 500_i. The clock module 500_i of FIG. 4 includes first and second clock inputs that receive first and second clock signals Clock_1 and Clock_2, respectively. Each of the external clock signals Clock_1 and Clock_2 can comprise clock signals from a separate upstream clock selector circuit in the network of FIG 2 or a clock signal from a reference clock circuit formed by an oscillator 508.

[0023] The clock selector circuit 500_i includes a pair of toggle detectors 502 and 504 which each receive a separate one of the Clock_1 and Clock_2 signals. Each toggle detector provides an output signal indicative of whether its respective input clock signal has toggled, i.e., a changed from one state to another. A logic block 506 receives the output signals of the toggle detectors 502 and 504, along with the output of an oscillator circuit 508 that generates a clock signal useful for meeting the timing requirements of various circuit elements. The logic block 506 also receives two external status signals; (1) A_not B and (2) Master_not Slave. The state of the status signal A_not B indicates whether or not the clock circuit 500_i will provide the primary clock signal. The state of the Master_not Slave signal determines the clock circuit 500_i operates as its own master, or as a slave to another clock signal.

[0024] The logic block 506 generates an output control for controlling a safe clock multiplexer system 510 to select among the clock signals Clock_1, Clock_2 and the output signal of the oscillator 508, to provide a single clock signal to downstream elements (not shown). The output control signal of the logic block 506 has a prescribed relationship to the logic circuit input signals as shown in Table 1, with the "x" entries constituting "don't care" values. (In other words, the value of the particular input signal has no effect on the output of the logic block 506.)

TABLE I

A_not B	Master_Not Slave	Toggle Detector 504	Toggle Detector 502	Safe clock multiplexer system 510 Output
1	1	x	x	Oscillator 508
0	1	x	1	Clock_2
0	1	x	0	Oscillator 508
x	0	1	x	Clock_1
x	0	0	1	Clock_2
x	0	0	0	Oscillator 508

[0025] As seen from Table 1, for so long as the Master_ Not Slave signal remains at a logic "1" level, the clock circuit 500_i only selects between Clock_2 and Oscillator 508. Under such conditions, the toggling of the Clock_1 signal, and hence the output signal of the toggle detector 504 has no effect. Conversely, when the clock circuit 500_i serves as a slave (i.e., the Master_ Not Slave signal remains at a logic "0" level), the output states of the toggle detector 504, and the output state of the toggle detector 502, determine which of the Clock_1, Clock_2, and oscillator 508 signals appear at the output of the safe clock multiplexer system 510. The clock signal selected by the safe clock multiplexer system 510 provides a timing signal for local use as well as for input to elements within the router 100 of FIG. 1.

[0026] In a preferred embodiment, the safe clock multiplexer system 510 of FIG. 4 has the structure shown in FIG. 5 to afford the clock module 500_i of FIG. 3 the ability to tolerate an input clock pulse that has become stuck. Within the safe clock multiplexer system 510 of FIG. 5, first and second toggle detectors 701_1 and 701_2 receive the Clock_1 and Clock_2 signals, respectively, as do each of a pair of multiplexers 702_1 and 702_2, respectively. Each of the multiplexers 702_1 and 702_2 receives a signal and a logic "0" level at its second input.

[0027] The toggle detectors 701_1 and 701_2 control the multiplexers 702_1 and 702_1 in accordance with the state of Clock_1 and Clock_2 signals, respectively, as measured against the output signal of the oscillator 508. In other words, each of the toggle detectors 701_1 and 701_2 determines whether a respective one of the Clock_1 and Clock_2 signals has changed state (i.e., toggled) relative to the output signal of the oscillator 508. If a respective one of the

toggle detectors 701_1 and 701_2 determines that a corresponding one of the Clock_1 and Clock_2 signals has toggled relative to the oscillator 508 output signal, then that toggle detector gates a corresponding one of the multiplexers 702_1 and 702_2. When gated, each of the multiplexers 702_1 and 702_2 passes and associated one of the Clock_1 and Clock_2 signals. Should a respective one of the clock signals Clock_1 and Clock_2 not toggle relative to the oscillator 508 output signal, then the corresponding one of the multiplexers 702_1 and 702_2 will output a logic zero level signal.

[0028] A multiplexer 704 receives at its first and second inputs the output signals of the multiplexers 702_1 and 702_2, respectively. In accordance with a signal from the logic block 506 of FIG. 4, the multiplexer passes the output signal of one of the multiplexers 702_1 and 702_2 to a first input of a multiplexer 706_1 and to the input of a toggle detector 708_1. The multiplexer 706_1 has its second input supplied with a signal at a logic zero level.

[0029] The toggle detector 708_1 controls the multiplexer 706_1 in accordance with the relationship between the output signal of the multiplexer 704 and the output signal of the oscillator 508. In other words, the toggle detector 708_1 determines whether the output signal of the multiplexer 704 has changed state relative to the output signal of the oscillator 508. If the output signal of the multiplexer 704 toggles relative to the oscillator 508 output signal, then the toggle detector 708_1 causes the multiplexers 706_1 to pass the output signal of the multiplexer 704. Otherwise, should the output signal of the multiplexer 704 not toggle relative to the output signal of the oscillator 508, the multiplexer 706_1 will output a logic zero level signal.

[0030] A multiplexer 706_2 receives at its first and second inputs the output signal of the oscillator 508 and a logic zero level signal, respectively. A toggle detector 708_2 controls the multiplexer 706_2 in accordance with the oscillator 508 output signal. In other words, the toggle detector 708_2 determines whether the output signal of the oscillator 508 periodically changes state. If the oscillator 508 output signal does toggle, then the toggle detector 708_2 gates the multiplexer 706_2 to pass the output signal of the oscillator 508. Otherwise, should the output signal of the oscillator 508 not toggle, then the multiplexer 706_2 will output a logic zero level signal.

[0031] A multiplexer 710 receives at its first and second inputs the output signals of the multiplexers 706_1 and 706_2, respectively. Like the multiplexer 704, the multiplexer 710 operates under the control of the logic block 506 of FIG. 4. Thus, depending on output signal

of the logic block 506, the multiplexer 710 will either output a selected one of the Clock_1 and Clock_2 signals (assuming at least one has toggled relative to the oscillator 508 output signal) or the output signal of the oscillator 508 (assuming it has toggled.)

[0032] An important distinction exists between the multiplexers 702_1 and 702_2 and the multiplexers 704 and 710. The multiplexers 704 and 710 serve as clock multiplexers as described earlier. Advantageously, described, the safe clock multiplexer system 510 of FIG. 5 precludes the possibility of a missing clock pulse. By controlling the passage of the Clock_1 and Clock_2 signals relative to the oscillator 508 output signal and by controlling the passage of the oscillator 508 output only if it has toggled, the safe clock multiplexer system 510 avoids a situation in which any or all of the clocks become stuck in a no-clock state.

[0033] The foregoing describes a clock selector circuit 500_i, including a safe multiplexer system 510, for distributing clock pulses so as to provide for redundancy while assuring clock synchronism.

CLAIMS

1. A router comprising:

at least a first router portion for routing asynchronous signals, said first router portion having first and second clock signal inputs for receiving first and second clock signals which each toggle at a clock rate, respectively; and

a clock selector within the at least first router portion for selecting from among said first and second clock signal, and an oscillator signal, as a common output clock signal for the at least first router portion, based in part on whether at least one of the first and second clock signals has toggled.

2. The router according to claim 1 wherein the clock selector circuit includes a safe clock multiplexer system for detecting whether each of the external clock signals has toggled relative to the oscillator, and if not replacing said each signal with a signal at a fixed logic state.

3. The router according claim 2 wherein the safe clock multiplexer circuit includes a pair of toggle detectors, each determining whether a separate one of the first and second external clock signals has toggled relative to the oscillator signal.

4. The router according to claim 1 wherein the clock selector circuit selects from among said first and second clock signal, and the oscillator signal, as a common output clock signal for the at least first router portion, based in part on whether at least one of the first and second clock signals has toggled and whether the clock selector circuit serves as a master or as a slave to another clock selector circuit.

5. The router according to claim 1 wherein the clock selector circuit selects from among said first and second clock signal, and the oscillator output signal, as a common output clock signal for the at least first router portion, based in part on: (i) whether at least one of the first and second clock signals has toggled, (ii) whether the clock serves as its own master, or as a slave to another clock selector circuit, and (iii) whether the common output clock signal will serve as a primary clock signal.

6. The router according to claim 1 wherein the clock selector circuit comprises:

a first toggle detector for generating an output signal determinative of whether the first external clock signal has toggled;

a second toggle detector for generating an output signal determinative of whether the second external clock signal has toggled;

a logic block for providing an output control signal which varies based in part on the output signal of the first and second toggle detectors; and

a multiplexer system for selecting among said first and second clock signal, and said oscillator signal, as a common output clock signal for the at least first router in accordance with the logic block output signal.

7. The router according to claim 6 wherein the logic block provides its output control signal based in part on whether at least one of the first and second clock signals has toggled, and whether the clock serves as its own master, or as a slave to another clock selector circuit.

8. The router according to claim 6 wherein the logic block provides its output control signal based in part on: (i) whether at least one of the first and second clock signals has toggled, (ii) whether the clock serves as its own master, or as a slave to another clock selector circuit, and (iii) whether the common output clock signal will serve as a primary clock signal.

9. The router according to claim 1 further comprising:

at least a second router portion for routing asynchronous signals, said first router portion respective first and second clock signal inputs for receiving first and second clock signals, respectively, which each toggle; and

a second clock selector within the at least second router portion for selecting from among said first and second clock signals, and an oscillator signal, as a common output clock signal for the at least first router, based in part on whether at least one of the first and second clock signals has toggled relative to the oscillator signal.

10. A method for selecting a clock signal, comprising the steps of

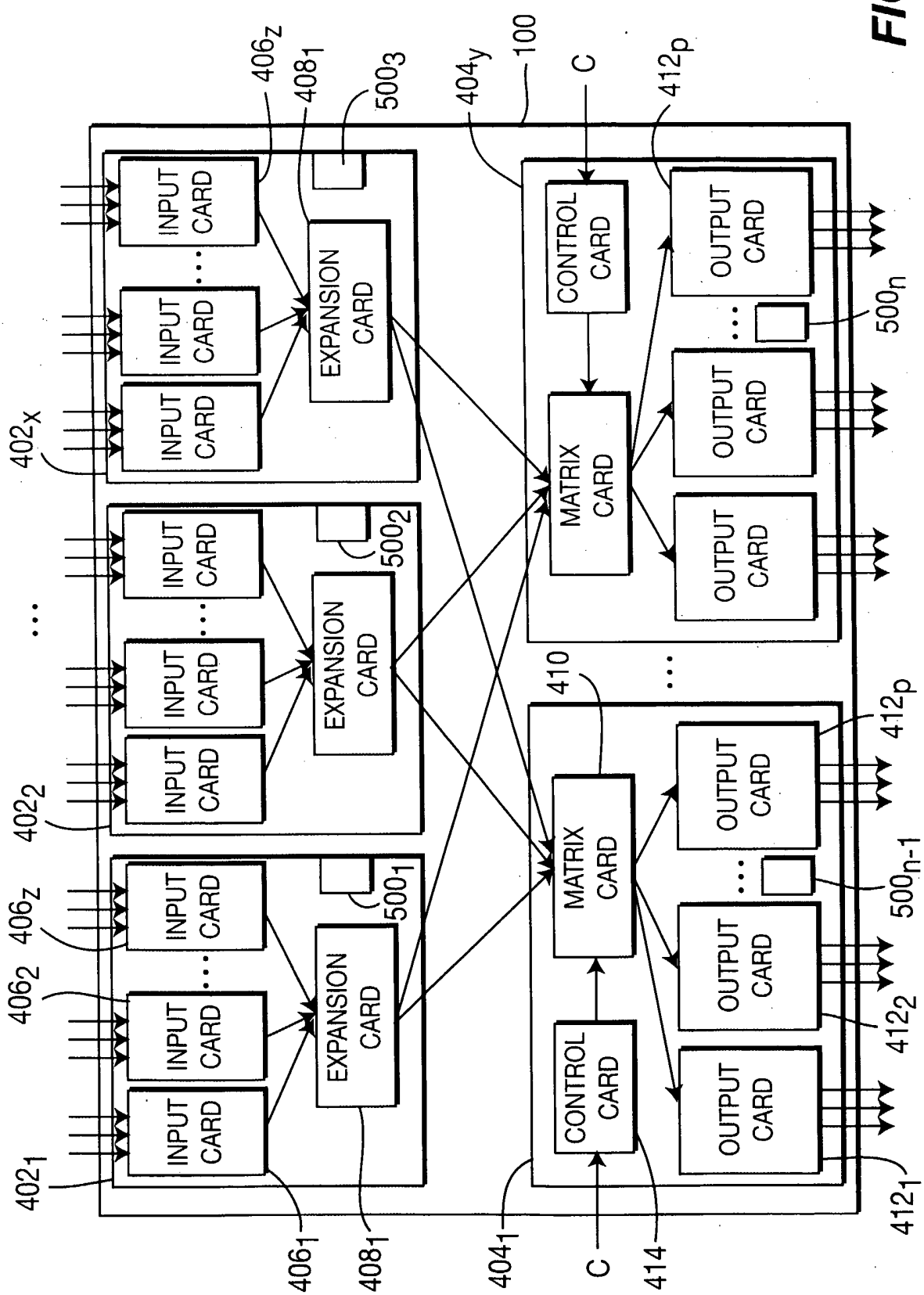
detecting a failure of a first clock signal to change state

detecting a failure of a second clock signal to change state; and

selecting from among the first and second clock signals and an oscillator signal, based in part on whether at least one of the first and second clock signals has toggled

11. The method according to claim 10 wherein the selecting step further comprises the step of selecting from among said first and second clock signal, and said oscillator signal, as a common output clock signal for the at least first router, based in part on whether at least one of the first and second clock signals has toggled and whether the clock selector circuit serves as a master or as slave to another clock selector circuit.

12. The method according to claim 10 wherein the selecting step further comprises selecting from among said first and second clock signal, and said an oscillator signal, as a common output clock signal for the at least first router, based in part on: (i) whether at least one of the first and second clock signals has toggled, (ii) whether the clock serves as its own master or as a slave to another clock selector circuit, and (iii) whether the common output clock signal will serve as a primary clock signal.


INPUT CARD
EXPANSION CARD
CONTROL CARD
MATRIX CARD
OUTPUT CARD
402_x
402_2
402_1
406_z
406_2
406_1
408_1
500_3
500_2
500_1
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C
414
410
412_p
412_2
412_1
500_n
500_{n-1}

FIG. 1

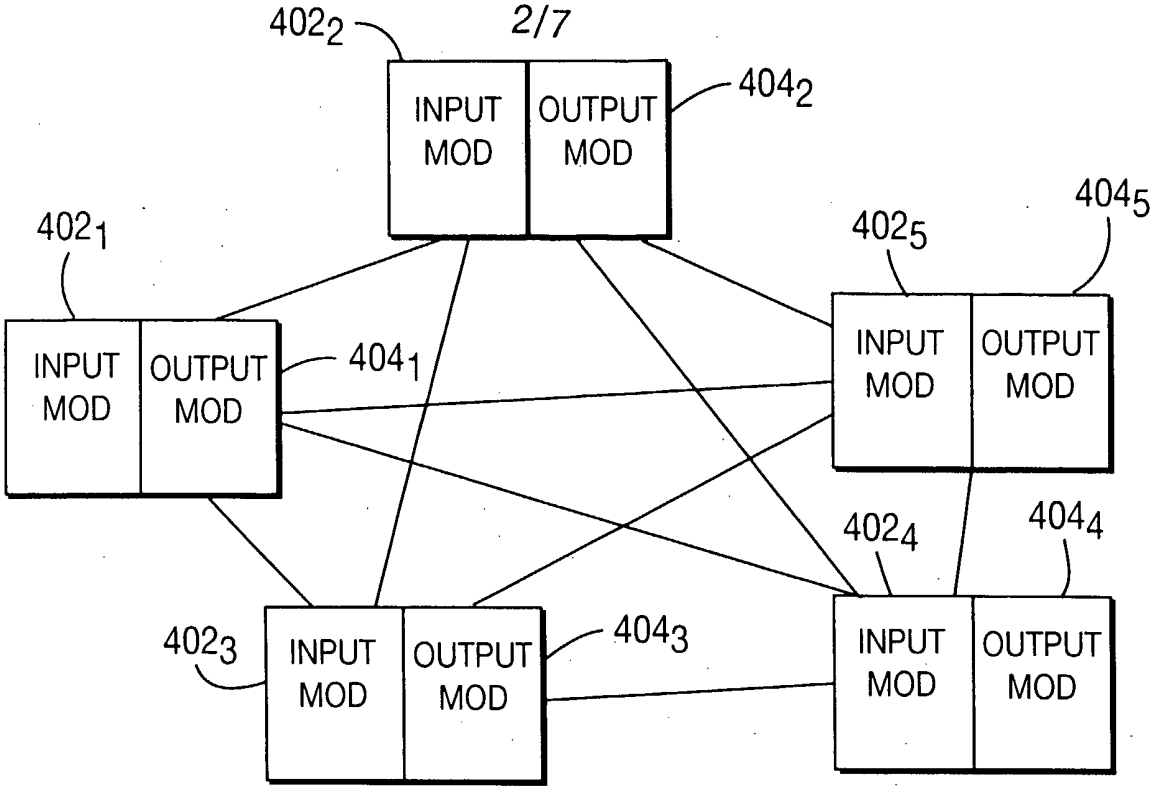


FIG. 2

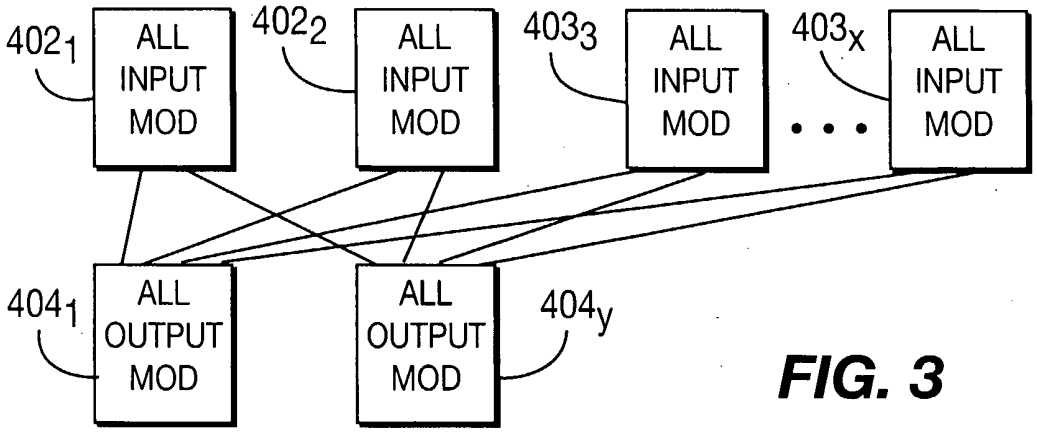


FIG. 3

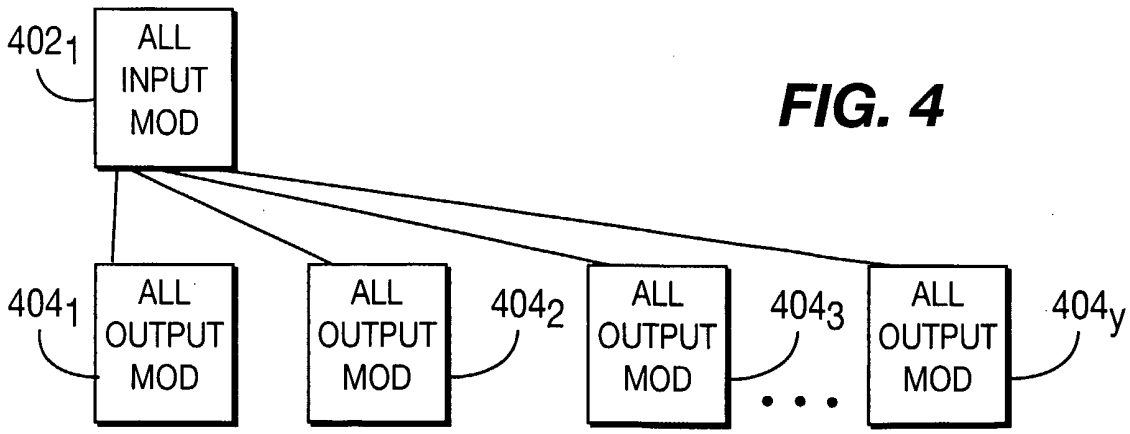
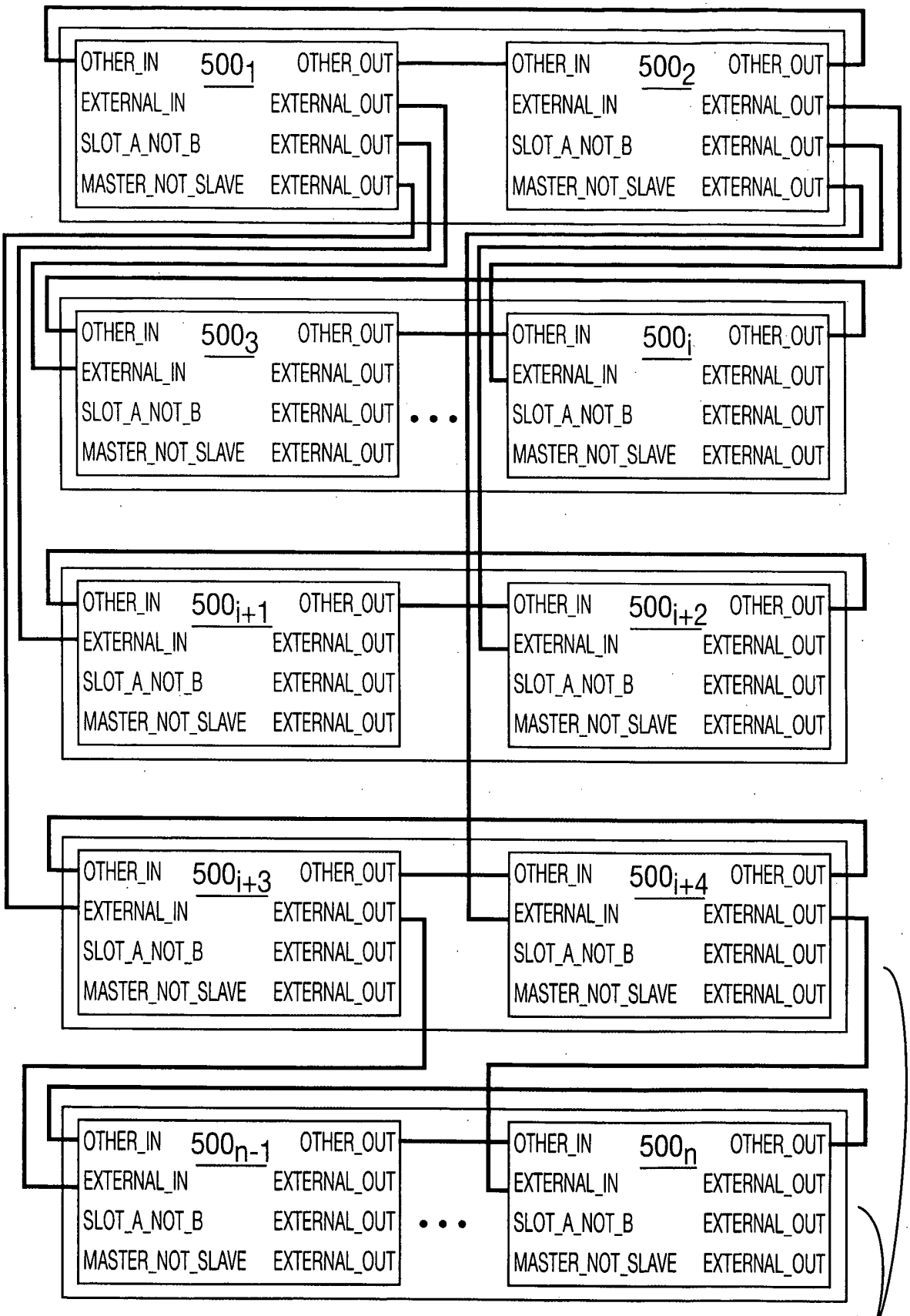


FIG. 4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OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
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EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
METHOD CAN BE EXTENDED PAST THE NUMBE
OF EXTERNAL OUT PORTS BY "DAISY CHAINING"

FIG. 5

FIG. 6 | FIG. 6A | FIG. 6B

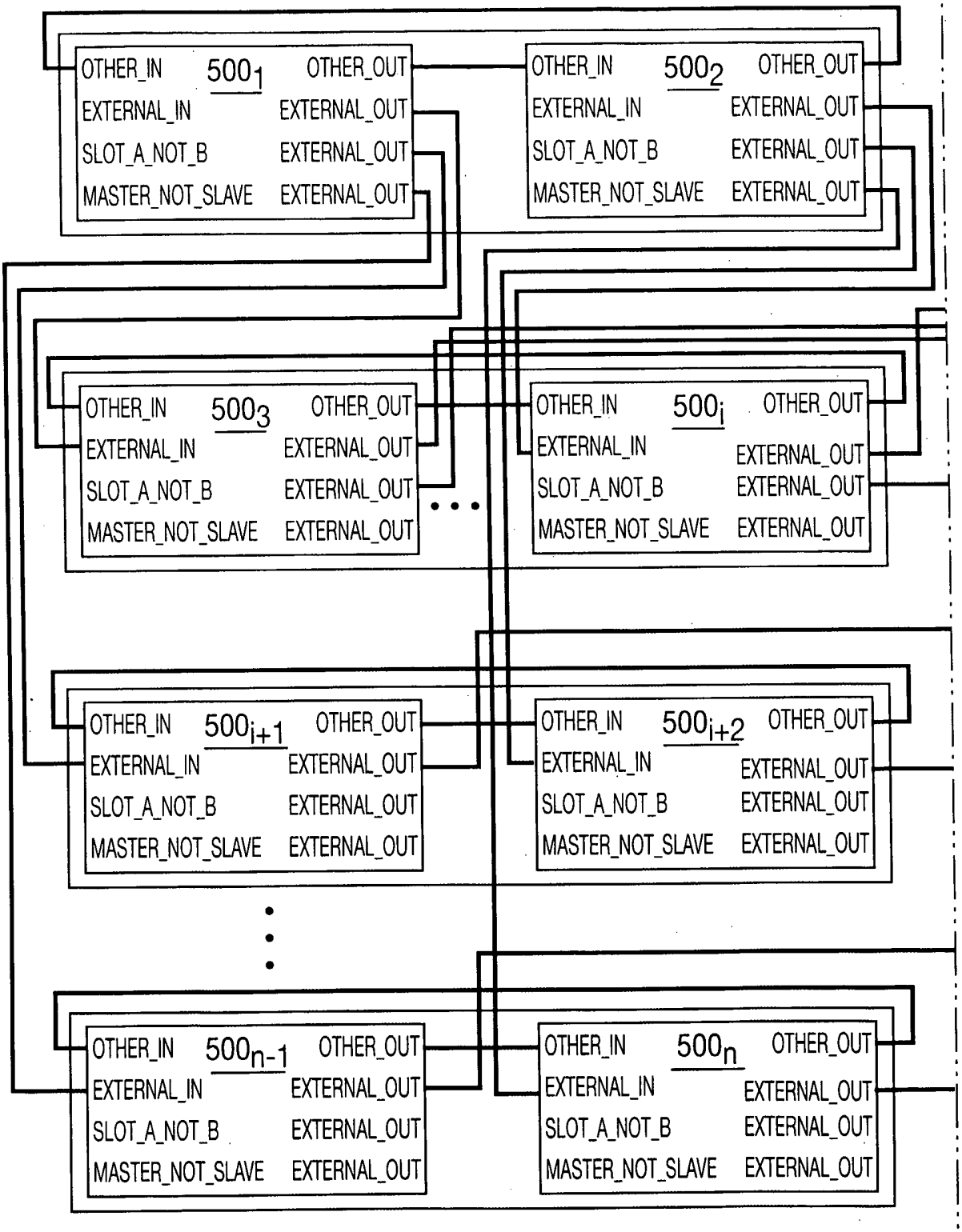
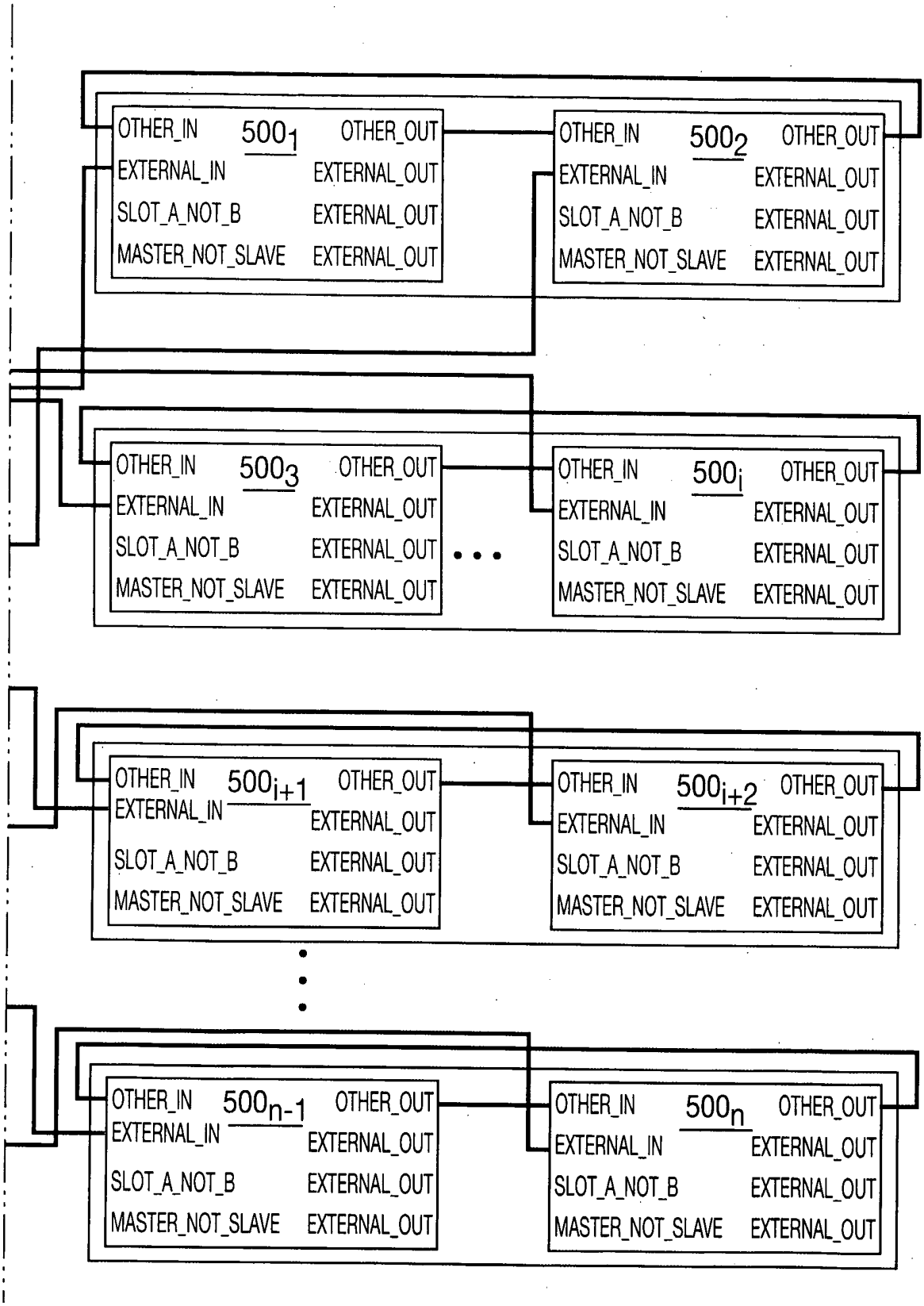


FIG. 6A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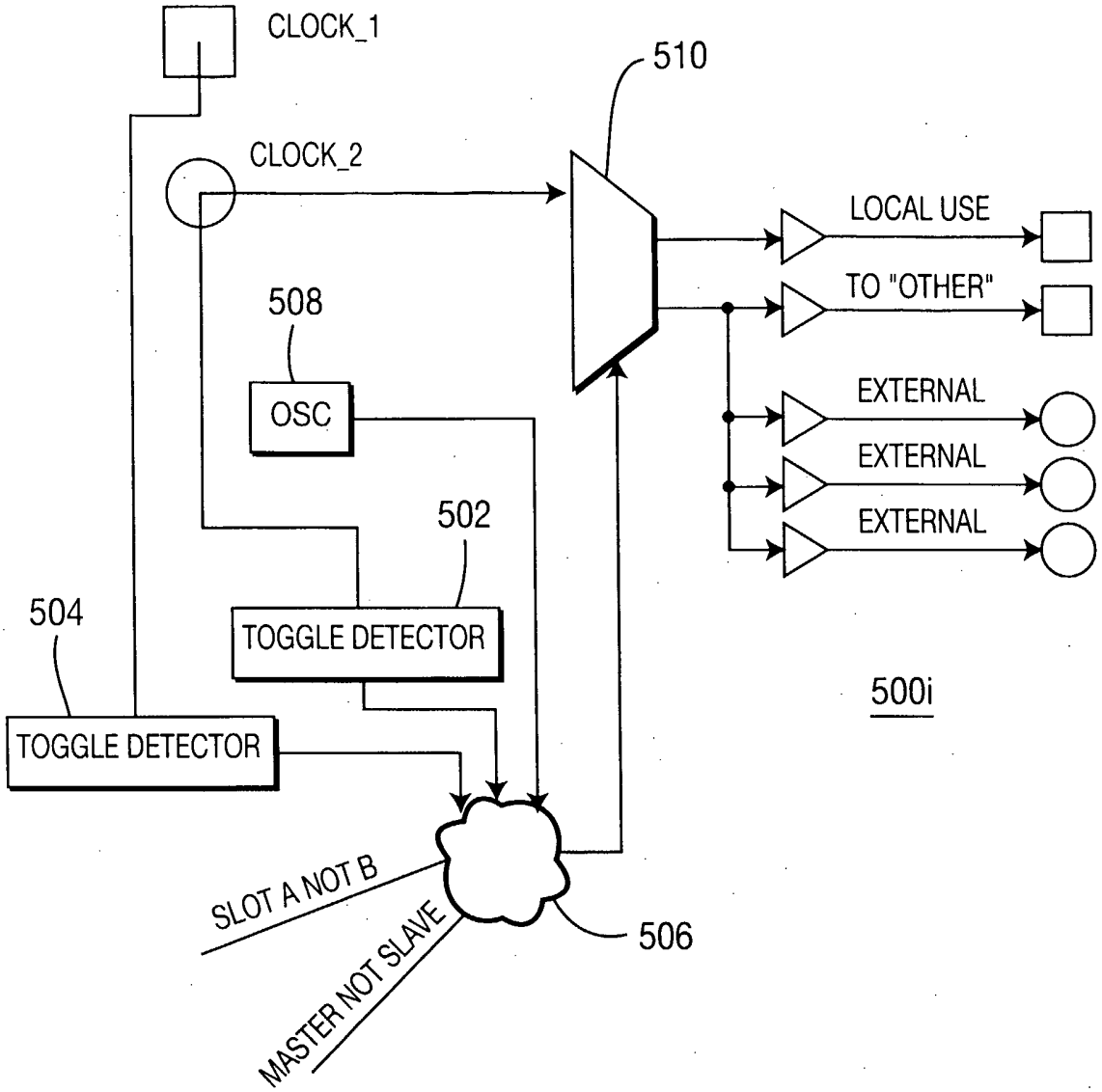
500$_1$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_2$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_3$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_i$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_{i+1}$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_{i+2}$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_{n-1}$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT
OTHER_IN
500$_n$
OTHER_OUT
EXTERNAL_IN
EXTERNAL_OUT
SLOT_A_NOT_B
EXTERNAL_OUT
MASTER_NOT_SLAVE
EXTERNAL_OUT

FIG. 6B



A_NOT B	MASTER NOT SLAVE	EXTERNAL_TOGGLE	OTHER_TOGGLE	SELECTION
1	1	X	X	OSC
0	1	x	1	CLOCK_2
0	1	x	0	OSC
x	0	1	x	CLOCK_1
x	0	0	1	CLOCK_2
x	0	0	0	OSC

FIG. 7

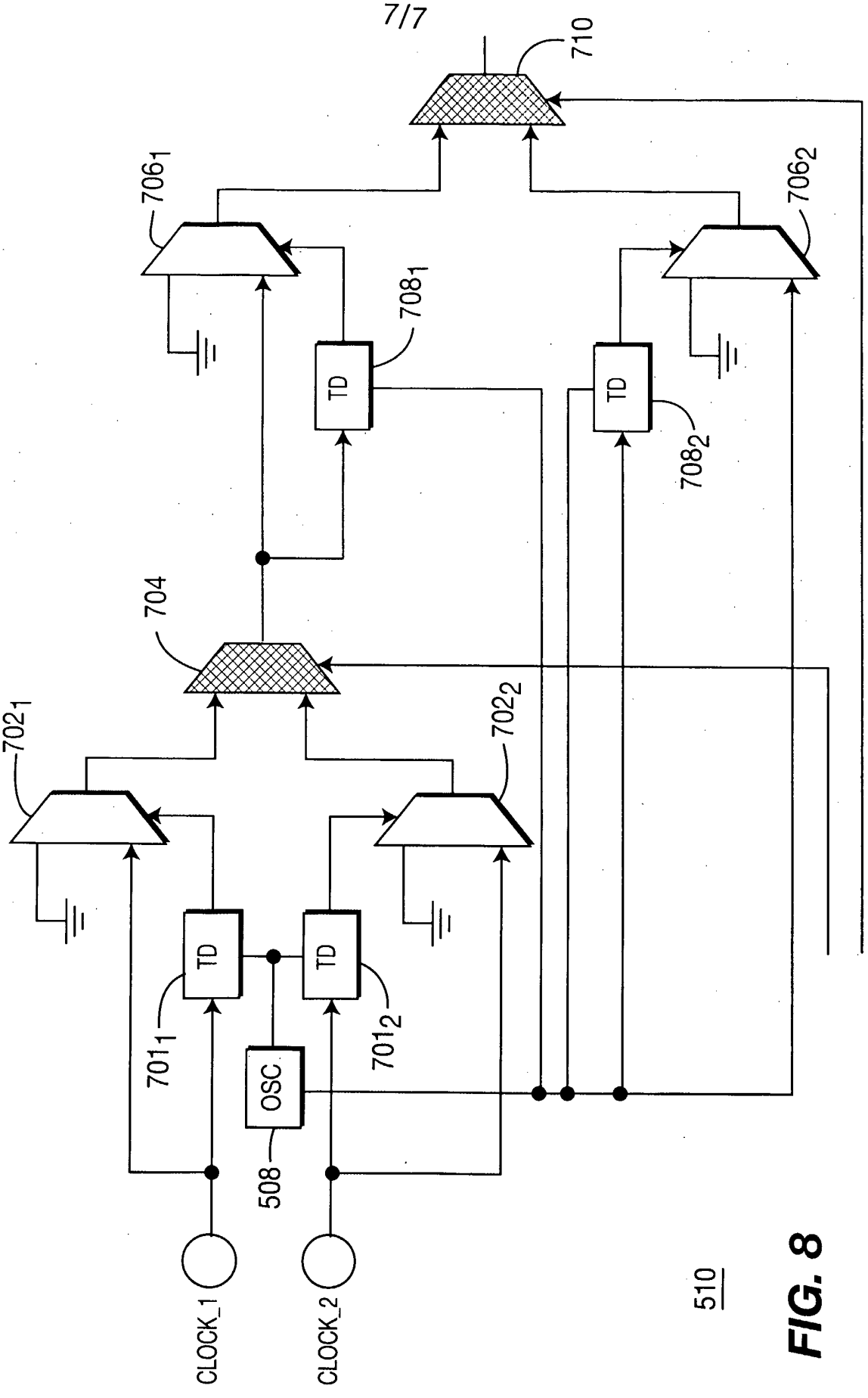

710
706$_1$
706$_2$
708$_1$
708$_2$
TD
704
702$_1$
702$_2$
701$_1$
701$_2$
OSC
508
CLOCK_1
CLOCK_2
510

FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/019115

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04J3/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04J H04L G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 4 322 580 A (KHAN ET AL) 30 March 1982 (1982-03-30) abstract; figure 1 column 3, line 48 - line 68	10 1-9,11, 12
Y	WO 2004/002089 A (THOMSON LICENSING S.A; CHRISTENSEN, CARL; BYTHEWAY, DAVID, LYNN) 31 December 2003 (2003-12-31) page 3, line 13 - line 19 page 9, line 3 - line 18 page 12, line 10 - line 14 page 15, line 29 - line 32 page 16, line 20 - page 17, line 16 column 18, line 6 - line 11 figures 1,2	1-9,11, 12

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 September 2005	22/09/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Pieper, T

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/019115

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