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(54) Title: METHOD AND SYSTEM FOR TRANSMITTING AND RECEIVING SIGNALS

(57) Abstract: The present invention relates to methods of efficiently transmitting signals, an efficient receiver, and methods of efficiently receiving the signals. In particular, the present invention relates to a receiver and receiving methods regarding performing a zero padding and a parity depuncturing. In addition, the present invention relates to methods of efficiently transmitting signals which are counterparts of the receiving methods.

WO 2009/038353 A2

Description

METHOD AND SYSTEM FOR TRANSMITTING AND RECEIVING SIGNALS

Technical Field

[1] The present application claims the benefit of priority under 35 U.S.C. 119 of U.S. provisional patent application No. 60/973,418 filed on Sep. 18, 2007, which is hereby expressly incorporated by reference.

[2] The present invention relates to a method of efficiently transmitting and receiving signals and efficient transmitter and receiver for an OFDM (Orthogonal Frequency Division Multiplexing) system including a TFS (Time-Frequency Slicing).

Background Art

[3] TFS (Time Frequency Slicing) technique has been introduced for broadcasting. When a TFS is used, a single service can be transmitted through multiple RF (Radio Frequency) channels on a two-dimensional time-frequency space.

[4] OFDM (Orthogonal Frequency Division Multiplexing) is a frequency-division multiplexing (FDM) scheme utilized as a digital multi-carrier modulation method. A large number of closely-spaced orthogonal sub-carriers are used to carry data. The data are divided into several parallel data streams or channels, one for each sub-carrier. Each sub-carrier is modulated with a conventional modulation scheme (such as quadrature amplitude modulation or phase shift keying) at a low symbol rate, maintaining total data rates similar to conventional single-carrier modulation schemes in the same bandwidth.

[5] OFDM has developed into a popular scheme for wideband digital communication, whether wireless or over copper wires, used in applications such as digital television and audio broadcasting, wireless networking and broadband internet access.

[6] When TFS, which uses multiple RF bands for each transmitter is combined with OFDM, frequency diversity gain and statistical multiplexing gain can be obtained, thus, resources can be efficiently utilized.

Disclosure of Invention

Technical Problem

[7] It is, therefore, an object of the present invention to provide a method of efficiently transmitting and receiving signals and efficient transmitter and receiver for an OFDM system including TFS.

Technical Solution

[8] One of the embodiments of the present invention provides a method of efficiently using LDPC code as an inner code for a TFS system and an efficient inner interleaving

method when hybrid modulation is used. Another embodiment of the present invention provides, for a case where DVB-S2 LDPC code is used as FEC, using new codeword for convolutional interleaving by using puncturing/shortening. Yet another embodiment of the present invention provides method of using dummy padding without loss of performance.

[9] According to an aspect of the present invention, there is provided a method of transmitting signals for an OFDM (Orthogonal Frequency Division Multiplexing) system including TFS (Time Frequency Slicing), comprising: encoding frames made of bitstreams; performing a modulation to transform the encoded frames into symbols; performing a puncturing and a shortening on the symbols such that the symbols have lengths of two consecutive integers multiplied by at least one integer; and encoding the puncturing and the shortening performed symbols into a multiple signal or a single signal.

[10] According to another aspect of the present invention, there is provided a receiver for an OFDM system including, comprising: a demodulator configured to transform received signals into OFDM symbols; a frame parser configured to perform modulation to transform the OFDM symbols into bitstreams; and a BICM(Bit-Interleaved Coding and Modulation) decoder configured to deinterleave the bitstreams through performing a zero padding on an information part of the bitstreams and performing a parity depuncturing on a parity part of the bitstreams.

[11] According to yet another aspect of the present invention, there is provided a method of receiving signals for an OFDM system including TFS comprising: transforming received signals into OFDM symbols; performing modulation to transform the OFDM symbols into bitstreams; and deinterleaving the bitstreams through performing a zero padding on an information part of the bitstreams and performing a parity depuncturing on a parity part of the bitstreams.

[12] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

[13] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

Advantageous Effects

[14] According to the present invention, it is possible to provide a method of efficiently

transmitting and receiving signals and efficient transmitter and receiver for an OFDM system including TFS.

Brief Description of the Drawings

[15] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[16] Fig. 1 is a block diagram of an example of a TFS (Time Frequency Slicing)-OFDM (Orthogonal Frequency Division Multiplexing) transmitter.

[17] Fig. 2 is a block diagram of an example of the input processor shown in the Fig. 1.

[18] Fig. 3 is a block diagram of an example of the BICM (Bit-Interleaved Coding and Modulation) shown in Fig. 1.

[19] Fig. 4 shows an example of LDPC encoding using shortening / puncturing.

[20] Fig. 5 is a block diagram of an example of the Frame Builder shown in Fig. 1.

[21] Fig. 6 is a table of an example of a hybrid modulation ratio when an LDPC block length is 64800 bits.

[22] Fig. 7 is a table of an example of a hybrid modulation ratio when an LDPC block length is 16200 bits.

[23] Fig. 8 is a block diagram of an example of the QAM mapper shown in Fig. 1.

[24] Fig. 9 is a block diagram of an example of the QAM mapper combined with an inner encoder and an inner interleaver.

[25] Fig. 10 is an example of a bit interleaver.

[26] Fig. 11 is a table of an example of the bit interleaver when an LDPC block length is 64800 bits.

[27] Fig. 12 is a table of an example of the bit interleaver when an LDPC block length is 16200 bits.

[28] Fig. 13 is an example of the demux shown in Fig. 1.

[29] Fig. 14 is another example of the demux shown in Fig. 1.

[30] Fig. 15 is a relationship between an input bitstream of the bit interleaver and an output bitstream of the demux.

[31] Fig. 16 is an example of a QAM symbol mapping.

[32] Fig. 17 shows an example of a timer interleaver.

[33] Figs. 18 and 19 show an example of a convolutional interleaving.

[34] Fig. 20 shows an example of a time interleaver and a TFS frame builder.

[35] Fig. 21 is a block diagram of an example of the MIMO/MISO decoder shown in Fig. 1.

[36] Fig. 22 is a block diagram of an example of the modulator, specifically an example

of an OFDM modulator.

[37] Fig. 23 is a block diagram of an example of the analog processor shown in Fig. 1.

[38] Fig. 24 is a block diagram of an example of a TFS-OFDM receiver.

[39] Fig. 25 is a block diagram of an example of the AFE (Analog Front End) shown in Fig. 24.

[40] Fig. 26 is a block diagram of an example of the demodulator, specifically an OFDM demodulator.

[41] Fig. 27 is a block diagram of an example of the MIMO/MISO decoder shown in Fig. 24.

[42] Fig. 28 is a block diagram of an example of the frame parser shown in Fig. 24.

[43] Fig. 29 is a block diagram of an example of the QAM demapper shown in Fig. 28.

[44] Fig. 30 is a block diagram of an example of the QAM demapper combined with an inner deinterleaver.

[45] Fig. 31 shows a time deinterleaver.

[46] Fig. 32 shows a time deinterleaver.

[47] Fig. 33 is a block diagram of an example of the BICM decoder shown in Fig. 24.

[48] Fig. 34 shows an example of LDPC decoding using padding /depuncturing.

[49] Fig. 35 is a block diagram of an example of the output processor shown in Fig. 24.

Best Mode for Carrying Out the Invention

[50] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[51] Fig. 1 shows an example of proposed TFS (Time Frequency Slicing)-OFDM (Orthogonal Frequency Division Multiplexing) transmitter. A multiple MPEG2-TS (Transport Stream) and a multiple Generic stream can be inputted into a TFS transmitter. The input processor (101) can split the inputted streams into a multiple output signals for a multiple PLP (Physical Layer Path). The BICM (Bit-Interleaved Coding and Modulation) (102) can encode and interleave the PLP individually. The frame builder (103) can transform the PLP into total R of RF bands. MIMO (Multiple-Input Multiple-Output)/MISO (Multiple-Input Single-Output) (104) technique can be applied for each RF band. Each RF band for each antenna can be individually modulated by the modulator (105a, b) and can be transmitted to antennas after being converted to an analog signal by the analog processor (106a, b).

[52] Fig. 24 shows an example of a TFS-OFDM receiver. When total R of RF bands are used for TFS system, received signals by AFE (Analog Front End) (801a,b) can be demodulated by demodulators (802a,b), then can be decoded by MIMO/MISO Decoder

(803) to obtain diversity gain. Frame parser (804) can restore multiple PLP signals from received TFS frame. BICM decoder (805) can correct errors in a transmission channel. Finally, output processor (806) can restore signals according to necessary format.

Mode for the Invention

[53] Fig. 2 is an example of the input processor. MPEG-TS (Transport Stream) can be multiplexed into a single output through TS-MUX (201a) and Generic streams (Internet protocol) can be transformed into a single output through GSE (General Stream Encapsulation) (201b). Each output from the TS-MUX and GSE can be split for multiple services by the service splitter (202a, b). PLP is a processing of each service. Each PLP can be transformed into a frame by the BB (Baseband) Frame (103a~d).

[54] Fig. 3 is an example of the BICM. The Outer encoder (301) and the inner encoder (303) can add redundancy for error correction in a transmission channel. The outer interleaver (302) and the inner interleaver (304) can interleave data randomly to mitigate burst errors.

[55] Fig. 4 shows an example of an LDPC encoding using shortening / puncturing. First, shortening process is performed on input blocks having having number of bits smaller than required number of bits for LDPC encoding. Zeros as many as bits required for LDPC encoding can be padded (301a). Zero Padded input bitstreams can have parity bit through LDPC encoding (302a). At this point, among output bitstreams, for bitstreams corresponding to original input bitstreams, padded zeros can be removed (303a) and for generated parity bit streams, puncturing can be performed according to code-rate (304a). These bit streams can be outputted after being multiplexed (305a) in order of data bit streams and parity bit streams.

[56] Fig. 5 is an example of the frame builder. QAM mapper (401a, b) can transform inputted bits into QAM symbols. Hybrid QAM can be used. Time domain interleaver (402a, b) can interleave data in time domain to make the data be robust against burst error. At this point, an effect of interleaving many RF bands can be obtained in a physical channel because the data are going to be transmitted to a multiple RF bands. TFS frame builder (403) can split inputted data to form TFS frames and send the TFS frames to total R of RF bands according to a TFS scheduling. Each RF band can be individually interleaved in frequency domain by frequency domain interleaver (404a, b) and can become robust against frequency selective fading. Ref (Reference Signals), PL (Physical Layer) signaling, and pilots can be inserted when the TFS frame is built (405).

[57] By hybriding two Even-QAMs, which transmits even number of bits per QAM

symbol, an Odd-QAM, which transmits odd number of bits per QAM symbol can be formed by a Hybrid QAM mapper. For example, hybrid 128-QAM can be obtained by hybriding 256-QAM and 64-QAM, hybrid 32-QAM can be obtained by hybriding 64-QAM and 16-QAM, and hybrid 8-QAM can be obtained by hybriding 16-QAM and 4-QAM.

[58] Figs. 6 and 7 show examples of a hybrid ratio when DVB-S2 LDPC (Low Density Parity Check) code is used as an inner code. The first column on the table represents constellation type. HOQ (Higher-Order QAM) ratio represents a ratio for higher-order QAM between two QAM types. LOQ (Lower-Order QAM) ratio is 1-HOQ ratio. Hybrid QAM can be obtained by two adjacent Even-QAMs. For example, hybrid 128-QAM (bit/cell=7) is obtained by hybriding 256-QAM and 64-QAM. HOQ bits and LOQ bits represent number of bits used for mapping into HOQ symbol and LOQ symbol respectively in one LDPC block. HOQ symbols and LOQ symbols represent number of symbols after symbol mapping. Total symbol is a sum of the HOQ symbols and the LOQ symbols. The last column on the table represents effective number of bits transmitted per QAM symbol. As seen on the table, only Hybrid 128-QAM shows a slight difference from 7 bit/cell.

[59] Fig. 7 shows a case when LDPC block length is 16200 bits. When a scheduling is performed to evenly distribute QAM symbols, which are generated by the Frame Builder, to RF bands of TFS system, the value of the total symbols should be divisible by a least common multiple of each index number of RF band. For example, if six RF bands are allowed, then the value of total symbols on the table should be divisible by a least common multiple of 1 through 6, i.e., 60. For the case shown in Fig. 6, it is divisible. However, for the case shown in Fig. 7, it is not divisible. If LDPC block length is 16200 bits as shown in Fig. 7, the total symbols on the table can be made divisible by 60 by combining four of the LDPC blocks into a single LDPC block having a length of 64800 as in Fig. 6.

[60] Convolution interleaver can be used as an example of the time interleavers (402, 402b) shown in Fig. 5. Interleaver depth is L*(L-1)*M for a case where a number of delay branch is L and a length of basic delay element is M. At this point, to be able to perform a convolutional interleaving on LDPC encoded and QAM mapped (401a, 401b) symbol streams, a length of the symbol stream corresponding to an LDPC block should be a multiple of L*(L-1).

[61] However, for a system where 4/16/64/256-QAM mappings are applied to an LDPC code using n = 64800bits or 16200 bits, 16200/8 is 2025 symbols, which is not a multiple of two consecutive integers. Further, even for a case where hybrid modulation is used, a symbol stream having a length of multiple of L*(L-1) may not be obtained.

[62] For such a case, a new LDPC code can be made by performing puncturing/shortening

such that n have 1440*44=63360 bits or 1440*10=14400 bits. Then, 1440 is 48*6*(6-1). Thus, a symbol stream having a length of multiple of two consecutive integers can be obtained.

[63] In addition, as shown in Figs. 6 and 7 where a hybrid modulation is used, HOQ ratio=13/22 and LOQ ratio=9/22 can be used for hyb 128-QAM and hyb 32-QAM, and HOQ ratio=2/3 and LOQ ratio=1/3 can be used for hyb 8-QAM. Then, convolutional interleaver can be implemented for every even QAM and hybrid QAM while satisfying length condition of integer multiples of L*(L-1).

[64] For a receiver side, the original codeword length according to the puncturing/shortening scheme can be restored, then LDPC decoding can be performed. If a convolutional interleaver where a single LDPC block is interleaved for two TFS frames can be defined as a basic convolutional interleaver (BCI) and if a number of LDPC blocks transmitted to TFS frame is N, then a final convolutional interleaver can be implemented by using total N of the BCI having the BCI as a basic unit.

[65] For such a case, each LDPC block can be assigned to a single BCI, thus, convolutional interleaver can be implemented without extra dummy padding. Total N of BCI output symbols can be multiplexed to form the final convolutional interleaver output. For a receiver side, symbols can be demultiplexed into N convolutional deinterleaver corresponding to BCI, a single output can be outputted by combining the number of LDPC blocks transmitted to the TFS frame.

[66] As another example, instead of the puncturing/shortening, dummy padding can be performed to convolutional interleaving input symbols such that a length become a multiple of L*(L-1). For this case, a receiver can perform a deinterleaving and then remove a predetermined number of dummy symbols. One of the advantages of this method can be no loss in performance because of not performing puncturing/shortening to the original LDPC code.

[67] Fig. 8 shows an example of QAM mapper using hybrid modulation. Bit stream parser(c-401) can parse inputted bitstreams into HOQ mapper(c-402a) and LOQ mapper(c-402b). The symbol merger(c-403) can merge the two inputted symbol streams into a single symbol stream. FEC (Forward Error Correction) block merger (c-404), for example, can combine four of bit symbol blocks having a length of 16200 into a single block having a length of 64800.

[68] Fig. 9 shows an example of QAM mapper combined with inner interleavers. Bitstreams can be divided by bitstream parser (d-402) into bitstreams for HOQ and LOQ mappers. Each bitstream goes through bit interleaving (d-403a, d-403b) and demux (d-404a, d-404b) processes. Throughout these processes, characteristics of LDPC codeword and constellation reliability can be combined. Each output can be converted into symbolstreams by the HOQ and LOQ mappers (d-405a, d-405b), then

merged into a single symbolstream by the symbol merger (d-406).

[69] Fig. 10 shows an example of bit interleaving. Bits can be saved into a matrix type memory having columns and rows in the direction of column or in the direction of the blue arrow. Then the saved bits can be read out in the direction of row or in the direction of the red arrow. Figs. 11 and 12 show numbers of columns and rows of HOQ bit interleaver (d-403a) and LOQ bit interleaver (d-403b) according to QAM modulation type. As seen in the tables, when a typical even-QAM is used but a hybrid modulation is not used, only HOQ interleaving is used.

[70] Fig. 13 shows an example of the demux. It shows that interleaved outputs according to QPSK, 16-QAM, 64-QAM, and 256-QAM can be demultiplexed and mapped. It also shows that the numbers of output bitstreams from demuxs are 2, 4, 6, and 8 respectively.

[71] Details of the demux operation are shown in Fig. 14. As seen in the figure, output order of interleaver can be changed by demux. For example, for the case of 16-QAM, bitstreams can be outputted as j-th output bitstream of each demux according to a value resulting from performing an modulo-4 operation on index of input bitstream b. Fig. 14 shows a relationship between a value resulting from a modulo operation and demux output branch index j.

[72] Fig. 15 shows a relationship between an input bitstream of bit interleaver and an output bitstream of demux. As seen in the equations, dividing index of input bitstream by 2, 4, 6, and 8 is a result by the interleaving and mapping each index to index of output bitstream is a result by the demux.

[73] Fig. 16 shows an example of QAM symbol mapping. Output bitstream of demux can be converted into symbolstream by using Gray mapping rule. Even if it is not shown, it can be extended to constellation of 256-QAM or more.

[74] Fig. 17 shows an example of a timer interleaver. For the inputted QAM symbols, the Dummy symbol generator (401j) can generate dummy symbols such that a number of symbols in a TFS frame become a multiple of L*(L-1). In addition, the multiplexer (402j) can perform padding to the QAM symbols. After this adjustment of number of input symbols, interleaving can be performed by the Convolutional interleaver (403j).

[75] Figs. 18 and 19 show an example of a convolutional interleaving. Using a convolutional interleaver in a TFS system where a multiple of RF bands are used may cause a decrease in frequency diversity gain. Figs. 18 and 19 show such a case. For simplification, a convolutional interleaving which uses four RF bands, FEC block composed of twenty symbols, four branches, and five for a length of elements is exemplified. Represents as (a) are source symbols. If necessary, by performing zero padding to the (a), (b) can be obtained which fills TFS frame length. By performing interleaving to the (b), (c) can be obtained. At this point, for the (n+1)th frame, by excluding padded

zeros and outputting only source symbols, (d) can be obtained. By assigning the outputted symbols sequentially to RF0~RF3, (e) can be finally outputted. For the RF bands where green and yellow colored FEC blocks are assigned, it can be seen that the blocks are not evenly distributed for the all four RF bands, but the blocks are more assigned for certain RF bands than other RF bands. Consequently, frequency diversity gain can be lowered.

[76] Fig. 20 shows an example of a time interleaver and a TFS frame builder. Specifically, Fig. 20 shows a case where a typical convolutional interleaver is implemented and a possible solution to a decrease in frequency diversity gain. As a solution to a decrease in frequency diversity gain, convolutional interleaving unit (CIU) can be used for each RF band and by doing this, for a single FEC block, a same number of symbol can be assigned to each RF band. Thus, even if convolutional interleaver is used in TFS system, decrease in frequency diversity gain can be prevented. The inputted symbols are sequentially inputted to total R of CIUs (4021~4011) which are assigned to total R of RF bands by the switching (4011). Total R of CIUs (4021~4041) can have a same structure as typical convolutional interleaver and can perform interleaving to the inputted symbols. At this point, the final outputs can be transmitted to TFS frame builder and the frame builder should perform a scheduling such that, for all PLPs, symbols assigned to a same RF band can be transmitted to the same RF band.

[77] Fig. 21 shows an example of MIMO/MISO Encoder. MIMO/MISO Encoder (501) applies MIMO/MISO method to obtain an additional diversity gain or payload gain. MIMO/MISO Encoder can output signals for total A of antennas. MIMO encoding can be performed individually on total A of antenna signals for each RF band among total R of RF bands. A is equal to or greater than 1.

[78] Fig. 22 shows an example of a modulator, specifically an example of an OFDM modulator. PAPR (Peak-to-Average Power Ratio) reduction 1 (601) can be performed on Antenna (m) signals of RF (n) bands. IFFT (602) can be performed for OFDM demodulation. PAPR reduction 2 (603) can be performed after the IFFT. ACE (Active Constellation Extension) and a tone reservation can be used for the PAPR reduction 2 (603). Lastly, guard interval (604) can be inserted.

[79] Fig. 23 shows an example of the analog processor. Output of each modulator can be converted to an analog-domain signal by a DAC (Digital to Analog Conversion) (701), then can be transmitted to antenna after up-conversion (702). Analog filtering (703) can be performed.

[80] Fig. 24 shows an example of a TFS-OFDM receiver. When total R of RF bands are used for TFS system, received signals by AFE (Analog Front End) (801a,b) can be demodulated by demodulators (802a,b), then can be decoded by MIMO/MISO Decoder (803) to obtain diversity gain. Frame parser (804) can restore multiple PLP signals

from received TFS frame. BICM decoder (805) can correct errors in a transmission channel. Finally, output processor (806) can restore signals according to necessary format.

[81] Fig. 25 shows an example of an AFE (Analog Front End). FH (Frequency Hopping)-tuner (901) can perform a frequency hopping and tune signals according to inputted RF center frequency. After down-conversion (902), signals can be converted to digital signals by ADC (Analog to Digital Conversion) (903).

[82] Fig. 26 shows an example of a demodulator, specifically an OFDM demodulator. TFS detector (1001) can detect TFS signals in a received digital signal. TFS sync (1002) can synchronize in time and frequency domains. After GI (Guard Interval) (1003) is removed, symbols in frequency domain can be obtained by performing FFT (1004) for OFDM demodulation. Channel Estimation (1005) can estimate distortion in a transmission channel based on pilot signals. Based on the estimated distortion, Channel Equalization (1006) can compensate distortion in the transmission channel. Finally, PL (Physical Layer) signaling information can be extracted from equalized data and can be transmitted to a system controller.

[83] Fig. 27 shows an example of MIMIO/MISO decoder. Diversity and multiplexing gain can be obtained from data received from total B of antennas. For MIMO, B is greater than 1. For MISO, B is 1.

[84] Fig. 28 shows an example of a Frame parser. Total R of the inputted RF bands data can undergo frequency deinterleaving (1201a, b), then can be reconstructed into datastream by TFS frame parser for each PLP (Physical Layer Path) according to a TFS scheduling. For each PLP, input data for BICM decoder can be obtained by using time domain deinterleaver (1203a, b) and QAM demapper (1204a, b). At this point, hybrid QAM demapper can be used as the QAM demapper.

[85] Fig. 29 shows an example of performing a QAM demapper, which is a counterpart of Fig. 8 of transmitter. FEC block splitter can split inputted symbol block unit having 64800 bits into four symbol blocks of 16200 bits when short DVB-S2 LDPC mode is used. Symbol splitter (a-1202) can split inputted symbol streams into two symbol streams for HOQ and LOQ demapper. HOQ demapper (a-1203a) and LOQ demapper (a-1203b) can perform HOQ and LOQ demapping respectively. Bitstream merger (a-1204) can merge two inputted bit streams into a single output bitstream.

[86] Fig. 30 shows an example of a QAM demapper combined with inner deinterleavers which are counterparts of Fig. 9 of transmitter. For each PLP, symbol splitter (b-1201) can split output of time domain deinterleaver into two symbol streams for HOQ and LOQ demappers. HOQ and LOQ Demapper (b-1202a, b-1202b) can convert symbolstreams into bitstreams. Each bitstream can be rearranged by multiplexer (b-1203a, b-1203b), which is a counterpart of the demux of Fig. 9 of transmitter. Two bit dein-

terleavers (b-1204a, b-1204b) can deinterleave bitstreams according to constellation type. Finally, bitstream merger (b-1205) can merge bitstreams into a single bitstream, then LDPC decoder (b-1206) can correct errors in a transmission channel.

[87] Fig. 31 shows a time deinterleaver, a counterpart of time interleaver shown in Fig. 17 Convolutional Deinterleaving (1201a) can be performed on input symbol streams and dummy symbols can be removed (1202a).

[88] Fig. 32 shows a time deinterleaver, a counterpart of time interleaver shown in Fig. 20. Convolutional Deinterleaving (1201b~1203b) can be performed on input symbol streams for each RF band and for each PLP symbol streams. Original PLP symbol streams can be restored by multiplexing (1204b) the outputs of each Convolutional deinterleaving unit to original sequence.

[89] Fig. 33 shows an example of a BICM decoder. Inner deinterleaver (1301) and outer deinterleaver (1303) can convert burst errors in a transmission channel into random errors. Inner decoder (1302) and outer decoder (1304) can correct errors in the transmission channel.

[90] Fig. 34 shows an example of LDPC decoding for shortened/punctured LDPC codeword. For input bit streams, demux (1301a) can separate systematic code into information part and parity part. For information part, zero padding (1302a) can be performed according to Number of Input bit of LDPC decoder. For parity part, input bit streams for LDPC decoder can be generated by depuncturing (1303a). Afterwards, LDPC decoding (1304a) can be performed and zeros in information part can be removed (1305a).

[91] Fig. 35 shows an example of an output processor. BB (Baseband) frame parser (1401a~d) can reconstruct input data into total P of PLP data. Service mergers (1402a, b) can merge data into a single TS (Transport Stream) and a single GSE stream. For TS, TS-demux (1403a) can reconstruct original TS. For GSE stream, GSE Decapsulation (1403b) can reconstruct generic stream.

[92] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

[1] A method of transmitting signals for an OFDM (Orthogonal Frequency Division Multiplexing) system including TFS (Time Frequency Slicing), comprising:
encoding frames made of bitstreams;
performing a modulation to transform the encoded frames into symbols;
performing a puncturing and a shortening on the symbols such that the symbols have lengths of two consecutive integers multiplied by at least one integer; and
encoding the puncturing and the shortening performed symbols into a multiple signal or a single signal.

[2] The method according to claim 1, wherein performing the modulation comprises:
parsing the frames into HOQ (Higher Order Quadrature Amplitude Modulation) bits and LOQ (Lower Order Quadrature Amplitude Modulation) bits;
mapping the HOQ bits into HOQ symbols;
mapping the LOQ bits into LOQ symbols; and
performing a hybrid modulation to the HOQ symbols and the LOQ symbols, wherein ratios used to perform the hybrid modulation are chosen to enable a convolutional interleaving of the HOQ symbols and the LOQ symbols.

[3] The method according to claim 1, further comprising:
performing a convolutional interleaving for each RF band on the puncturing and the shortening performed symbols.

[4] The method according to claim 3, further comprising:
demuxing the puncturing and the shortening performed symbols to each RF band such that each RF band receives a same number of symbols.

[5] The method according to claim 1, wherein performing the puncturing and the shortening on the symbols further comprises:
generating and inserting dummy symbols such that the symbols have lengths of two consecutive integers multiplied by at least one integer.

[6] A receiver for an OFDM (Orthogonal Frequency Division Multiplexing) system including TFS (Time Frequency Slicing), comprising:
a demodulator (802a) configured to transform received signals into OFDM symbols;
a frame parser (804) configured to perform modulation to transform the OFDM symbols into bitstreams; and
a BICM(Bit-Interleaved Coding and Modulation) decoder (805) configured to deinterleave the bitstreams through performing a zero padding on an information part of the bitstreams and performing a parity depuncturing on a parity part of the bitstreams.

[7] The receiver according to claim 6, further comprising:
a convolutional deinterleaver (1201a) configured to perform convolutional deinterleaving on the OFDM symbols, wherein the convolutional deinterleaver comprises a plurality of a CDU (Convolutional Deinterleaving Unit) (1201b), wherein each CDU is configured to perform convolutional deinterleaving on the OFDM symbols which correspond to a RF band that is different from every other RF band.

[8] The receiver according to claim 7, further comprising:
a demux (1204b) configured to demux outputs from the CDUs into symbol streams.

[9] The receiver according to claim 8, further comprising:
a dummy removal unit (1202a) configured to remove dummy symbols from the demuxed symbol streams.

[10] The receiver according to claim 6, further comprising:
a decoder (1304a) configured to decode the zero padded bitstreams and the parity depunctured bitstreams.

[11] A method of receiving signals for an OFDM (Orthogonal Frequency Division Multiplexing) system including TFS (Time Frequency Slicing), comprising:
transforming received signals into OFDM symbols;
performing modulation to transform the OFDM symbols into bitstreams; and
deinterleaving the bitstreams through performing a zero padding on an information part of the bitstreams and performing a parity depuncturing on a parity part of the bitstreams.

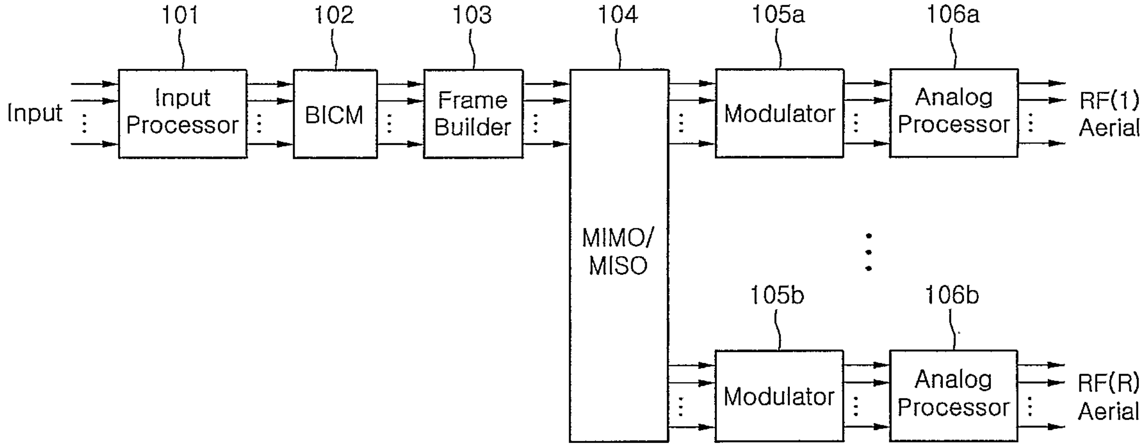
[12] The method according to claim 11, further comprising:
performing convolutional deinterleaving on the OFDM symbols which correspond to a RF band that is different from every other RF band.

[13] The method according to claim 12, further comprising:
demuxing the convolutional deinterleaved OFDM symbols into symbol streams.

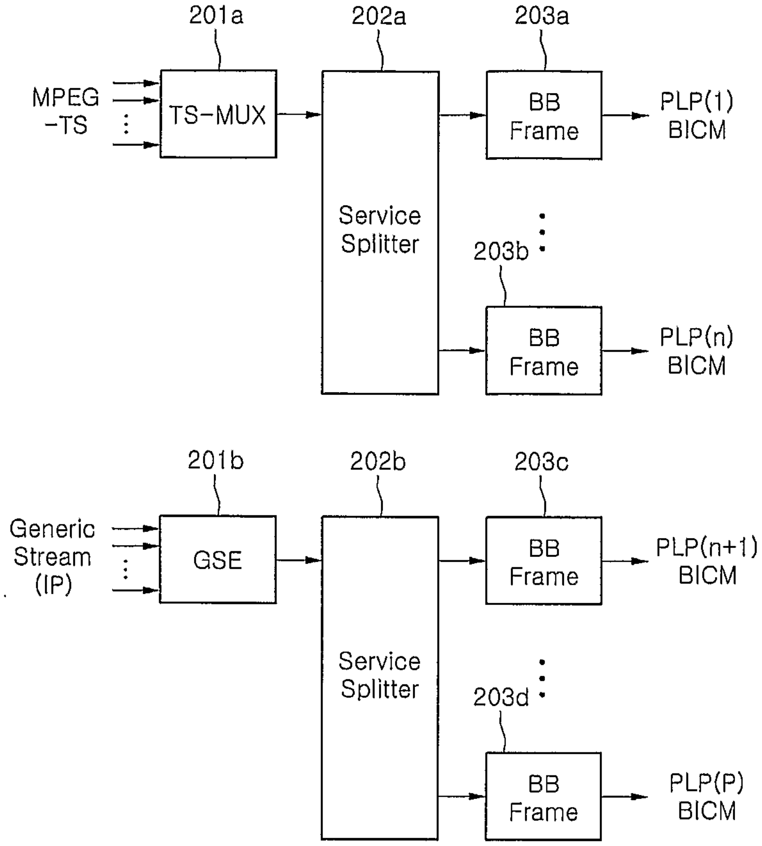
[14] The method according to claim 13, further comprising:
removing dummy symbols from the demuxed symbol streams.

[15] The method according to claim 11, further comprising:
decoding the zero padded bitstreams and the parity depunctured bitstreams.

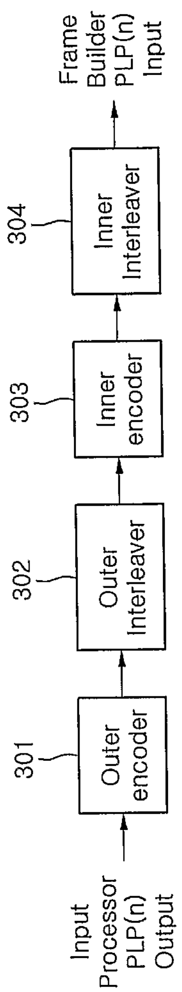
[Fig. 1]


Input
101
Input Processor
102
BICM
103
Frame Builder
104
MIMO/ MISO
105a
Modulator
106a
Analog Processor
RF(1) Aerial
105b
Modulator
106b
Analog Processor
RF(R) Aerial

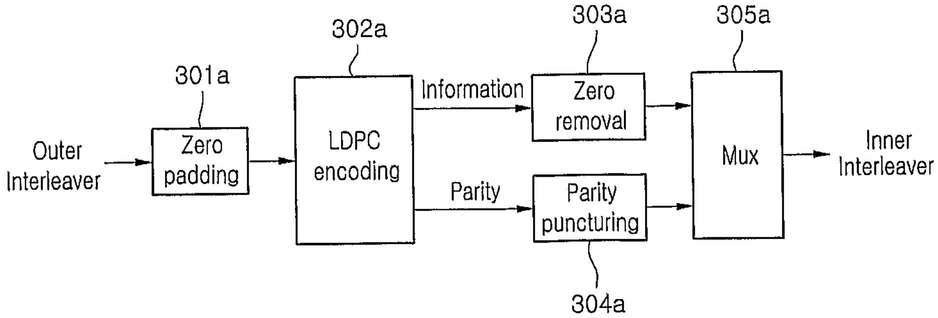
[Fig. 2]


201a
202a
203a
MPEG
-TS
TS-MUX
Service
Splitter
BB
Frame
PLP(1)
BICM
203b
BB
Frame
PLP(n)
BICM
201b
202b
203c
Generic
Stream
(IP)
GSE
Service
Splitter
BB
Frame
PLP(n+1)
BICM
203d
BB
Frame
PLP(P)
BICM

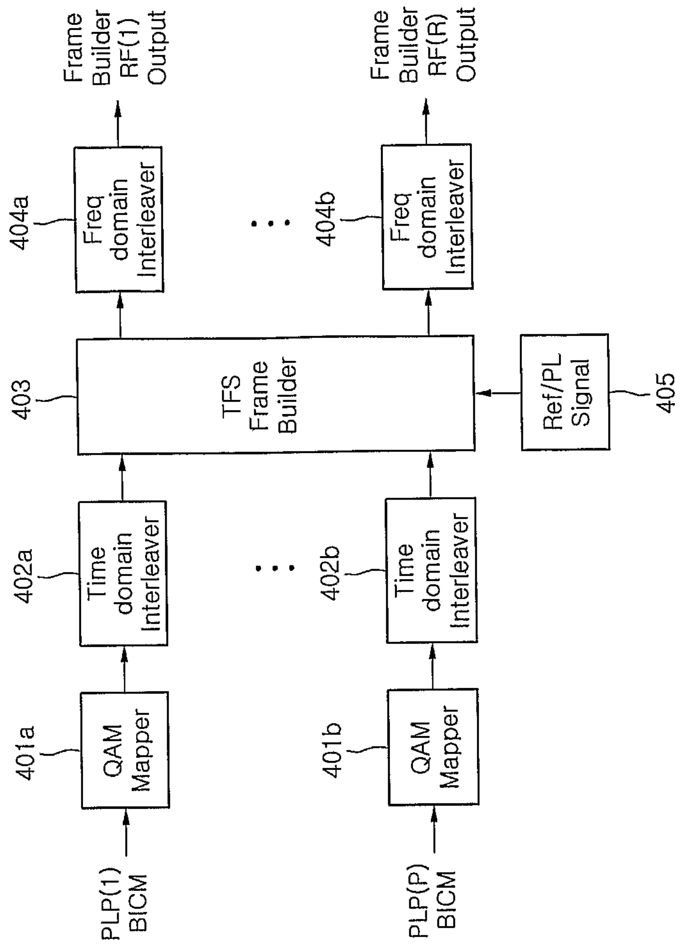
[Fig. 3]


Frame Builder PLP(n) Input
304
Inner Interleaver
303
Inner encoder
302
Outer Interleaver
301
Outer encoder
Input Processor PLP(n) Output

[Fig. 4]


302a
303a
305a
301a
Information
Zero removal
Outer Interleaver
Zero padding
LDPC encoding
Mux
Inner Interleaver
Parity
Parity puncturing
304a

[Fig. 5]



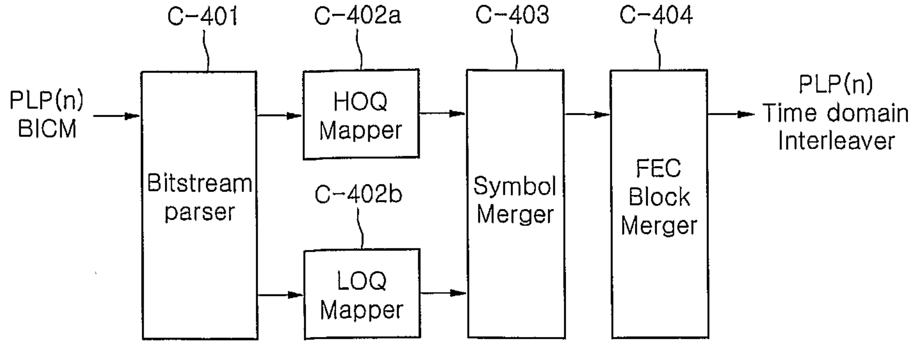
[Fig. 6]

Constellation Type	HOQ ratio	HOQ bits	LOQ bits	HOQ symbols	LOQ symbols	Total symbols	bit/cell
256-QAM	1	64800	0	8100	0	8100	8
Hybrid 128-QAM	3/5	38880	25920	4860	4320	9180	7.0588
64-QAM	1	64800	0	10800	0	10800	6
Hybrid 32-QAM	3/5	38880	25920	6480	6480	12960	5
16-QAM	1	64800	0	16200	0	16200	4
Hybrid 8-QAM	2/3	43200	21600	10800	10800	21600	3
QPSK	1	64800	0	32400	0	32400	2

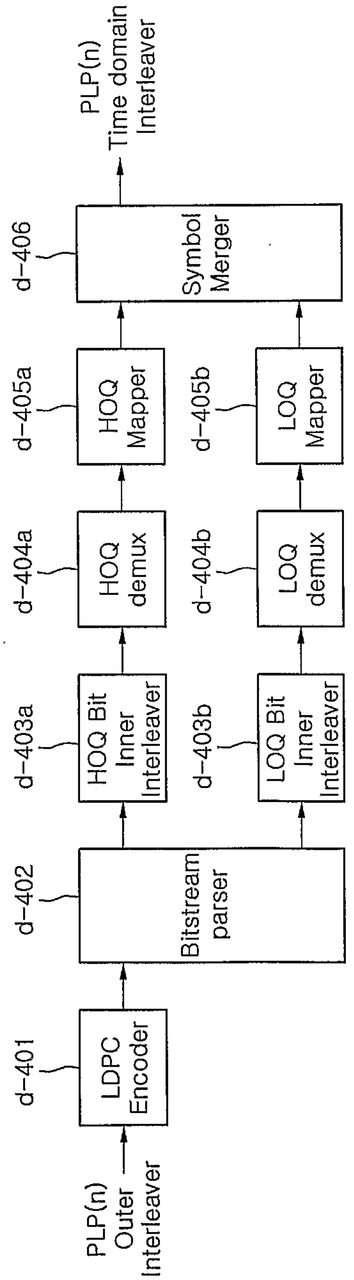
[Fig. 7]

Constellation Type	HOQ ratio	HOQ bits	LOQ bits	HOQ symbols	LOQ symbols	Total symbols	bit/cell
256-QAM	1	16200	0	2025	0	2025	8
Hybrid 128-QAM	3/5	9720	6480	1215	1080	2295	7.0588
64-QAM	1	16200	0	2700	0	2700	6
Hybrid 32-QAM	3/5	9720	6480	1620	1620	3240	5
16-QAM	1	16200	0	4050	0	4050	4
Hybrid 8-QAM	2/3	10800	5400	2700	2700	5400	3
QPSK	1	16200	0	8100	0	8100	2

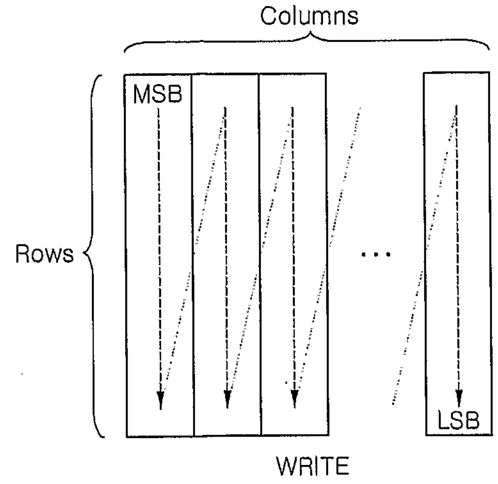
[Fig. 8]

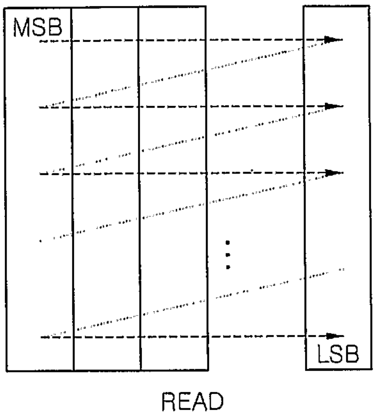

C-401
C-402a
C-403
C-404
PLP(n) BICM
Bitstream parser
HOQ Mapper
C-402b
LOQ Mapper
Symbol Merger
FEC Block Merger
PLP(n) Time domain Interleaver

[Fig. 9]


PLP(n) Outer Interleaver
d-401
LDPC Encoder
d-402
Bitstream parser
d-403a
HOQ Bit Inner Interleaver
d-403b
LOQ Bit Inner Interleaver
d-404a
HOQ demux
d-404b
LOQ demux
d-405a
HOQ Mapper
d-405b
LOQ Mapper
d-406
Symbol Merger
PLP(n) Time domain Interleaver

[Fig. 10]





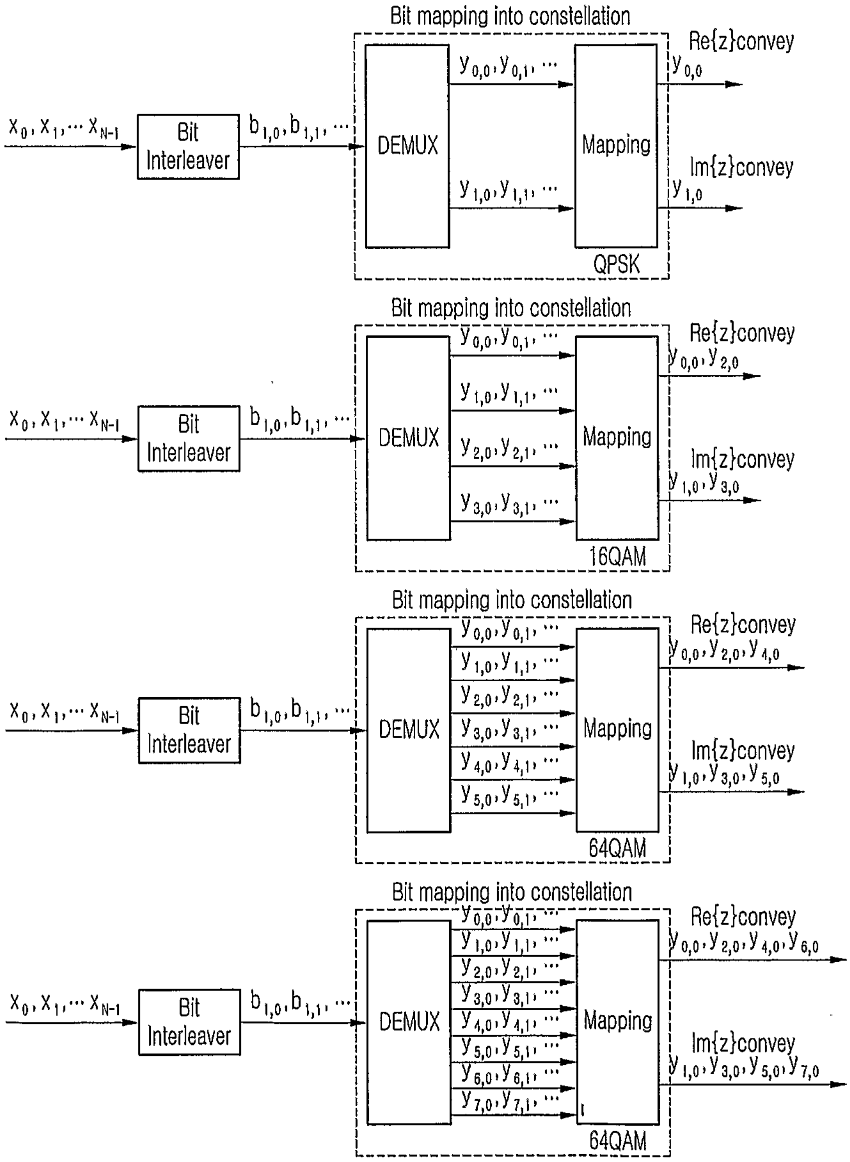
[Fig. 11]

QAM type	HOQ Rows	HOQ Columns	LOQ Rows	LOQ Columns
256-QAM	8100	8		
Hybrid 128-QAM	4860	8	4320	6
64-QAM	10800	6		
Hybrid 32-QAM	6480	6	6480	4
16-QAM	16200	4		
Hybrid 8-QAM	10800	4	10800	2
4-QAM	32400	2		

[Fig. 12]

QAM type	HOQ Rows	HOQ Columns	LOQ Rows	LOQ Columns
256-QAM	2025	8		
Hybrid 128-QAM	1215	8	1080	6
64-QAM	2700	6		
Hybrid 32-QAM	1620	6	1620	4
16-QAM	4050	4		
Hybrid 8-QAM	2700	4	2700	2
4-QAM	8100	2		

[Fig. 13]



[Fig. 14]

QPSK
b 0 maps to y0.0 b 1 maps to y1.0

16-QAM
b 0 maps to y2.0 b 1 maps to y3.0 b 2 maps to y0.0 b 3 maps to y1.0

64-QAM
b 0 maps to y4.0 b 1 maps to y5.0 b 2 maps to y2.0 b 3 maps to y3.0 b 4 maps to y0.0 b 5 maps to y1.0

256-QAM
b 0 maps to y6.0 b 1 maps to y7.0 b 2 maps to y4.0 b 3 maps to y5.0 b 4 maps to y2.0 b 5 maps to y3.0 b 6 maps to y0.0 b 7 maps to y1.0

[Fig. 15]

QPSK: $i = 0, 1, 2, \ldots, \frac{N}{2} - 1$,

$$(y_{0,i}, y_{1,i}) = (x_i, x_{N/2+i}),$$

16-QAM: $i = 0, 1, 2, \ldots, \frac{N}{4} - 1$,

$$(y_{0,i}, y_{1,i}, y_{2,i}, y_{3,i}) = \left(x_{\frac{2N}{4}+i}, x_{\frac{3N}{4}+i}, x_i, x_{\frac{N}{4}+i}\right)$$

64-QAM: $i = 0, 1, 2, \ldots, \frac{N}{6} - 1$,

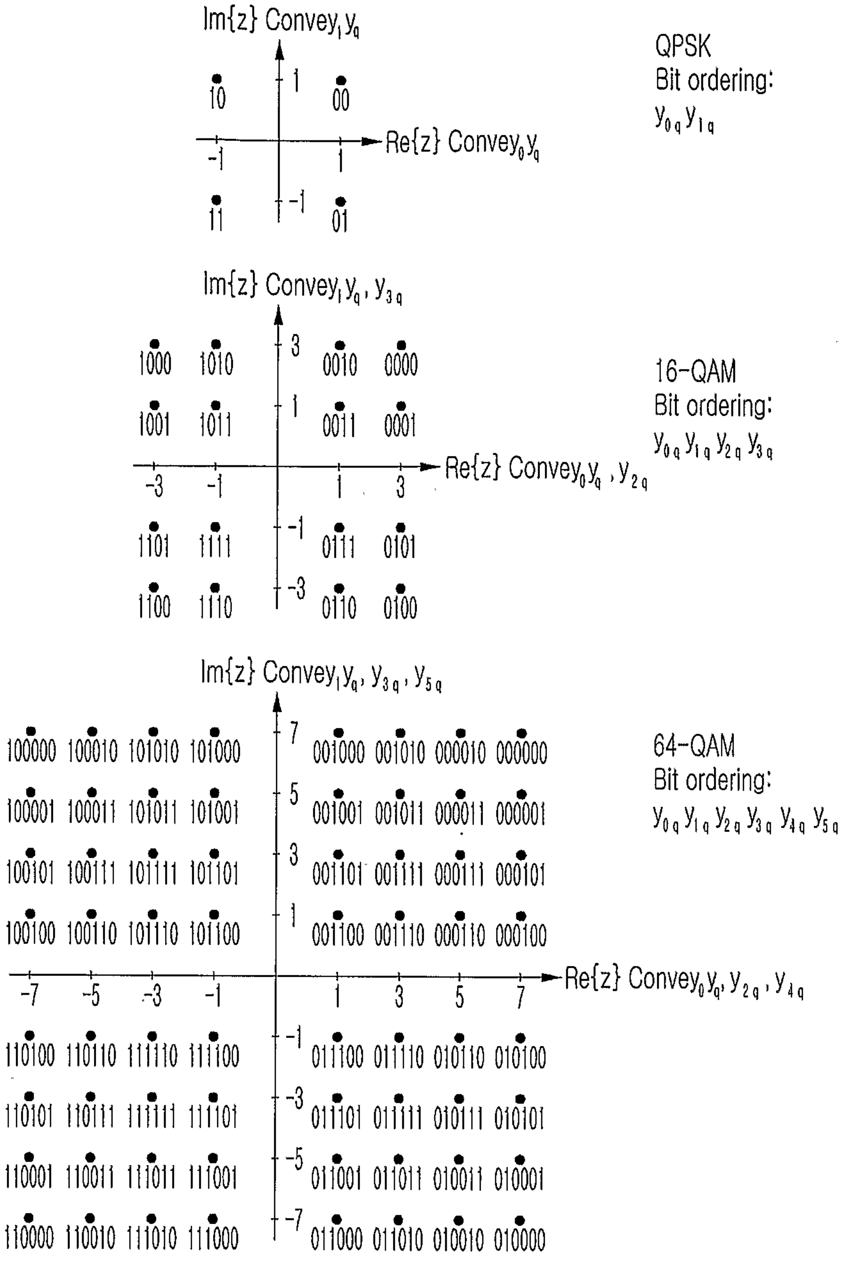
$$(y_{0,i}, y_{1,i}, y_{2,i}, y_{3,i}, y_{4,i}, y_{5,i}) = \left(x_{\frac{4N}{6}+i}, x_{\frac{5N}{6}+i}, x_{\frac{2N}{6}+i}, x_{\frac{3N}{6}+i}, x_i, x_{\frac{N}{6}+i}\right)$$

256-QAM: $i = 0, 1, 2, \ldots, \frac{N}{8} - 1$,

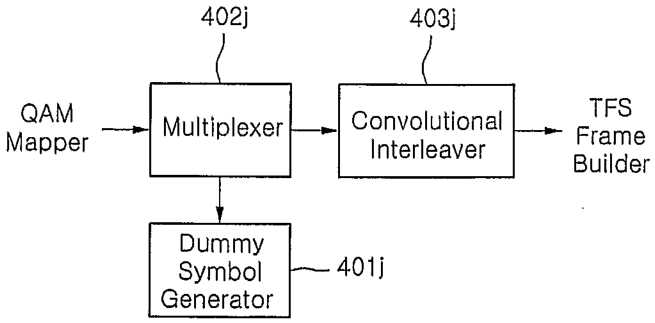
$$(y_{0,i}, y_{1,i}, y_{2,i}, y_{3,i}, y_{4,i}, y_{5,i}, y_{4,i}, y_{7,i}) = \left(x_{\frac{6N}{8}+i}, x_{\frac{7N}{8}+i}, x_{\frac{4N}{8}+i}, x_{\frac{5N}{8}+i}, x_{\frac{2N}{8}+i}, x_{\frac{3N}{8}+i}\ x_i, x_{\frac{N}{8}+i}\right)$$

N = number of HOQ/LOQ bits for bit interleaver input
x_i = i-th bit of HOQ/LOQ bits block for bit interleaver input
$Y_{j,i}$ = i-th bit of j-th demultiplexed bitstream output

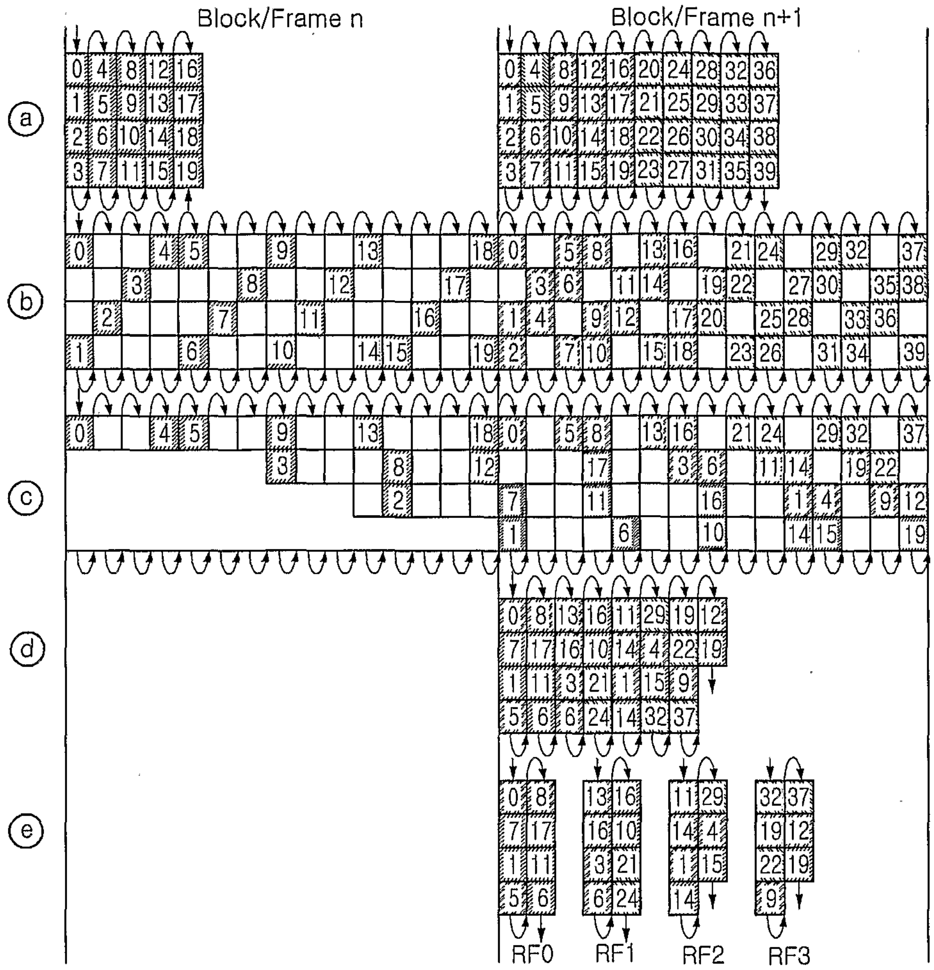
[Fig. 16]


Im{z} Convey$_1$y$_q$
QPSK
Bit ordering:
$y_{0q}\,y_{1q}$
10
00
1
Re{z} Convey$_0$y$_q$
-1
1
11
01
-1
Im{z} Convey$_1$y$_q$, y_{3q}
1000 1010 0010 0000
1001 1011 0011 0001
3
1
16-QAM
Bit ordering:
$y_{0q}\,y_{1q}\,y_{2q}\,y_{3q}$
Re{z} Convey$_0$y$_q$, y_{2q}
-3 -1 1 3
1101 1111 0111 0101
1100 1110 0110 0100
-1
-3
Im{z} Convey$_1$y$_q$, y_{3q}, y_{5q}
64-QAM
Bit ordering:
$y_{0q}\,y_{1q}\,y_{2q}\,y_{3q}\,y_{4q}\,y_{5q}$
7
5
3
1
100000 100010 101010 101000 001000 001010 000010 000000
100001 100011 101011 101001 001001 001011 000011 000001
100101 100111 101111 101101 001101 001111 000111 000101
100100 100110 101110 101100 001100 001110 000110 000100
Re{z} Convey$_0$y$_q$, y_{2q}, y_{4q}
-7 -5 -3 -1 1 3 5 7
-1
-3
-5
-7
110100 110110 111110 111100 011100 011110 010110 010100
110101 110111 111111 111101 011101 011111 010111 010101
110001 110011 111011 111001 011001 011011 010011 010001
110000 110010 111010 111000 011000 011010 010010 010000

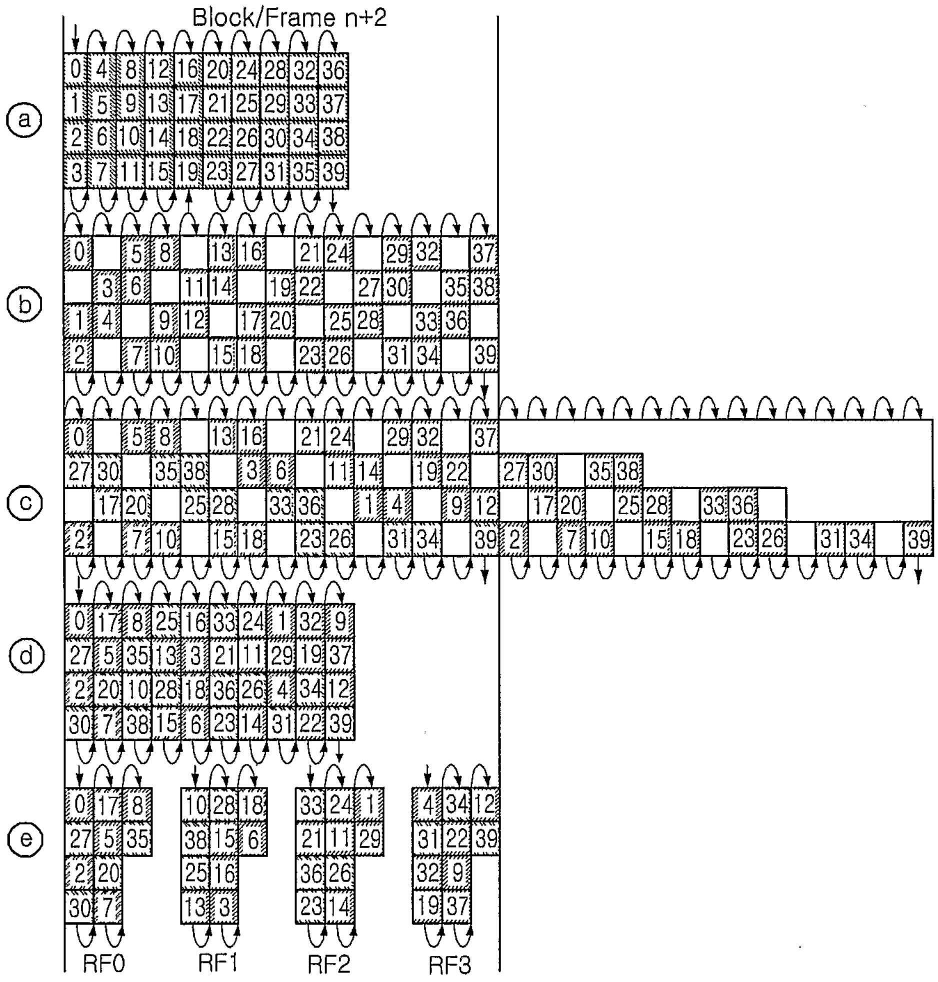
[Fig. 17]


402j
403j
QAM Mapper
Multiplexer
Convolutional Interleaver
TFS Frame Builder
Dummy Symbol Generator
401j

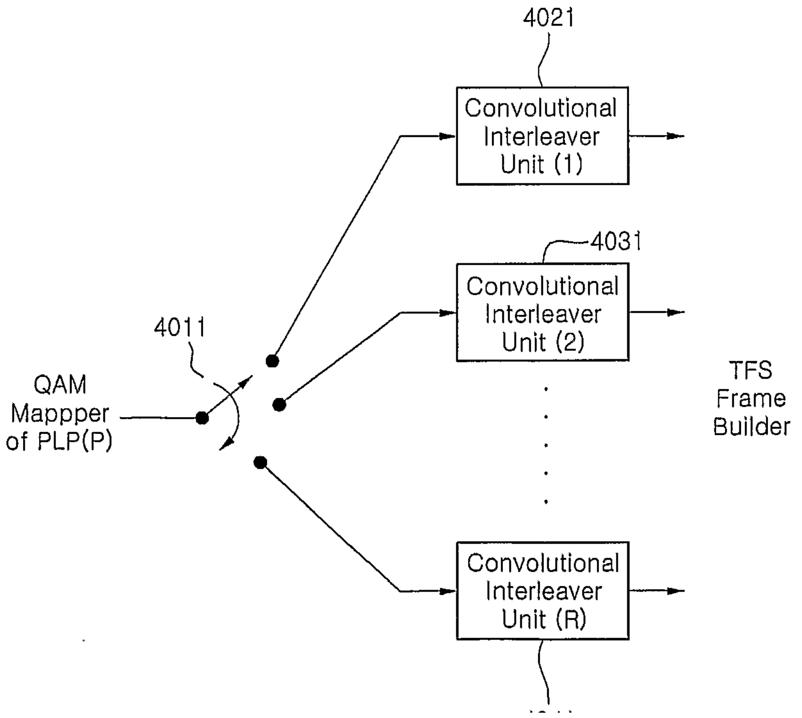
[Fig. 18]



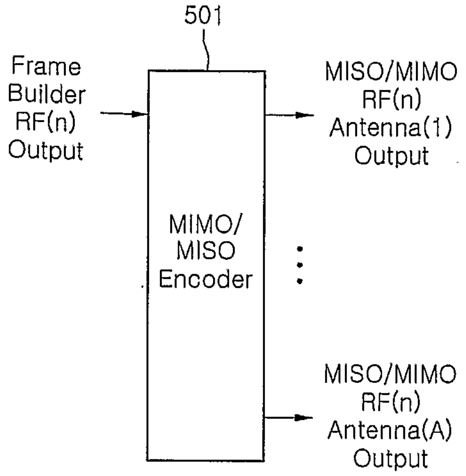
[Fig. 19]


Block/Frame n+2
ⓐ
ⓑ
ⓒ
ⓓ
ⓔ
RF0
RF1
RF2
RF3

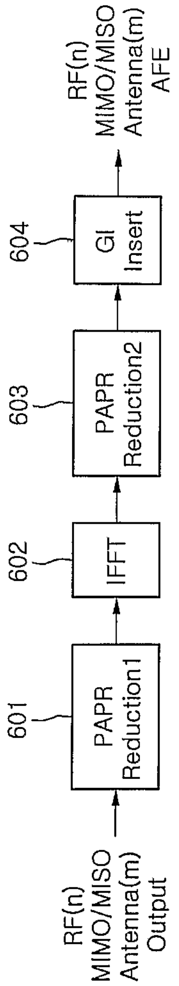
[Fig. 20]


4021
Convolutional Interleaver Unit (1)
4031
Convolutional Interleaver Unit (2)
4011
QAM Mappper of PLP(P)
TFS Frame Builder
Convolutional Interleaver Unit (R)

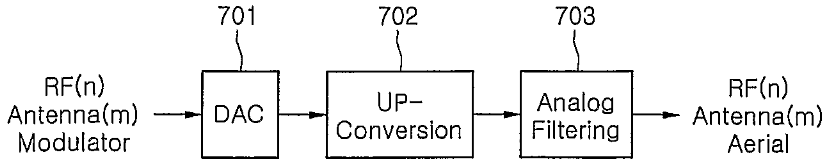
[Fig. 21]



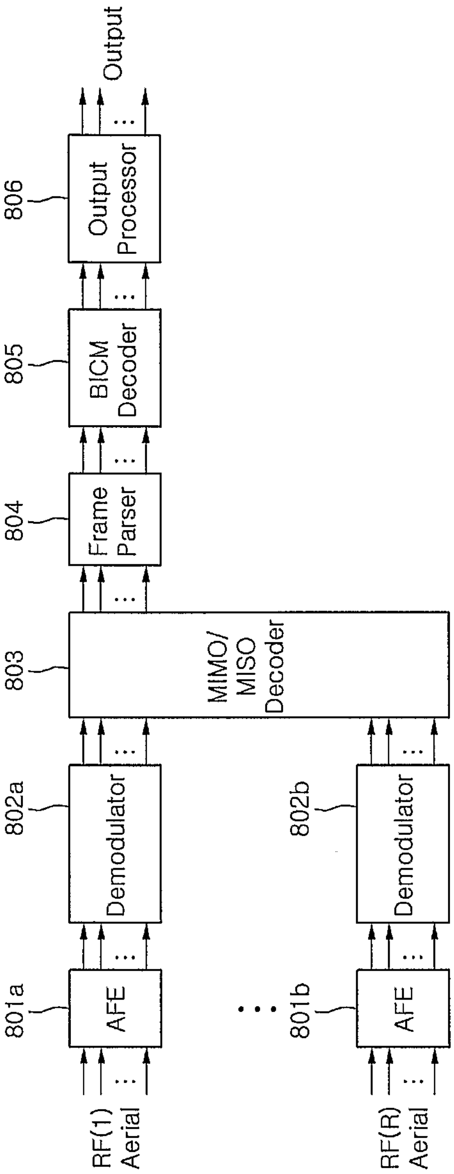
[Fig. 22]



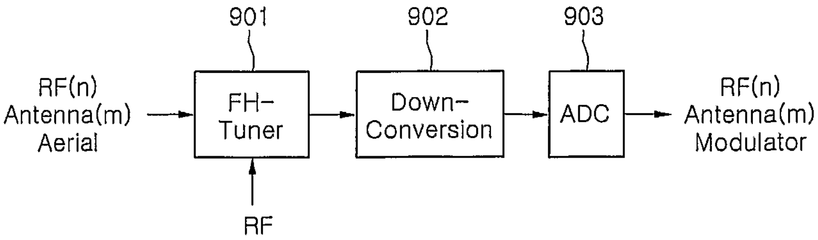
[Fig. 23]



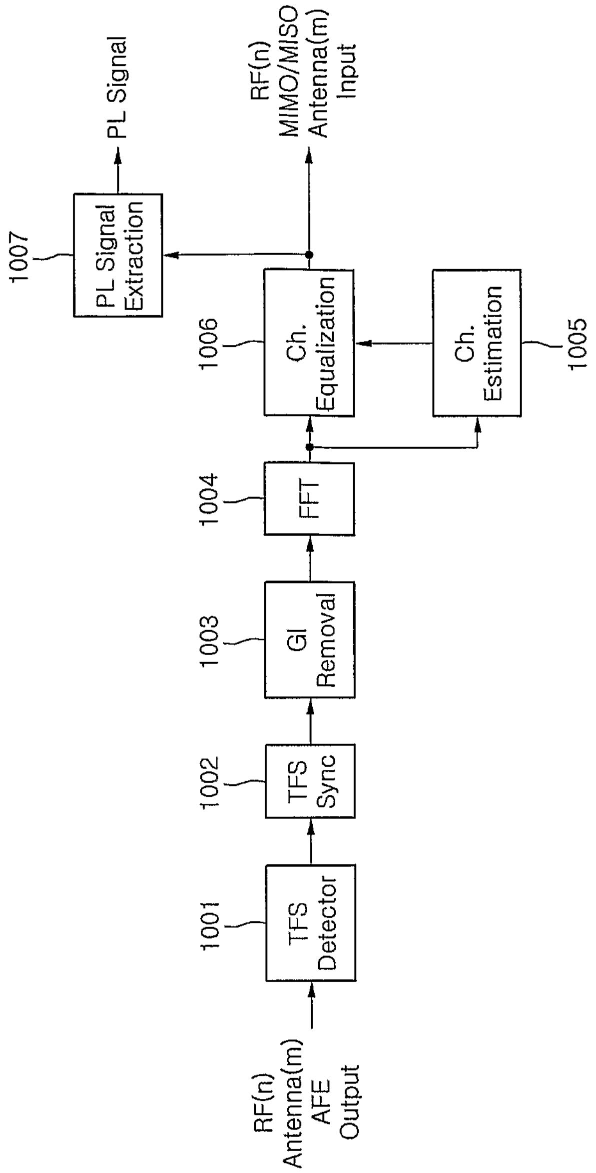
[Fig. 24]


Output
806
Output Processor
805
BICM Decoder
804
Frame Parser
803
MIMO/ MISO Decoder
802a
Demodulator
802b
Demodulator
801a
AFE
801b
AFE
RF(1) Aerial
RF(R) Aerial

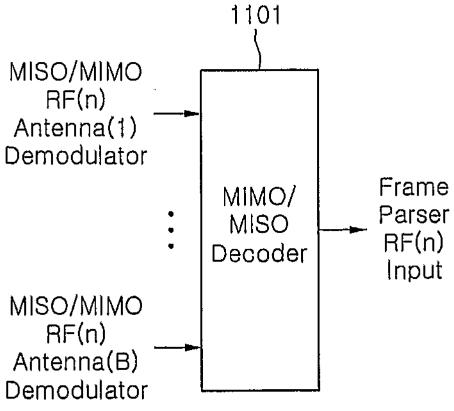
[Fig. 25]


901
902
903
RF(n) Antenna(m) Aerial
FH-Tuner
Down-Conversion
ADC
RF(n) Antenna(m) Modulator
RF

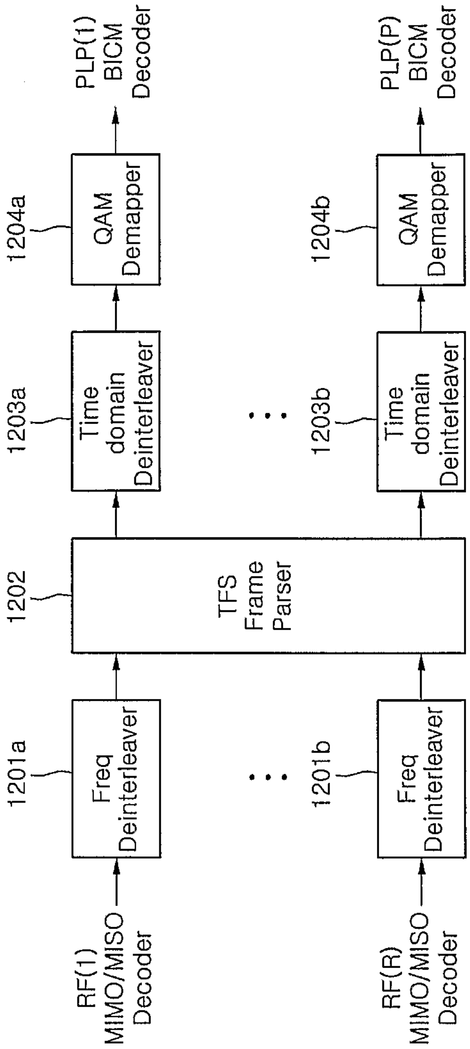
[Fig. 26]


RF(n)
Antenna(m)
AFE
Output
1001
TFS
Detector
1002
TFS
Sync
1003
GI
Removal
1004
FFT
1005
Ch.
Estimation
1006
Ch.
Equalization
1007
PL Signal
Extraction
PL Signal
RF(n)
MIMO/MISO
Antenna(m)
Input

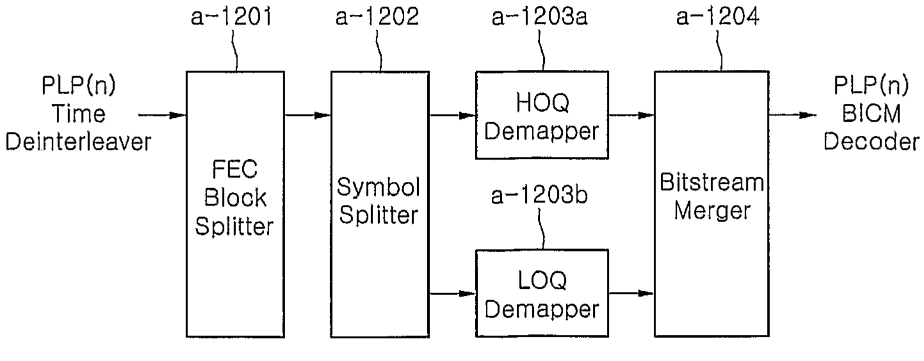
[Fig. 27]


1101
MISO/MIMO
RF(n)
Antenna(1)
Demodulator
MISO/MIMO
RF(n)
Antenna(B)
Demodulator
MIMO/
MISO
Decoder
Frame
Parser
RF(n)
Input

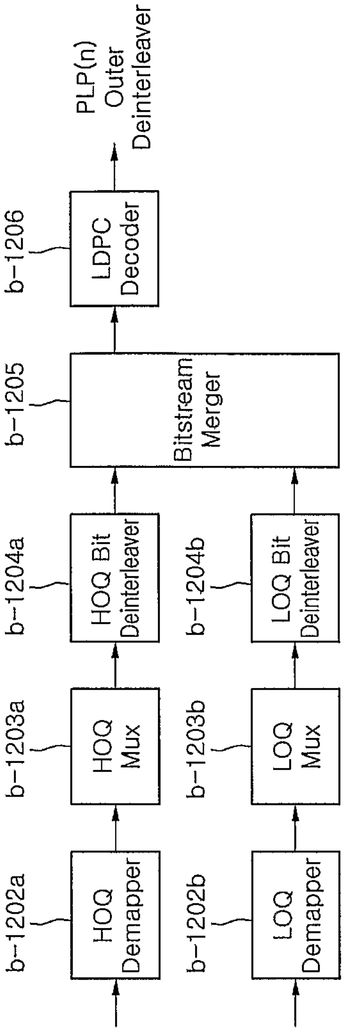
[Fig. 28]


RF(1) MIMO/MISO Decoder
1201a
Freq Deinterleaver
1202
TFS Frame Parser
1203a
Time domain Deinterleaver
1204a
QAM Demapper
PLP(1) BICM Decoder
RF(R) MIMO/MISO Decoder
1201b
Freq Deinterleaver
1203b
Time domain Deinterleaver
1204b
QAM Demapper
PLP(P) BICM Decoder
...
...

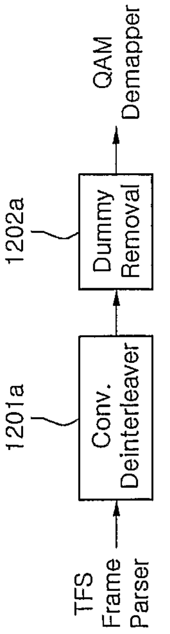
[Fig. 29]


PLP(n) Time Deinterleaver
a-1201
FEC Block Splitter
a-1202
Symbol Splitter
a-1203a
HOQ Demapper
a-1203b
LOQ Demapper
a-1204
Bitstream Merger
PLP(n) BICM Decoder

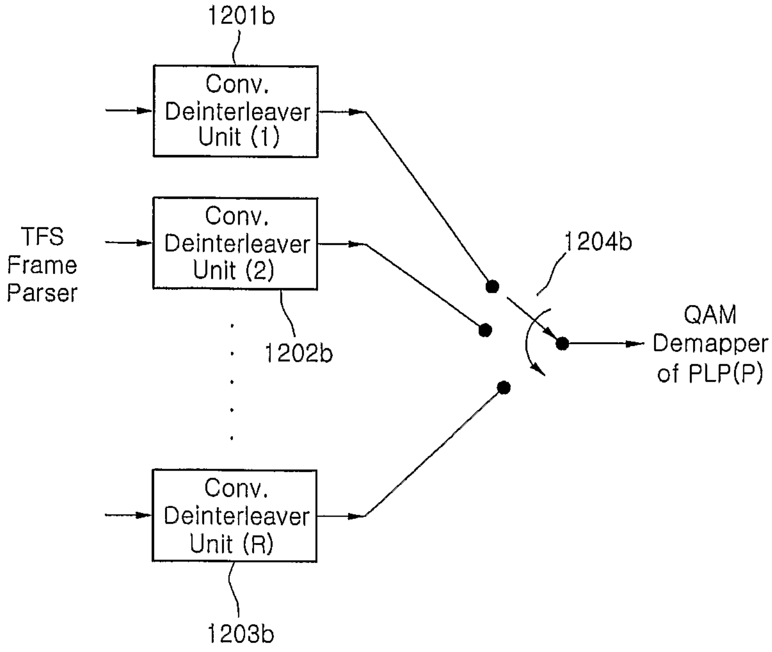
[Fig. 30]


b-1202a
HOQ Demapper
b-1203a
HOQ Mux
b-1204a
HOQ Bit Deinterleaver
b-1202b
LOQ Demapper
b-1203b
LOQ Mux
b-1204b
LOQ Bit Deinterleaver
b-1205
Bitstream Merger
b-1206
LDPC Decoder
PLP(n) Outer Deinterleaver

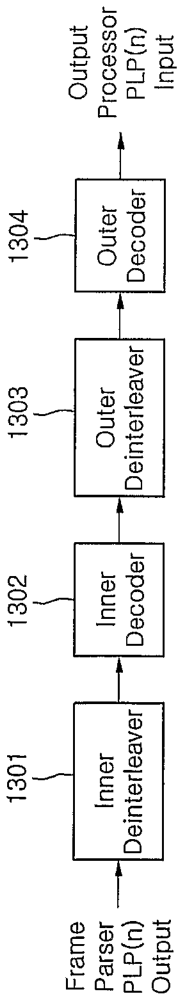
[Fig. 31]


TFS Frame Parser
1201a
Conv. Deinterleaver
1202a
Dummy Removal
QAM Demapper

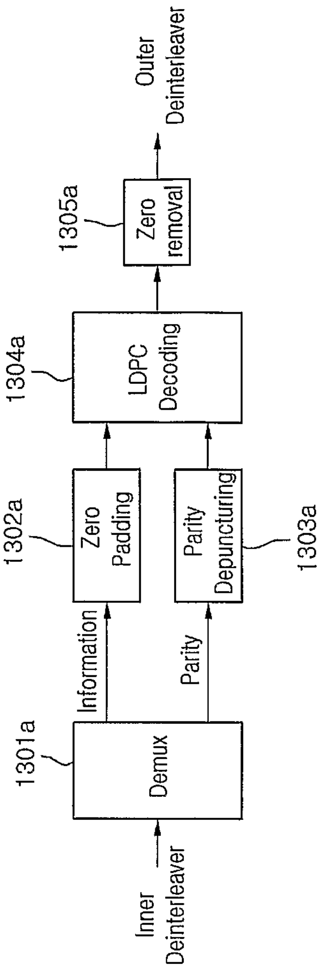
[Fig. 32]


1201b
Conv. Deinterleaver Unit (1)
TFS Frame Parser
Conv. Deinterleaver Unit (2)
1202b
1204b
QAM Demapper of PLP(P)
Conv. Deinterleaver Unit (R)
1203b

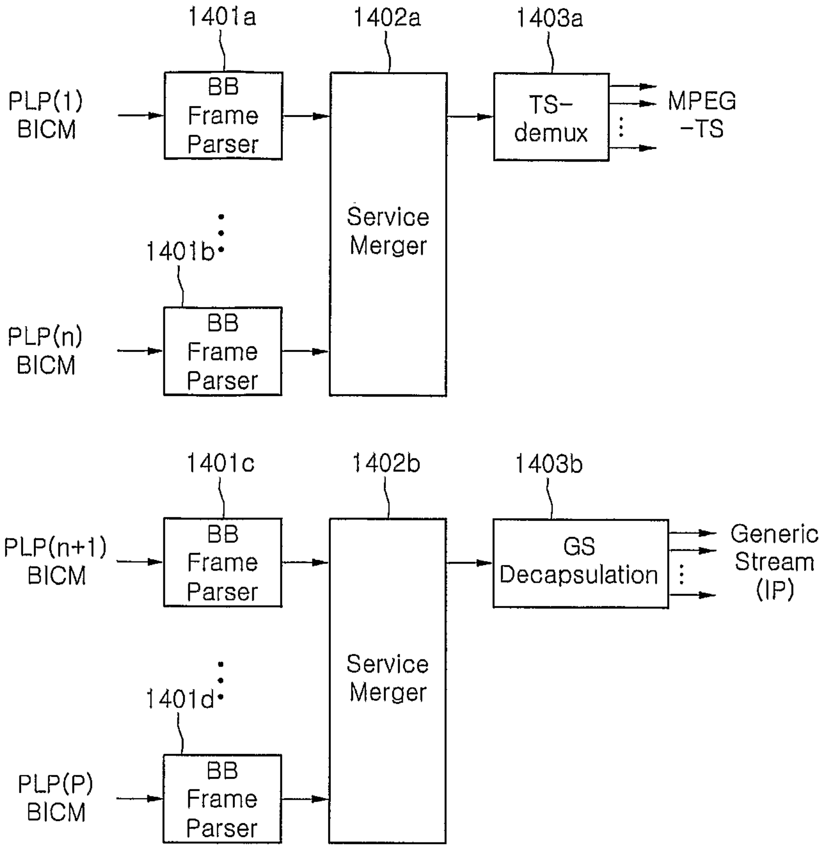
[Fig. 33]


Frame Parser PLP(n) Output
1301
Inner Deinterleaver
1302
Inner Decoder
1303
Outer Deinterleaver
1304
Outer Decoder
Output Processor PLP(n) Input

[Fig. 34]


Inner Deinterleaver
1301a
Demux
Information
Parity
1302a
Zero Padding
1303a
Parity Depuncturing
1304a
LDPC Decoding
1305a
Zero removal
Outer Deinterleaver

[Fig. 35]


1401a
1402a
1403a
PLP(1) BICM
BB Frame Parser
Service Merger
TS-demux
MPEG -TS
1401b
PLP(n) BICM
BB Frame Parser
1401c
1402b
1403b
PLP(n+1) BICM
BB Frame Parser
Service Merger
GS Decapsulation
Generic Stream (IP)
1401d
PLP(P) BICM
BB Frame Parser