US 20100012998A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2010/0012998 A1**

(43) **Pub. Date: Jan. 21, 2010**

**LEE et al.**

(54) **FLASH MEMORY DEVICE WITH STACKED DIELECTRIC STRUCTURE INCLUDING ZIRCONIUM OXIDE AND METHOD FOR FABRICATING THE SAME**

(75) Inventors: **Seung-Ryong LEE**, Ichon-shi (KR); **Moon-Sig Joo**, Ichon-shi (KR)

Correspondence Address:
**TOWNSEND AND TOWNSEND AND CREW, LLP**
**TWO EMBARCADERO CENTER, EIGHTH FLOOR**
**SAN FRANCISCO, CA 94111-3834 (US)**

(73) Assignee: **Hynix Semiconductor Inc.**, Ichon-shi (KR)

(21) Appl. No.: **12/568,591**

(22) Filed: **Sep. 28, 2009**

**Related U.S. Application Data**

(62) Division of application No. 11/582,705, filed on Oct. 17, 2006, now Pat. No. 7,595,240.

(30) **Foreign Application Priority Data**

Apr. 24, 2006 (KR) ..... 2006-0036924

**Publication Classification**

(51) **Int. Cl.**
***H01L 27/115*** (2006.01)
***H01L 29/788*** (2006.01)

(52) **U.S. Cl.** ..... **257/321**; 257/316; 257/E27.103; 257/E29.3

(57) **ABSTRACT**

A dielectric structure disposed between a floating gate and a control gate of a flash memory device includes: a first dielectric layer; a third dielectric layer having a k-dielectric constant substantially the same as that of the first dielectric layer; and a second dielectric layer disposed between the first dielectric layer and the third dielectric layer, having a greater k-dielectric constant than that of the first and third dielectric layers and formed by alternately and repeatedly stacking a plurality of aluminum oxide ($Al_2O_3$) layers and a plurality of zirconium oxide ($ZrO_2$) layers.

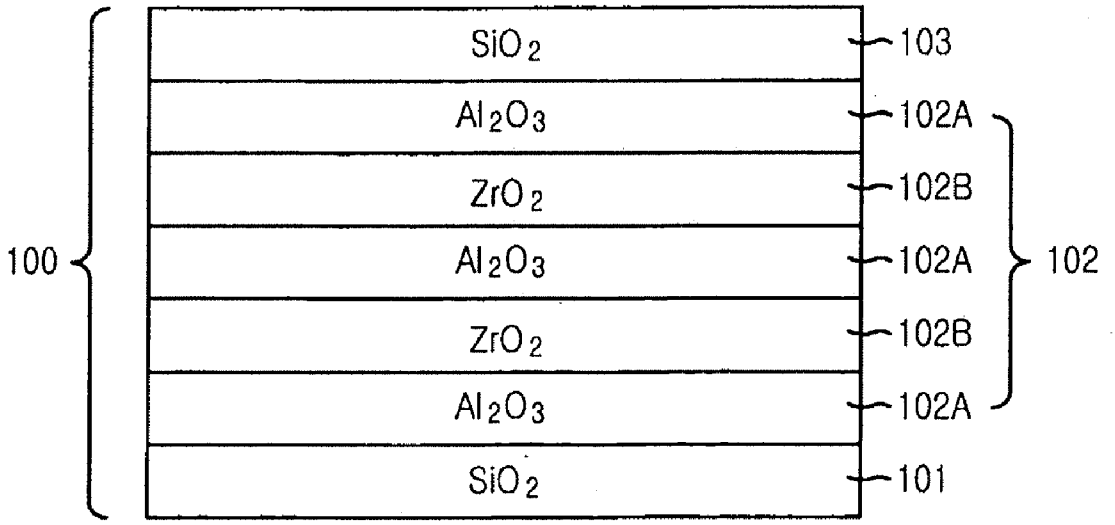


FIG. 1
(RELATED ART)

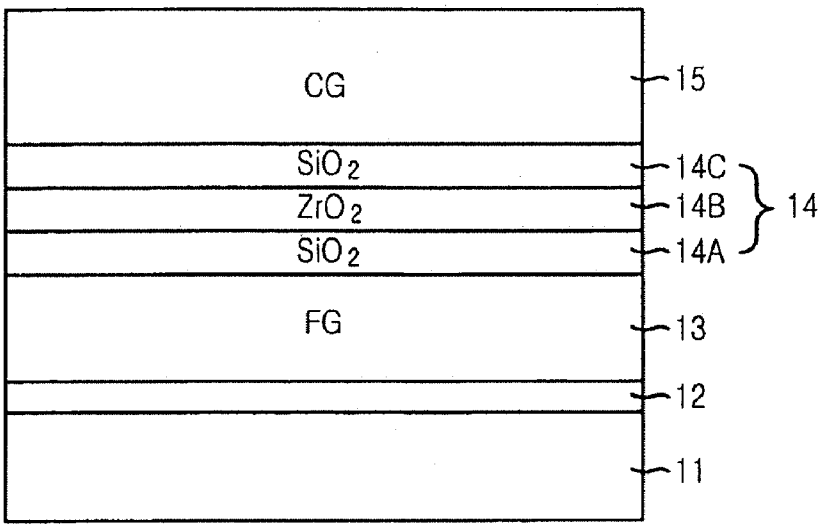



FIG. 2

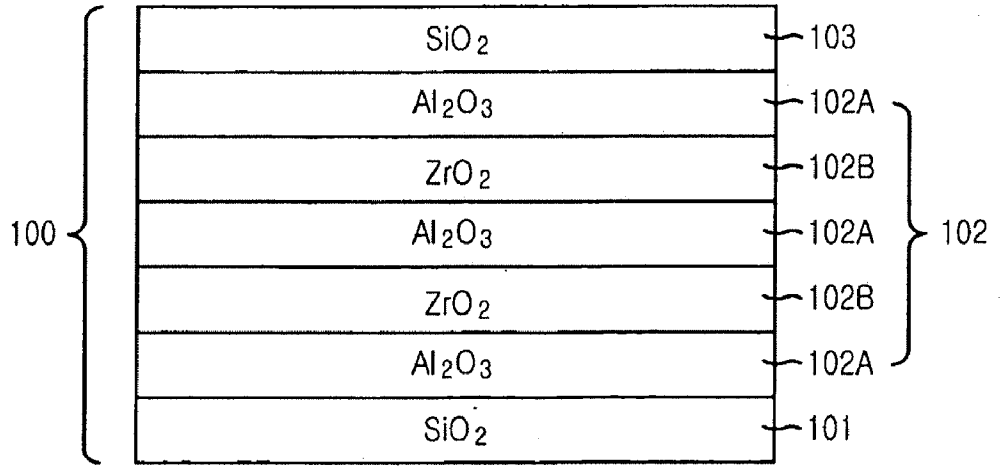


FIG. 3A

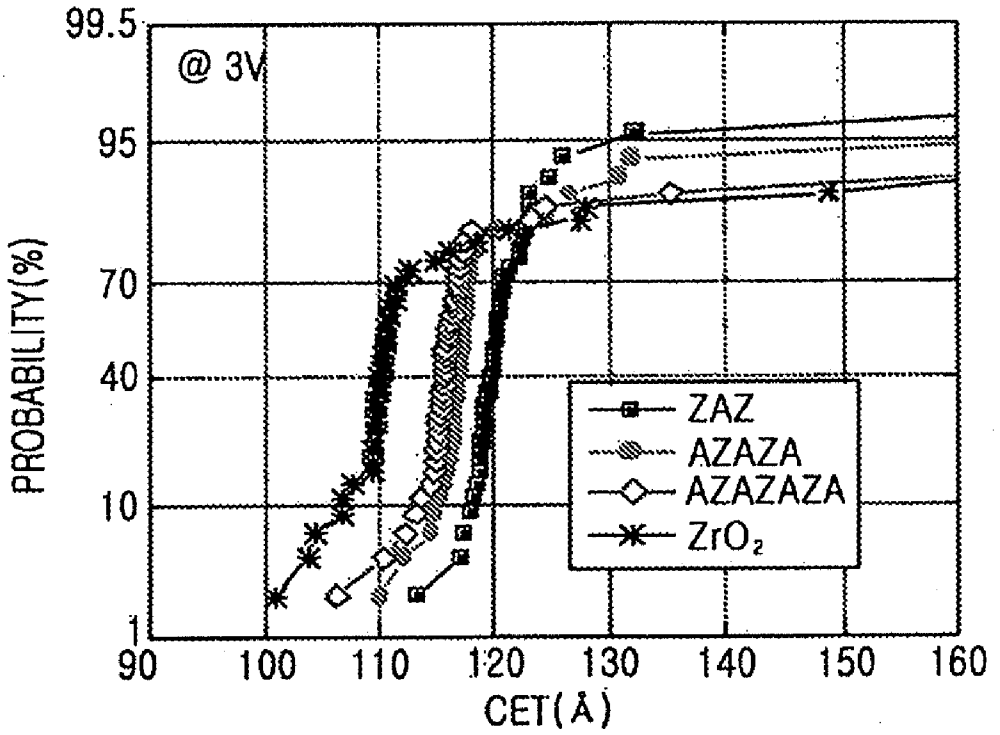

99.5
@ 3V
95
70
40
10
1
PROBABILITY(%)
90
100
110
120
130
140
150
160
CET(Å)
ZAZ
AZAZA
AZAZAZA
ZrO2

FIG. 3B

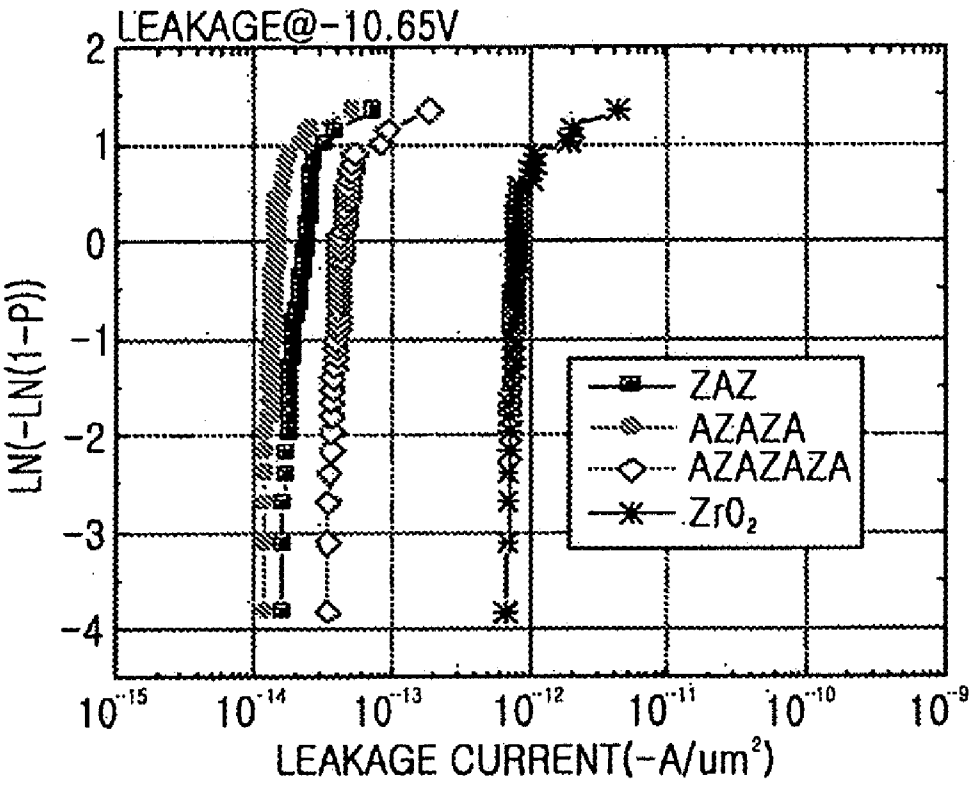

LEAKAGE@-10.65V
LN(-LN(1-P))
2
1
0
-1
-2
-3
-4
ZAZ
AZAZA
AZAZAZA
ZrO2
10^-15
10^-14
10^-13
10^-12
10^-11
10^-10
10^-9
LEAKAGE CURRENT(-A/um^2)

FIG. 4

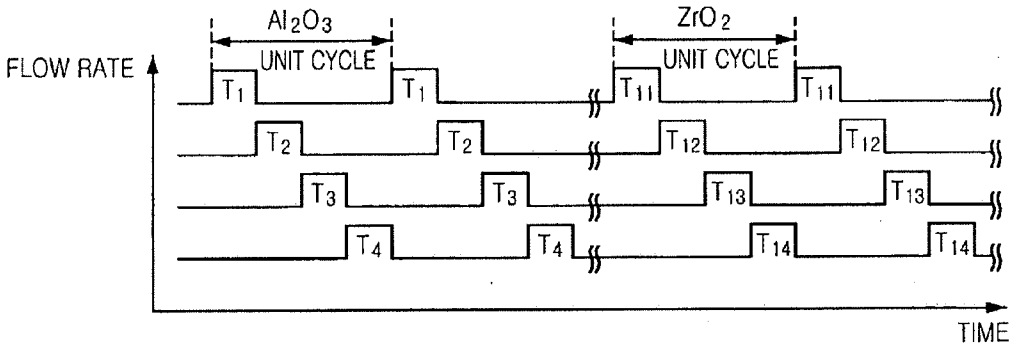

Al2O3
UNIT CYCLE
ZrO2
UNIT CYCLE
FLOW RATE
T1
T1
T11
T11
T2
T2
T12
T12
T3
T3
T13
T13
T4
T4
T14
T14
TIME

FIG. 5

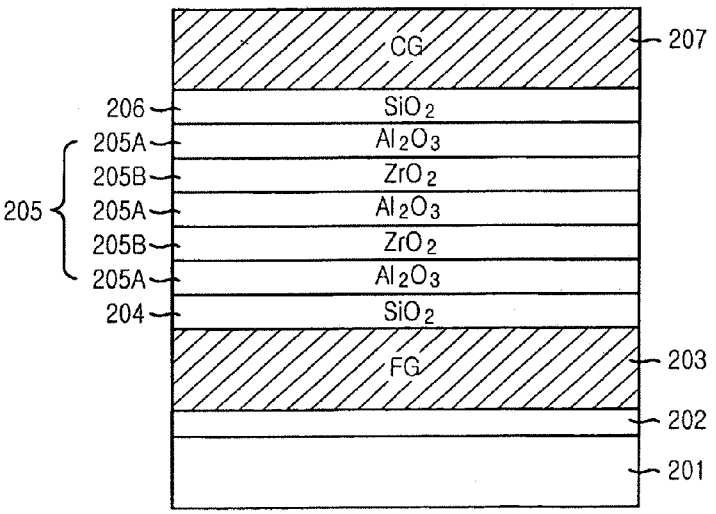

CG
207
206
SiO2
205A
Al2O3
205B
ZrO2
205
205A
Al2O3
205B
ZrO2
205A
Al2O3
204
SiO2
FG
203
202
201

FIG. 6A

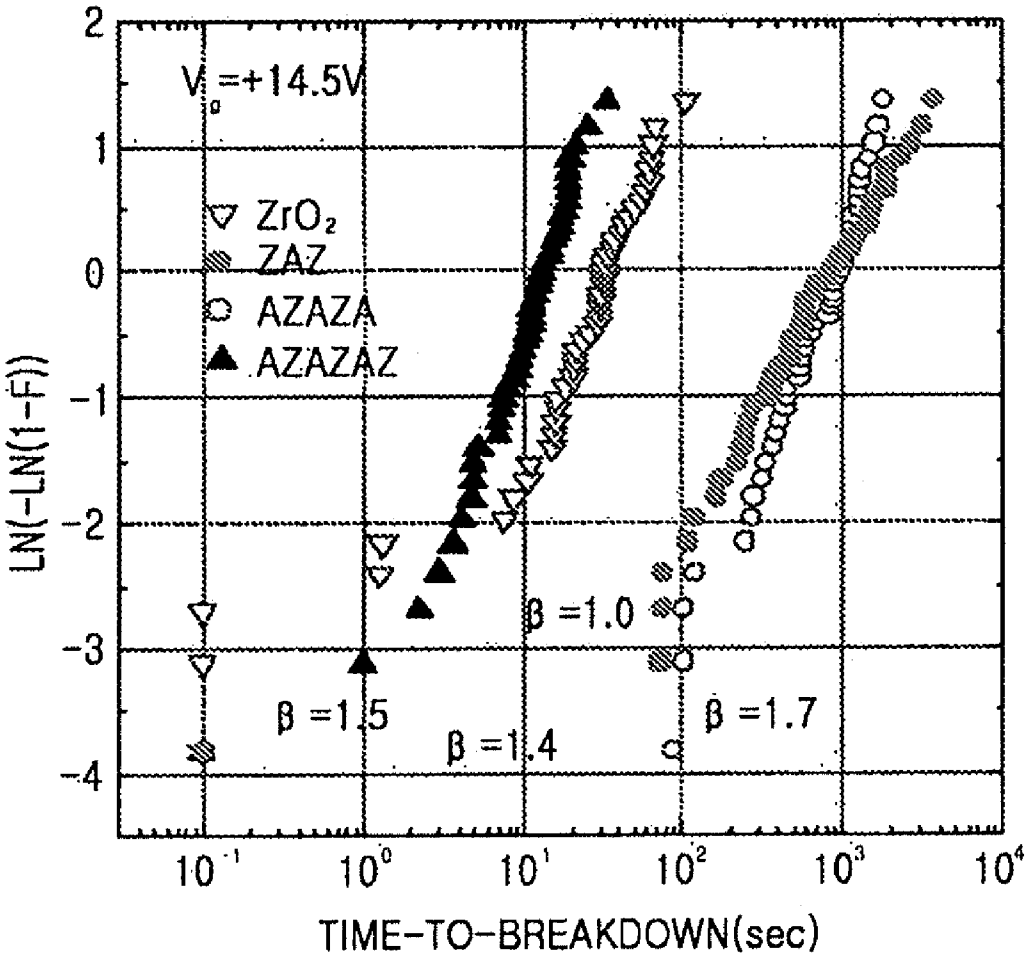
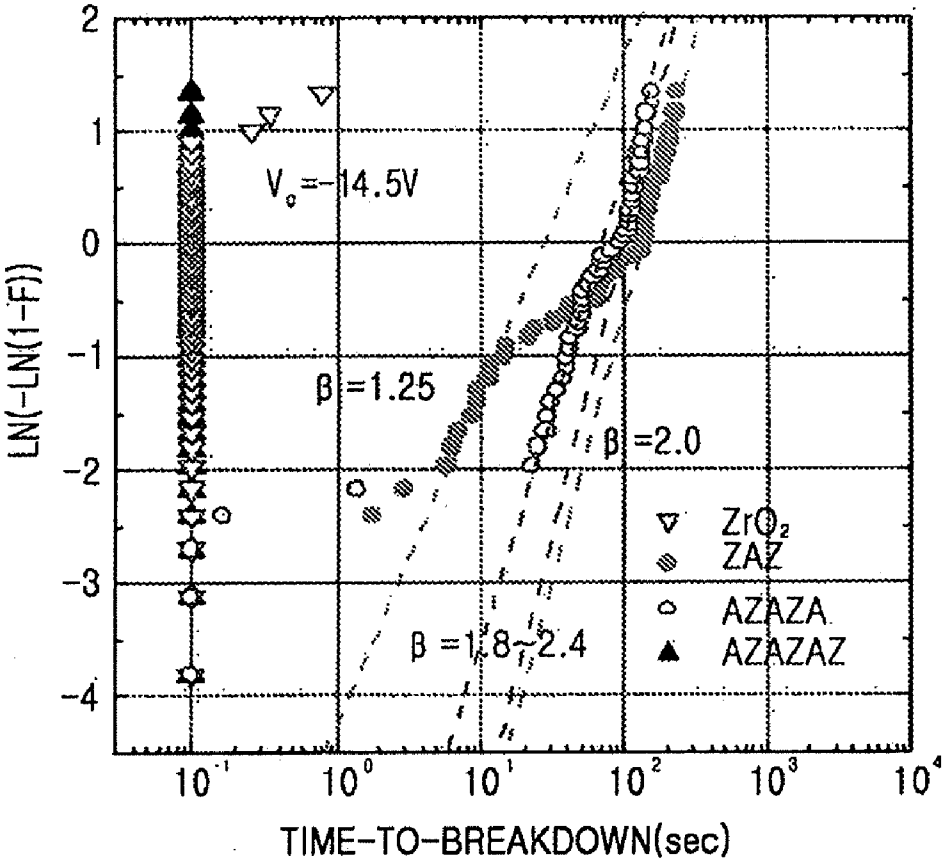

$V_g$ =+14.5V
$ZrO_2$
ZAZ
AZAZA
AZAZAZ
β =1.0
β =1.5
β =1.4
β =1.7
LN(-LN(1-F))
TIME-TO-BREAKDOWN(sec)
2
1
0
-1
-2
-3
-4
$10^{-1}$
$10^{0}$
$10^{1}$
$10^{2}$
$10^{3}$
$10^{4}$

FIG. 6B


LN(-LN(1-F))
TIME-TO-BREAKDOWN(sec)
$V_g$=-14.5V
β=1.25
β=2.0
β=1.8~2.4
$ZrO_2$
ZAZ
AZAZA
AZAZAZ

# FLASH MEMORY DEVICE WITH STACKED DIELECTRIC STRUCTURE INCLUDING ZIRCONIUM OXIDE AND METHOD FOR FABRICATING THE SAME

## CROSS-REFERENCES TO RELATED APPLICATIONS

**[0001]** The present application is a divisional of U.S. application Ser. No. 11/582,705, filed Oct. 17, 2006, which claims priority to Korean Application No. KR 2006-0036924, filed Apr. 24, 2006, which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

**[0002]** The present invention relates to a method for fabricating a semiconductor device; and more particularly, to a flash memory device with a dielectric layer having a high k-dielectric constant and a method for fabricating the same.

**[0003]** When using a conventional oxide-nitride-oxide (ONO) structure as a dielectric structure (i.e., an inter-poly oxide (IPO) layer or an inter-poly dielectric (IPD) layer) existing between a floating gate (FG) and a control gate (CG), a distance between devices decreases as the integration scale of semiconductor devices improves. Accordingly, it becomes difficult to perform a gap-filling process and thus, the devices are often hardly isolated.

**[0004]** Furthermore, as a size of the device has been reduced, a property of a capacitor for storing electric charges may be degraded. Accordingly, a high k-dielectric thin layer having a small thickness and a high k-dielectric constant is used as the IPO layer or the IPD layer.

**[0005]** Recently, a process of using a high k-dielectric thin layer with an OZO structure, formed by sequentially stacking an oxide layer, a zirconium oxide ($ZrO_2$) layer and an oxide layer has been suggested to overcome the aforementioned limitations.

**[0006]** FIG. **1** is a cross-sectional view illustrating a conventional flash memory device.

**[0007]** A tunnel oxide layer **12** is formed over a substrate **11**, and a floating gate **13** is formed over the tunnel oxide layer **12**. A dielectric structure **14** is formed over the floating gate **13**. The dielectric structure **14** is formed by sequentially stacking a first silicon oxide ($SiO_2$) layer **14**A, a zirconium oxide ($ZrO_2$) layer **14**B, and a second silicon oxide ($SiO_2$) layer **14**C. A control gate **15** is formed over the dielectric structure **14**.

**[0008]** However, in the case of using the $ZrO_2$ layer, the $ZrO_2$ layer may be crystallized at a predetermined thickness or greater while forming a thin layer. Accordingly, along a grain boundary, current is likely to leak or a defect may be generated. As a result, device reliability may be degraded.

## BRIEF SUMMARY OF THE INVENTION

**[0009]** The present invention provides a flash memory device using a zirconium oxide ($ZrO_2$) layer having a high k-dielectric constant as a dielectric layer, a low capacitive equivalent thickness (CET), a low leakage current level, and improved reliability, and a method for fabricating the same.

**[0010]** In accordance with one embodiment of the present invention, there is provided a dielectric structure disposed between a floating gate and a control gate of a flash memory device, including: a first dielectric layer; a third dielectric layer having a k-dielectric constant substantially the same as that of the first dielectric layer; and a second dielectric layer disposed between the first dielectric layer and the third dielectric layer, having a greater k-dielectric constant than that of the first and third dielectric layers and formed by alternately and repeatedly stacking a plurality of aluminum oxide ($Al_2O_3$) layers and a plurality of zirconium oxide ($ZrO_2$) layers.

**[0011]** In accordance with another embodiment of the present invention, there is provided a flash memory device, including: a substrate; a tunnel oxide layer formed over the substrate; a floating gate formed over the tunnel oxide layer; a first dielectric layer formed over the floating gate; a second dielectric layer formed by alternately and repeatedly stacking a plurality of $Al_2O_3$ layers and a plurality of $ZrO_2$ layers over the first dielectric layer and having a greater k-dielectric constant than that of the first dielectric layer; a third dielectric layer formed over the second dielectric layer and having substantially the same k-dielectric constant as that of the first dielectric layer; and a control gate formed over the third dielectric layer.

**[0012]** In accordance with a further embodiment of the present invention, there is provided a method for forming a dielectric structure disposed between a floating gate and a control gate of a flash memory device, including: forming a first dielectric layer; forming a second dielectric layer in a stack structure that has a greater k-dielectric constant than that of the first dielectric layer by alternately and repeatedly stacking a plurality of $Al_2O_3$ layers and a plurality of $ZrO_2$ layers over the first dielectric layer; and forming a third dielectric layer that has substantially the same k-dielectric constant as that of the first dielectric layer over the second dielectric layer.

**[0013]** In accordance with still another embodiment of the present invention, there is provided a method for fabricating a flash memory device, including: forming a tunnel oxide layer over a substrate; forming a floating gate over the tunnel oxide layer; forming a first dielectric layer over the floating gate; forming a second dielectric layer in a stack structure that has a greater k-dielectric constant than that of the first dielectric layer by alternately and repeatedly stacking a plurality of $Al_2O_3$ layers and a plurality of $ZrO_2$ layers over the first dielectric layer; forming a third dielectric layer that has substantially the same k-dielectric constant as that of the first dielectric layer over the second dielectric layer; and forming a control gate over the third dielectric layer.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]** The above features of the present invention will become better understood with respect to the following description of the exemplary embodiments given in conjunction with the accompanying drawings, in which:

**[0015]** FIG. **1** is a cross-sectional view illustrating a conventional flash memory device;

**[0016]** FIG. **2** is a cross-sectional view illustrating a dielectric structure of a flash memory device in accordance with an embodiment of the present invention;

**[0017]** FIG. **3**A is a graph of a capacitive equivalent thickness (CET) that varies depending on various stack structures;

**[0018]** FIG. **3**B is a graph of leakage current level that varies depending on various stack structure;

**[0019]** FIG. **4** is a simplified diagram illustrating an atomic layer deposition (ALD) method to form an $Al_2O_3/ZrO_2/Al_2O_3/ZrO_2/Al_2O_3$ structure in accordance with an embodiment of present invention;

**[0020]** FIG. **5** is a cross-sectional view illustrating a flash memory device using the dielectric structure shown in FIG. **2**; and

**[0021]** FIGS. **6**A and **6**B are Weibull plots illustrating time-to-breakdown (TBD) distributions in accordance with the embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

**[0022]** Hereinafter, detailed descriptions on certain embodiments of the present invention will be provided with reference to the accompanying drawings.

**[0023]** FIG. **2** is a cross-sectional view illustrating a dielectric structure of a flash memory device in accordance with an embodiment of the present invention.

**[0024]** The dielectric structure **100** of the flash memory device includes a first dielectric layer **101**; a third dielectric layer **103** having substantially the same k-dielectric constant as the first dielectric layer **101**; and a second dielectric layer **102** disposed between the first dielectric layer **101** and the third dielectric layer **103**. The second dielectric layer **102** has a greater k-dielectric constant than the first dielectric layer **101** and the third dielectric layer **103**, and is formed by alternately and repeatedly stacking an aluminum oxide ($Al_2O_3$) layer **102**A and a zirconium oxide ($ZrO_2$) layer **102**B. The dielectric structure **100** has a stack structure formed by sequentially stacking the first dielectric layer **101**, the second dielectric layer **102** and the third dielectric layer **103**. Particularly, these alternately and repeatedly stacked $Al_2O_3$ layer **102**A and the $ZrO_2$ layer **102**B will be denoted as "AZAZA structure".

**[0025]** The first dielectric layer **101** and the third dielectric layer **103** individually include a silicon oxide ($SiO_2$) layer, and the second dielectric layer **102** is a stacked AZAZA structure. Thus, the dielectric structure **100** becomes an OAZAZAO structure.

**[0026]** In more detail about the second dielectric layer **102**, the $Al_2O_3$ layer **102**A contacts with the first dielectric layer **101** and the third dielectric layer **103** as shown in the AZAZA structure to reduce silicon diffusion. Specifically, the $Al_2O_3$ layer **102**A can prevent silicon from the first dielectric layer **101** and from the third dielectric layer **103** from diffusing to the corresponding $ZrO_2$ layer **102**B by being interposed between the first dielectric layer **101** and the $ZrO_2$ layer **102**B and between the third dielectric layer and the $ZrO_2$ layer **102**B.

**[0027]** Accordingly, the OAZAZAO structure in this embodiment of the present invention has a stack structure which additionally includes the $Al_2O_3$ layers **102**A between the $SiO_2$ layers and the ZAZ structure. In one embodiment of the present invention, a k-dielectric constant of the $ZrO_2$ layer **102**B is not decreased due to the additionally formed $Al_2O_3$ layers **102**A.

**[0028]** Furthermore, for the number of stacked $Al_2O_3$ layers, the OAZAZAO structure includes two more $Al_2O_3$ layers than the ZAZ structure and thus, the $ZrO_2$ layer **102**B can have substantially the same k-dielectric constant as the ZAZ structure although the $ZrO_2$ layers **102**B are thinly formed. Accordingly, since the $ZrO_2$ layers **102**B can be thinly formed, the $ZrO_2$ layers **102**B is not likely to be crystallized while forming the $ZrO_2$ layers **102**B.

**[0029]** As shown in the OAZAZAO structure (or stacked structure), the $ZrO_2$ layer **102**B is stacked twice and the $Al_2O_3$ layer **102**A is stacked three times. It should be appreciated that stacking more of the $Al_2O_3$ layers could be undesirable. For instance, if the $Al_2O_3$ layer **102**A is stacked four times, the number of the $ZrO_2$ layers **102**B to be stacked is decreased to one. That is, if a proportion of the $ZrO_2$ layers **102**B is decreased (i.e., from two layers to one layer) in the stacked structure, a capacitive equivalent thickness (CET) and a leakage current level are increased. Accordingly, a desirable stack structure to obtain a low CET and a low leakage current level is the OAZAZAO structure.

**[0030]** FIG. **3**A is a graph of a capacitive equivalent thickness (CET) that varies depending on various stack structures and FIG. **3**B is a graph of leakage current level that varies depending on various stack structures. The stacked dielectric structures compared with each other in FIGS. **3**A and **3**B are a ZAZ structure, an AZAZA structure, an AZAZAZA structure and a $ZrO_2$ layer.

**[0031]** As shown in FIG. **3**A, the $ZrO_2$ layer has the lowest CET and the ZAZ structure has the highest CET. The AZAZA structure has a larger CET than the AZAZAZA structure but a lower CET than the ZAZ structure.

**[0032]** As shown in FIG. **3**B, the $ZrO_2$ layer has the highest leakage current, and the AZAZA structure has the lowest leakage current. For reference, the AZAZAZA structure has higher leakage current than the ZAZ structure.

**[0033]** From the results shown in FIGS. **3**A and **3**B, the AZAZA structure has a larger CET and a lower leakage current than the AZAZAZA structure and the ZAZ structure.

**[0034]** The second dielectric layer **102** with the AZAZA structure shown in FIG. **2** can be formed through an atomic layer deposition (ALD) method or a chemical vapor deposition (CVD) method.

**[0035]** Hereinafter, a deposition method of the AZAZA structure through the ALD method will be examined.

**[0036]** FIG. **4** is a diagram briefly illustrating an ALD method to form an AZAZA structure in accordance with an embodiment of the present invention.

**[0037]** The ALD method is generally performed by repeating a unit cycle until an atomic layer with a desirable thickness is obtained. The unit cycle includes supplying a source gas to a wafer loaded into a chamber, supplying a purge gas thereto, supplying a reaction gas thereto, and supplying a purge gas thereto.

**[0038]** In more detail of an $Al_2O_3$ layer deposition, an aluminum (Al) source gas is supplied to a chamber where a wafer is loaded and then, absorbed into a surface of the wafer. The Al source gas includes $Al(CH_3)_3$.

**[0039]** A purge gas is supplied into the chamber to purge out non-adsorbed parts of the Al source gas remaining inside the chamber. The purge gas includes an inert gas selected from a group consisting of argon (Ar), helium (He), nitrogen ($N_2$), or a combination thereof.

**[0040]** A reaction gas is supplied into the chamber. The reaction gas includes one selected from a group consisting of ozone ($O_3$), oxygen ($O_2$) plasma, and water ($H_2O$). A reaction between the Al source gas and the reaction gas is induced to deposit an $Al_2O_3$ layer. Accordingly, the $Al_2O_3$ layer is formed over the surface of the wafer in an atomic unit.

**[0041]** A purge gas is supplied into the chamber to purge out non-reacted parts of the reaction gas and byproducts. The purge gas includes an inert gas selected from a group consisting of Ar, He, $H_2$, or a combination thereof.

**[0042]** As described above, the $Al_2O_3$ layer with a desirable thickness can be deposited by repeating the unit cycle including supplying the Al source gas, supplying the purge gas,

supplying the reaction gas, and supply the purge gas. Theses sequential steps are denoted with reference letters $T_1$, $T_2$, $T_3$, and $T_4$ in FIG. **4**.

**[0043]** Depositing a $ZrO_2$ layer based on the ALD method will be examined hereinafter.

**[0044]** A zirconium (Zr) source gas is supplied to a chamber where a wafer is loaded and then, adsorbed into a surface of the wafer. The Zr source gas includes one selected from a group consisting of $Zr(O\text{-}tBu)_4$, $Zr[N(CH_3)_2]_4$, $Zr[N(C_2Hs)(CH_3)]_4$, $Zr[N(C_2H_5)_2]_4$, $Zr(tmhd)_4$, $Zr(OiC_3H_7)_3(tmhd)$ and $Zr(OtBu)_4$. The above listed materials are known as a precursor.

**[0045]** A purge gas is supplied into the chamber to purge out non-adsorbed parts of the Zr source gas remaining inside the chamber. The purge gas includes an inert gas selected from a group consisting of Ar, He, $N_2$, or a combination thereof.

**[0046]** A reaction gas is supplied into the chamber. The reaction gas includes one selected from a group consisting of $O_3$, $O_2$ plasma and $H_2O$. A reaction between the Zr source gas and the reaction gas is induced to deposit a $ZrO_2$ layer. Accordingly, the $ZrO_2$ layer is formed over the surface of the wafer in an atomic unit.

**[0047]** A purge gas is supplied into the chamber to purge out non-reacted parts of the reaction gas and byproducts. The purge gas includes an inert gas selected from a group consisting of Ar, He, $N_2$, or a combination thereof.

**[0048]** As described above, the $ZrO_2$ layer with a desirable thickness can be deposited by repeating the unit cycle including supplying the Zr source gas, supplying the purge gas, supplying the reaction gas, and supplying the purge gas. These sequential steps are denoted with reference letters $T_{11}$, $T_{12}$, $T_{13}$, and $T_{14}$ in FIG. **4**.

**[0049]** The $Al_2O_3$ layers and the $ZrO_2$ layers are alternately deposited through the ALD method to form the AZAZA structure. Meanwhile, the depositing of the $Al_2O_3$ layers and the $ZrO_2$ layers uses the same purge gas and reaction gas except for the source gas. Accordingly, the $Al_2O_3$ layers and the $ZrO_2$ layers can be alternately deposited only by changing the source gas at the same ALD chamber.

**[0050]** FIG. **5** is a cross-sectional view illustrating a flash memory device using the dielectric structure shown in FIG. **2**.

**[0051]** The flash memory device includes a substrate **201**, a tunnel oxide layer **202** over the substrate **201**, a floating gate FG **203**, a first dielectric layer **204** over the floating gate FG **203**, a second dielectric layer **205** having a k-dielectric constant greater than the first dielectric layer **204** formed over the first dielectric layer **204** by alternately and repeatedly stacking an $Al_2O_3$ layer **205**A and a $ZrO_2$ layer **205**B, a third dielectric layer **206** formed over the second dielectric layer **205** and having substantially the same k-dielectric constant as the first dielectric layer **204**, and a control gate CG **207** over the third dielectric layer **206**.

**[0052]** The tunnel oxide layer **202** includes a $SiO_2$ layer, and the floating gate FG **203** and the control gate CG **207** includes a polysilicon layer.

**[0053]** The first dielectric layer **204** and the third dielectric layer **206** are $SiO_2$ layers, and the second dielectric layer **205** has an AZAZA structure, which is a stack structure of the $Al_2O_3$ layer **205**A, the $ZrO_2$ layer **205**B, the $Al_2O_3$ layer **205**A, the $ZrO_2$ layer **205**B, and the $Al_2O_3$ layer **205**A.

**[0054]** A method for fabricating the flash memory device shown in FIG. **5** will be examined hereinafter.

**[0055]** The tunnel oxide layer **202** is formed over the substrate **201** completed with a well formation process and a channel ion-implantation process and other related processes. The tunnel oxide layer **202** is formed through one of a thermal oxidation method and a CVD method.

**[0056]** The floating gate **203** is formed over the tunnel oxide layer **202**. The floating gate **203** includes the polysilicon layer.

**[0057]** The first dielectric layer **204** is formed over the floating gate **203**. The first dielectric layer includes the $SiO_2$ layer formed through an ALD method or a CVD method.

**[0058]** A dielectric layer having a greater k-dielectric constant than the first dielectric layer **204** is formed over the first dielectric layer **204**. That is, an AZAZA structure is formed by alternately and repeatedly stacking the $Al_2O_3$ layer **205**A and the $ZrO_2$ layer **205**B over the first dielectric layer **204**. When the $Al_2O_3$ layer **205**A and the $ZrO_2$ layer **205**B are alternately and repeatedly stacked, the $Al_2O_3$ layer **205**A contacts with the first dielectric layer **204** or the third dielectric layer **206**. The third dielectric layer **206** is formed over the second dielectric layer **205**. The third dielectric layer **206** includes the $SiO_2$ layer as similar to the first dielectric layer **204**. Accordingly, the high k-dielectric second dielectric layer **205** formed between the low k-dielectric first dielectric layer **204** and the low k-dielectric third dielectric layer **206** gives rise to an OAZAZAO structure.

**[0059]** The control gate **207** is formed over the third dielectric layer **206**, and the control gate **207** includes the polysilicon layer.

**[0060]** The dielectric structure of the flash memory device between the floating gate **203** and the control gate **207** is a stack structure of the first dielectric layer **204**, the second dielectric layer **205**, and the third dielectric layer **206**, more particularly, of an OAZAZAO ($SiO_2/Al_2O_3/ZrO_2/Al_2O_3/ZrO_2/Al_2O_3/SiO_2$) structure. The OAZAZAO structure is formed with a thickness ranging from approximately 50 Å to approximately 200 Å.

**[0061]** Comparing the OAZAZAO dielectric structure with the OZAZO dielectric structure, the OAZAZAO dielectric structure can prevent silicon from diffusing to the $ZrO_2$ layer **205**B by interposing repeatedly the $Al_2O_3$ layer **205**A between the $ZrO_2$ layer **205**B before depositing the third electric layer including the $SiO_2$ layer. Accordingly, a ZrSiO layer cannot be formed, and a k-dielectric constant of the $ZrO_2$ layer cannot be reduced.

**[0062]** Furthermore, in an OZAO structure or an OZO structure, as impurities such as silicon diffuse into a grain boundary of the $ZrO_2$ layer **205**B, a leakage current is likely to increase and device reliability may be degraded. However, in the OAZAZAO structure, the above described limitations can be reduced by repeatedly interposing the $Al_2O_3$ layer **205**A between the $ZrO_2$ layers **205**B. Thus, the leakage current can be decreased and the device reliability can be improved.

**[0063]** FIGS. **6**A and **6**B are Weibull plots illustrating time-to-breakdown (TBD) distributions in accordance with an embodiment of the present invention. FIG. **6**A shows the TBD distribution when a positive polarity stress is exerted, and FIG. **6**B shows the TBD distribution when a negative polarity stress is exerted. Herein, the positive polarity stress voltage level is approximately +14.5 V and the negative polarity stress voltage level is approximately −14.5 V.

**[0064]** A ZAZ structure seems to exhibit a TBD distribution obtained when a bi-modal breakdown process is applied

under a stress voltage of approximately −14.5 V. The ZAZ structure seems to have small (with β=approximately 1.25) and large (with β=approximately 2.0) TBD distribution components together.

**[0065]** In more details about FIGS. **6**A and **6**B, the AZAZA dielectric structure has a much longer lifetime than other dielectric structures. Accordingly, comparing with other dielectric structures, reliability of the AZAZA dielectric structure can be improved.

**[0066]** According to this embodiment of the present invention, a dielectric structure of a flash memory device uses an OAZAZAO ($SiO_2/Al_2O_3/ZrO_2/Al_2O_3/ZrO_2/Al_2O_3/SiO_2$) structure and thus, it is possible to obtain the flash memory device having a low CET level and a low leakage current level.

**[0067]** Furthermore, impurities such as silicon cannot diffuse into a grain boundary of a $ZrO_2$ layer and thus, reliability can be improved.

**[0068]** While the present invention has been described with respect to certain embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.

What is claimed is:

**1**. A non-volatile memory device, comprising:
- a floating gate provide over a substrate;
- a control gate provided over the floating gate; and
- a dielectric structure provided between the floating gate and the control gate, the dielectric structure including:
  - a first dielectric layer;
  - a second dielectric layer formed over the first dielectric layer and having a k-dielectric constant greater than that of the first dielectric layer, the second dielectric layer including a plurality of aluminum oxide ($Al_2O_3$) layers and a plurality of zirconium oxide ($ZrO_2$) layers; and
  - a third dielectric layer formed over the second dielectric layer.

**2**. The device of claim **1**, wherein a first $Al_2O_3$ layer and a last $Al_2O_3$ layer contact the first dielectric layer and the third dielectric layer, respectively,
- wherein the third dielectric layer has a k-dielectric constant substantially the same as that of the first dielectric layer.

**3**. The device of claim **1**, wherein a first $Al_2O_3$ layer and a third $Al_2O_3$ layer contact the first dielectric layer and the third dielectric layer, respectively, and
- wherein the second dielectric layer comprises the first $Al_2O_3$ layer, a first $ZrO_2$ layer, a second $Al_2O_3$ layer, a second $ZrO_2$ layer, and the third $Al_2O_3$ layer.

**4**. The device of claim **3**, wherein the first dielectric layer and the third dielectric layer comprise a silicon oxide ($SiO_2$) layer.

**5**. The device of claim **4**, wherein a total thickness of the dielectric structure from the first dielectric layer to the third dielectric layer ranges from approximately 50 Å to approximately 200 Å.

**6**. A flash memory device, comprising:
- a substrate;
- a tunnel oxide layer formed over the substrate;
- a floating gate formed over the tunnel oxide layer;
- a first dielectric layer formed over the floating gate;
- a second dielectric layer over the first dielectric layer and formed by alternately stacking a aluminum oxide ($Al_2O_3$) layer and a zirconium oxide ($ZrO_2$) layer, so that the second dielectric layer has at least five different layers, the second dielectric layer having a greater k-dielectric constant than that of the first dielectric layer;
- a third dielectric layer formed over the second dielectric layer; and
- a control gate formed over the third dielectric layer.

**7**. The flash memory device of claim **6**, wherein the $Al_2O_3$ layers and the $ZrO_2$ layers of the second dielectric layer are stacked such that a first $Al_2O_3$ layer and a third $Al_2O_3$ layer contact the first dielectric layer and with the third dielectric layer, respectively, and
- wherein the third dielectric layer having a k-dielectric constant substantially the same as that of the first dielectric layer.

**8**. The flash memory device of claim **6**, wherein the $Al_2O_3$ layers and the $ZrO_2$ layers of the second dielectric layer are stacked such that a first $Al_2O_3$ layer and a last $Al_2O_3$ layer contact the first dielectric layer and with the third dielectric layer, respectively,
- wherein the third dielectric layer having a k-dielectric constant substantially the same as that of the first dielectric layer, and
- wherein the second dielectric layer comprises the first $Al_2O_3$ layer, a first $ZrO_2$ layer, a second $Al_2O_3$ layer, a second $ZrO_2$ layer, and the last $Al_2O_3$ layer.

**9**. The flash memory device of claim **8**, wherein the first dielectric layer and the third dielectric layer comprise a $SiO_2$ layer.

**10**. The flash memory device of claim **9**, wherein a total thickness of the first dielectric layer, the second dielectric layer, and the third dielectric layer ranges from approximately 50 Å to approximately 200 Å.

* * * * *