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CA 2637343 A1 2010/01/29

(21) 2 637 343

(12) DEMANDE DE BREVET CANADIEN
CANADIAN PATENT APPLICATION

(13) A1

(22) Date de dépôt/Filing Date: 2008/07/29

(41) Mise à la disp. pub./Open to Public Insp.: 2010/01/29

(51) Cl.Int./Int.Cl. *G09G 3/20* (2006.01),
G09G 3/32 (2006.01), *G09G 3/36* (2006.01)

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(54) Titre : AMELIORATION DE PILOTE DE SOURCE D'AFFICHAGE
(54) Title: IMPROVING THE DISPLAY SOURCE DRIVER

(57) Abrégé/Abstract:
Disclosed is a technique to develop a low cost driver for display applications

ABSTRACT

Disclosed is a technique to develop a low cost driver for display applications

FIELD OF THE INVENTION

The present invention generally relates to drive a display such as light modulating (e.g. LCD) and light emitting (e.g. OLED) displays.

SUMMARY OF INVENTION

The disclosed technique reduces the driver die area by sharing and putting some parts of the driver on the panel.

ADVANTAGES

The new techniques can reduce the die area, and thus the cost, without sacrificing the driver performance.

FIG. 1 (a, b): shows the gate driver muxing.
FIG. 2 (a, b): shows another method of gate driver muxing.
FIG. 3: (prior art) shows a method for muxing the multiple gammas in a source driver.
FIG. 4: shows a method for muxing the multiple gammas and dividing the DAC to NMOS and PMOS DAC.
FIG. 5: shows the method of FIG 4 for quad RGBW pixel structure.
FIG. 6: shows the method of FIG 4 using external gamma buffers.
FIG. 7: shows the method of FIG 4 using internal configurable gammas for a divided DAC.
FIG. 8: shows the prior art for muxing the data values.
FIG. 9: shows a muxing method for data values using shift register.
FIG. 10: shows a method of using segmented decoder for implementing high voltage DAC using low voltage process.

To reduce the number of gate driver output, one can multiplex ("mux" or "muxing") the output signals in the driver and de-multiplex ("de-mux" or "de-muxing") the same signals on the panel side. **FIG. 1 (a)** highlights a method of muxing the gate driver outputs based on the frequency reduction. Here, an individual gate output is active for **M** rows. On the panel, the activated gate driver output is assigned to each individual row in sequence using the structure presented in **FIG. 1(b).** As a result, the number of outputs and address cells is reduced by a factor of **M**. However, the signals controlling the de-muxing on the panel should work at the normal gate frequency. This can impose a limit on higher resolution and larger area displays.

FIG. 2 (a) shows another method of gate driver muxing in which the operation frequency of the de-muxing control signals is reduced. In the structure demonstrated in **FIG. 2(b)**, real physical mux is used at the gate driver side. As a result, the number of address cells remains the same while the output number is reduced. The number of row in each set can be increased for further reduction in output of the gate driver and the frequency of the control signals. To reduce the number of address cells, a loop structure is used as highlighted in **FIG.2(c)**. Here, the address loops within a set of address cells for the number of muxed addresses. Then the controller passes the address token to the next set of address cells. This can be implemented in both decoder and shift register structure. In decoder, eliminating the less significant bits in the address will generate the loop inherently, whereas, a physical loop is required for the shift register structure.

Most light emitting displays require different gammas for different sub-pixels. This requires different decoders for different outputs even when muxing the outputs. **FIG. 3** shows a prior art method for muxing the multiple gammas in a source driver to share the DAC decoder, keeping it at just one instead of several. The output is de-muxed at the panel side and goes to different sub-pixels.

However, the output range of the voltage required for the light emitting displays is high and so the source driver should be a rail-to-rail. Currently, this results in using CMOS decoders for the DAC which leads to a larger area source driver. Here, **FIG. 4:** shows a method for muxing the multiple gammas and dividing the DAC into separate NMOS and PMOS DAC. For low voltage level of the gamma we use a NMOS decoder and for the high gamma voltages we use a PMOS decoder. The last stage is a CMOS mux. To accommodate different gammas for different pixel architectures and characteristics, the middle part of the gamma is shared between both PMOS and NMOS. Also, based on the gamma information stored into the register (indicating the flipping point to different decoders) and the gray scale value a programmable decoder decides which part of the DAC sends the data to the output buffer.

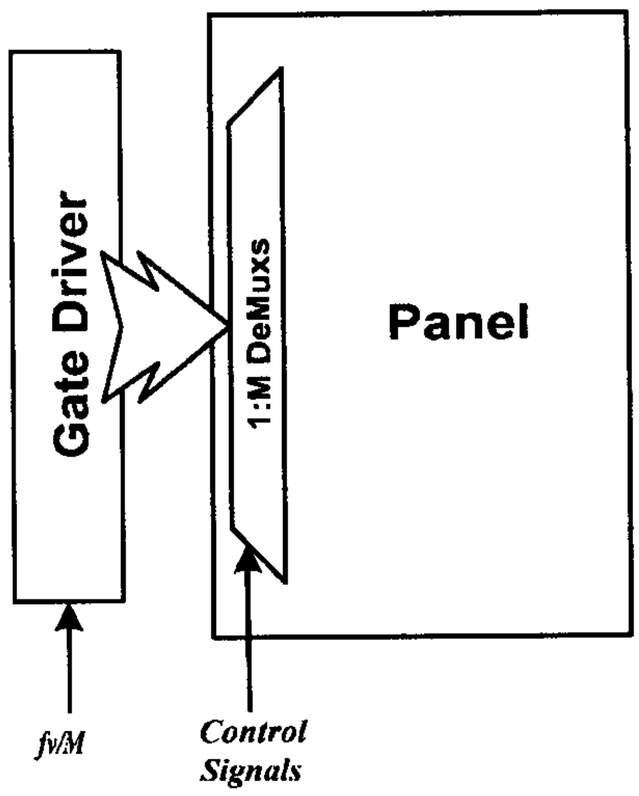
FIG. 5: shows the method of **FIG 4** for quad RGBW pixel structure. Here, the sub pixels are divided in two rows and two columns. Therefore, the source driver provides date for two sub-pixels at a time.

FIG. 6: shows the method of **FIG 4** using external gamma buffers. Here an external multiplexer is used to mux the gamma voltages. As a result, the number of input required for the gamma is reduced as well.

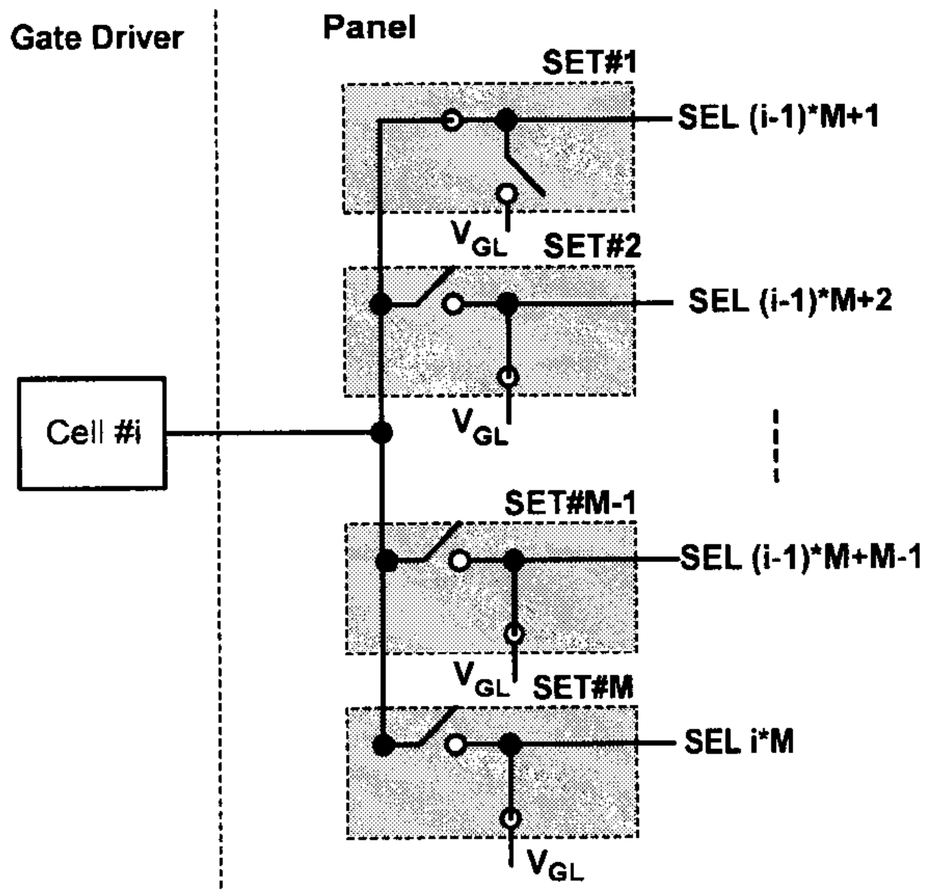
For small displays, the gamma is internally programmable. The data for gamma is stored in internal registers. To reduce the number of gamma resistors, DAC resistive ladders, and DAC decoder, the gamma registers are muxed. For programming each color, the corresponding gamma color is assigned to the gamma block (see **FIG. 7**).

To develop muxing in the source driver, the data for each color should be muxed as well. **FIG. 8** shows one of the prior arts for muxing the data values. To further reduce the area, one can replace the latch registers with shift registers using the new method discussed in **FIG. 9**. After the first color is programmed, the latch data is shifted by the number of required bits, so that the second data is stored in the latch connected to the DAC. This can happen for other colors as well until all the colors are programmed. This implementation results in a simpler routing and smaller die area.

Another issue, resulting in large die area, is using high voltage fabrication process for developing DAC decoders. However, as shown in **FIG. 10**, the DAC decoder can be segmented, and each segment operate at low voltage. To do so, each segment needs to be in its own well so that the body bias can be adjusted accordingly. Now, the decoder can be implemented in low voltage process, leading to smaller die area (over three times saving).


Gate Driver
1:M DeMuxs
Panel
fv/M
Control Signals

(a)


Gate Driver
Panel
SET#1
SEL (i-1)*M+1
VGL
SET#2
SEL (i-1)*M+2
Cell #i
VGL
SET#M-1
SEL (i-1)*M+M-1
VGL
SET#M
SEL i*M
VGL

(b)

FIG 1

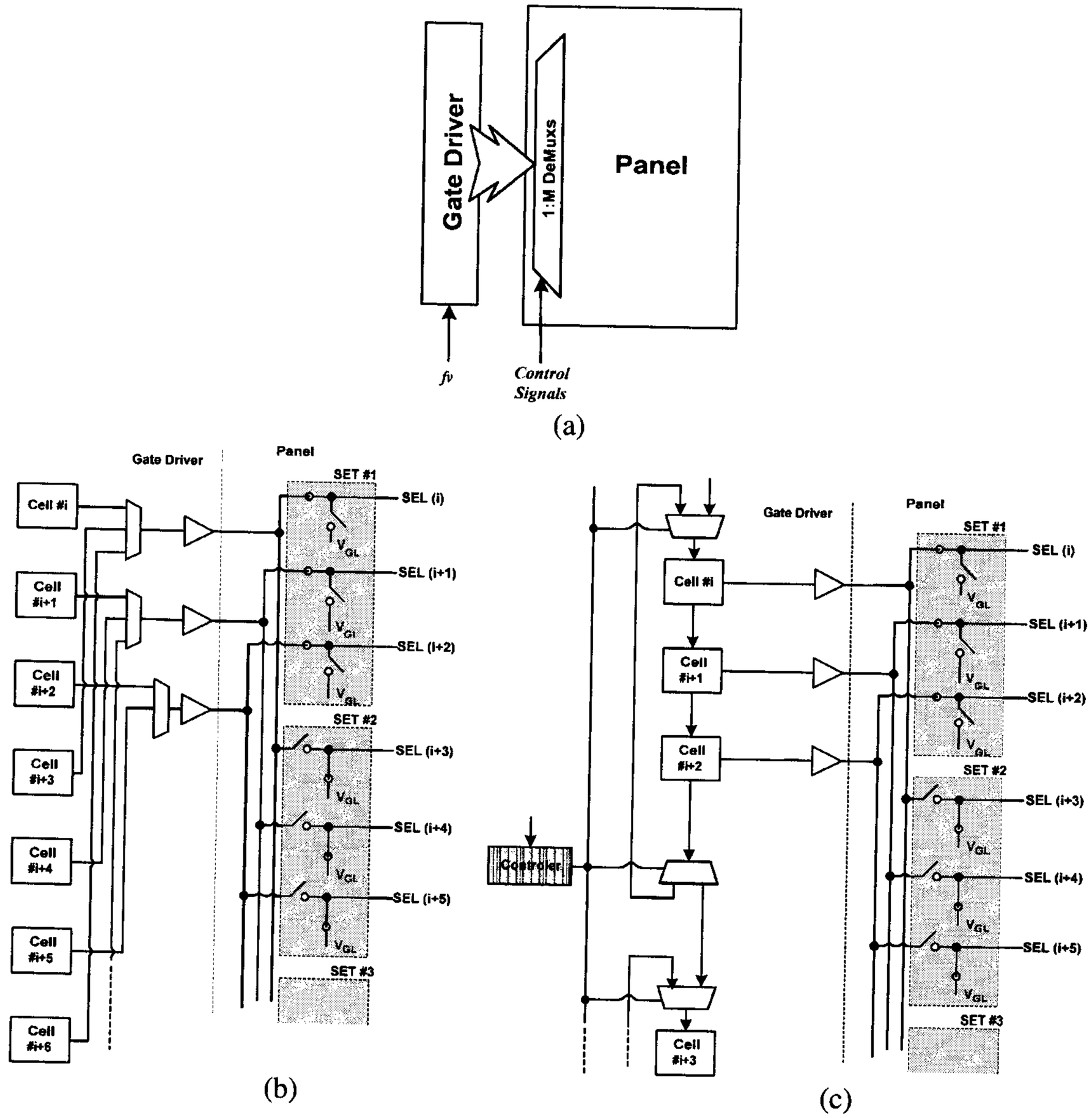

Gate Driver
1:M DeMuxs
Panel
fv
Control Signals
(a)
Gate Driver
Panel
Cell #i
Cell #i+1
Cell #i+2
Cell #i+3
Cell #i+4
Cell #i+5
Cell #i+6
SET #1
SET #2
SET #3
SEL (i)
SEL (i+1)
SEL (i+2)
SEL (i+3)
SEL (i+4)
SEL (i+5)
V_{GL}
(b)
Controller
Gate Driver
Panel
Cell #i
Cell #i+1
Cell #i+2
Cell #i+3
SET #1
SET #2
SET #3
SEL (i)
SEL (i+1)
SEL (i+2)
SEL (i+3)
SEL (i+4)
SEL (i+5)
V_{GL}
(c)

FIG 2

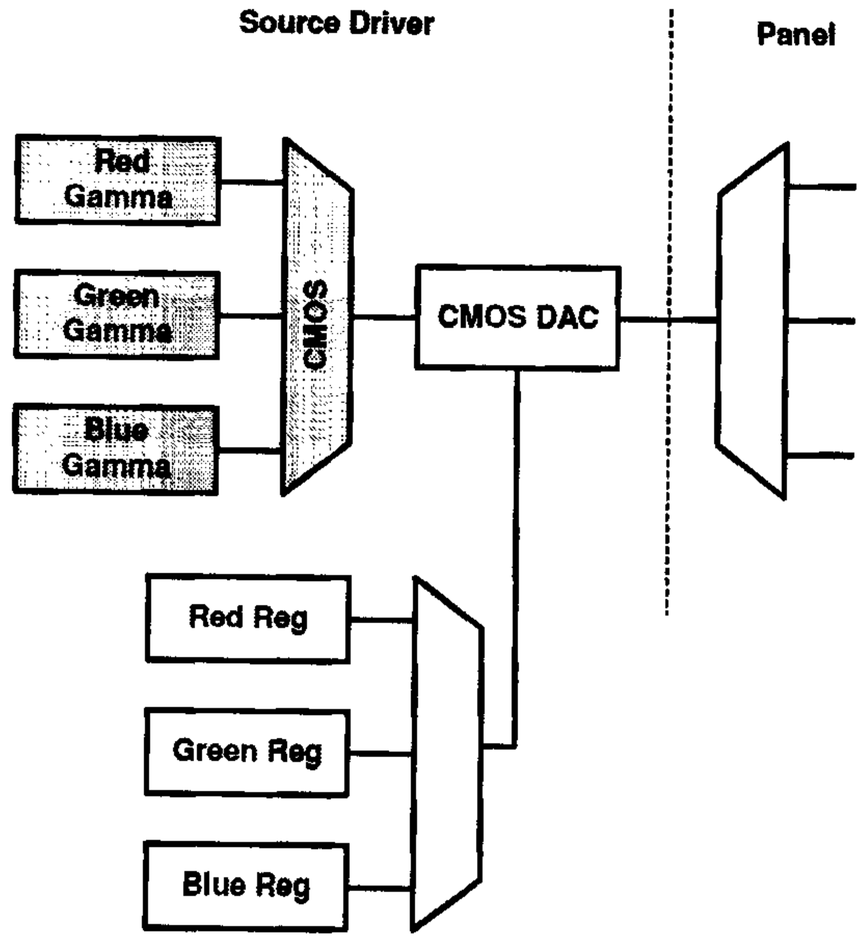


FIG 3: prior art

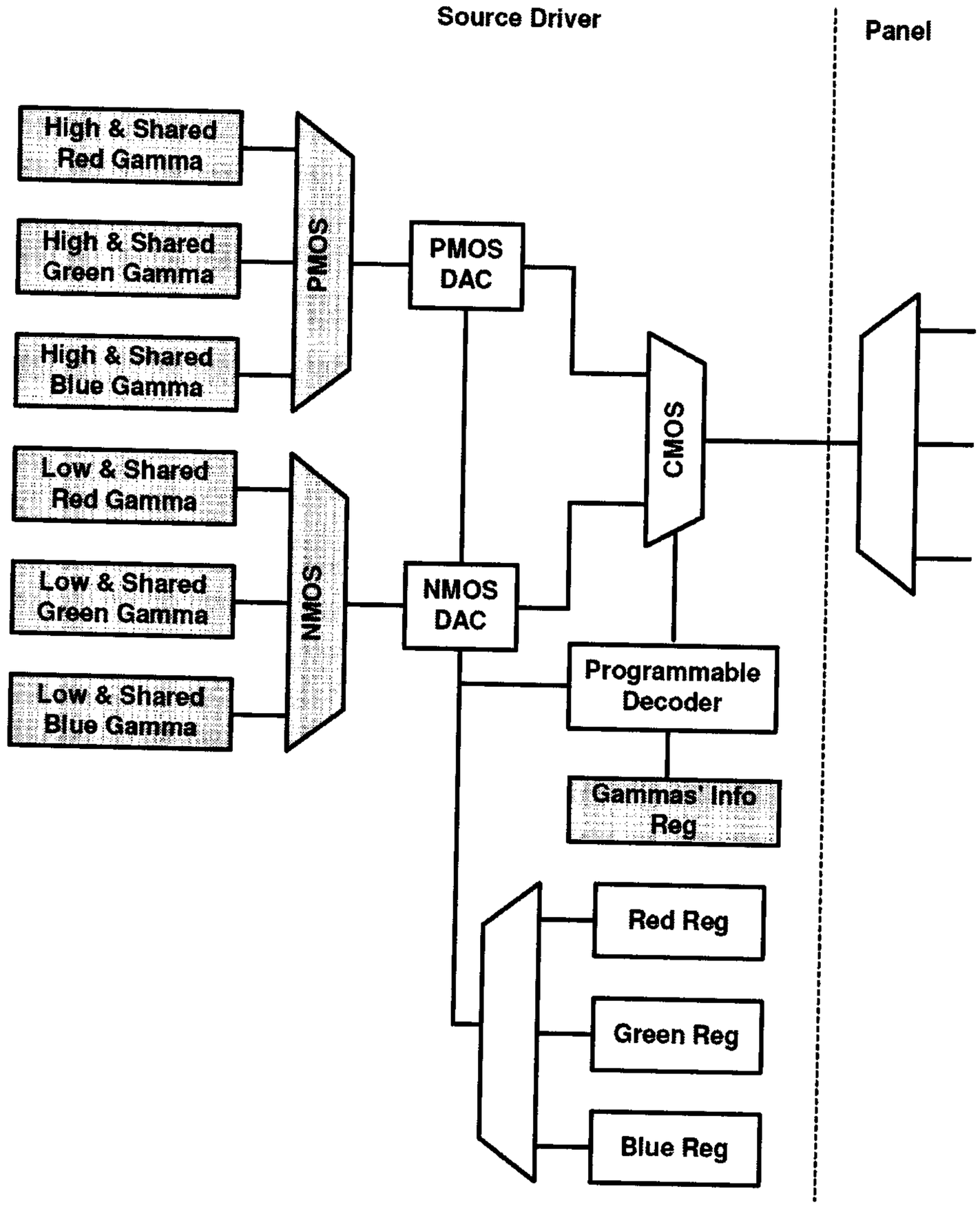

Source Driver
Panel
High & Shared Red Gamma
High & Shared Green Gamma
High & Shared Blue Gamma
PMOS
PMOS DAC
CMOS
Low & Shared Red Gamma
Low & Shared Green Gamma
Low & Shared Blue Gamma
NMOS
NMOS DAC
Programmable Decoder
Gammas' Info Reg
Red Reg
Green Reg
Blue Reg

FIG 4

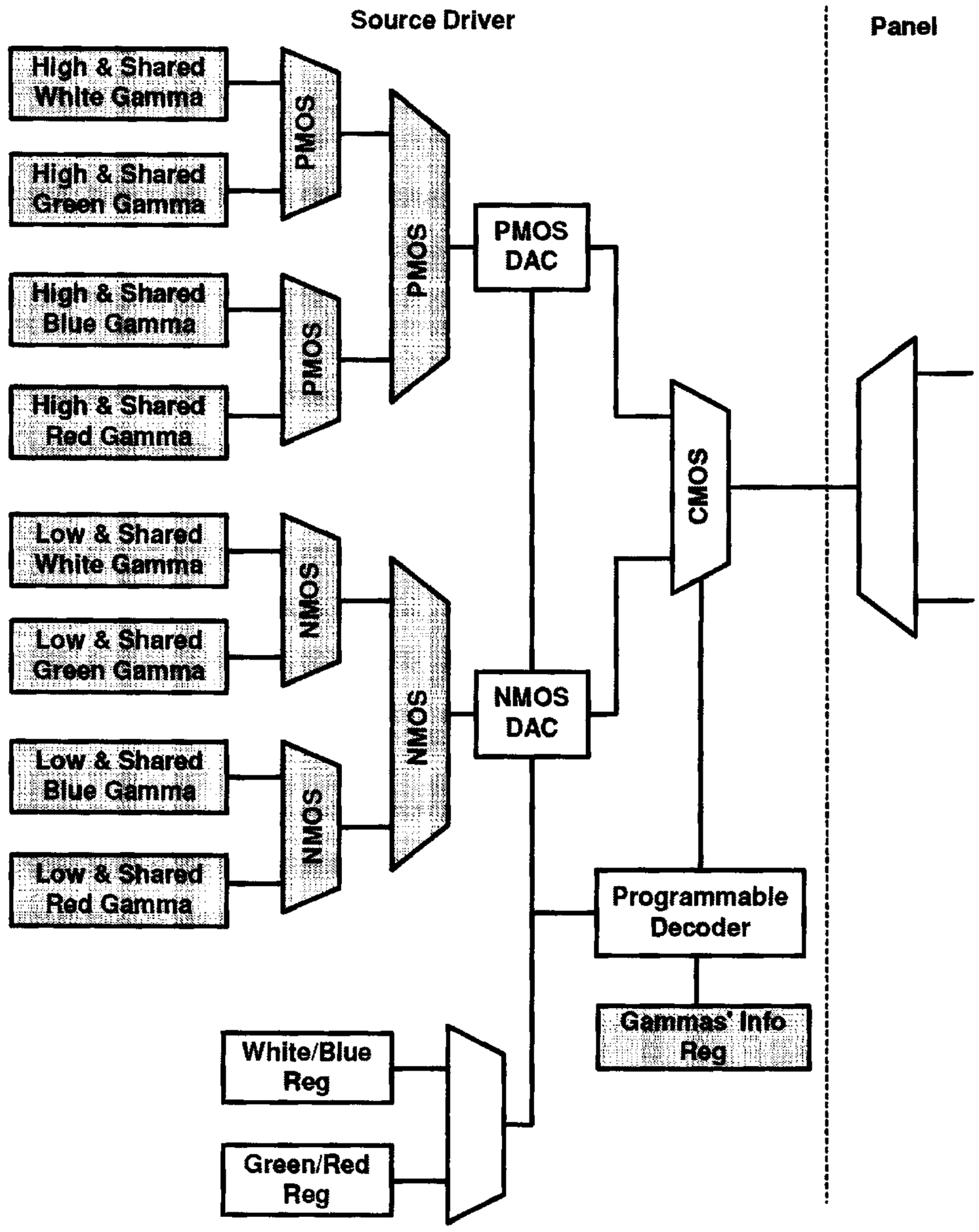

Source Driver
Panel
High & Shared White Gamma
High & Shared Green Gamma
High & Shared Blue Gamma
High & Shared Red Gamma
Low & Shared White Gamma
Low & Shared Green Gamma
Low & Shared Blue Gamma
Low & Shared Red Gamma
PMOS
PMOS
PMOS
NMOS
NMOS
NMOS
PMOS DAC
NMOS DAC
CMOS
Programmable Decoder
Gammas' Info Reg
White/Blue Reg
Green/Red Reg

FIG 5

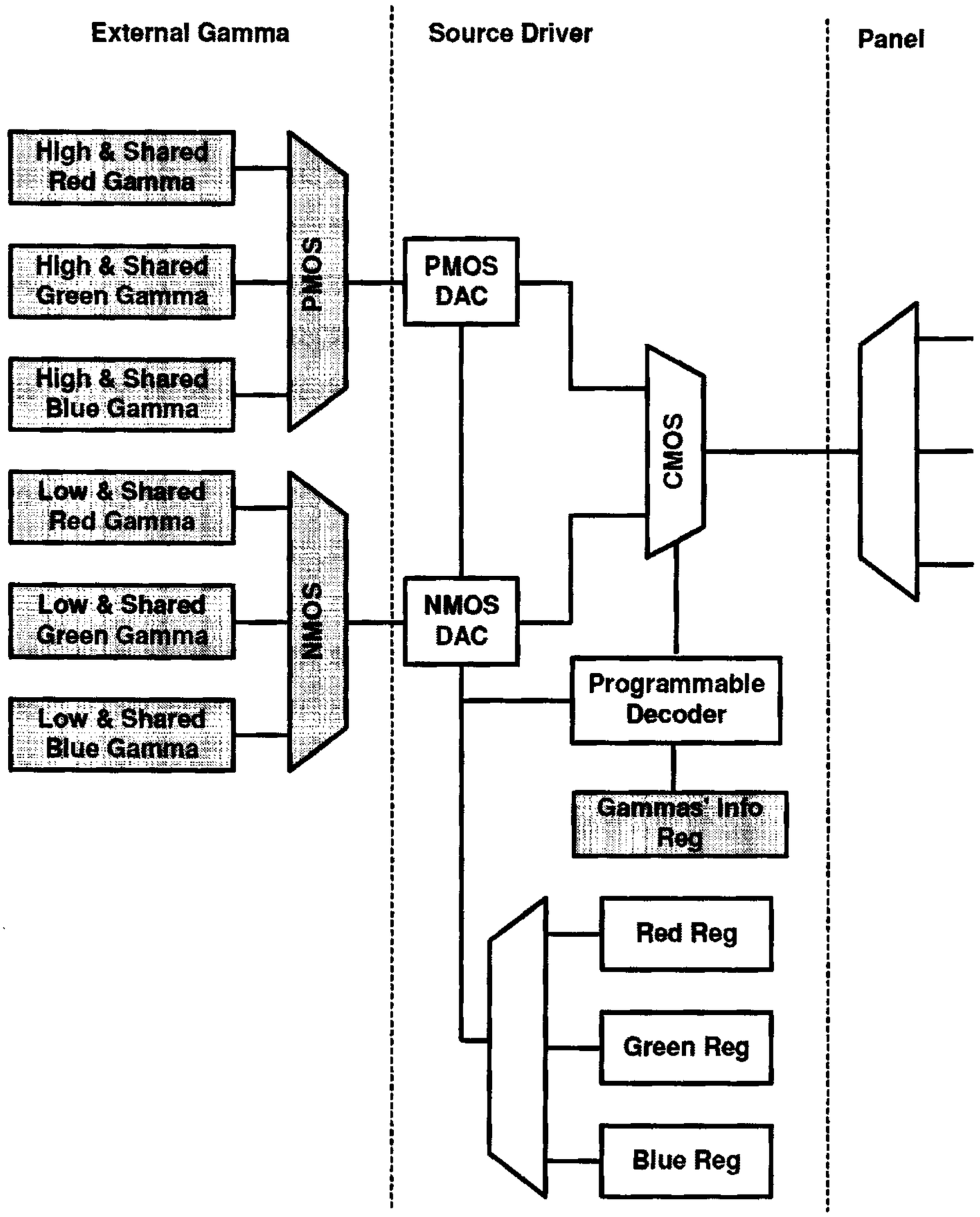

External Gamma
Source Driver
Panel
High & Shared Red Gamma
High & Shared Green Gamma
High & Shared Blue Gamma
Low & Shared Red Gamma
Low & Shared Green Gamma
Low & Shared Blue Gamma
PMOS
NMOS
PMOS DAC
NMOS DAC
CMOS
Programmable Decoder
Gammas' Info Reg
Red Reg
Green Reg
Blue Reg

FIG 6

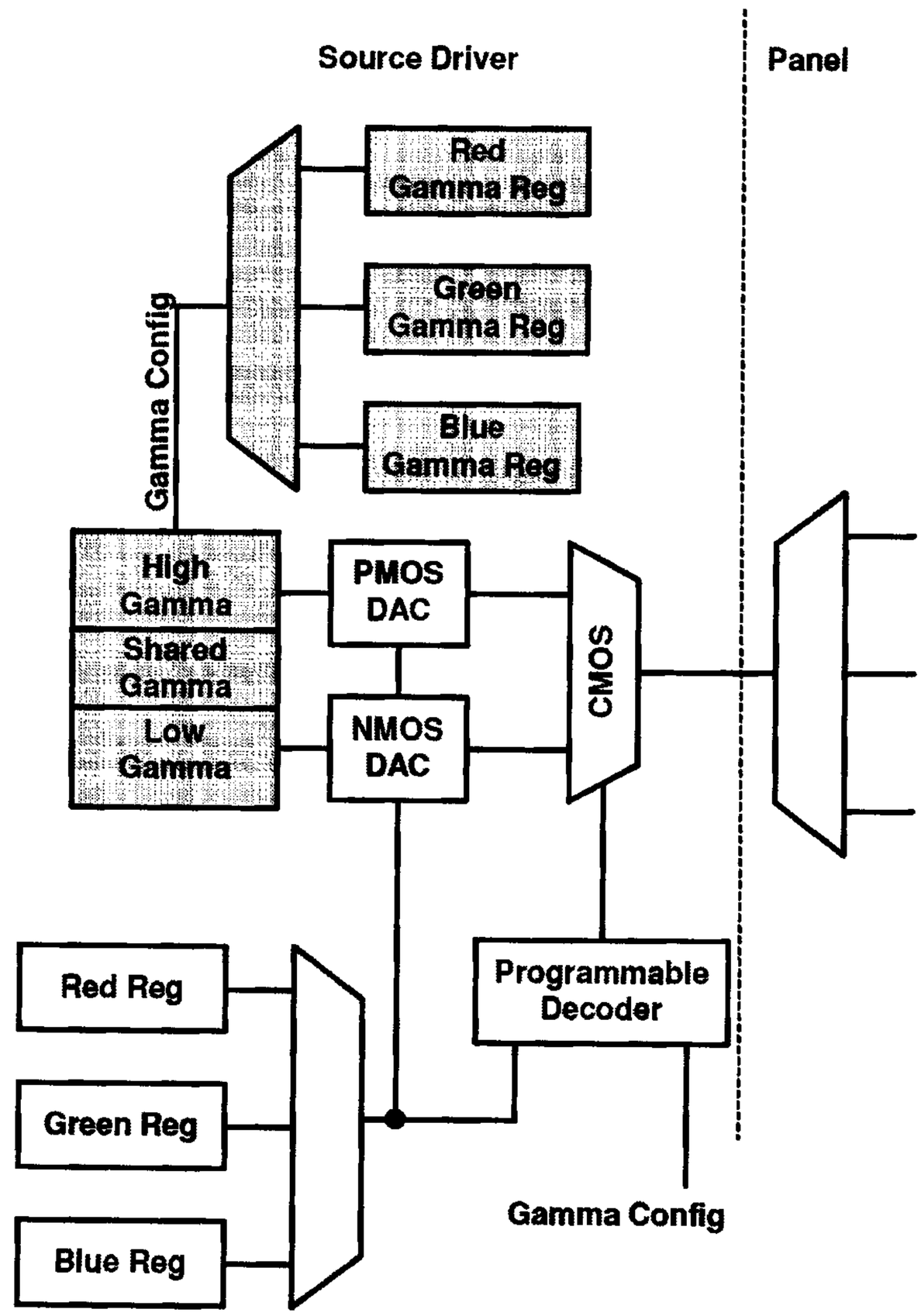

Source Driver
Panel
Red Gamma Reg
Green Gamma Reg
Blue Gamma Reg
Gamma Config
High Gamma
Shared Gamma
Low Gamma
PMOS DAC
NMOS DAC
CMOS
Red Reg
Green Reg
Blue Reg
Programmable Decoder
Gamma Config

FIG 7

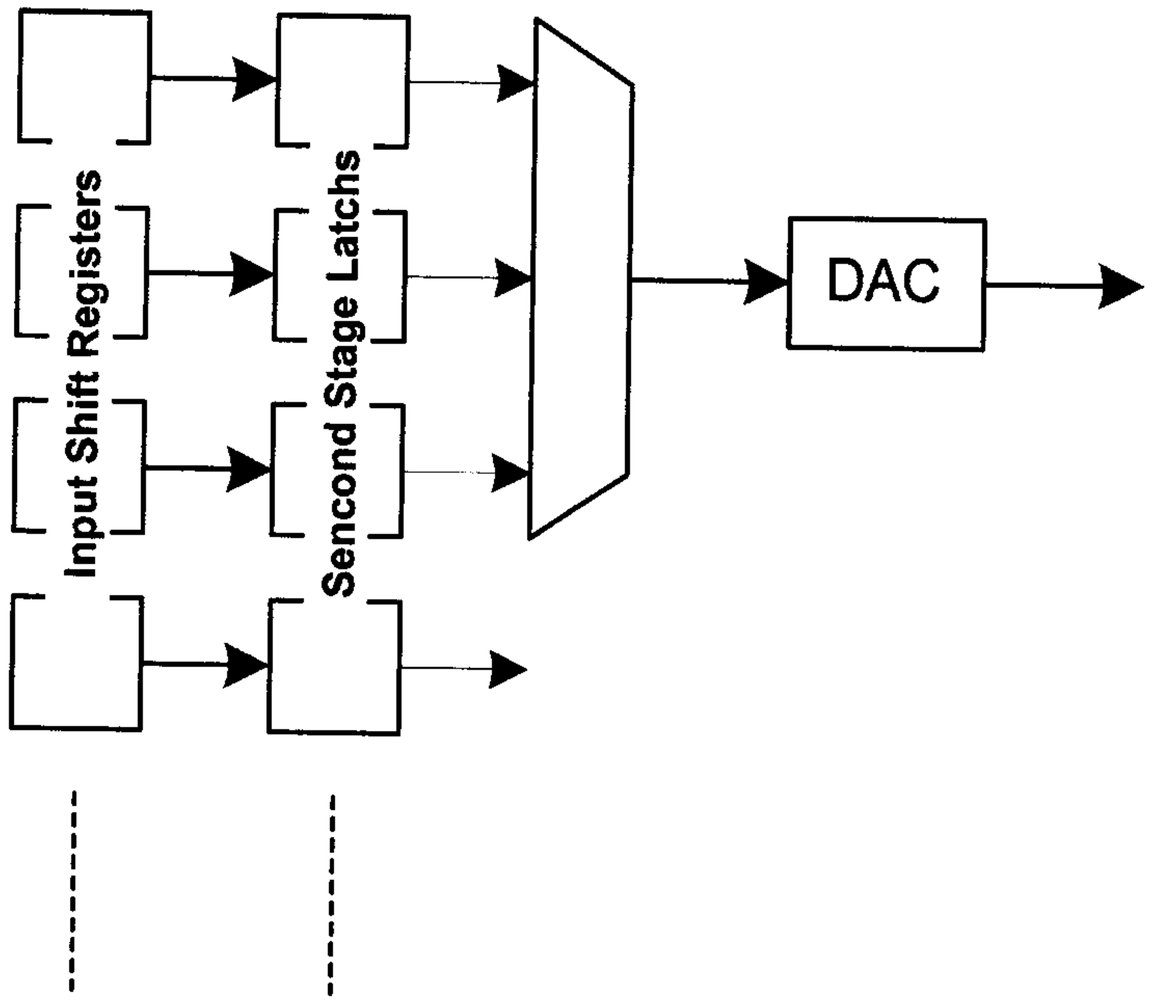


FIG 8

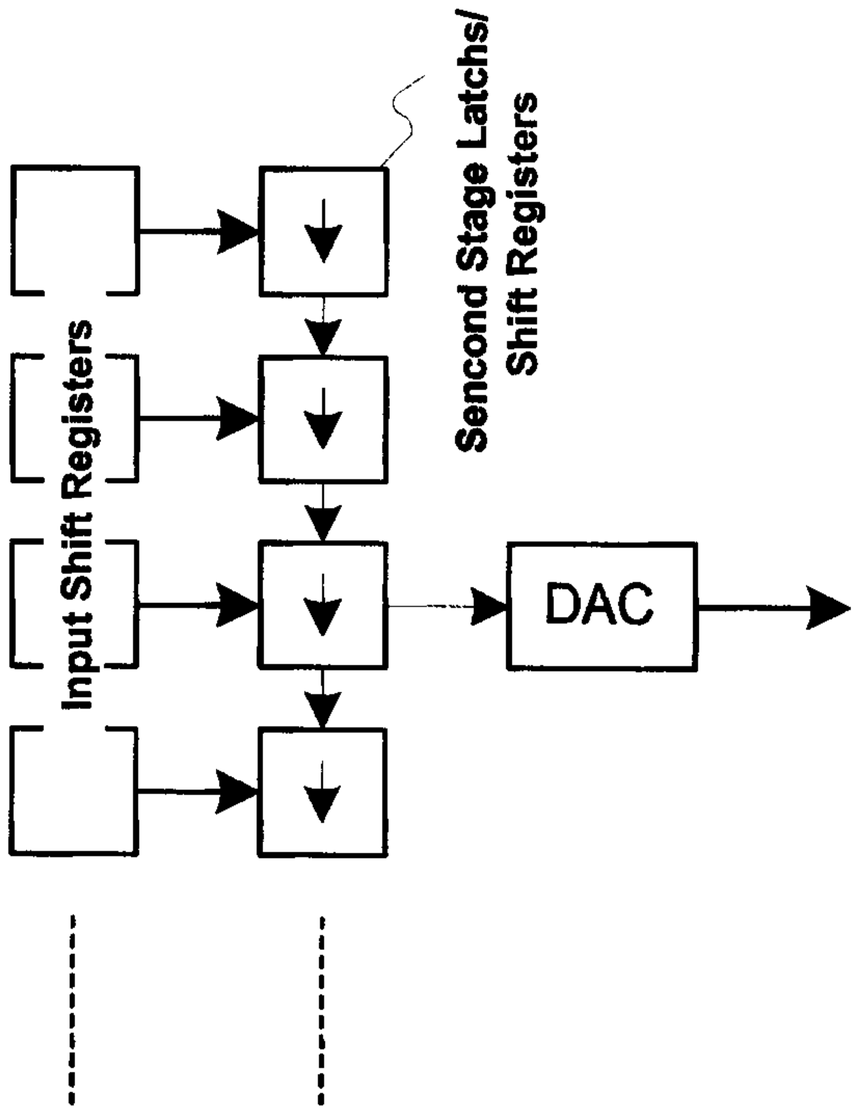

Sencond Stage Latchs/
Shift Registers
Input Shift Registers
DAC

FIG 9

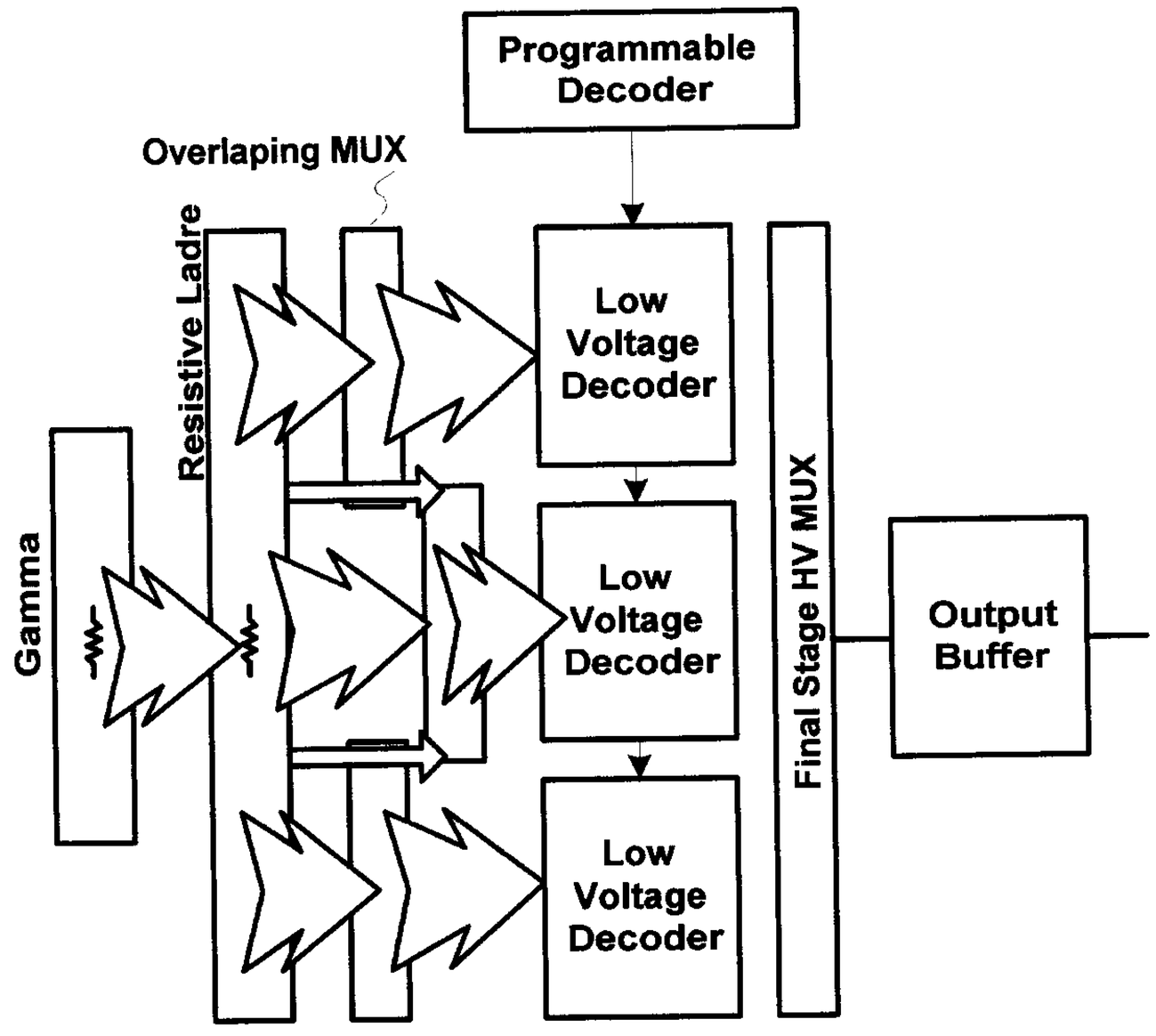

Programmable Decoder
Overlaping MUX
Resistive Ladre
Gamma
Low Voltage Decoder
Low Voltage Decoder
Low Voltage Decoder
Final Stage HV MUX
Output Buffer

FIG 10