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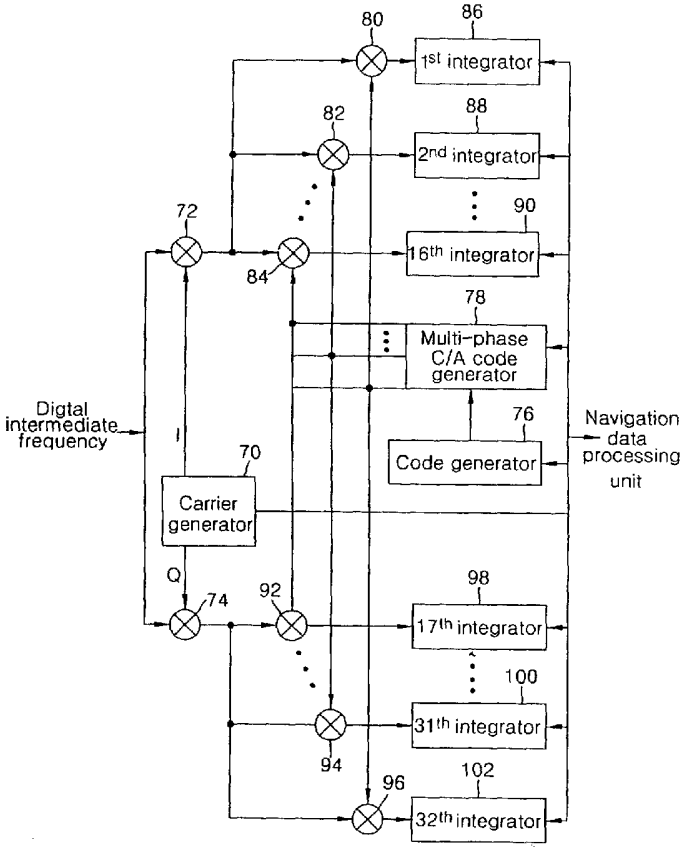
[Continued on next page]

(54) Title: POWER MANAGING APPARATUS FOR RECEIVING OF GLOBAL POSITIONING SYSTEM



(57) Abstract: The present invention relates to a power managing apparatus for used in GPS receiver, capable of reducing power consumption. There is provided a power managing apparatus for preventing unnecessary power consumption of a GPS receiver by fast receiving signals from the satellites through estimating power break time. The power break time can be estimated by using a correction function for real time clock and simultaneous search of a plurality of code phase correspondent to GPS signal.

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POWER MANAGING APPARATUS FOR RECEIVING OF GLOBAL POSITIONING SYSTEM

Technical Fleld

The present invention relates to a power managing apparatus for a receiver of Global Positioning System (hereinafter 'GPS receiver'), and more particularly to a power managing apparatus being capable of reducing a power consumption of the GPS receiver.

Background Art

Fig. 1 is a block diagram of a conventional GPS receiver, wherein a digital signal processor (hereinafter 'DSP') unit 12, provided with digital signals of intermediate frequency from an intermediate frequency (hereinafter 'IF') unit 10, processes the digital signals for use in processing a navigation data and provides processed digital signals to a navigation data processing unit 18. The DSP unit 12 includes a correlator 14 and a real time clock (hereinafter 'RTC') unit 16.

The conventional GPS receiver will be described in detail with reference to Fig. 2.

Fig. 2 is a block diagram illustrating an example of

the correlator 14 shown in Fig. 1. The correlator 14 comprises a carrier numerically controlled oscillator (hereinafter 'carrier NCO') 22, a first carrier mixer 24, a second carrier mixer 26, a code numerically controlled oscillator (hereinafter 'code NCO') 28, a C/A code generator 30, a first to a sixth code mixers 32, 34, 36, 44, 46, 48, and a first to a sixth integrators 38, 40, 42, 50, 52, 54.

In Fig. 1 and Fig. 2, the IF unit 10 converts radio frequency signals received from satellites into IF signals, and provides the IF signals for the correlator 14 in the DSP unit 12.

The carrier NCO 22 generates sinusoidal waves for use in eliminating carrier waves received from satellite signals. In detail, the frequency of carrier wave provided from the navigation data processing unit 18 is inputted. Then, sine signals (I) and cosine signals (Q) are generated and provided for the first carrier mixer 24 and the second carrier mixer 26, respectively.

The first carrier mixer 24 multiplies the sine signals (I) provided from the carrier NCO 24 by the digital signals of IF, and provides multiplied signals for the first, the second and the third code mixer 32, 34 and 36, respectively.

The code NCO 28 generates a reference frequency for use in generating a pseudo random noise (hereinafter 'PRN') code of GPS satellites, and provides the reference frequency for the C/A code generator 30.

The C/A code generator 30 generates the PRN codes of the GPS satellites by using the reference frequency provided from the code generator 28. In detail, the C/A code generator generates an early code, a prompt code and a late code, and provides the early code, the prompt code and the late code for the first, the second and the third code mixers 32, 34 and 36, respectively.

The first code mixer 32 multiplies the early code received from the C/A code mixer 30 by output signals from the first carrier mixer 24, and provides multiplied signals to the first integrator 38. The first integrator 38 integrates an output of the first code mixer 32 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing unit 18. The C/A code is the PRN code of the GPS satellite.

The second code mixer 34 multiplies the prompt code received from the C/A code mixer 30 by output signals from the first carrier mixer 24, and provides multiplied signals to the second integrator 40. The second integrator 40 integrates an output of the second code mixer 34 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing unit 18.

The third code mixer 36 multiplies the late code received from the C/A code mixer 30 by output signals from the first carrier mixer 24, and provides multiplied signals

to the third integrator 42. The third integrator 42 integrates an output of the third code mixer 36 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing unit 18.

Similarly, each of the fourth, fifth and sixth code mixer 44, 46, 48 multiplies an early code, a prompt code and a late code received from the C/A code mixer 30 by output signals of the second carrier mixer 26, and provides multiplied signals to the fourth, the fifth and the sixth integrator 50, 52 and 54 respectively. Each of the fourth, the fifth and the sixth integrator integrates an output of the fourth, the fifth and the sixth code mixer 44, 46 and 48 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing unit 18, respectively.

According to the above-described prior art, however, the GPS receiver continuously consumes power even after acquiring a required data, and thus, the GPS receiver exacts unnecessarily high power consumption.

Disclosure of Invention

An object of the present invention is to provide a power managing apparatus for the GPS receiver for preventing unnecessary power consumption of the GPS receiver by fast

receiving signals from the satellites through estimating power break time being estimated by using a correction function for real time clock and simultaneous search of a plurality of code phases corresponding to GPS signal.

According to an aspect of the present invention, there is provided a power managing system for a GPS receiver comprising: an intermediate frequency generating means for generating a intermediate frequency by converting a radio frequency of signals received from a satellite to the intermediate frequency; a digital signal processing means for processing intermediate frequency signals provided by the intermediate frequency generating means to be used in a navigation data processes; a navigation data processing means for calculating satellite navigation data based on a processed digital signals from the digital signal processing means, estimating a power break time, and generating a power control signals capable of providing power to the intermediate frequency generating means and the digital signal processing means only when satellite data required for a calculation of the satellite navigation data is received; and a power supply means for controlling a power supply to the intermediate frequency generating means and the digital signal processing means on the basis of the power control signals provided from the navigation data processing means.

Brief Description of Drawings

The above and other objects and features of the present invention will become apparent from the following description of a preferred embodiment given in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a conventional GPS receiver;

Fig. 2 is a block diagram illustrating an exemplary structure of a correlator in Fig. 1;

Fig. 3 is a block diagram showing an embodiment of a power managing apparatus for GPS receiver in accordance with the present invention;

Fig. 4 is a graph describing an algorithm used in the power managing apparatus for GPS receiver of Fig. 3;

Fig. 5 is a timing diagram describing a principle of an estimation of a power break time for use in the GPS receiver shown in Fig. 3;

Fig. 6 is a diagram showing an embodiment of a real time clock application unit illustrated in Fig. 3;

Fig. 7 and Fig. 8 are timing diagrams for describing an operation of the real time clock application unit shown in Fig. 6; and

Fig. 9 is a block diagram illustrating an embodiment of a correlator shown in Fig. 3.

Best Mode for Carrying Out the Invention

Hereinafter, a preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings.

Fig. 3 is a block diagram showing an embodiment of a power managing apparatus for GPS receiver in accordance with the present invention. In the power managing apparatus for GPS receiver in Fig. 3, a navigation data processing means 118 receives output signals received from a digital signal processing means 112 and calculates a satellite navigation data by using the output signals. In addition, the navigation data processing means 118 controls a power supply means 120 so that the power supply means 120 provides power to an intermediate frequency generating means 110 and the digital signal processing means 112 once satellite data required for calculation of the satellite navigation data is received. The digital signal processing means 112 includes a correlator 114 and a real time clock application unit 116.

The power managing apparatus in accordance with the present invention will be described in more detail with reference to Fig. 4 to Fig. 9.

Fig. 4 is a graph describing an algorithm of the power managing apparatus for GPS receiver shown in Fig. 3.

In Fig. 4, the digital signal processing means 112 generates signals as shown in Fig. 5b from satellite signals as shown in Fig. 5a, the navigation data processing means 118 estimates the power break time by using a correction function for real time clock of the real time clock application unit 116. In addition, the navigation data processing means 118 controls the power supply means 120 to intermittently supply power for the intermediate frequency generating means 110 and the digital signal processing means 112 based on the estimated power break time. The real time clock application unit 116 corrects the real time clock by using a clock source of the GPS receiver. The clock source of the GPS receiver, for example, may be a main clock of the digital application processing means 112.

Thus, the intermediate frequency generating means 110 and the digital signal processing means 112 are supplied with power from the power supply means 120, and operate only while information required for a navigation calculation is received from satellites. Symbols 'RF', 'DSP' and 'CPU' shown in Fig. 4 mean the intermediate frequency generating means 110, the digital signal processing means 112 and the navigation data processing means 118, respectively.

Precise estimation of the power break time or power supply interruption time is required in order to maintain a signal synchronization. For a precise estimation of the

power break time, a method for estimating the power break time by using the real time clock may be used. In general, however, various crystal oscillators used for the real time clock have different frequencies which may differ from a product to another, and further frequency characteristics of each crystal oscillator may vary with time. Thus, it is difficult to maintain the signal synchronization by using a nominal frequency value presented by an oscillator manufacturer. Therefore, an extra means is required to estimate an oscillator frequency used in a real time application.

Referring to Fig. 6, the real time clock application unit 116 comprises a write register 60, a frequency measuring unit 62, a power supply control unit 64 for controlling power supply time and a read register 66.

As shown in Fig.6, the write register 60 provides the frequency measuring unit 62 with an initial value of a calibration counter set as illustrated in Fig. 7d and signals as illustrated in Fig. 8b. In addition, the write register 60 provides a wake-up time for the navigation data processing means 118 for the control unit 64 as shown in Fig. 7e.

The frequency measuring unit 62 estimates frequencies of the real time clock. In detail, the frequency measuring unit 62 counts the number of main clocks within the real time clocks, as shown in Fig. 7a, defined by a user and

provided from an outside, and transfers the number of the main clocks to the navigation data processing means 118 via the read register 66.

The power supply control unit 64 controls a power supply time, in particular, receives the wake-up time of the navigation data processing means 118 from the write register 60 and transfers signals as shown in Fig. 7f to the navigation data processing means 118. For example, if the navigation data processing means 118 sets a value of "7" for the wake-up time, the power supply control unit 64 provides signals as shown in Fig.7f to the navigation data processing means 118 after seven clocks of the real time clock as Fig. 7a. The signals as shown in Fig. 7b are provided from an outside. The signals as shown in Fig.7f may be used as an interrupt of the navigation data processing means 118.

The signals as depicted in Fig. 8c are internal signals as a down counter using the real time clock as shown in Fig. 8a, and the signals in Fig. 8d are maintained at a value of "1" during the signals of Fig. 8c are not zero.

The signals as shown in Fig. 8g are internal signals for transferring the main clock while the signals of Fig. 8d remain "1" level. The signals as shown in Fig. 8h keep count by using the main clocks transferred. Latching and clearing operations of signals may be performed by using

the internal signals as shown in Fig. 8e and Fig. 8f. Latched signals are transferred to the read register 66.

Though, however, estimation of a frequency of a clock used for a real time application is readily obtainable by using the frequency measuring unit 62, an estimation error may increase in proportion to the increase of the power break time because of time-varying characteristics of the crystal oscillator. Therefore, a signal processor in accordance with the present invention is designed to be capable of maintaining synchronization by using a plurality of integrators despite the existence of an error ranging ±5 microseconds.

Fig.9 is a block diagram illustrating an example of the correlator 114 as shown in Fig. 3, wherein the correlator comprises a carrier generator 70, a first carrier mixer 72, a second carrier mixer 74, a code generator 76, a multi-phase C/A code generator 78, a first to a thirty-second code mixers 80~84, 92~96, and a first to a thirty-second integrator 86~90, 98~102.

In Fig. 9, the carrier generator 70 generates sinusoidal signals used for eliminating a carrier wave from satellite signals. The carrier generator 70 inputs the frequency provided for the navigation data processing means 118, generates sine signals (I) and cosine signals (Q), and provides the sine and cosine signals to the first and second carrier mixers 72 and 74, respectively.

The first carrier mixer 72 multiplies the sine signals (I) from the carrier generator 70 by a digital intermediate frequency from the intermediate frequency generating means 110, and provides multiplied signals for the first to the sixteenth code mixers 80~84.

The code generator 76 generates a reference frequency used for generating a PRN code of GPS, and feeds the reference frequency to the multi-phase C/A code generator 78.

The multi-phase C/A code generator 78 generates 16 numbers of PRN codes with different phase each other by using the reference frequency from the code generator 76, and provides the PRN codes for the first to the thirty-second code mixers 80~96.

The first code mixer 80 multiplies the PRN code from the multi-phase C/A code generator 78 by an output of the first carrier mixer 72, and consequently, provides multiplied signals for the first integrator 86. The first integrator 86 integrates an output of the first code mixer 80 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing means 118.

The second code mixer 82 multiplies the PRN code from the multi-phase C/A code generator 78 by an output of the first carrier mixer 72, and provides multiplied signals for the second integrator 88. The second integrator 88

integrates an output of the second code mixer 82 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing means 118.

The sixteenth code mixer 84 multiplies the PRN code from the multi-phase C/A code generator 78 by an output of the first carrier mixer 72, and provides multiplied signals for the sixteenth integrator 90. The sixteenth integrator 90 integrates an output of the sixteenth code mixer 84 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing means 118.

Similarly, each of the seventeenth, the thirty-first and the thirty-second code mixers 92, 94, and 96 multiplies the PRN code from the multi-phase C/A code generator 78 by an output of the second carrier mixer 74, and provides multiplied signals for the seventeenth, the thirty-first and the thirty-second integrators 98, 100 and 102. Each of the seventeenth, the thirty-first and the thirty-second integrators 98, 100 and 102 integrates an output of the seventeenth, the thirty-first and the thirty-second code mixers 92, 94 and 96 during one period of a C/A code, i.e., 1 millisecond, and provides an integration result for the navigation data processing means 118.

The power supply means 120 controls power supplied to the intermediate frequency generating means 110 and the

digital signal processing means 112 pursuant to power control signals provided from the navigation data processing means 118.

Industrial Applicability

In accordance with the present invention, it is possible to fast acquire signals from satellites by using the power break time estimated by a correction function for a real time clock and simultaneous search of a plurality of code phase corresponding to GPS signals, and thus to prevent unnecessary power consumption of a GPS receiver.

What is claimed is:

1. A power managing apparatus for a GPS receiver comprising:

an intermediate frequency generating means for converting an intermediate a radio frequency received from a satellite into an intermediate frequency signals;

a digital signal processing means for generating processed digital signals by processing the intermediate frequency signal provided by the intermediate frequency generating means to be used in a navigation data processes, and performing a correction of a real time clock;

a navigation data processing means for calculating satellite navigation data based on the processed digital signals from the digital signal processing means, estimating a power break time, and generating power control signals for use in providing power to the intermediate frequency generating means and the digital signal processing means only when satellite data required for a calculation of the satellite navigation data is received; and

a power supply means for controlling a power supplied to the intermediate frequency generating means and the digital signal processing means on the basis of the power control signals provided from the navigation data processing means.

2. The apparatus as claimed in claim 1,

the power break time of the navigation data processing means is estimated and determined by using both the correction of the real time clock of the digital signal processing means and search of a plurality of code phase correspondent to a pseudo random noise (PRN) code of satellite data from the satellite.

3. The apparatus as claimed in claim 1 or 2,

the correction of the real time clock is performed by using a clock source of the GPS receiver.

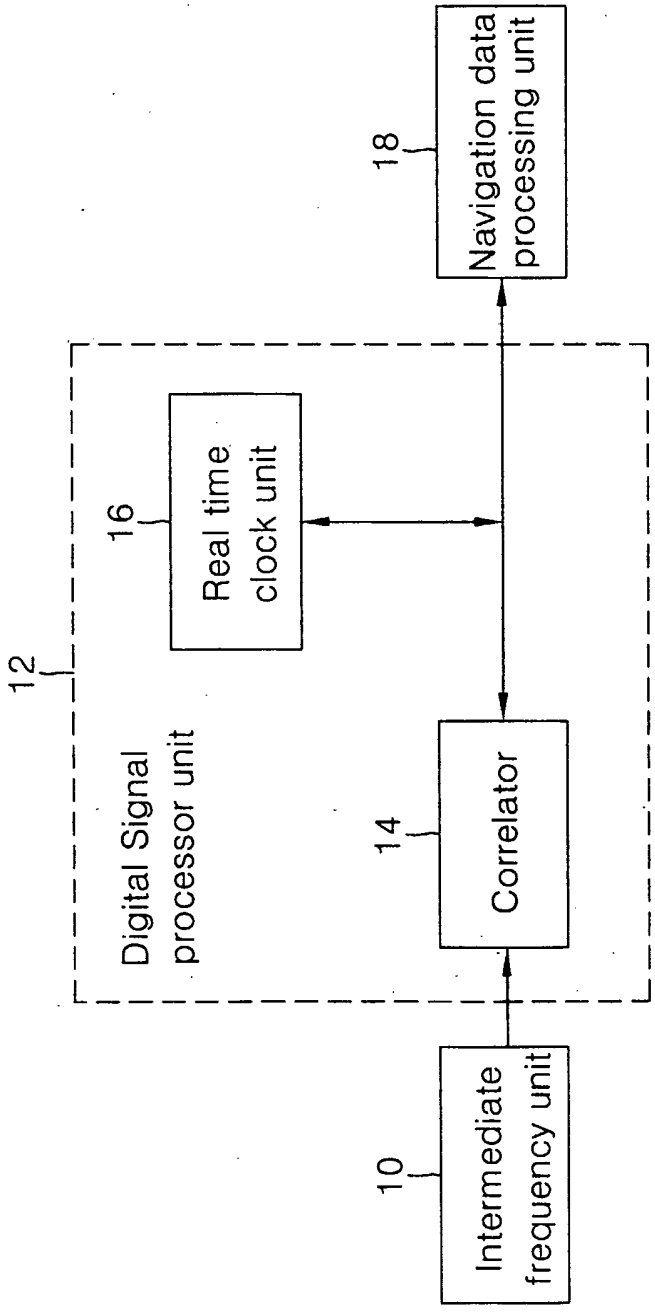
Navigation data processing unit
18
Real time clock unit
16
Digital Signal processor unit
12
Correlator
14
Intermediate frequency unit
10

FIG. 1

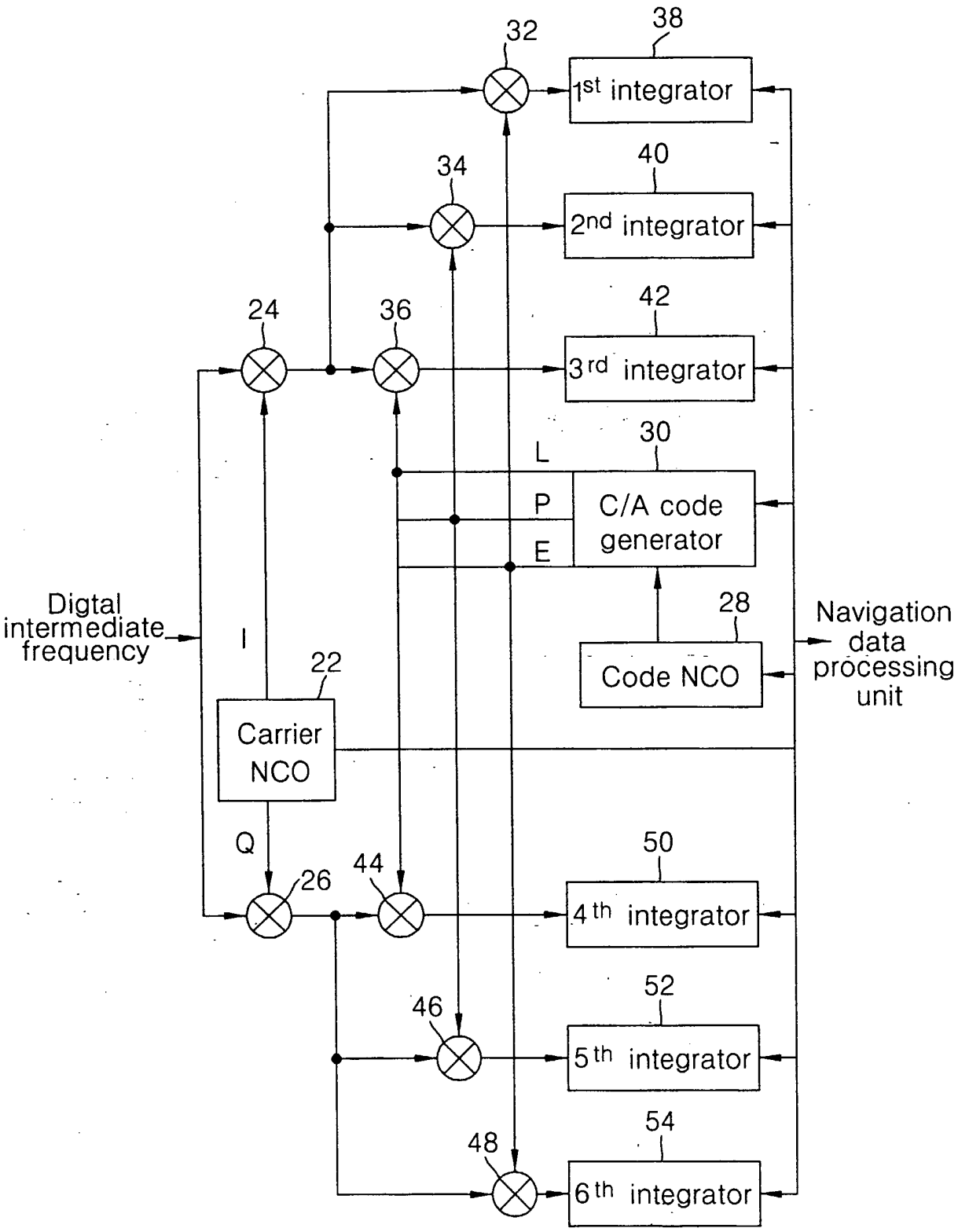
32
38
1st integrator
34
40
2nd integrator
24
36
42
3rd integrator
L
30
P
C/A code generator
E
Digtal intermediate frequency
I
28
Navigation data processing unit
22
Code NCO
Carrier NCO
Q
50
44
26
4th integrator
52
46
5th integrator
54
48
6th integrator

FIG.2

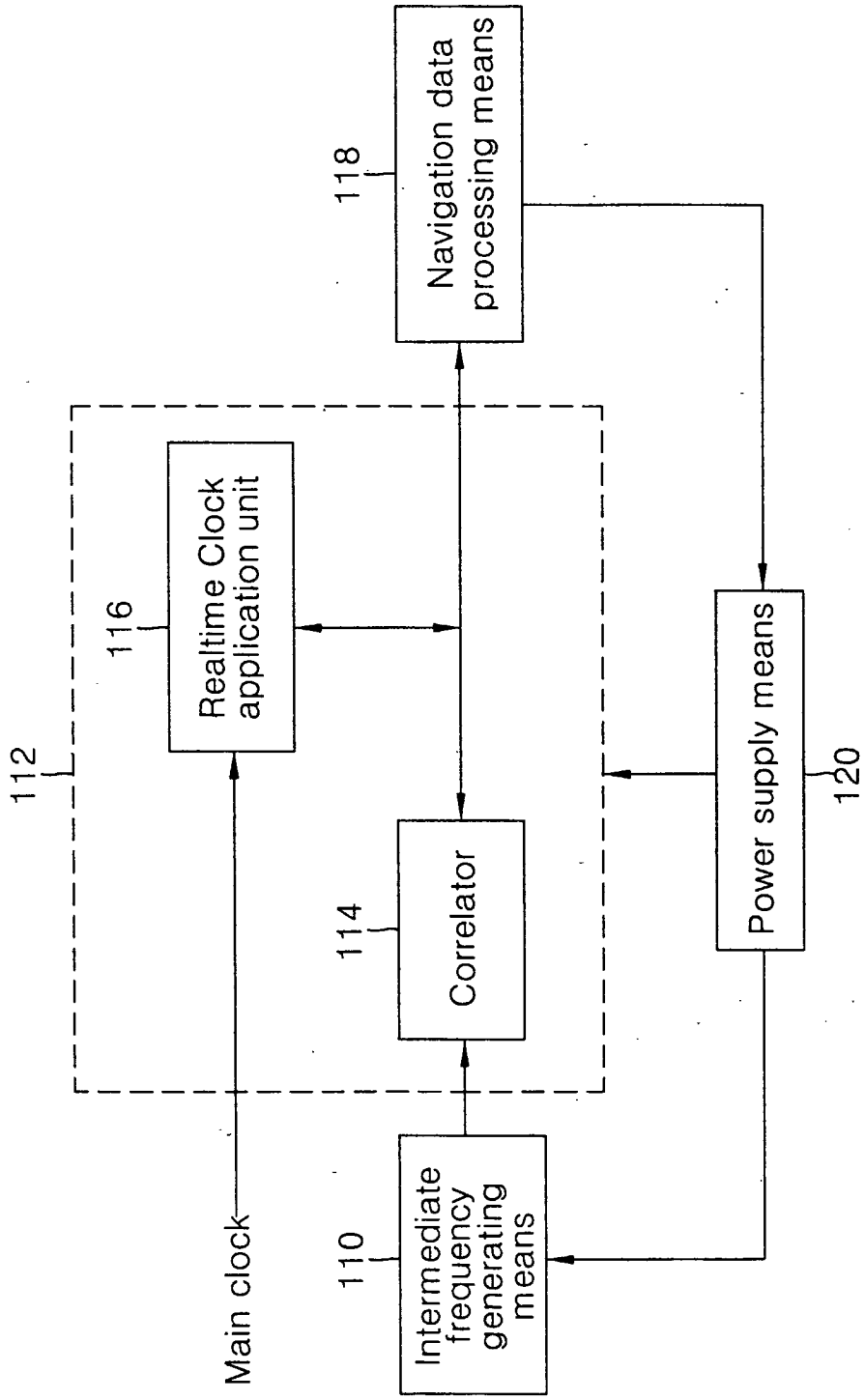
Navigation data processing means
118
Realtime Clock application unit
116
112
Correlator
114
Power supply means
120
Main clock
Intermediate frequency generating means
110

FIG.3

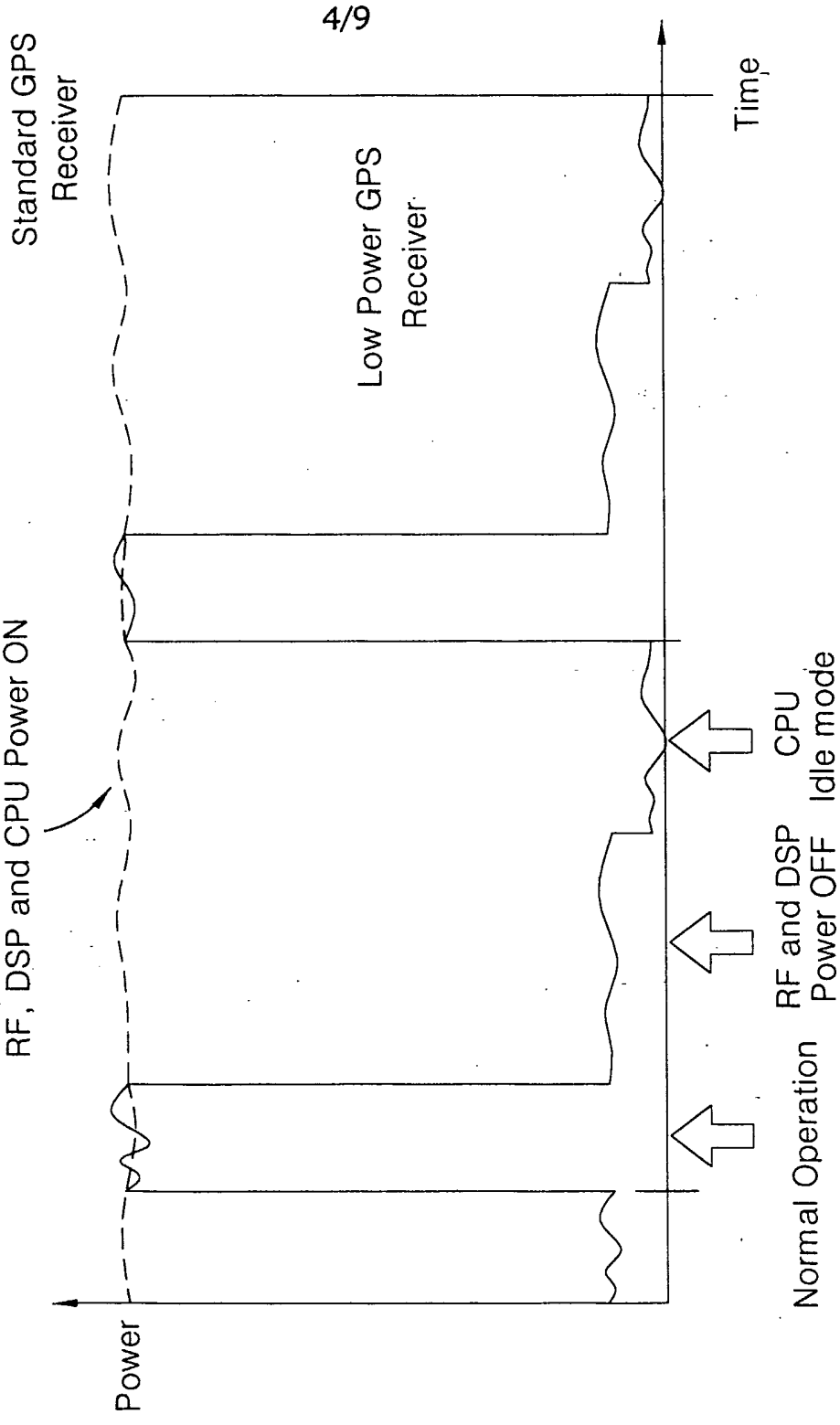
Standard GPS Receiver
Low Power GPS Receiver
Time
RF, DSP and CPU Power ON
Power
Normal Operation
RF and DSP Power OFF
CPU Idle mode

FIG. 4

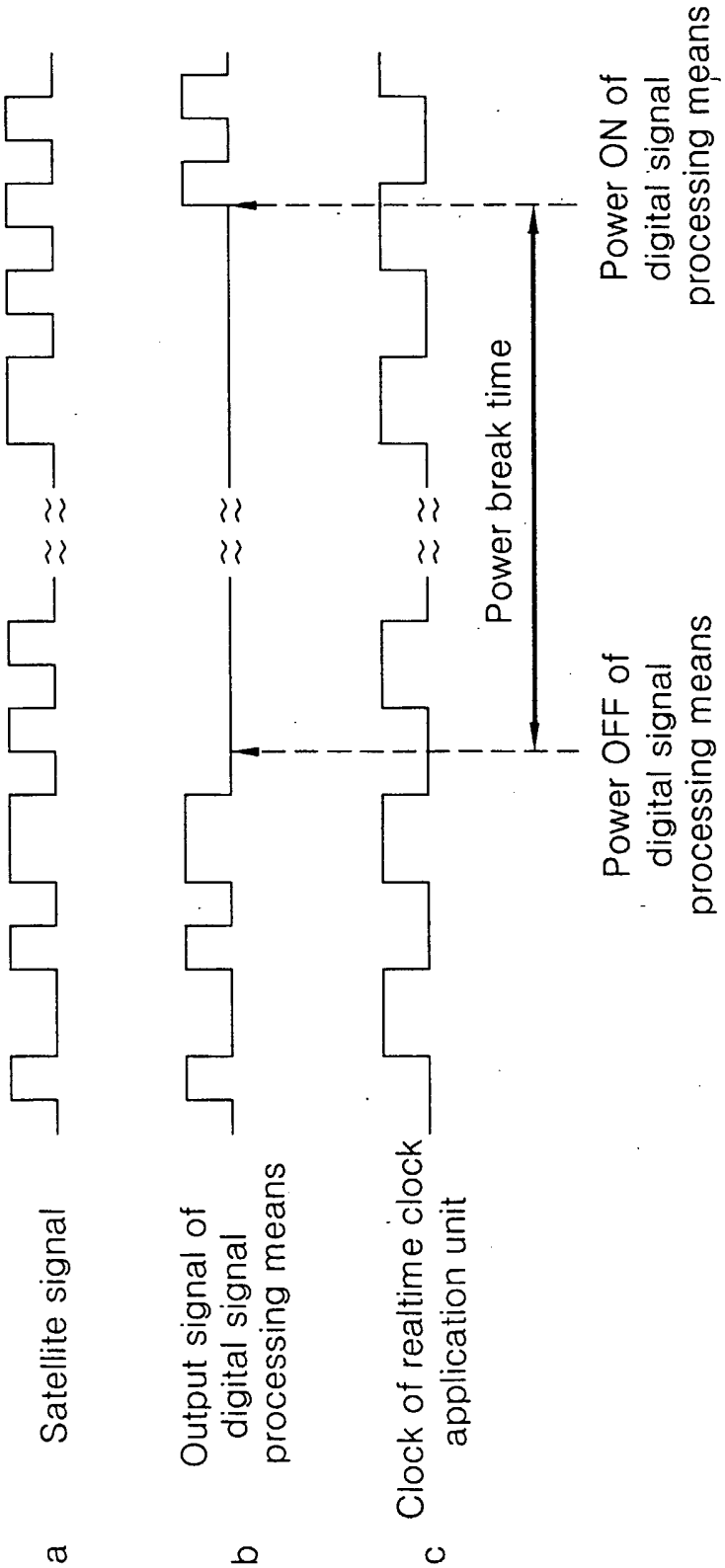
a
Satellite signal
b
Output signal of digital signal processing means
c
Clock of realtime clock application unit
Power break time
Power OFF of digital signal processing means
Power ON of digital signal processing means

FIG.5

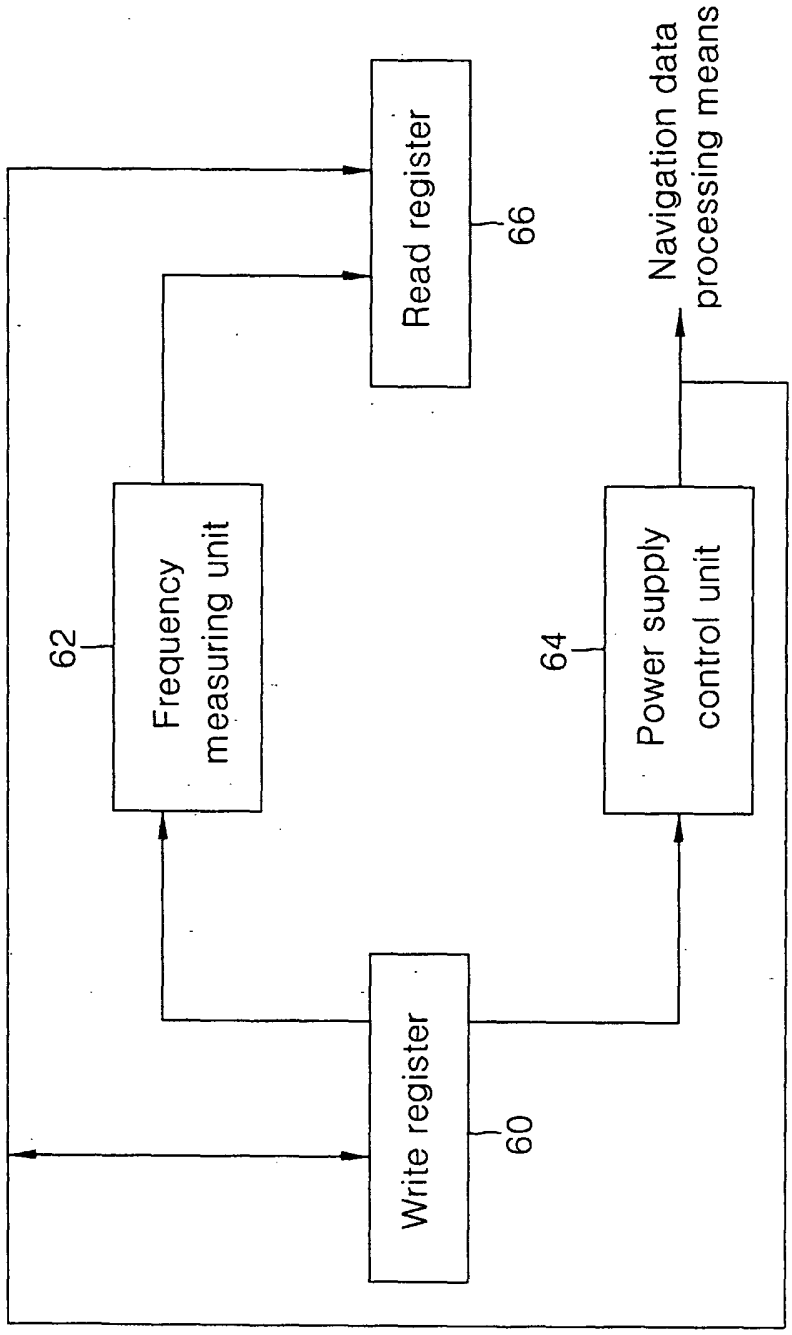
Navigation data processing means
Read register
66
Frequency measuring unit
62
Power supply control unit
64
Write register
60

FIG. 6

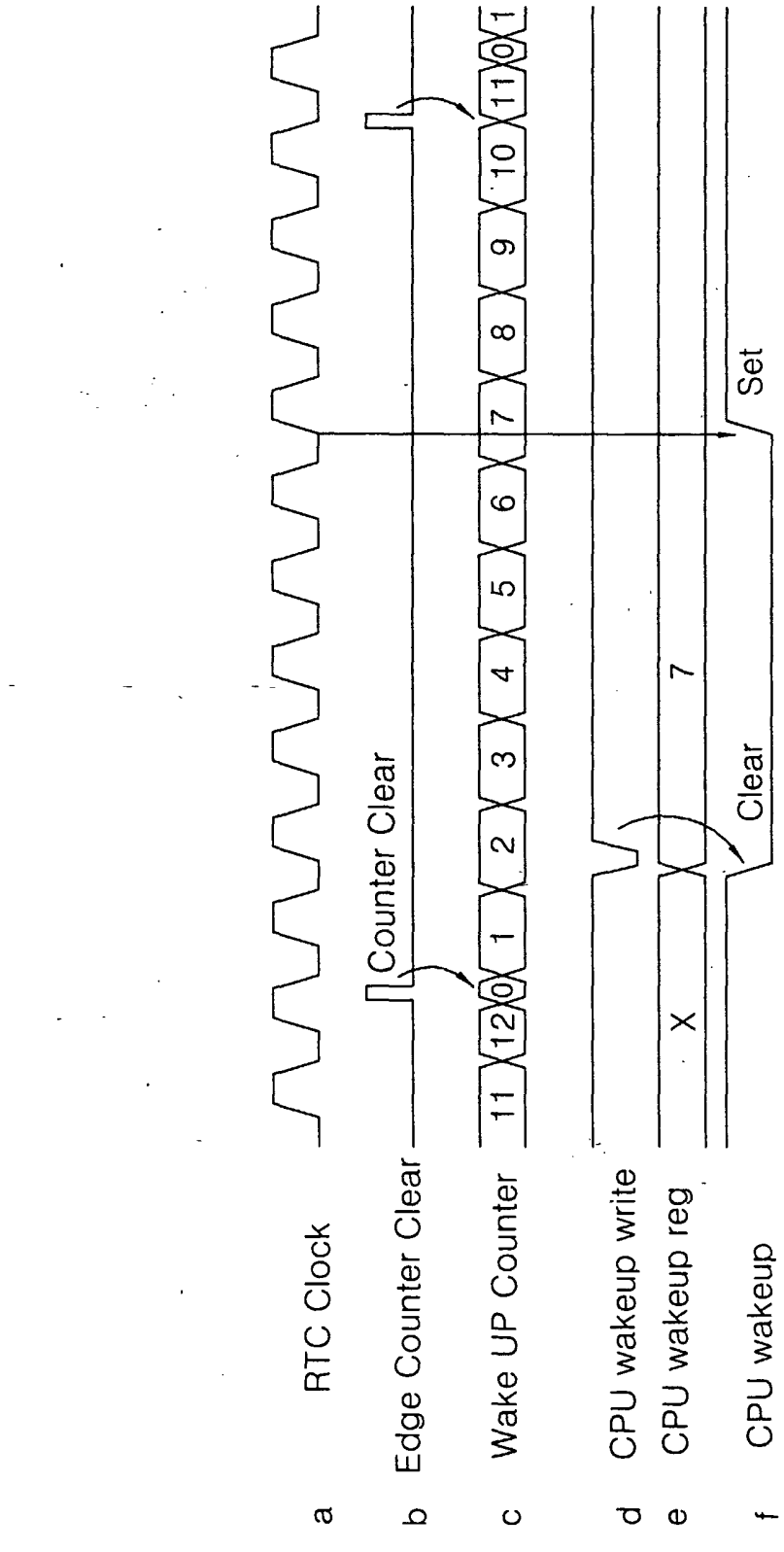
a RTC Clock
b Edge Counter Clear
c Wake UP Counter
d CPU wakeup write
e CPU wakeup reg
f CPU wakeup
Counter Clear
Set
Clear
11 12 0 1 2 3 4 5 6 7 8 9 10 11 0 1
X
7

FIG. 7

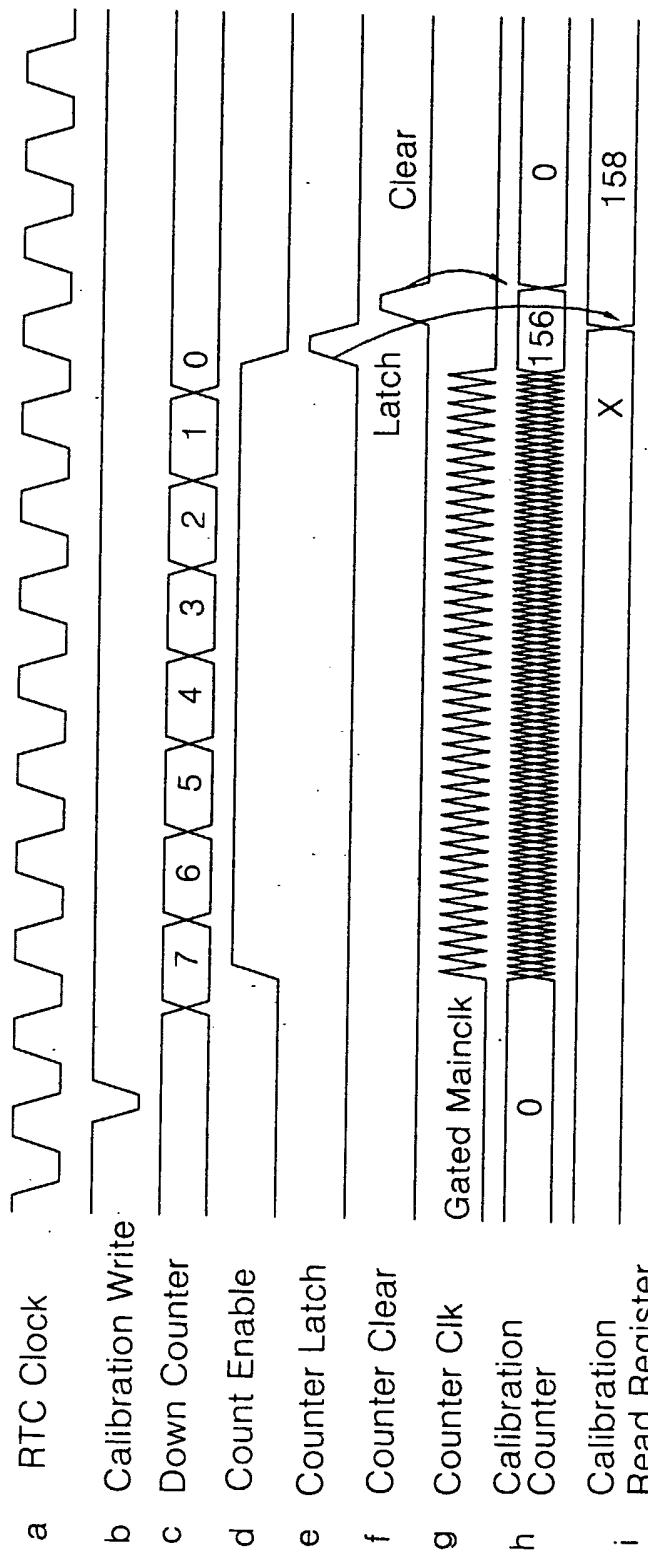
a RTC Clock
b Calibration Write
c Down Counter
7
6
5
4
3
2
1
0
d Count Enable
e Counter Latch
Latch
f Counter Clear
Clear
g Counter Clk
Gated Mainclk
h Calibration Counter
0
156
0
i Calibration Read Register
X
158

FIG.8

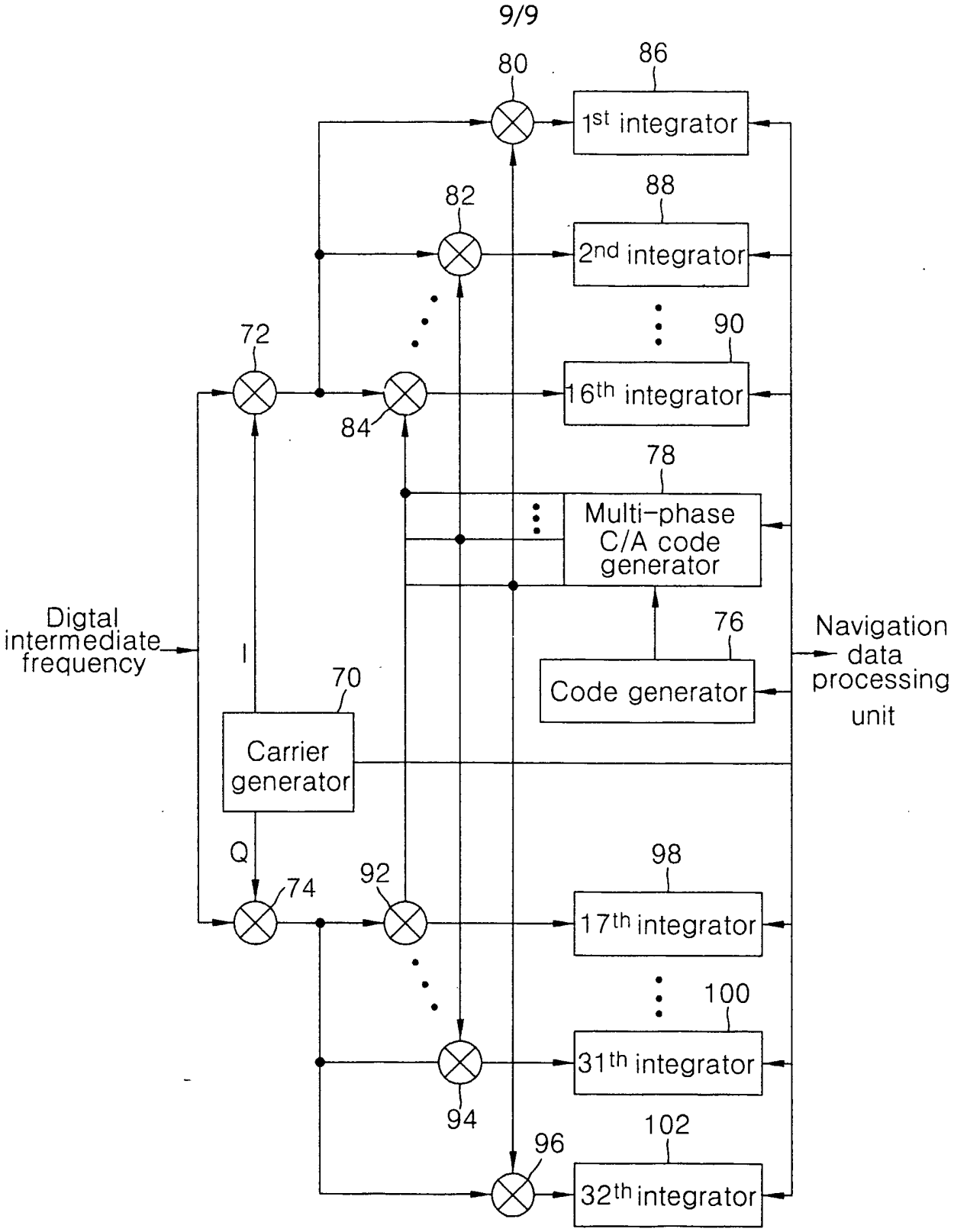
80
86
1st integrator
82
88
2nd integrator
72
90
16th integrator
84
78
Multi-phase C/A code generator
Digtal intermediate frequency
I
76
Navigation data processing unit
70
Code generator
Carrier generator
Q
74
92
98
17th integrator
100
31th integrator
94
102
96
32th integrator

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR02/00799

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 G01S 5/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 G01S 5/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,133,871 A(SnapTrack, Inc.) Oct. 17, 2000 see col. 4 ~ 20, fig. 2 ~ 7	1 ~ 3
A	US 5,995,042 A(Motorola, Inc.) Nov. 30, 1999 see col. 2 ~ 7, fig. fig. 2	1 ~ 3

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 JULY 2002 (29.07.2002)	29 JULY 2002 (29.07.2002)

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Telephone No. 82-42-481-5673