

- [54] **MULTI-INTERSECTION TRAFFIC CONTROL SYSTEM**
[75] Inventors: **Jerome W. Meyer**, Santa Clara;
Phillip A. Annen, Sunnyvale, both of Calif.
[73] Assignee: **The Singer Company**, Binghamton, N.Y.
[22] Filed: **Nov. 8, 1971**
[21] Appl. No.: **196,312**

Related U.S. Application Data

- [63] Continuation-in-part of Ser. No. 166,915, July 28, 1971, abandoned.
[52] U.S. Cl. **340/35**
[51] Int. Cl. **G08g 1/08**
[58] Field of Search..... **340/35, 31 A, 40**

References Cited

UNITED STATES PATENTS

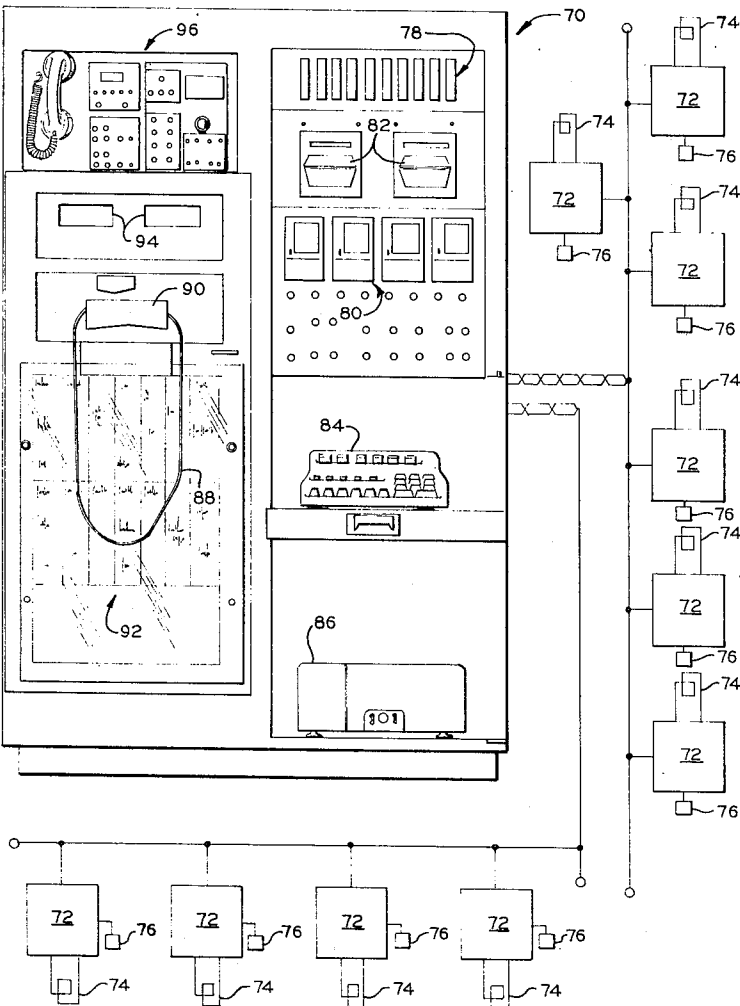
3,239,653	3/1966	Barker	235/150.24
3,254,324	5/1966	Casciato et al.	340/35
3,397,306	8/1968	Auer	235/150.24
3,482,208	12/1969	Auer et al.	340/35
3,675,196	7/1972	Molloy	340/40

Primary Examiner—William C. Cooper
Attorney, Agent, or Firm—J. Ronald Richbourg; James C. Kesterson

[57] **ABSTRACT**

A master traffic control system including both methods of and apparatus for selecting, from a plurality of pre-recorded programs, a particular program to control the energization of traffic lights at a number of intersections. The program may be chosen in response to various traffic parameters computed from signals supplied by vehicle detectors, or by the time of day, as determined by selective programming of the master controller. The traffic parameters are represented as an analog voltage cumulatively variable with changes in traffic activity, and the traffic control program may be selected in accordance with various selected averages, ratios and ranges of the computed parameters. Novel circuitry is also provided for accomplishing various functions in the master controller, such as monitoring the detector inputs, providing the analog output voltage representing the traffic parameters, averaging the voltages, etc. Various indicating devices receive outputs from control system values and operations to provide visual displays and printed records of traffic parameter values, program identifications, etc.

35 Claims, 76 Drawing Figures



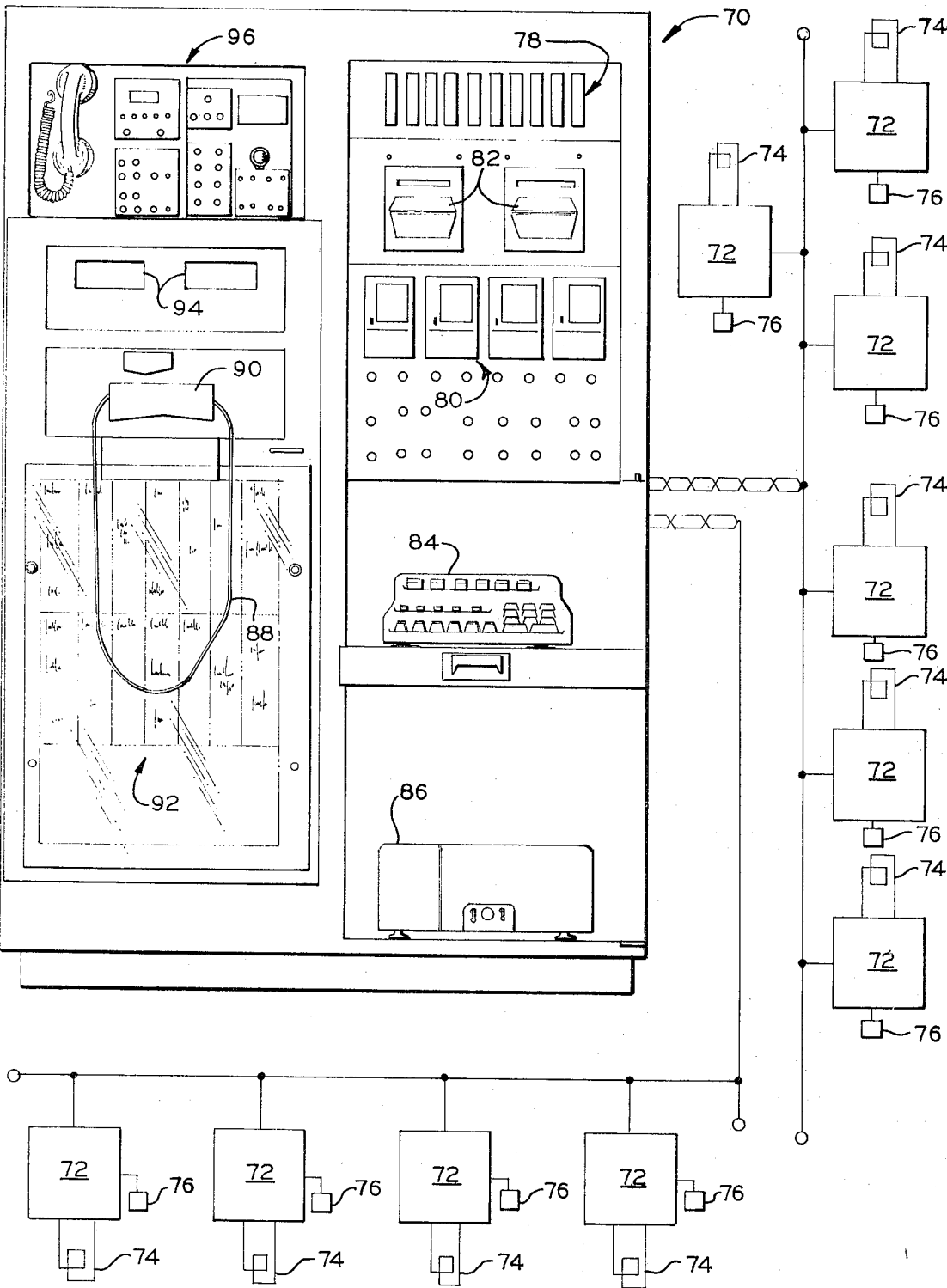


FIG. 1

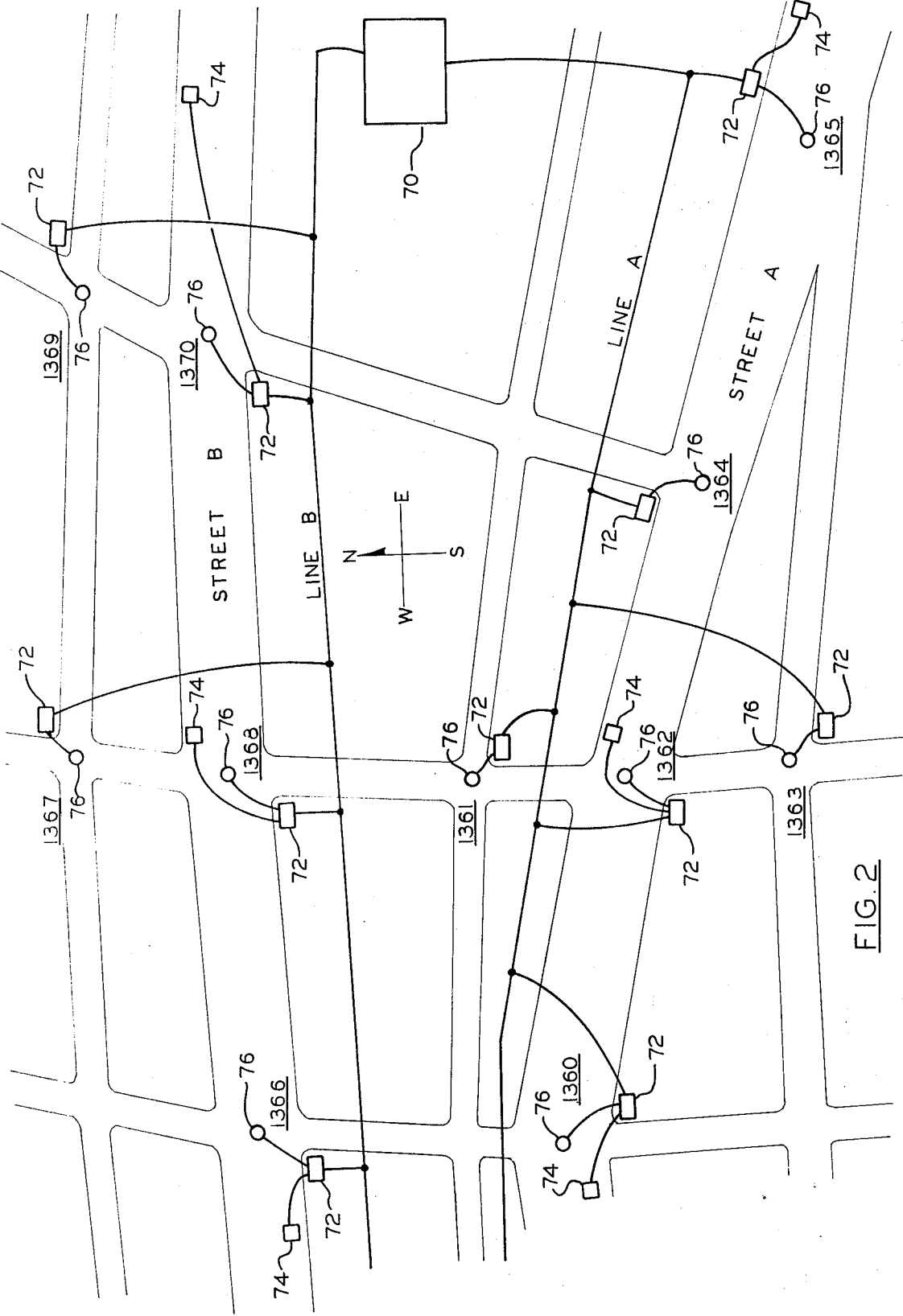


FIG. 2

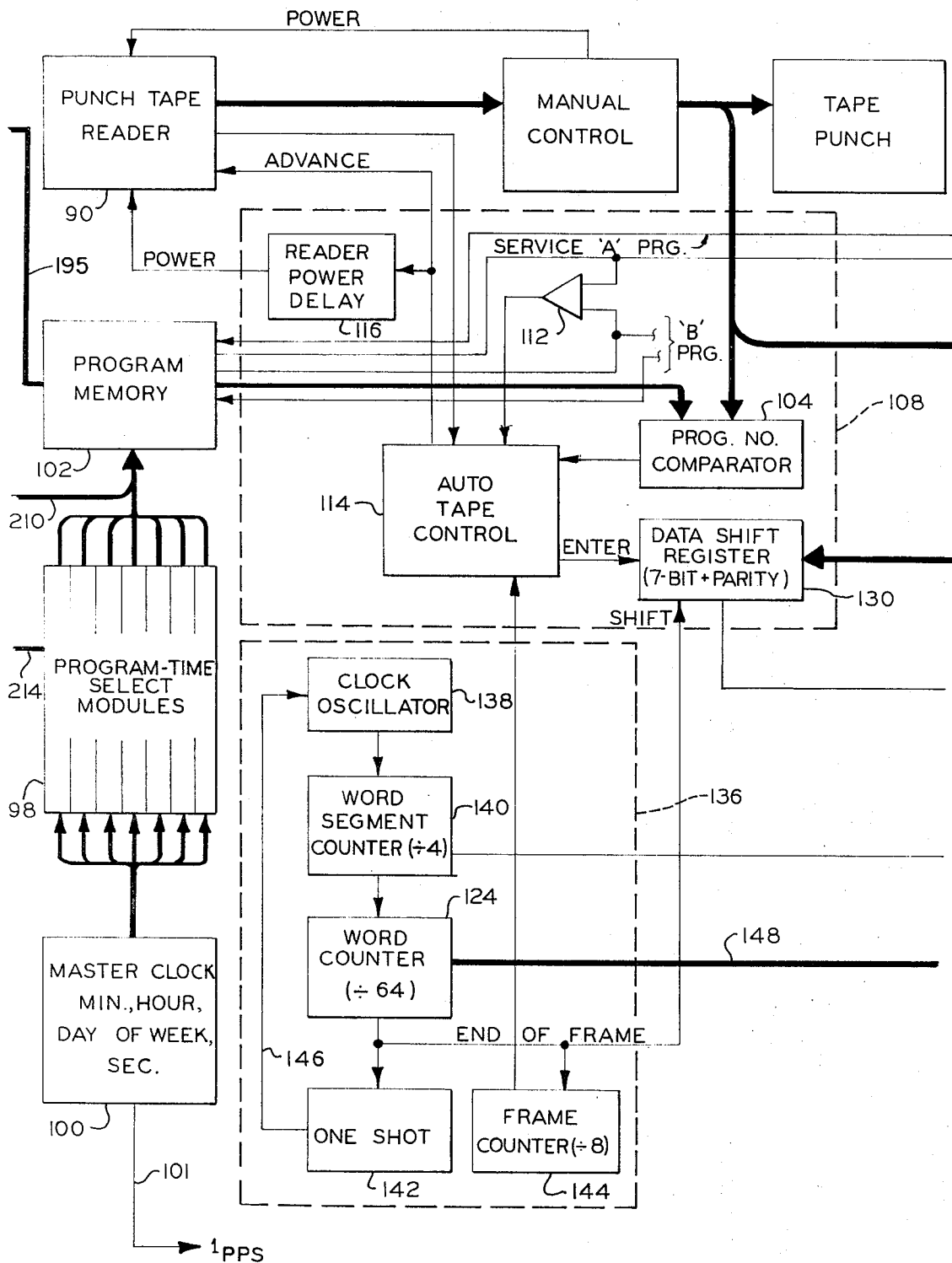


FIG. 3A

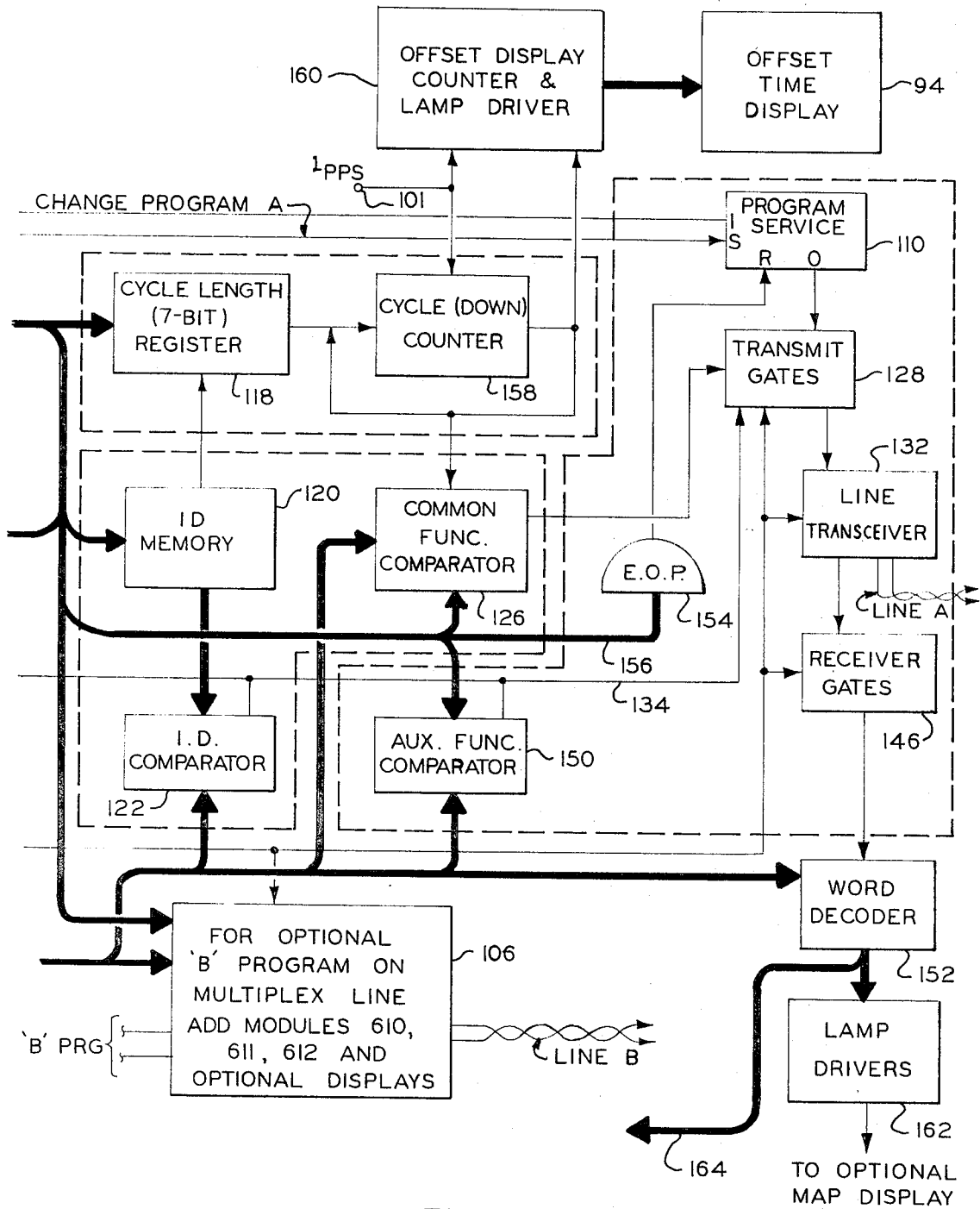


FIG. 3B

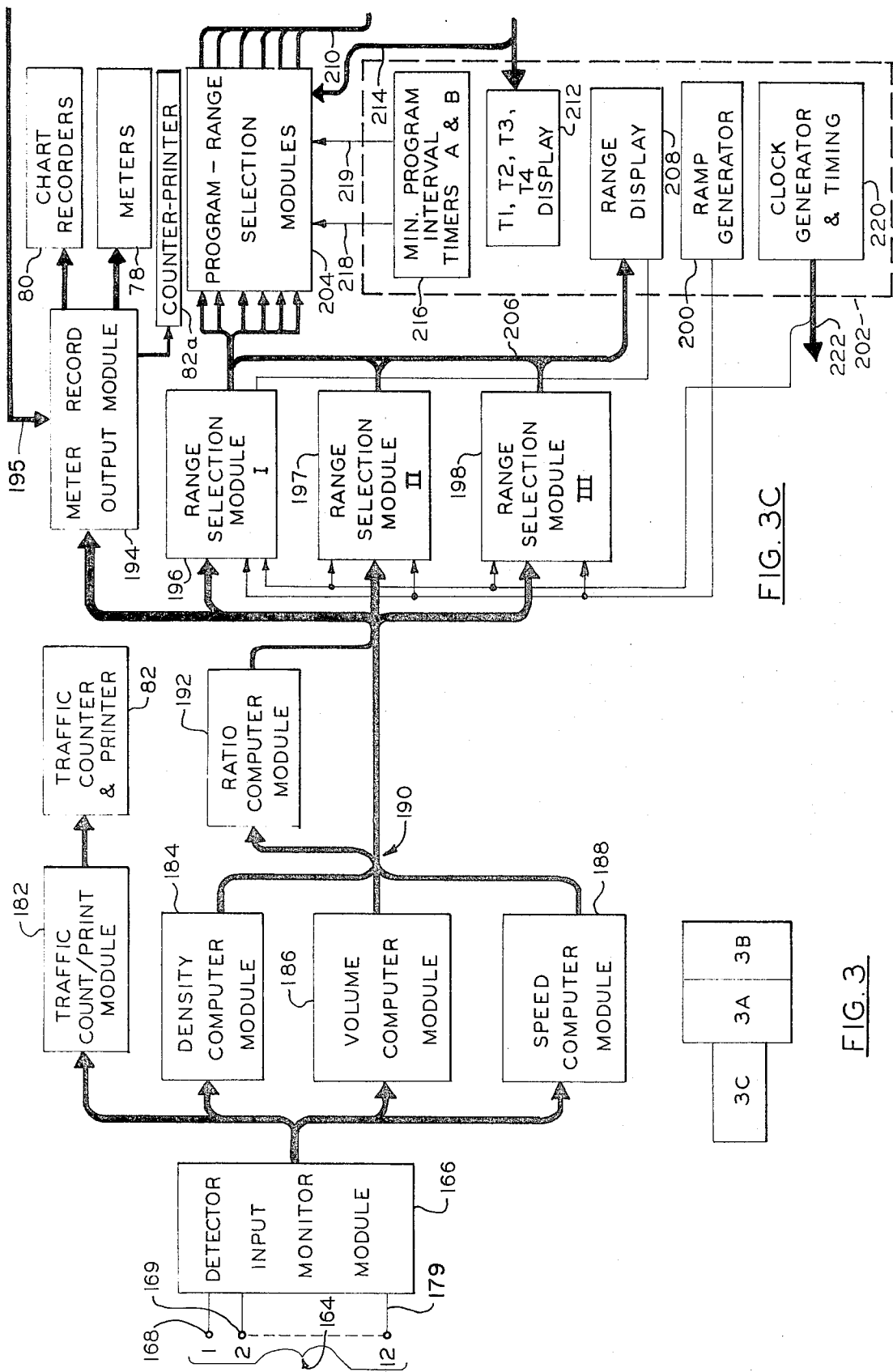


FIG. 3

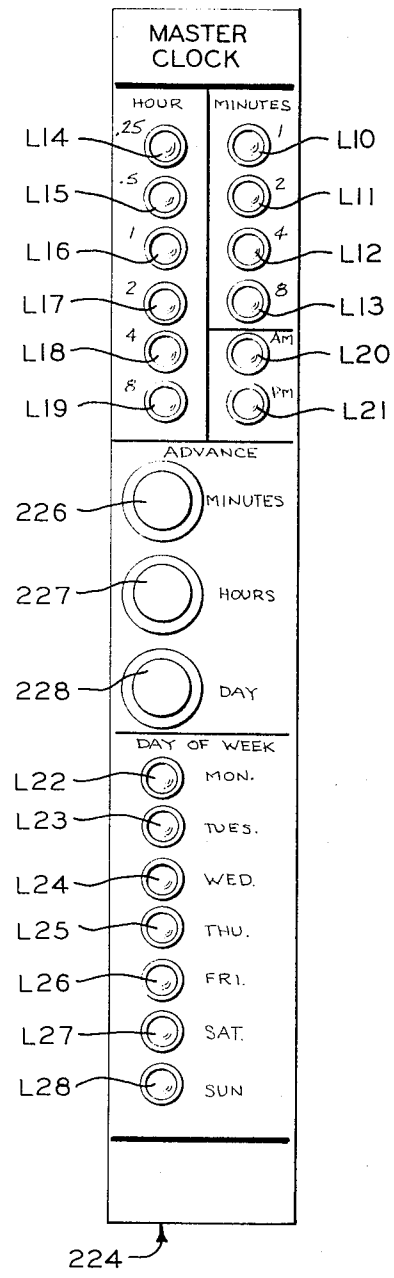


FIG. 4

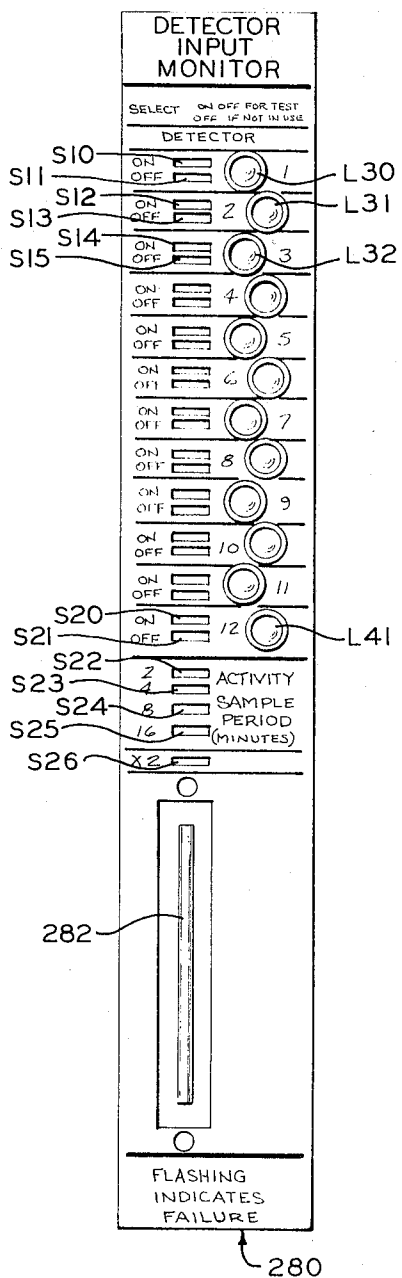


FIG. 6

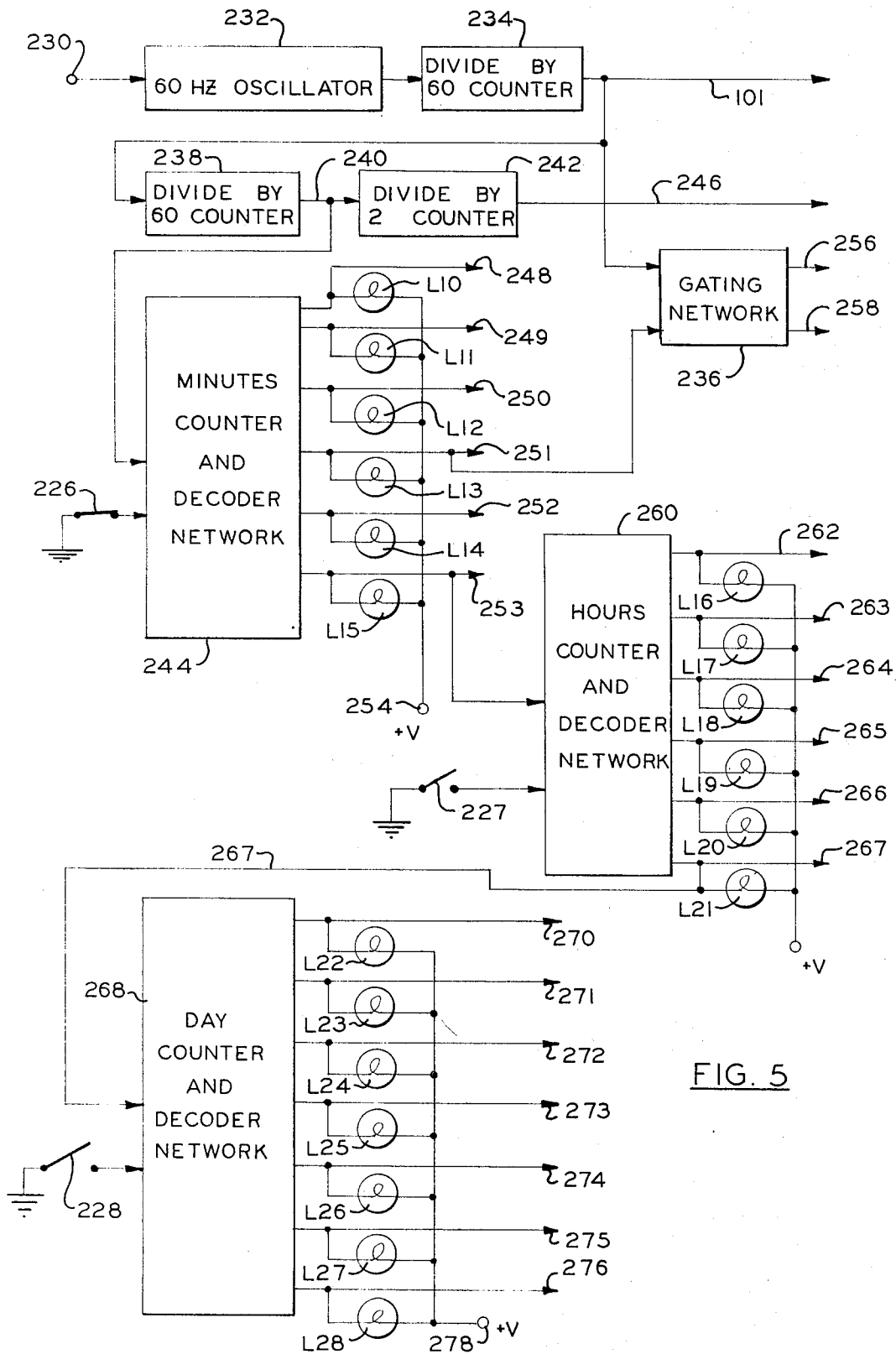


FIG. 5

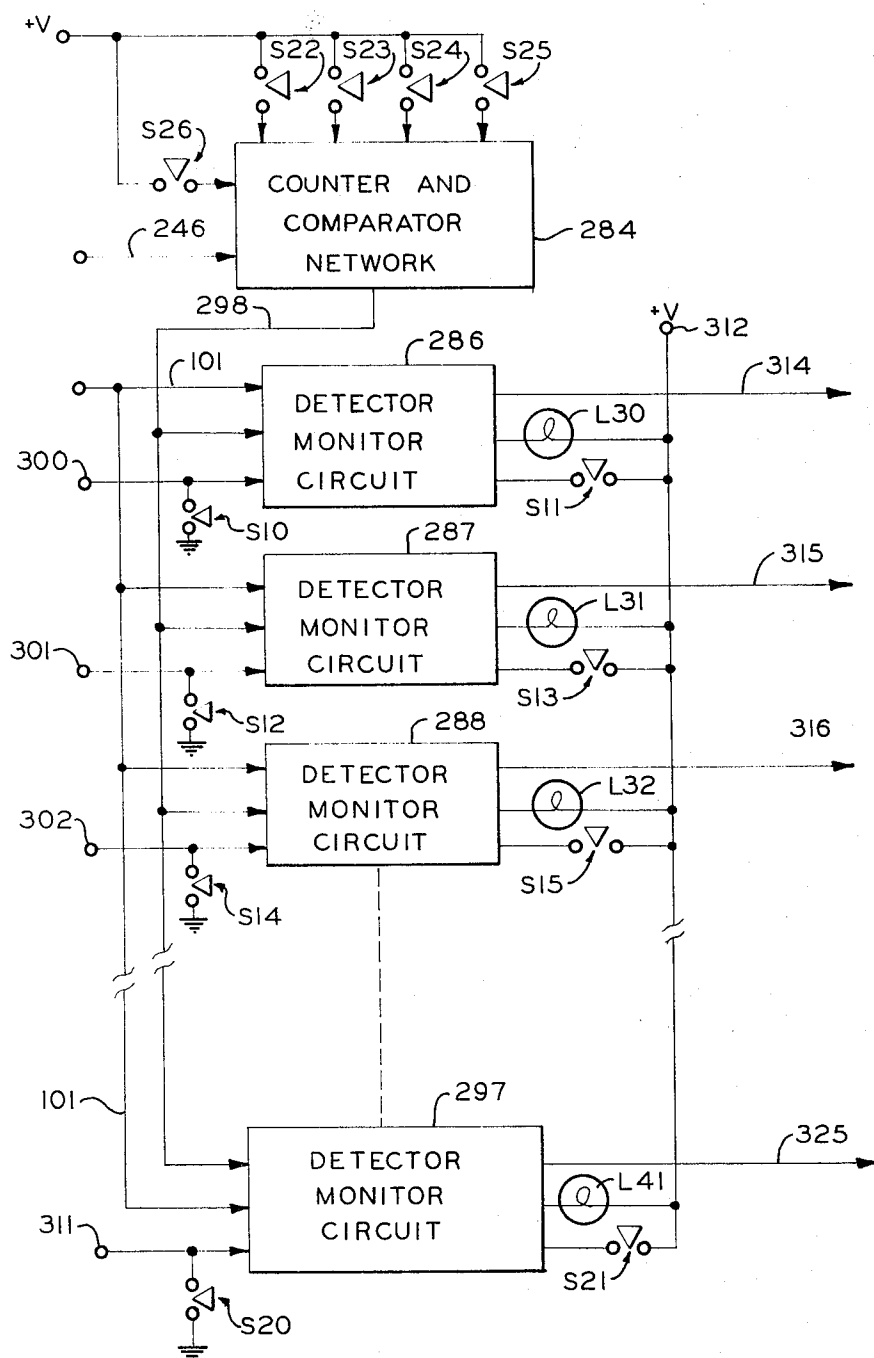


FIG. 7

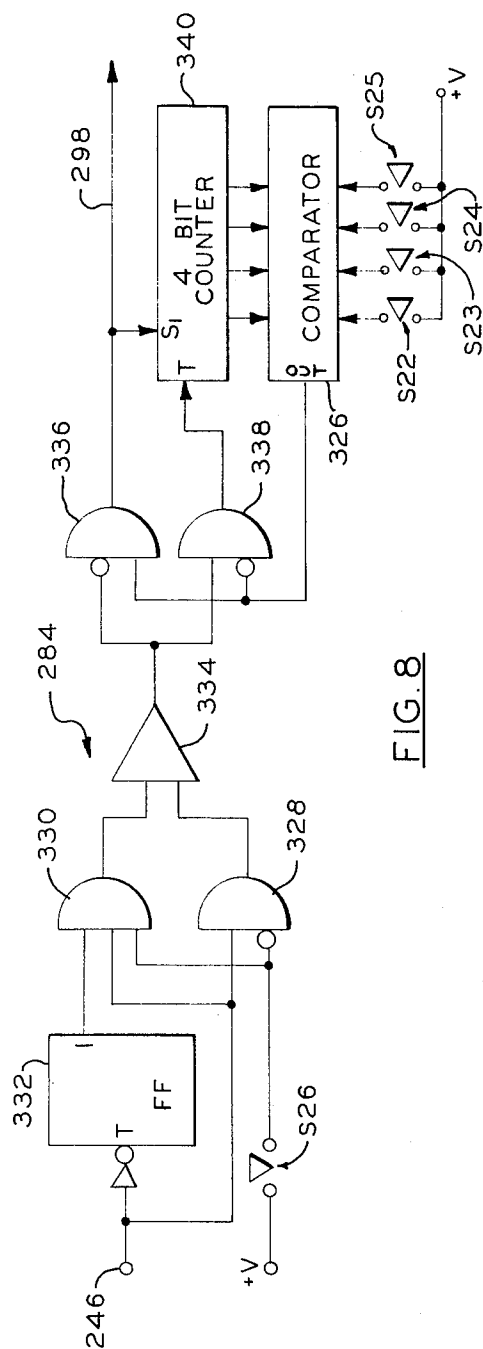
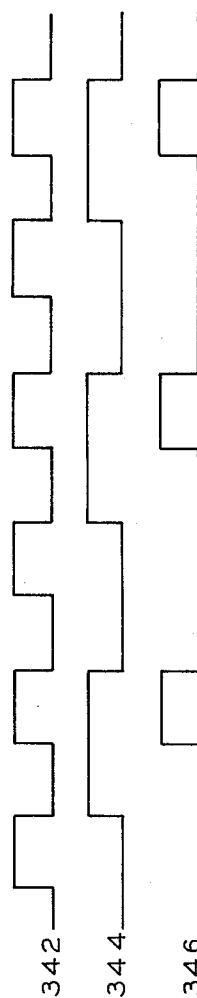
FIG. 8

FIG. 9

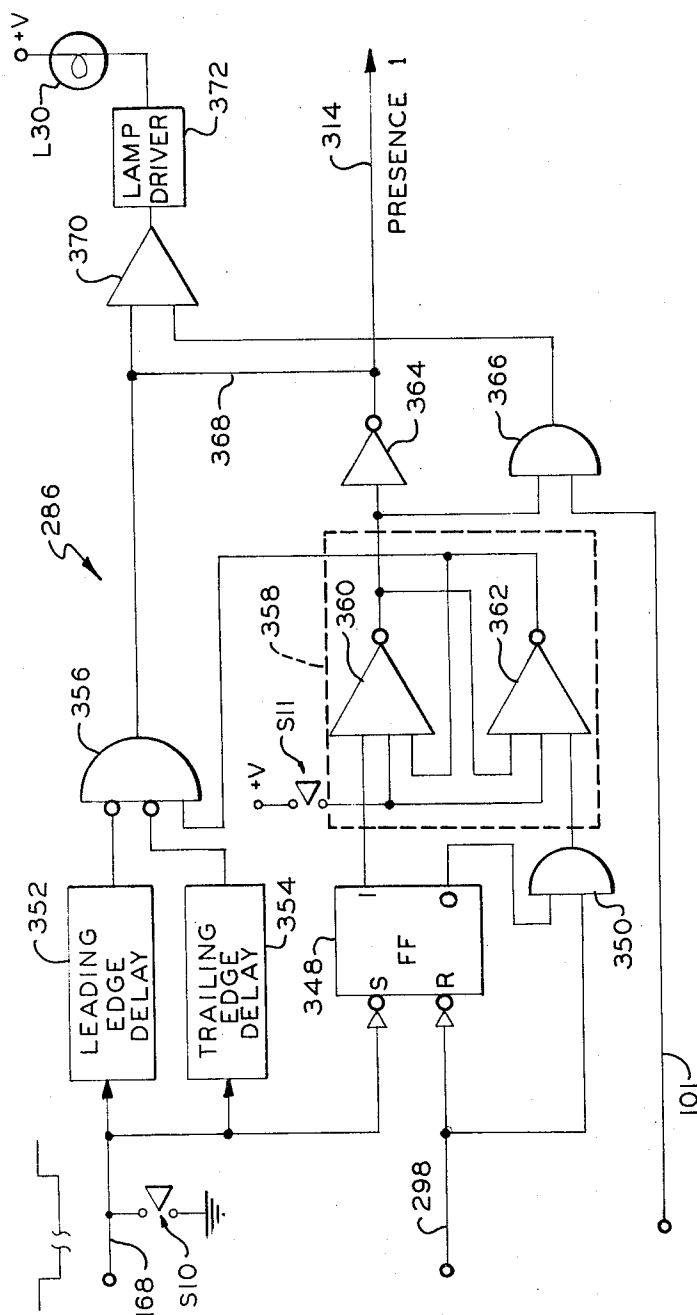


FIG. 10

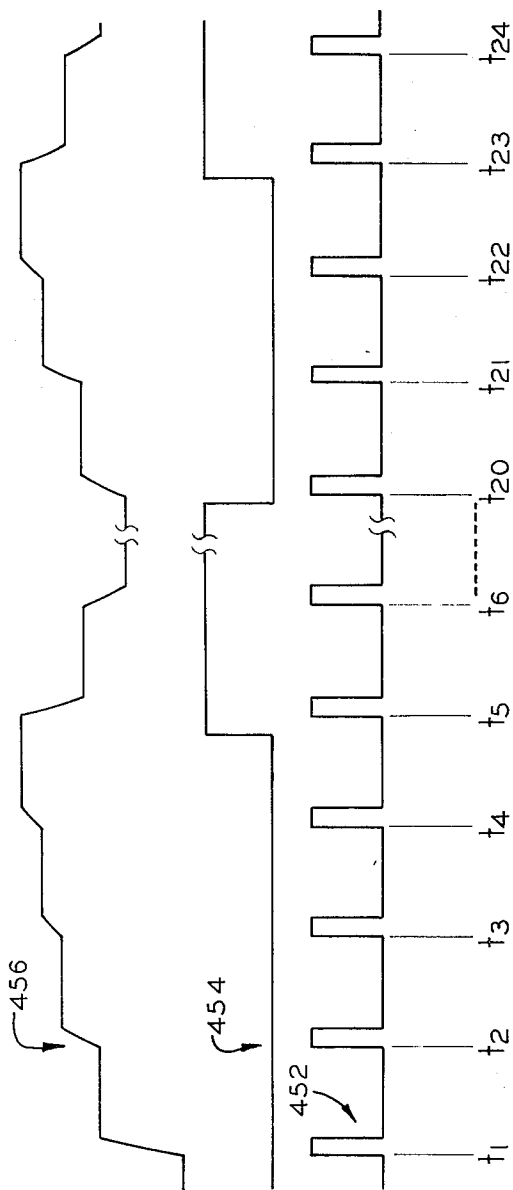


FIG. 16

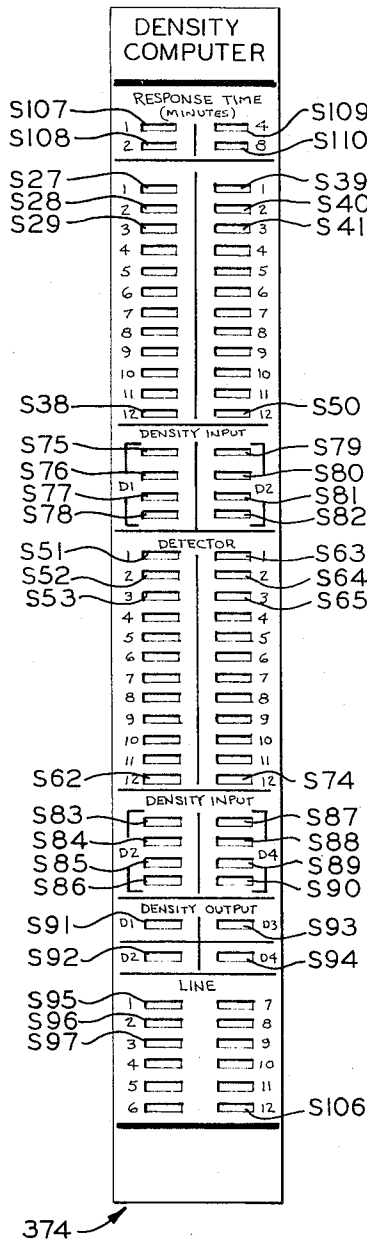
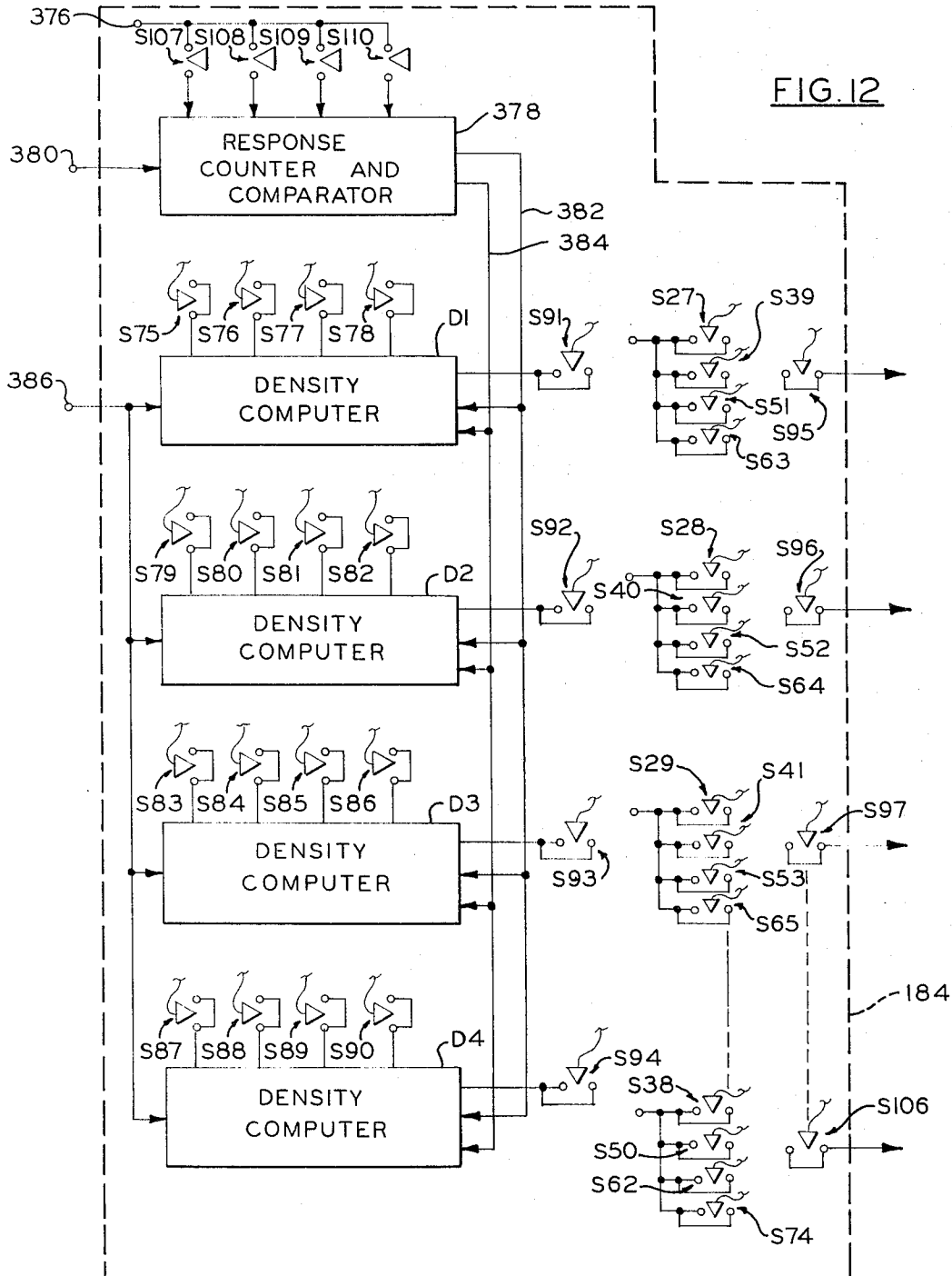


FIG. 11



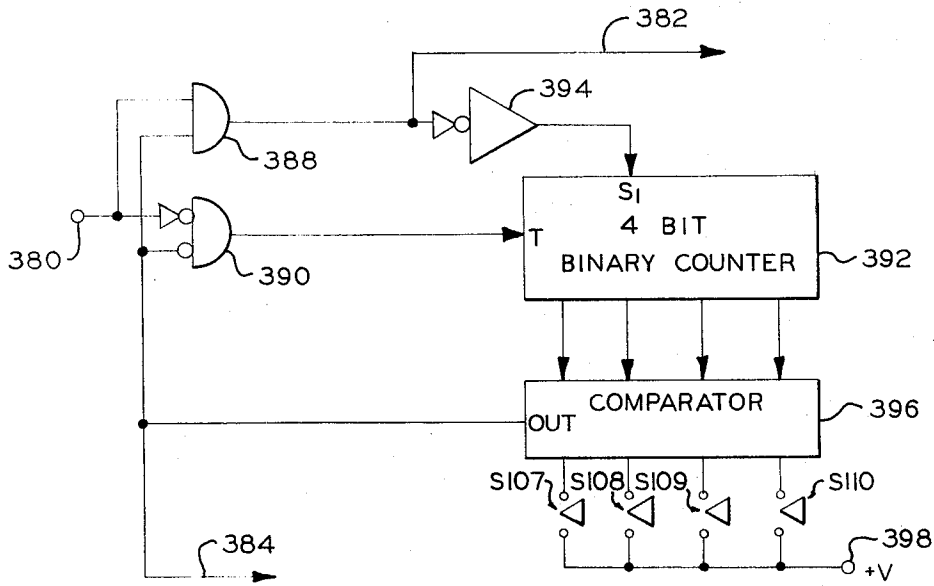


FIG. 13

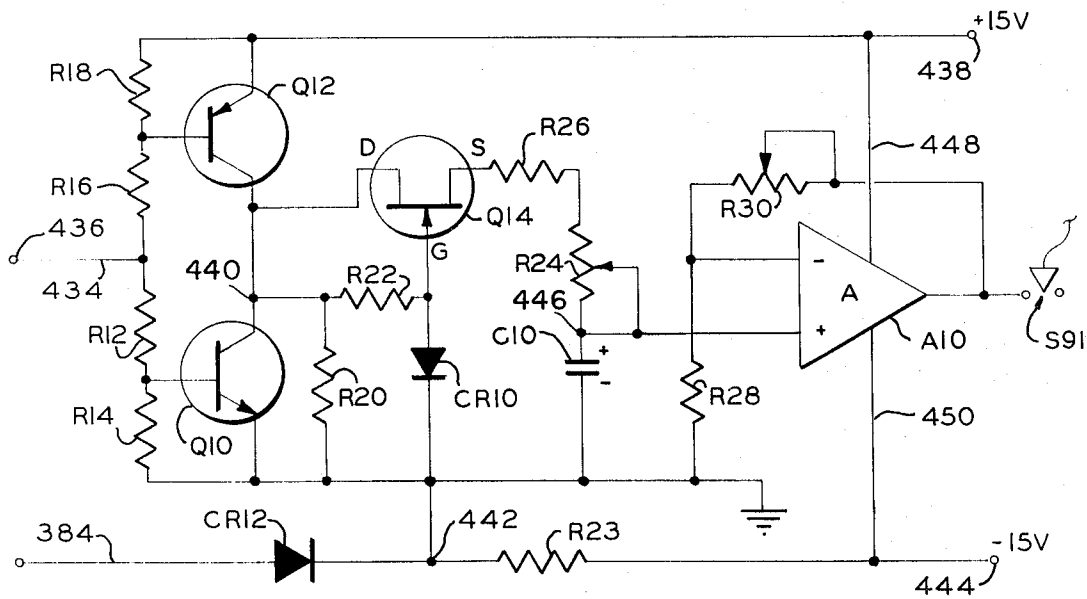


FIG. 15

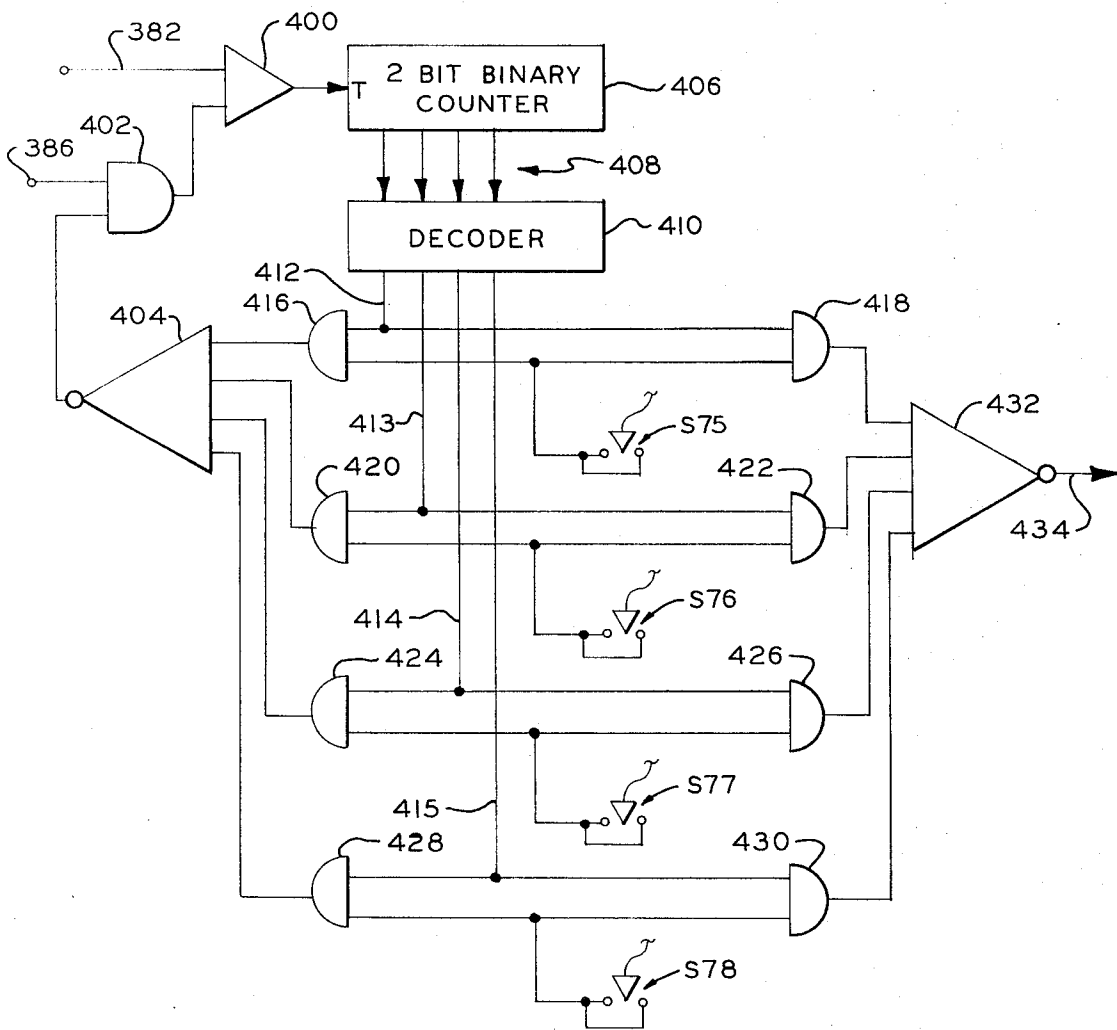


FIG. 14

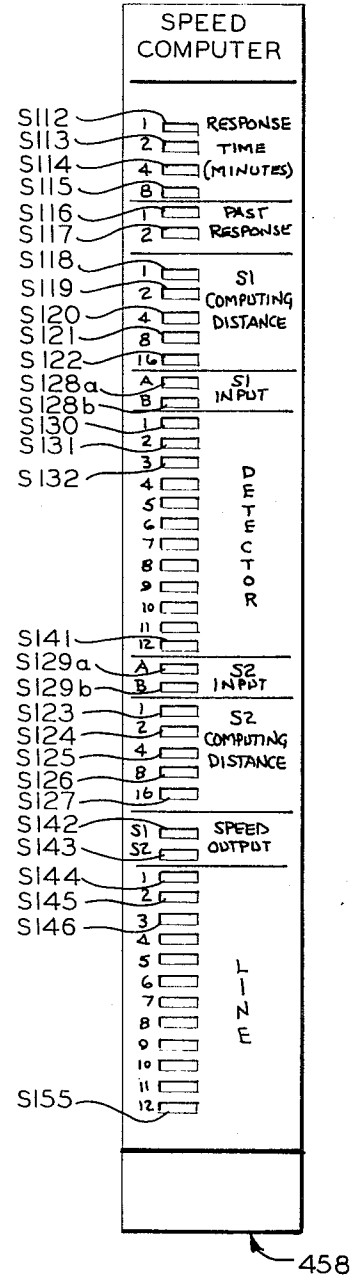


FIG. 17

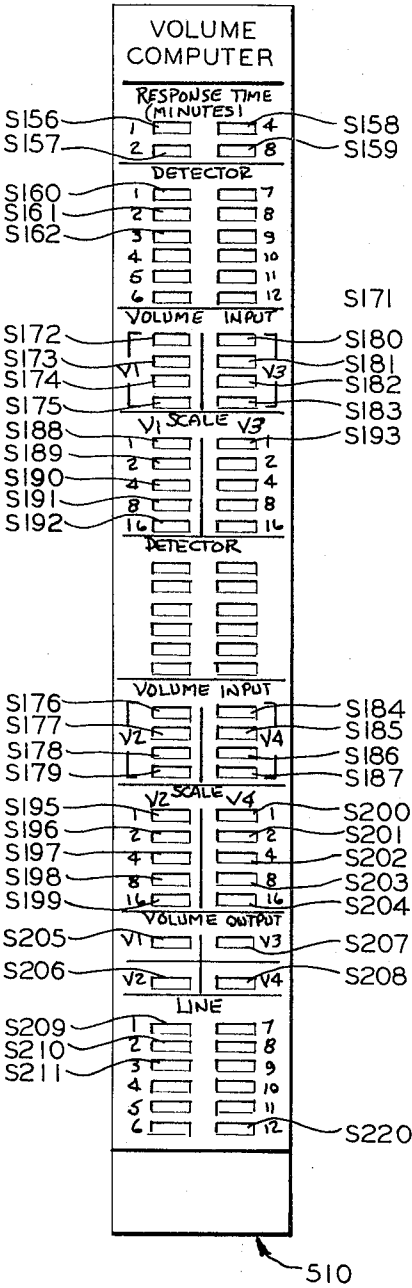


FIG. 18

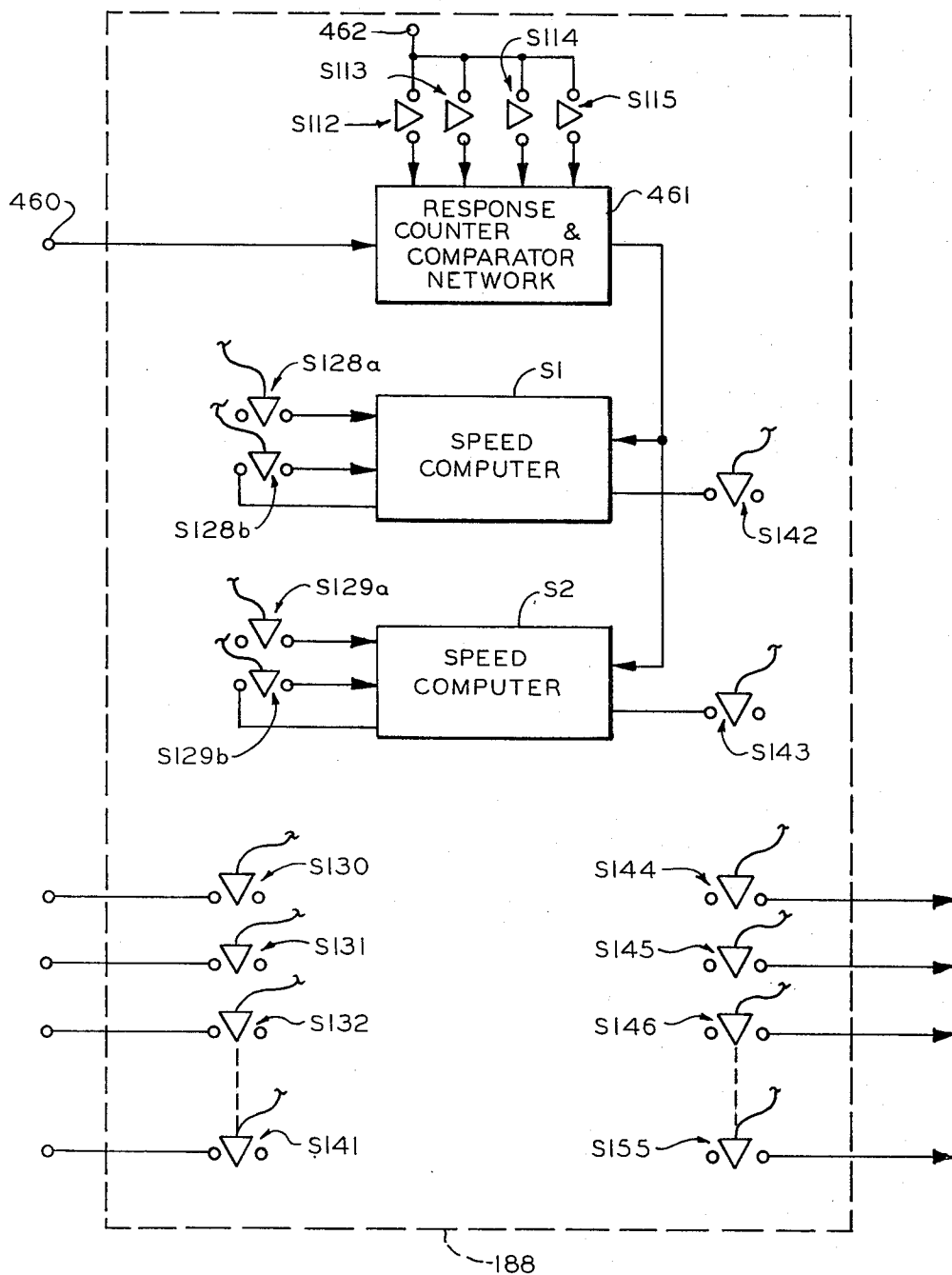
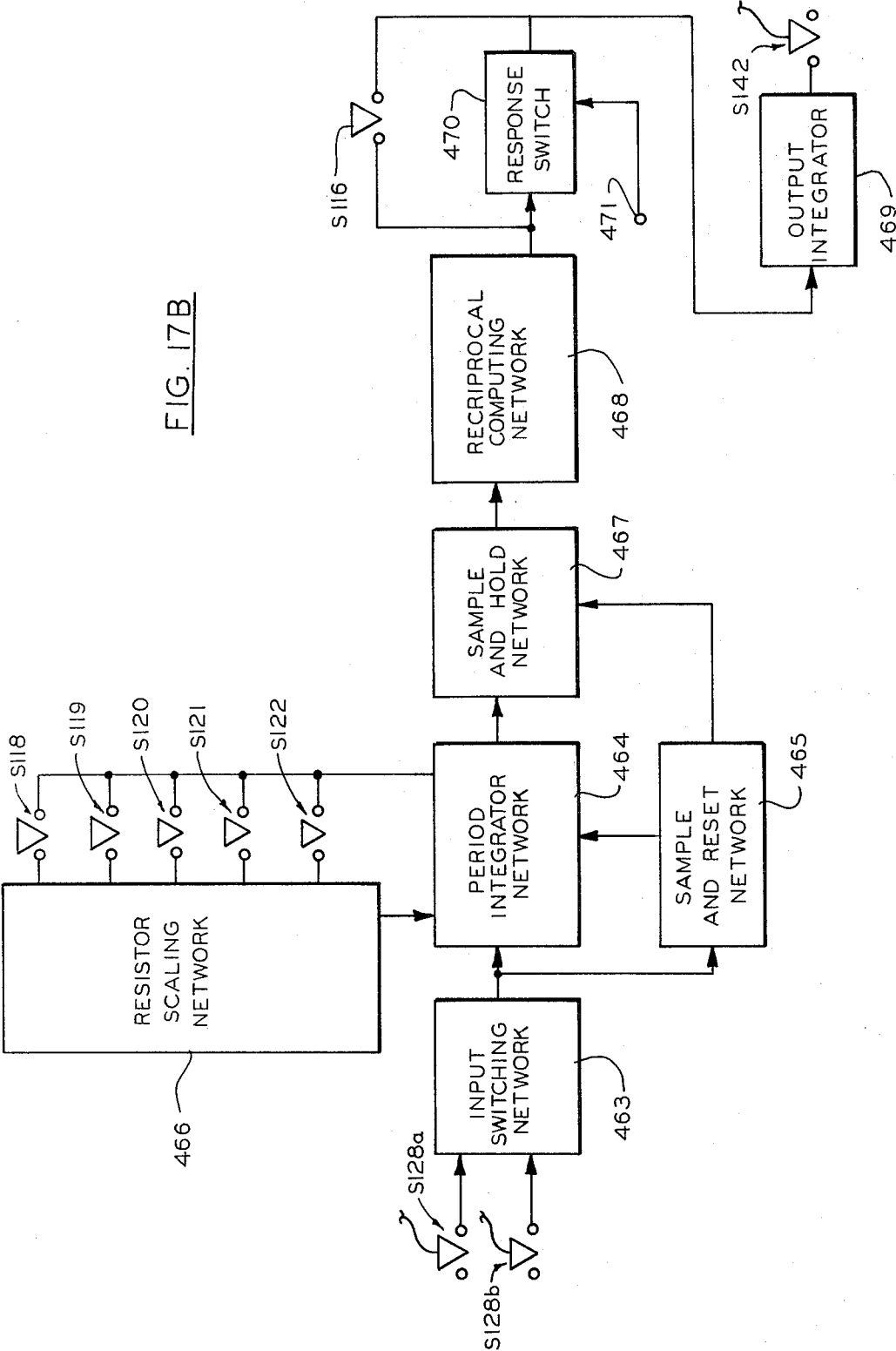


FIG. 17A

FIG. 17B



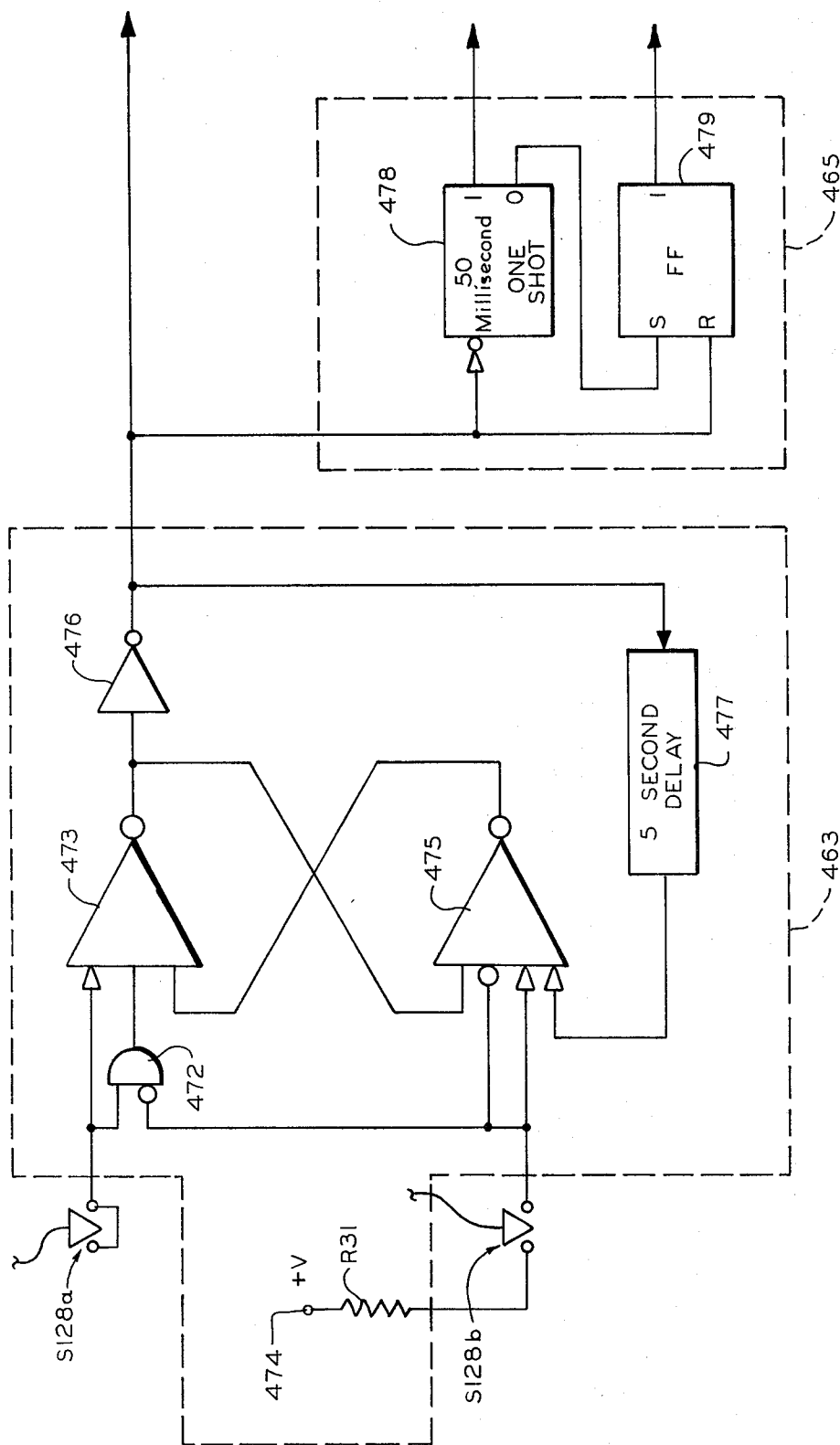


FIG. 17C

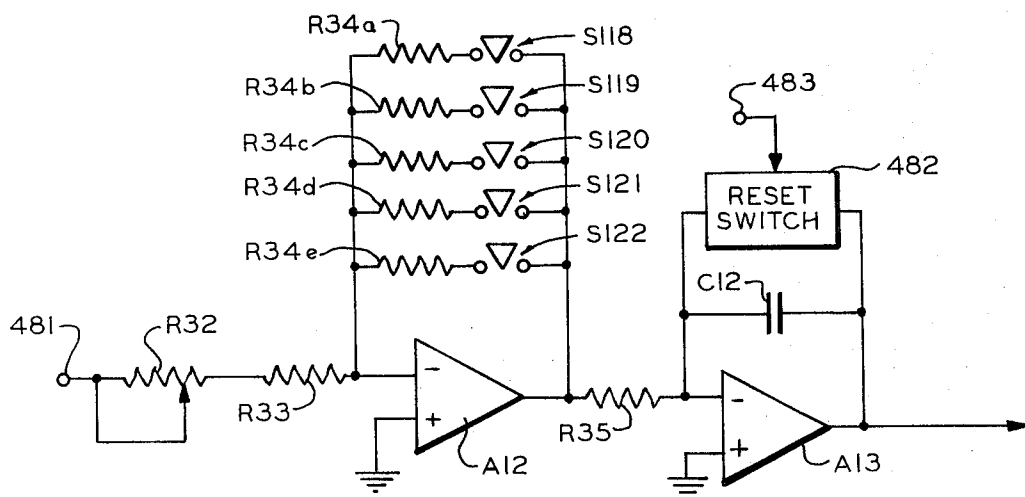


FIG. 17D

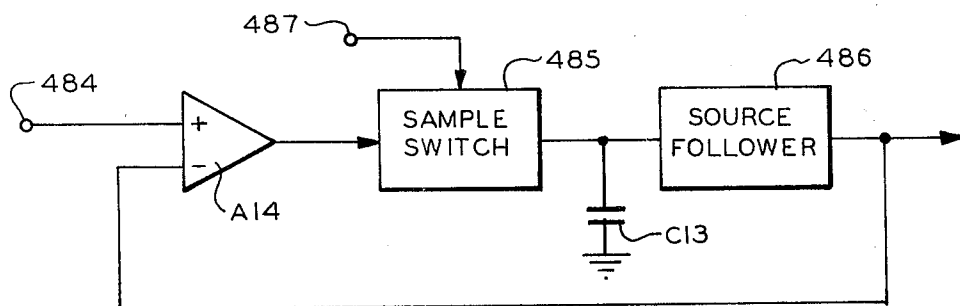


FIG. 17E

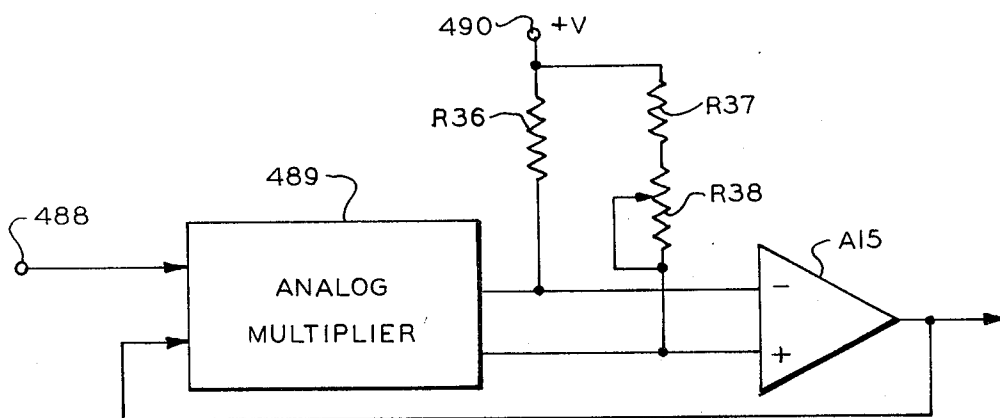


FIG. 17F

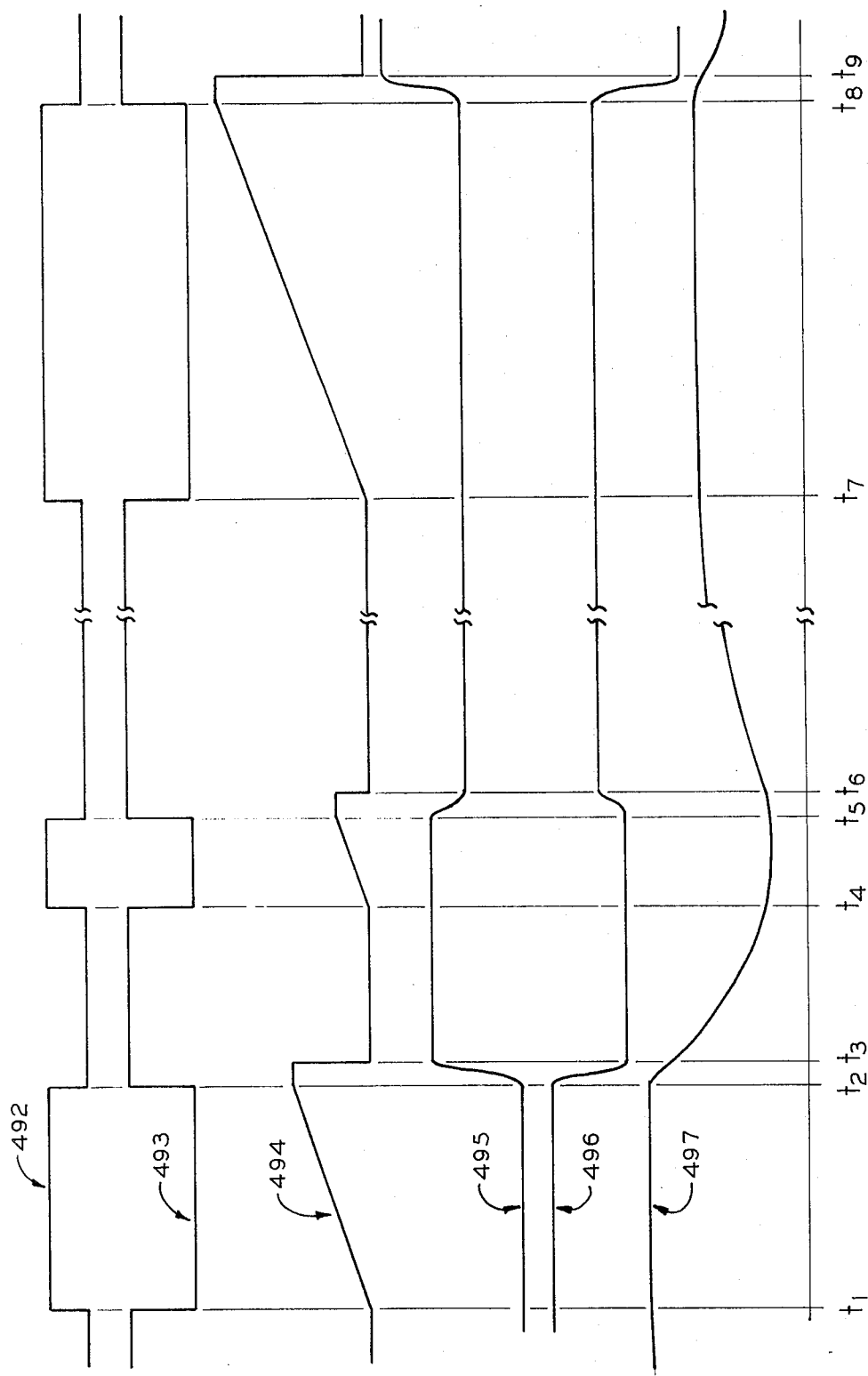
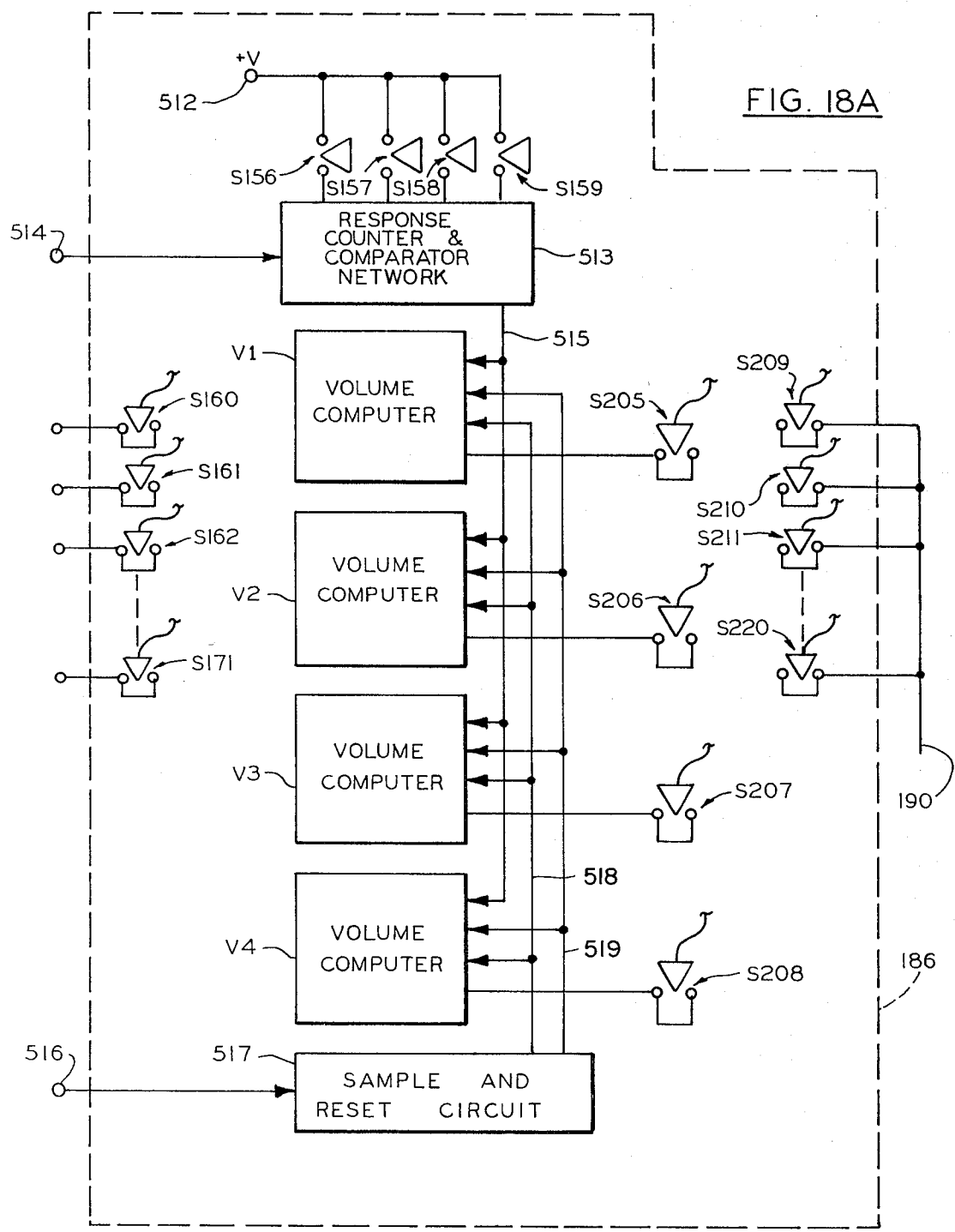


FIG. 17G

FIG. 18A



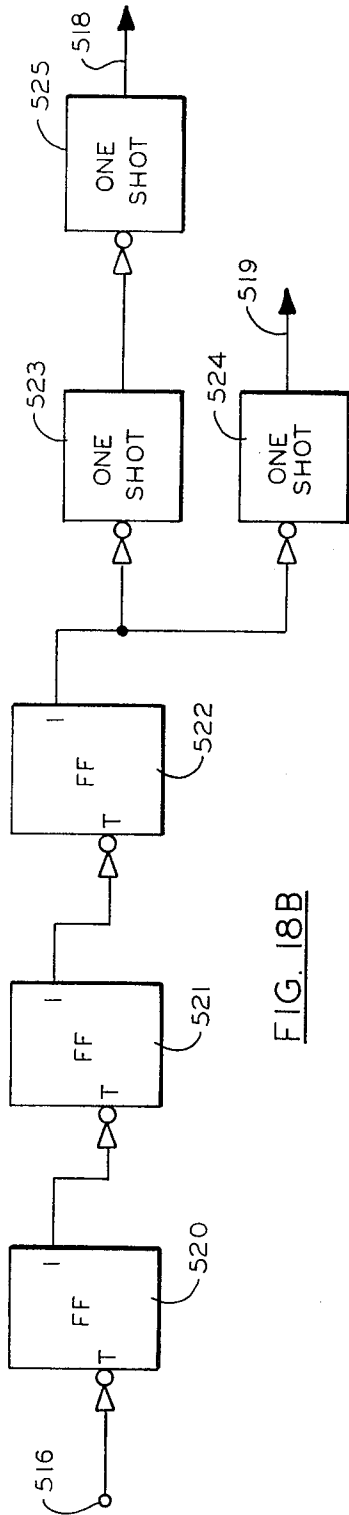


FIG. 18B

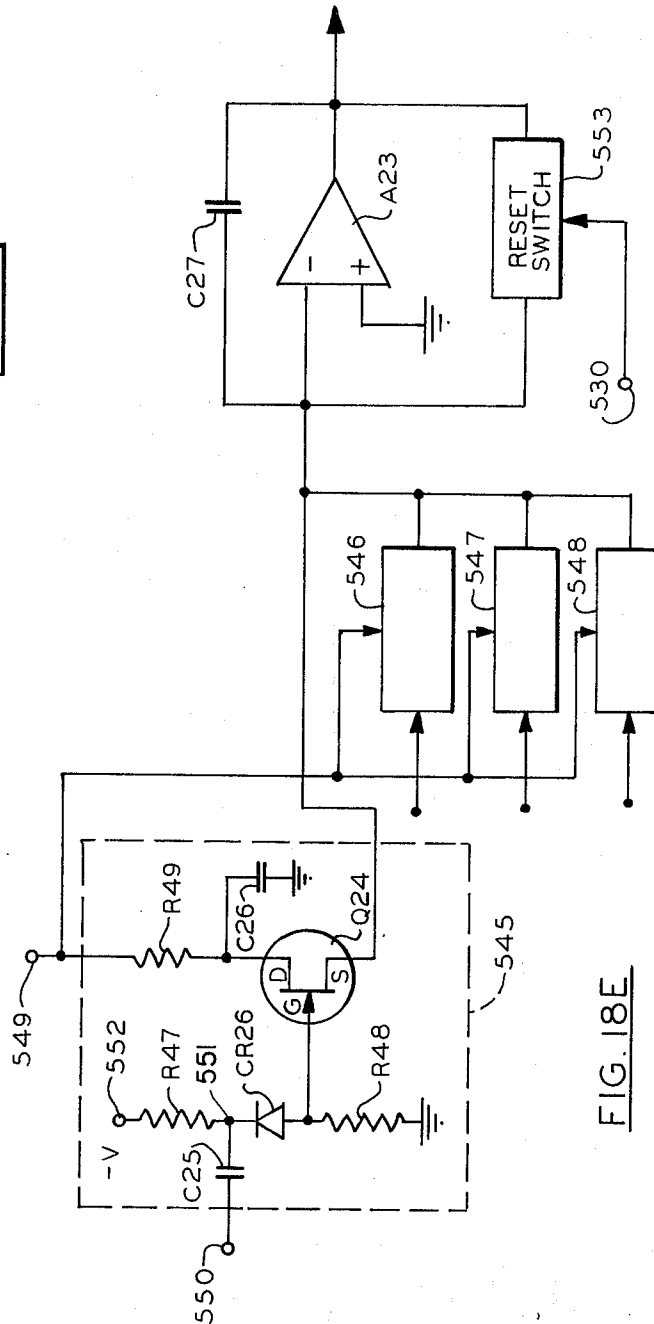


FIG. 18E

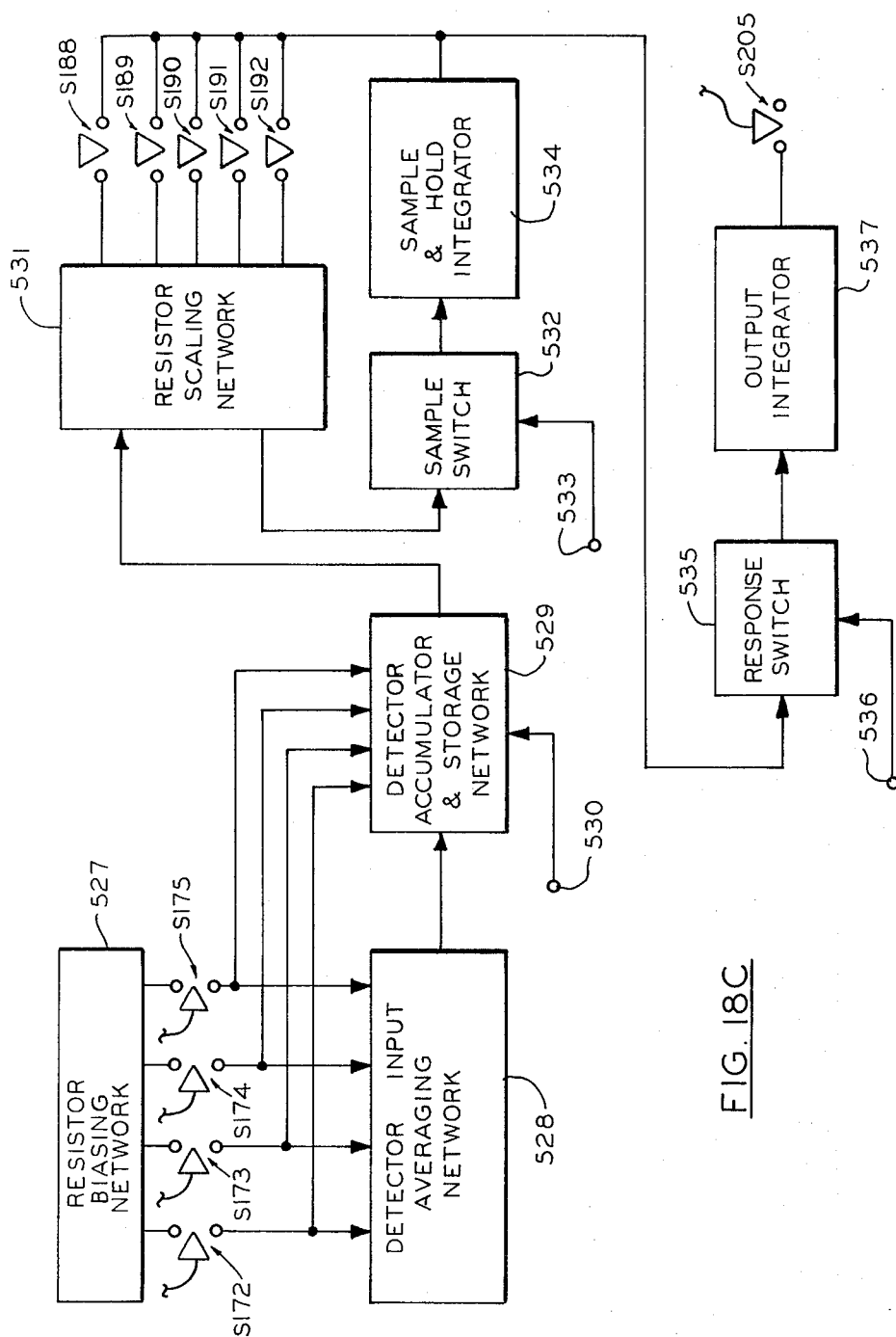


FIG. 18C

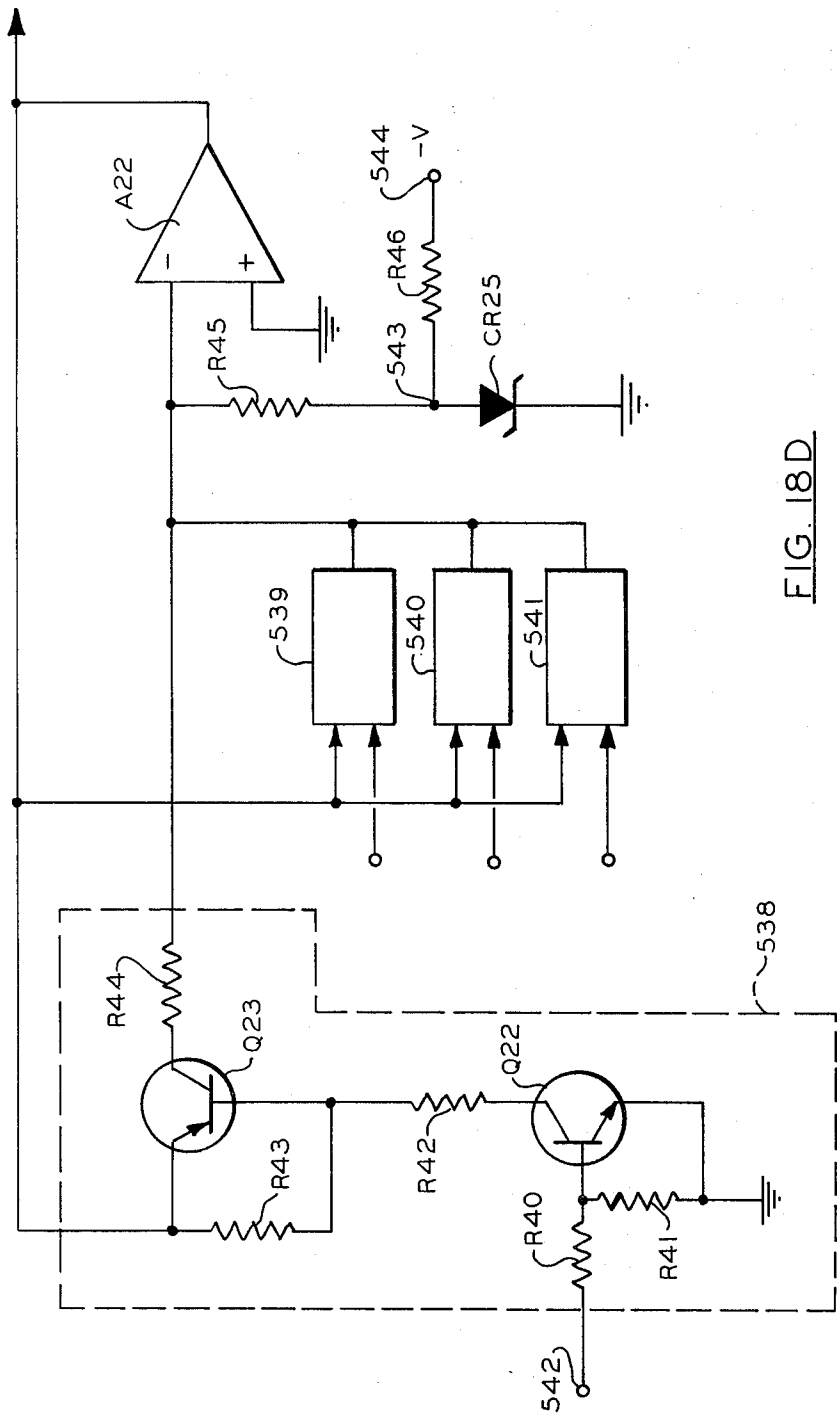


FIG. 18D

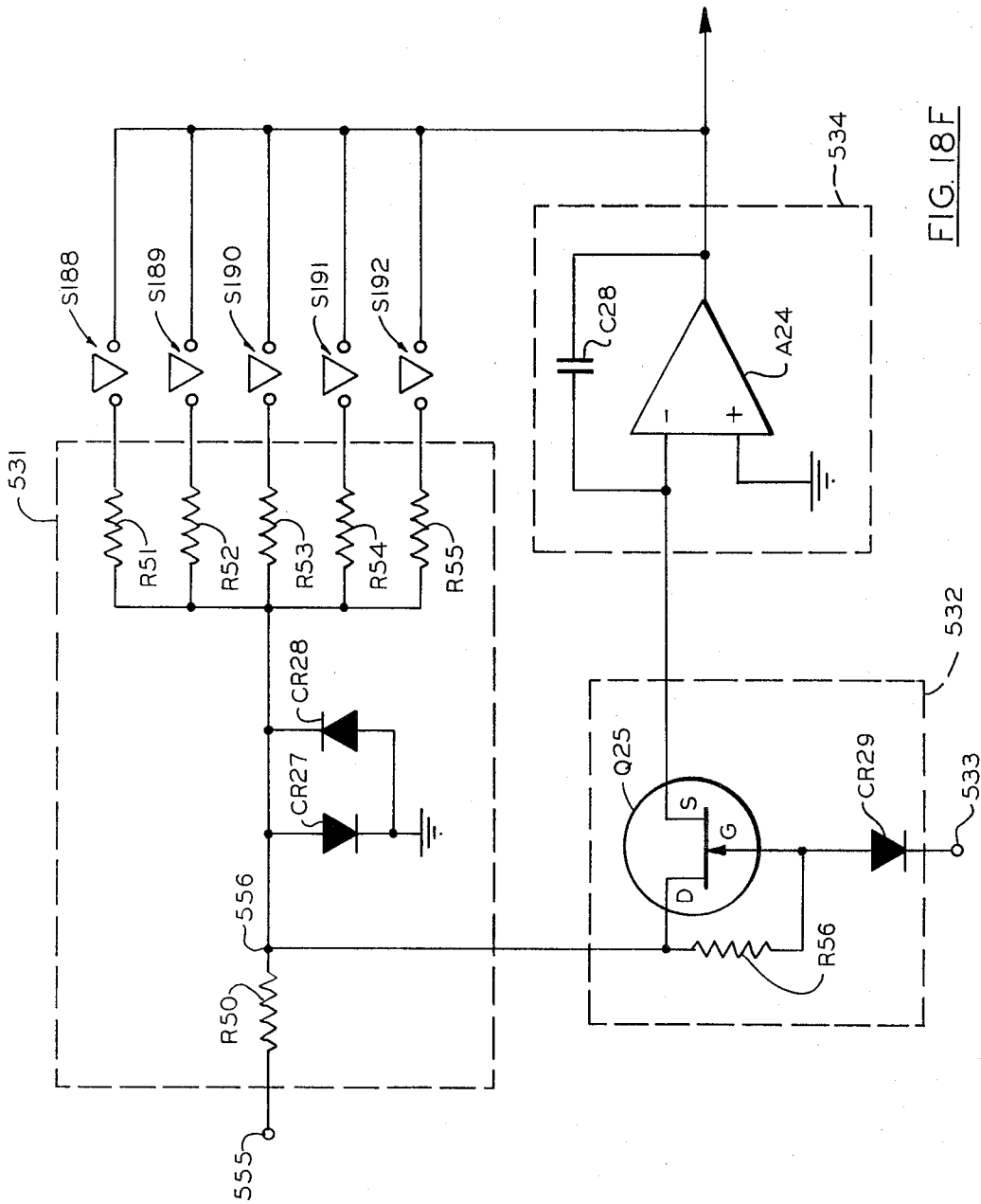


FIG. 18F

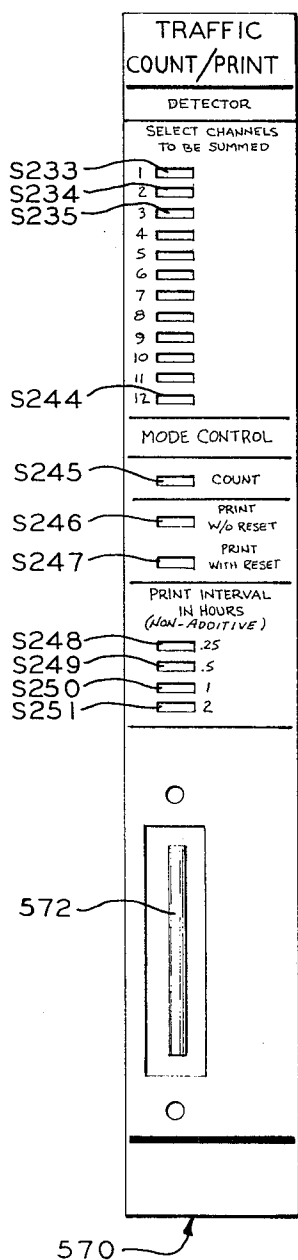


FIG. 19

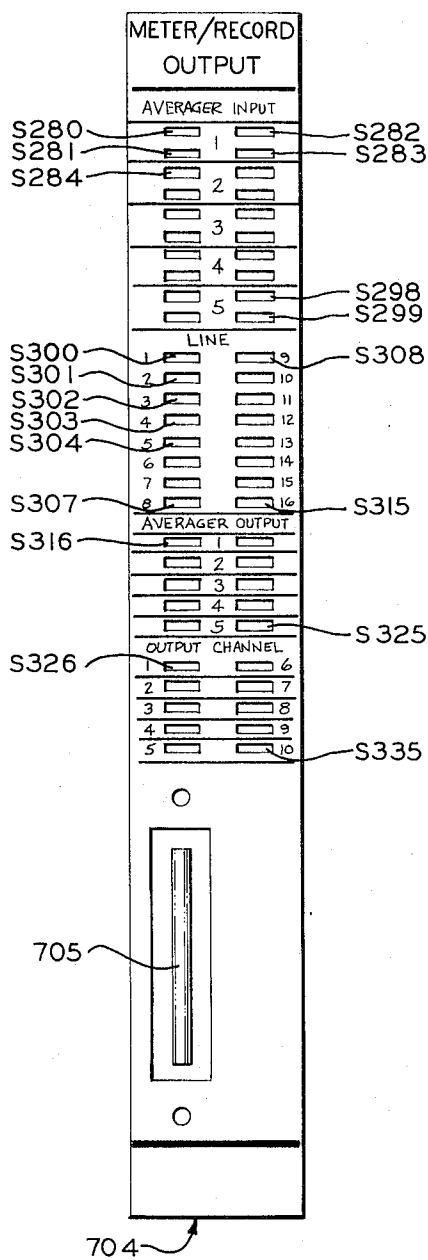


FIG. 28

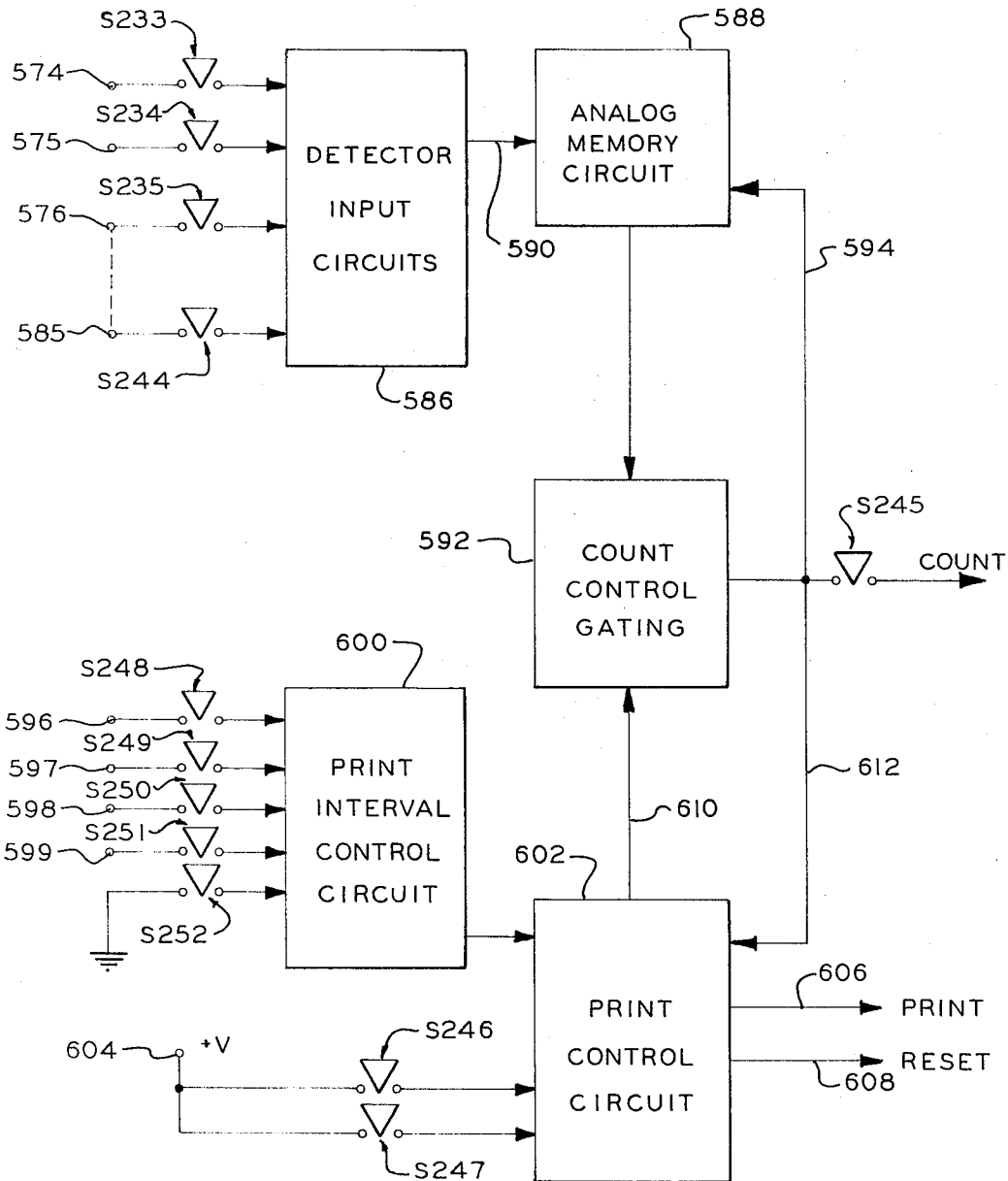


FIG. 20

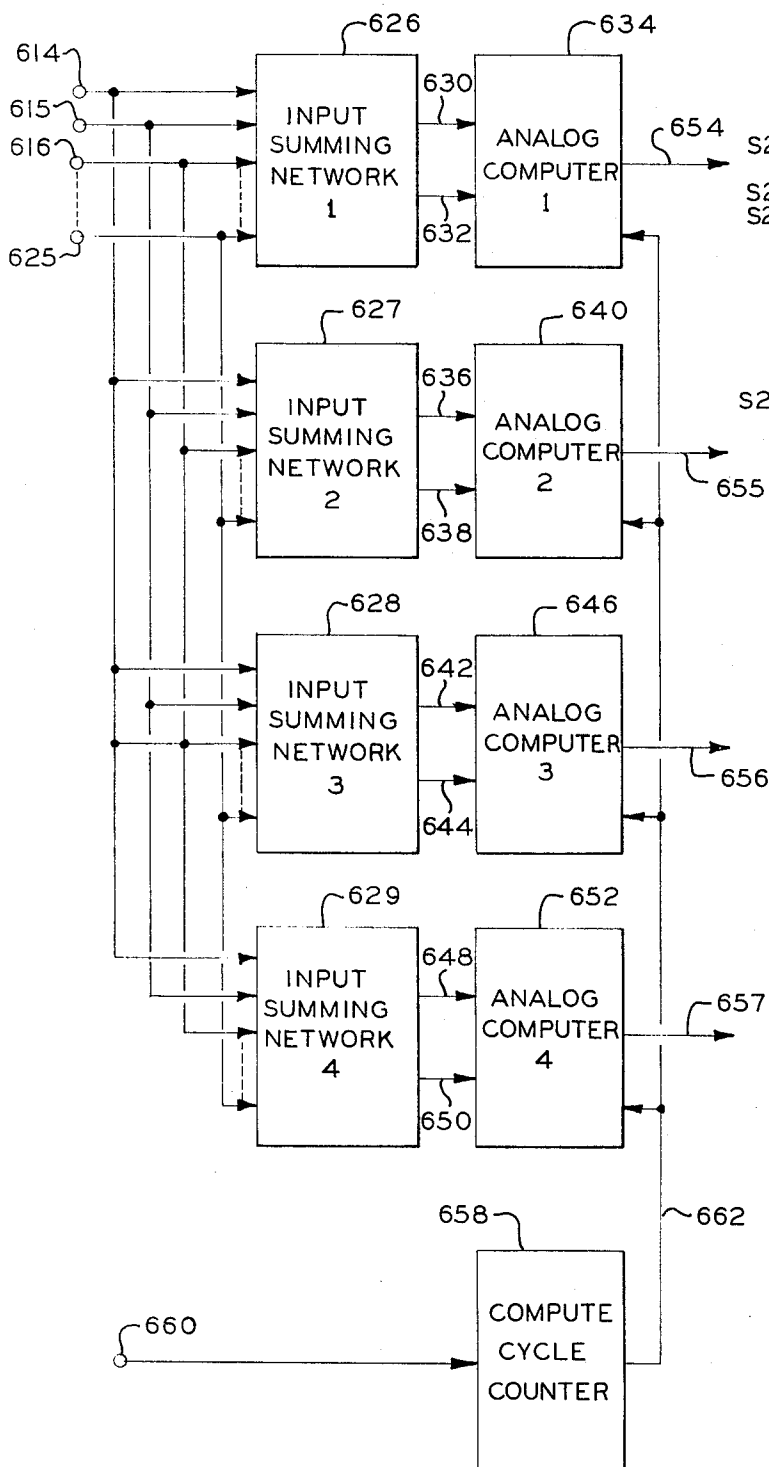


FIG. 22

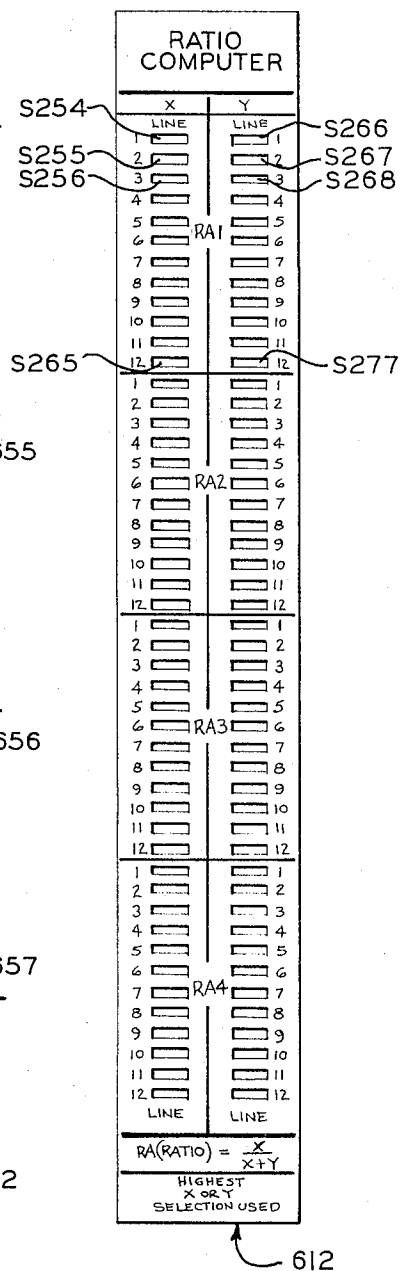


FIG. 21

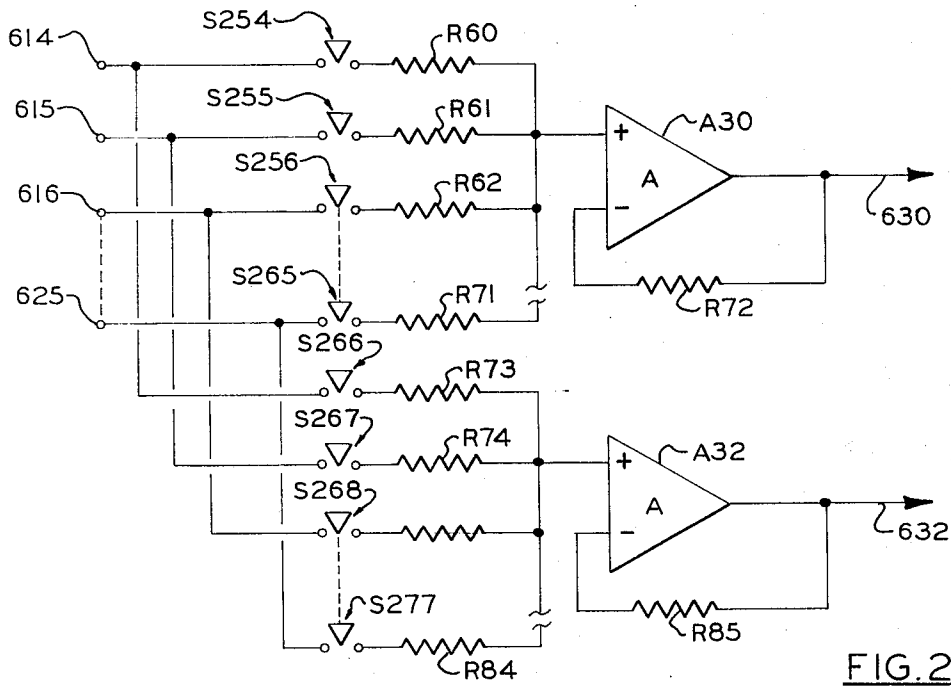


FIG. 23

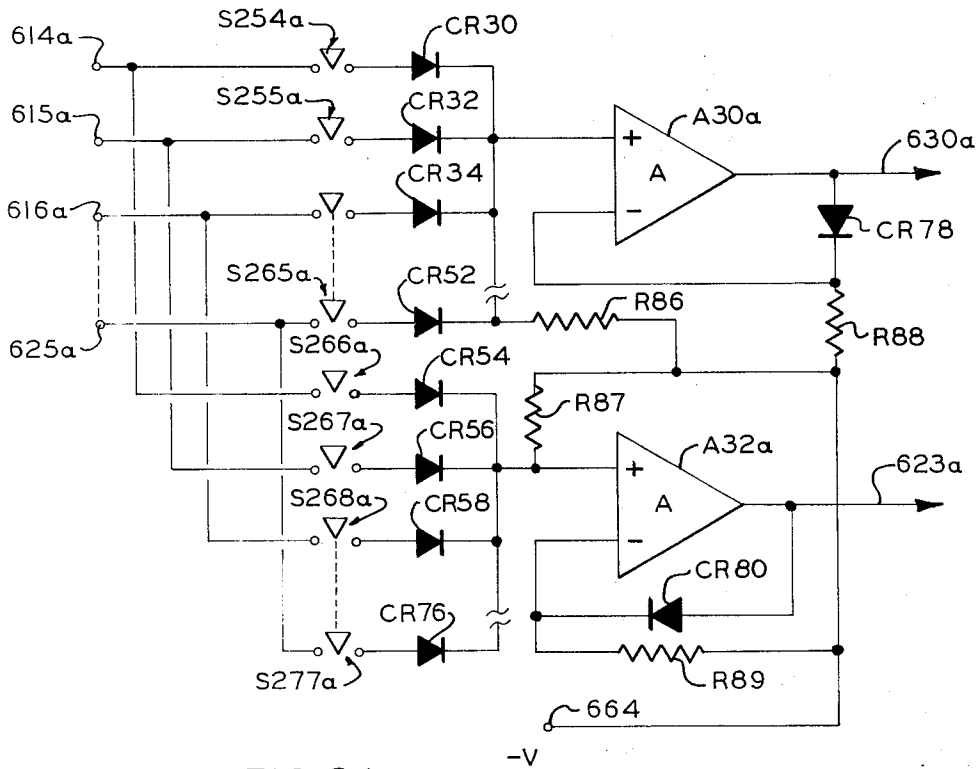


FIG. 24

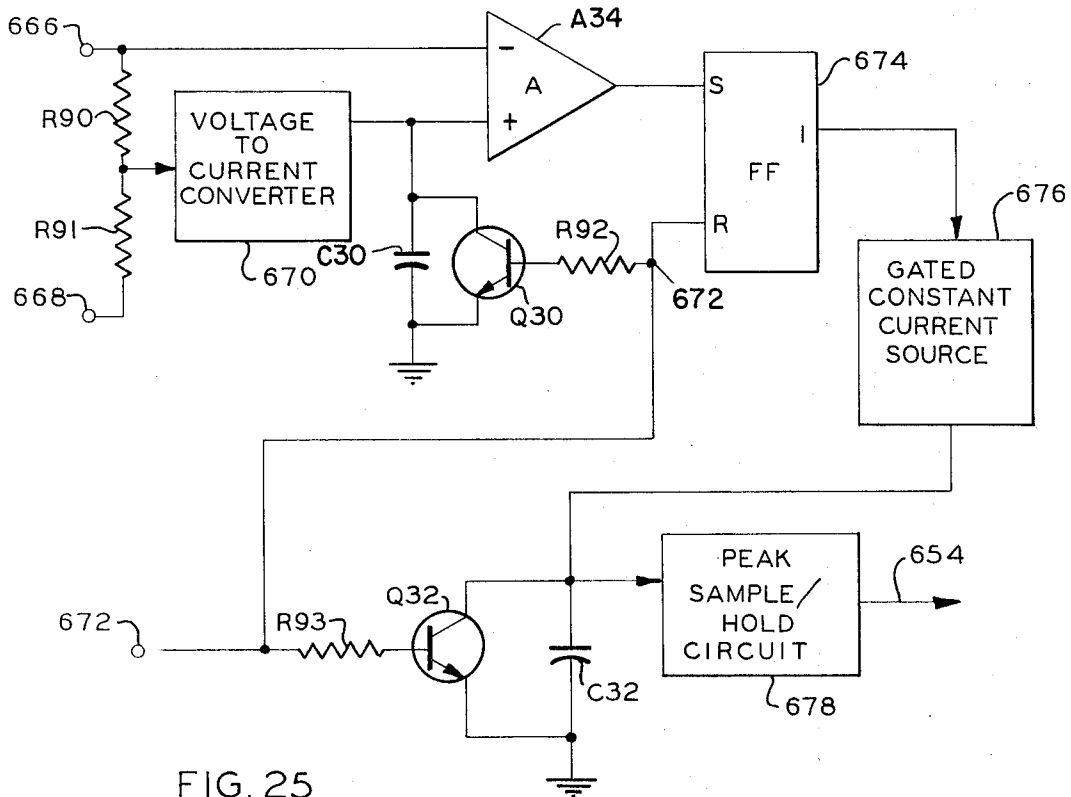


FIG. 25

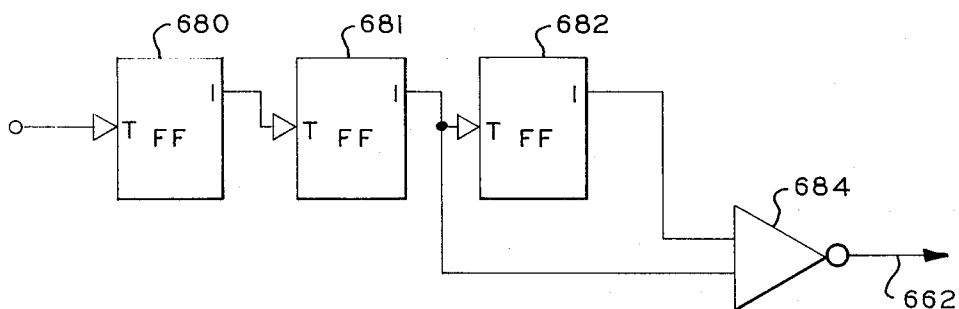


FIG. 26

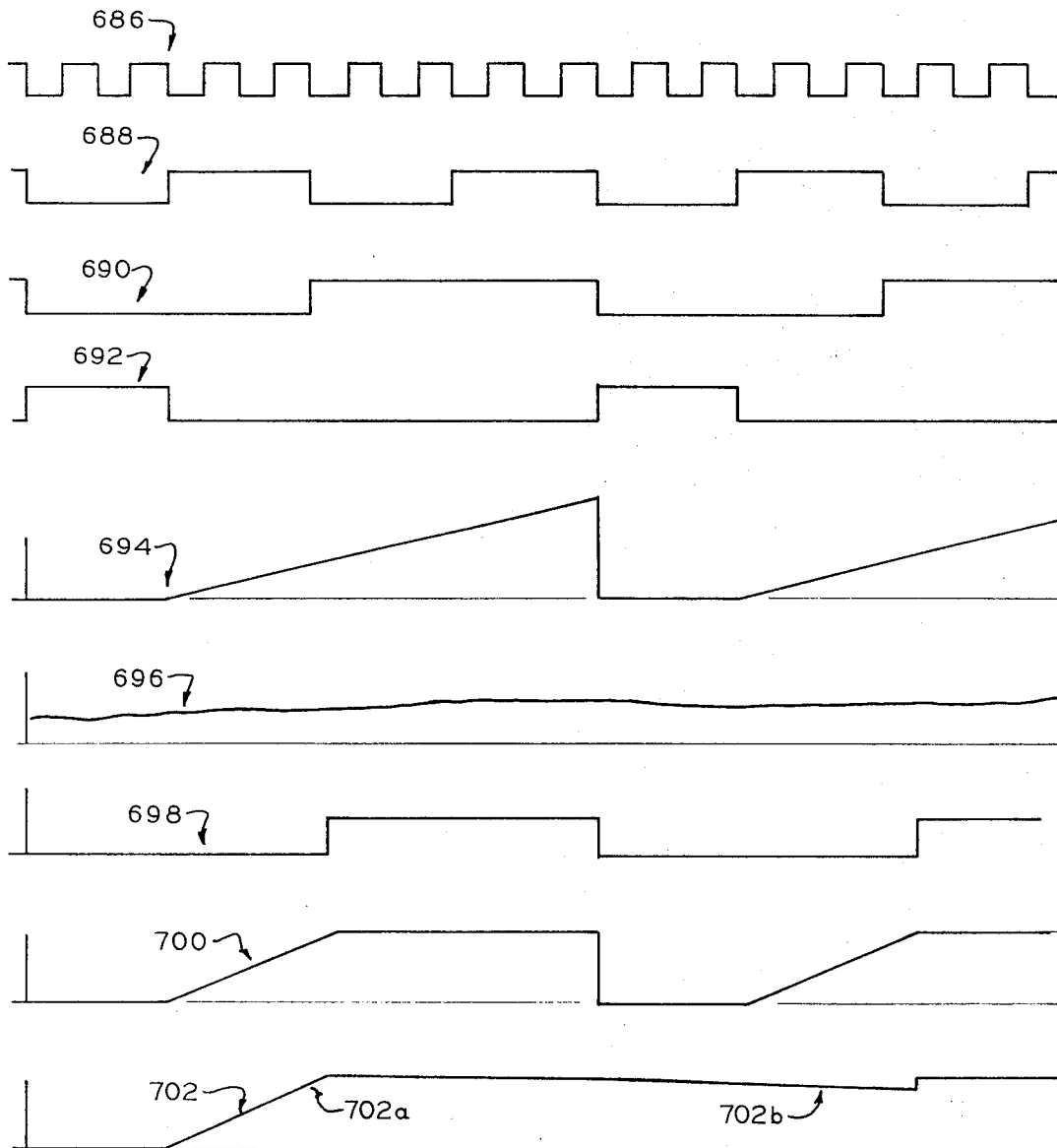


FIG. 27

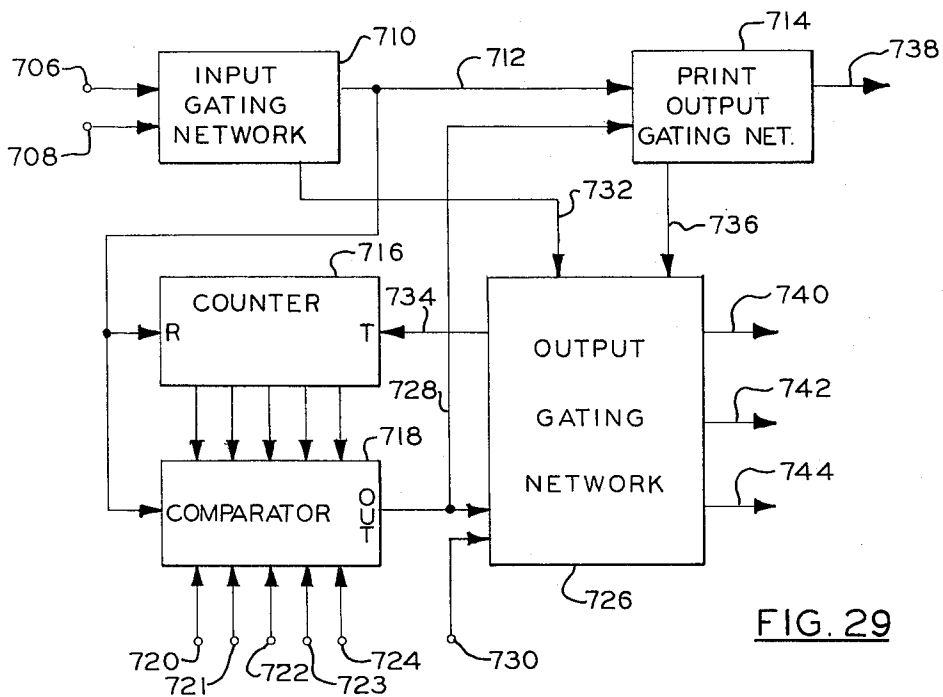


FIG. 29

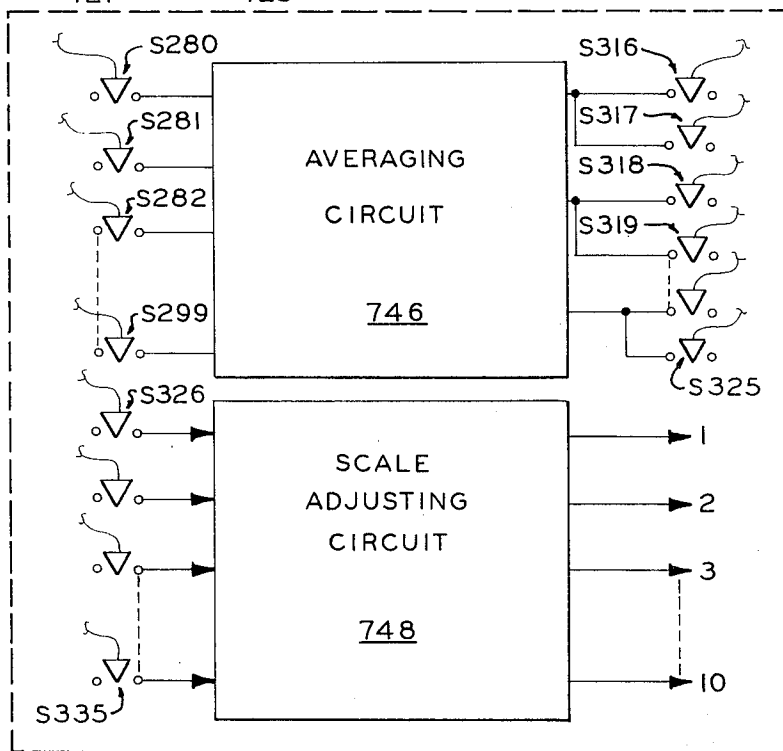
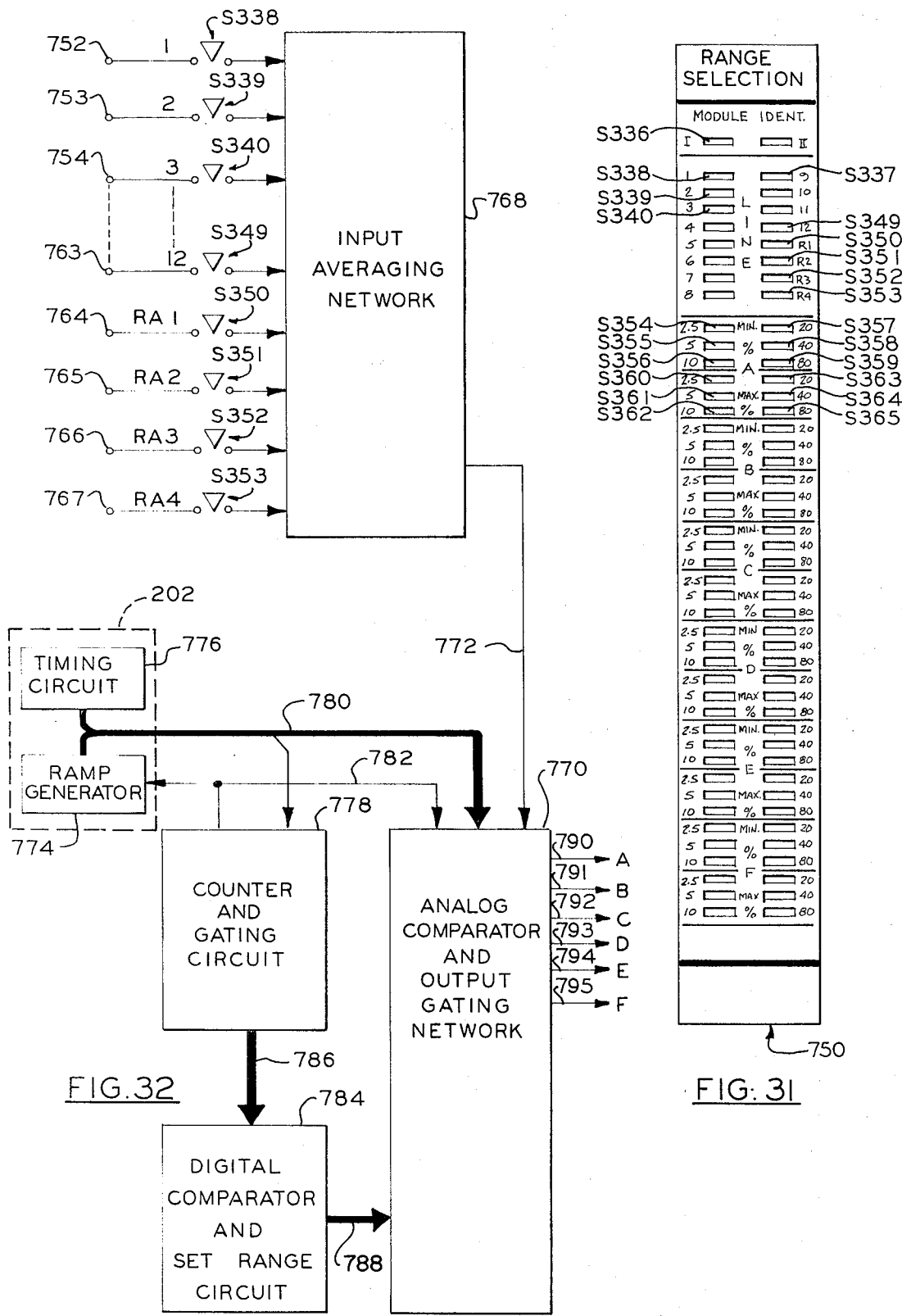
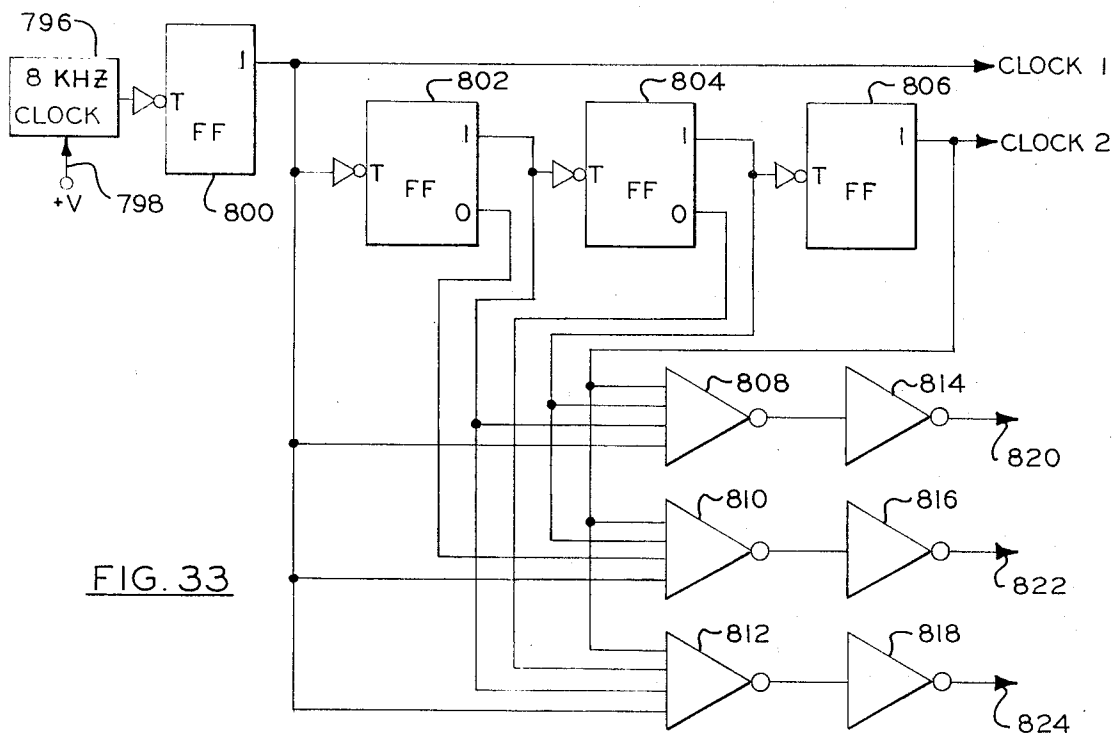
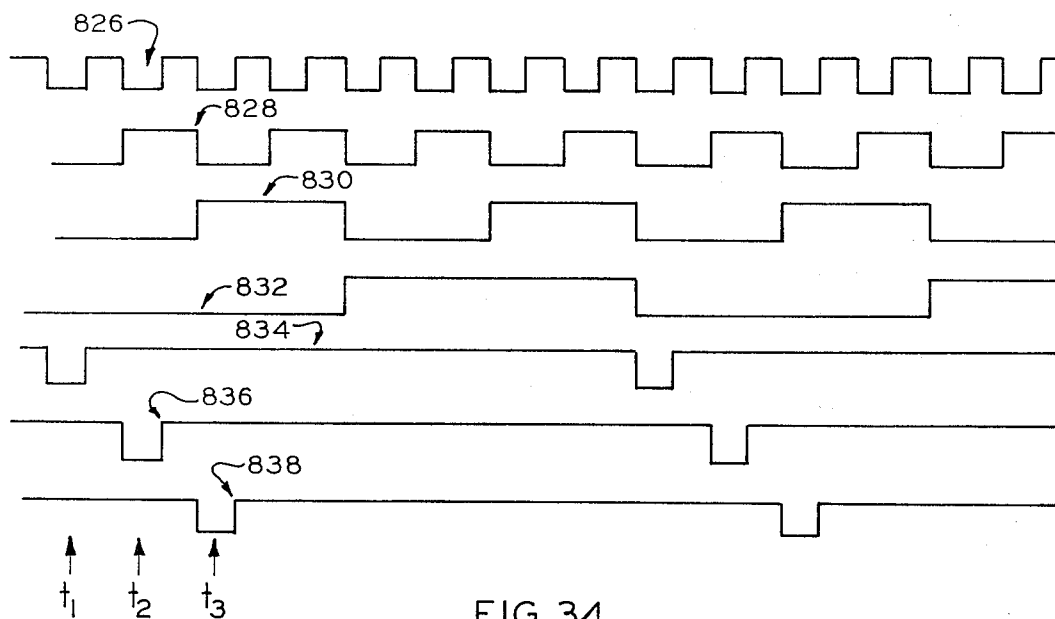
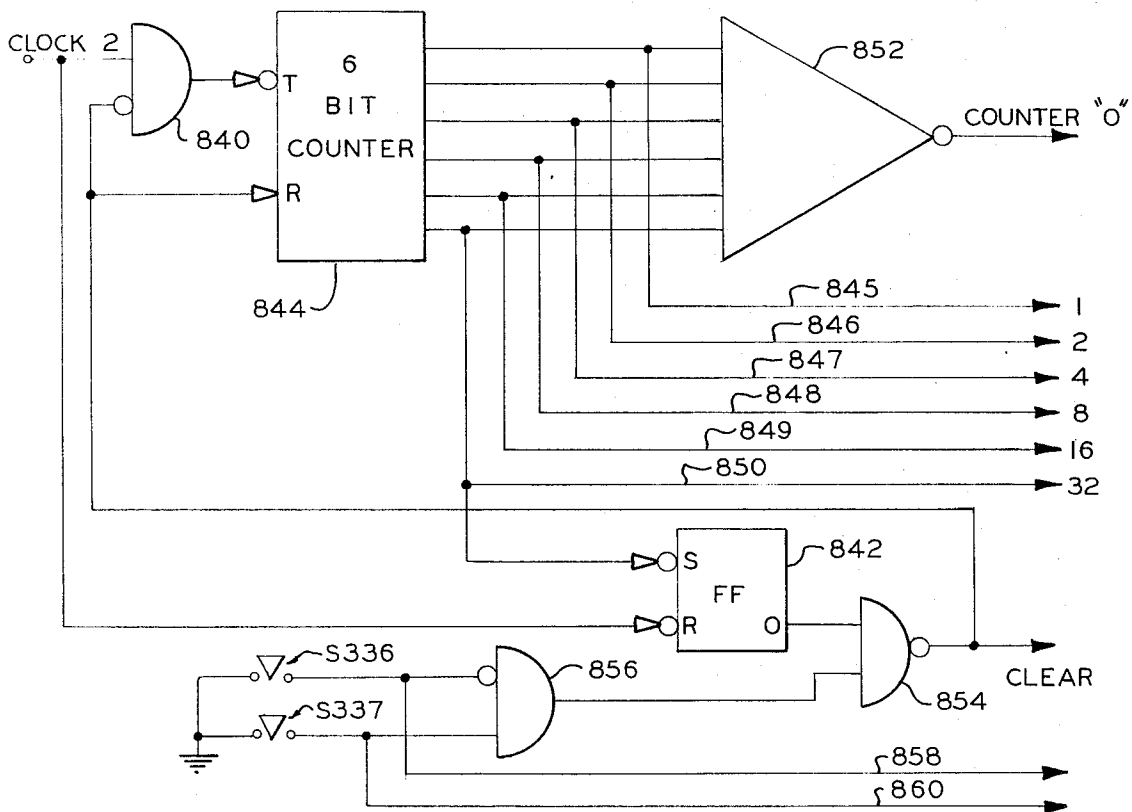
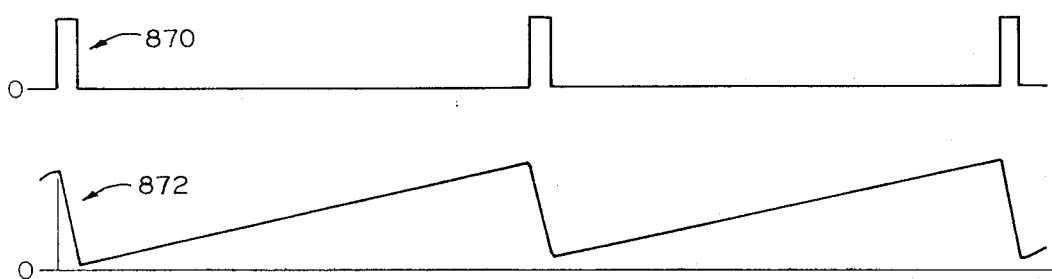
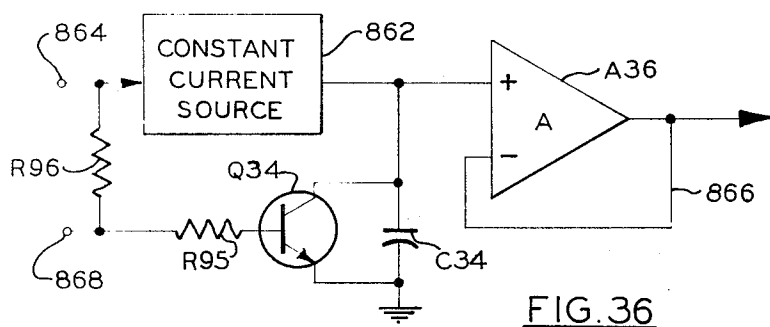
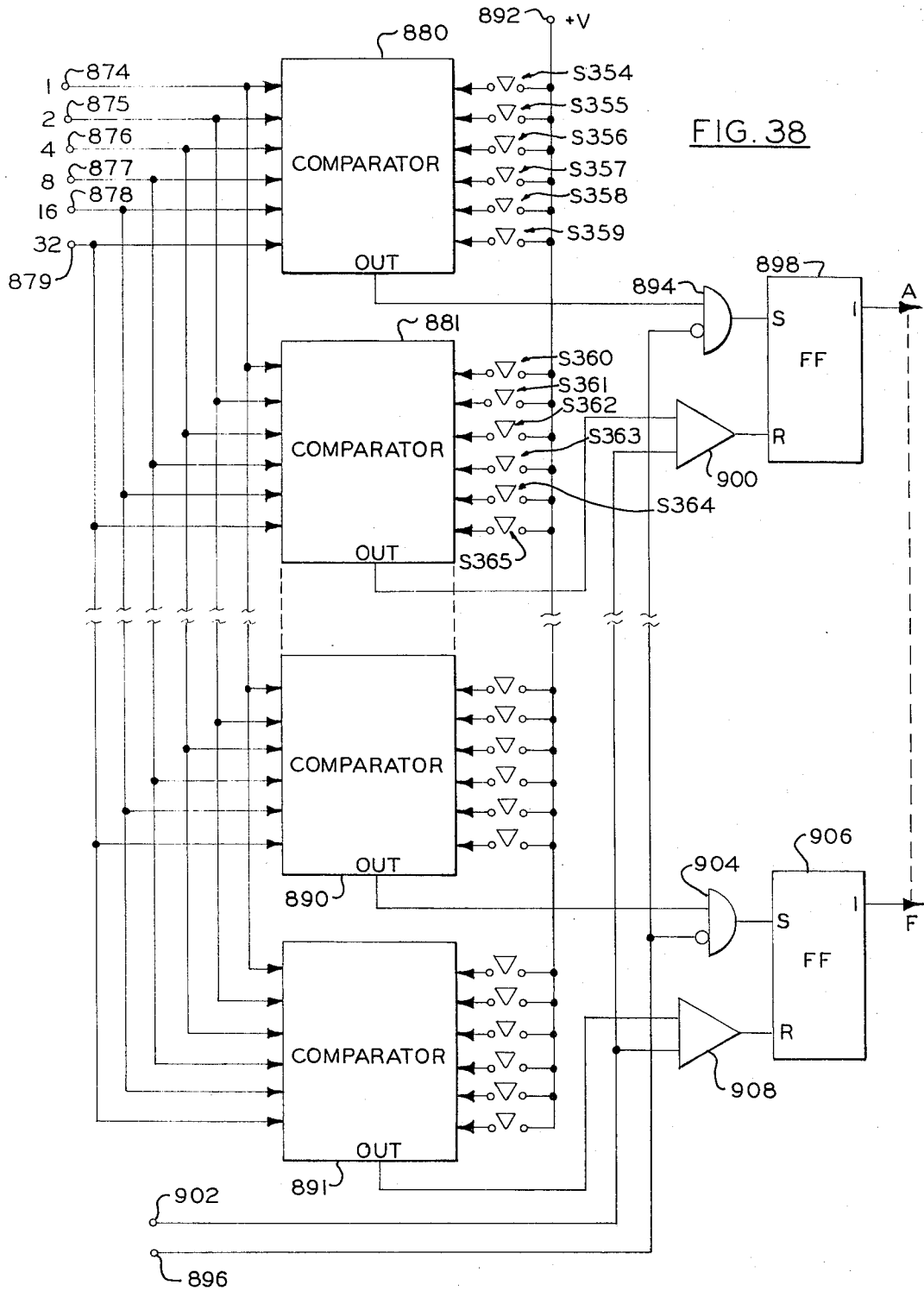


FIG. 30









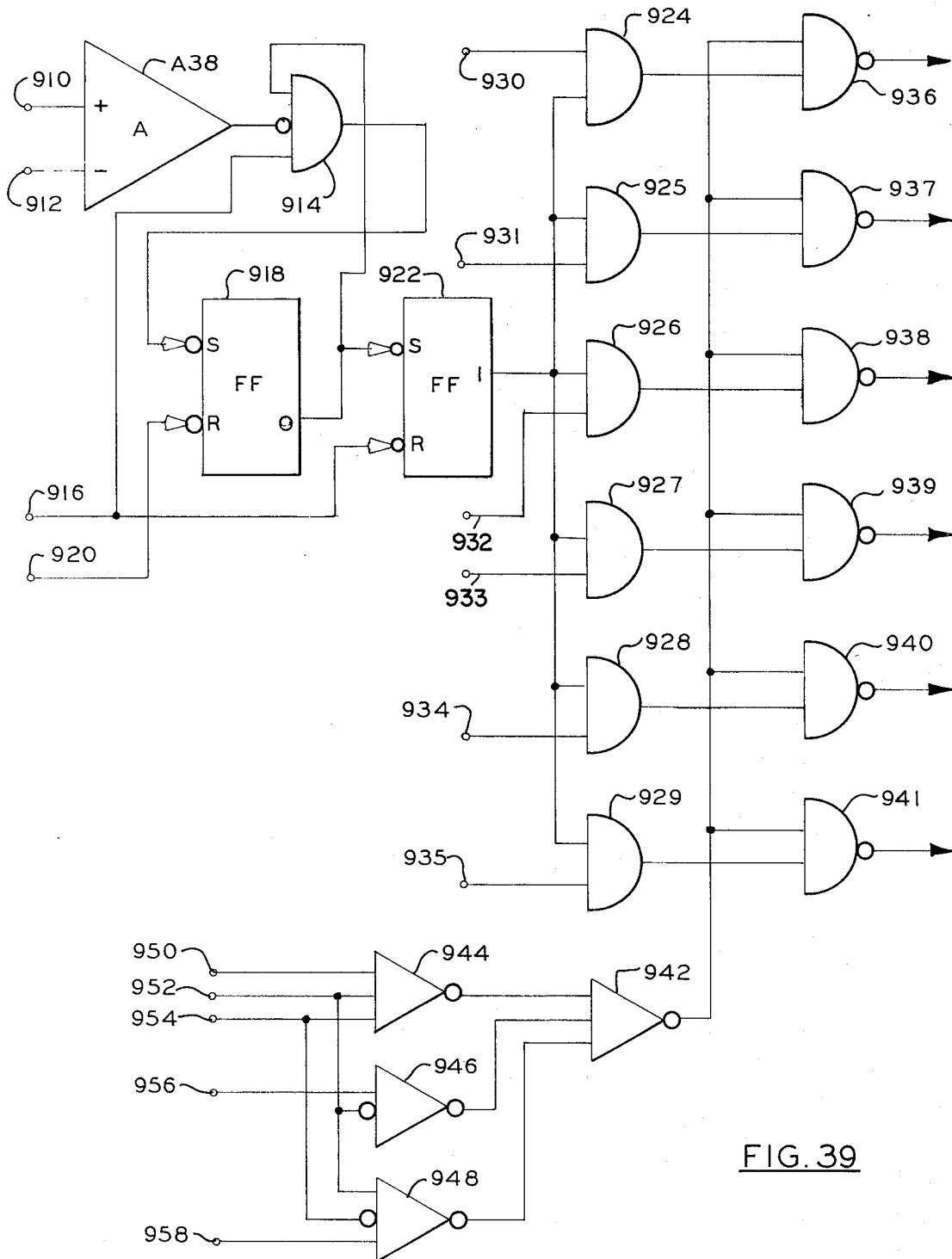


FIG. 39

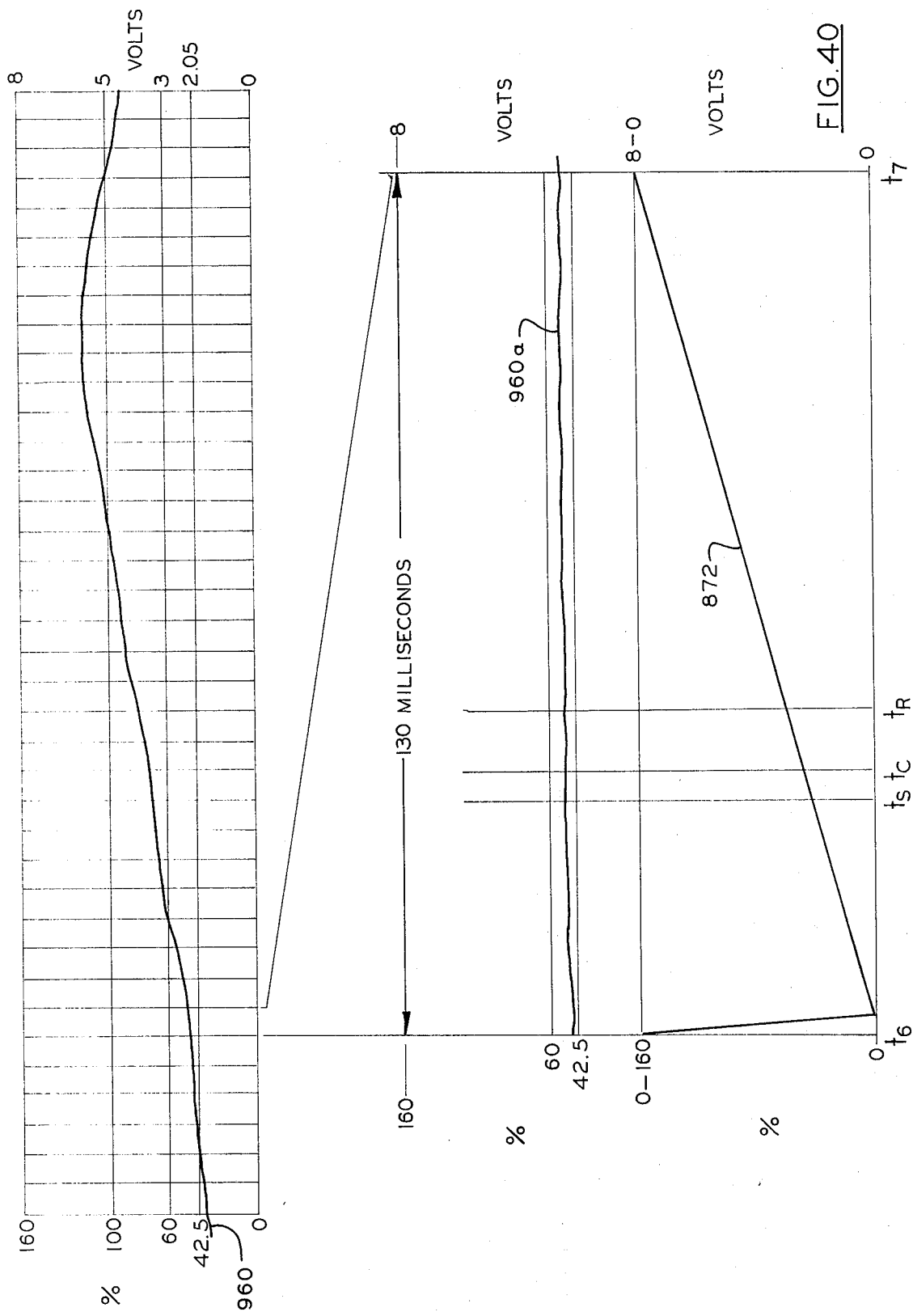


FIG. 40

PROGRAM RANGE SELECTION

SELECT

S438

A

PROGRAMS

S439

B

S440

TI

OVERIDE DURING

T3

S442

S441

T2

T4

S443

S444

A

MINIMUM PROGRAM INTERVAL

S445

B

PROGRAM NUMBER

4

S448

S446

1

8

S449

S447

2

16

S450

RANGES

A

D

S454

S451

B

I

E

S455

S452

C

F

S456

S457

A

D

S458

B

II

E

S459

C

F

S460

A

D

S462

S461

B

III

E

S463

C

F

S468

S464

S465

PROGRAM NUMBER

4

1

8

2

16

RANGES

A

D

B

I

E

C

F

A

D

B

II

E

C

F

A

D

B

III

E

C

F

1172

FIG. 52

PROGRAM TIME SELECTION

DAY

S370

MON

FRI

S374

S371

TUE

SAT

S375

S372

WED

SUN

S376

S373

THU

TIME (HR)

PROG. NO

S377

25

1

S384

S378

5

2

S385

S379

1

4

S386

S380

2

8

S387

S381

4

16

S388

S382

8

A

S389

S383

PM

B

S390

S391

T1

START

T3

S393

S392

T2

T4

S394

TIME (HR)

PROG. NO

S395

25

1

S402

S396

5

2

S403

S397

1

4

S404

S398

2

8

S405

S399

4

16

S406

S400

8

A

S407

S401

PM

B

S408

S409

T1

T3

S411

S410

T2

T4

S412

DAY

FRI

MON

SAT

TUE

SUN

WED

THU

TIME (HR)

PROG. NO

S413

25

1

S415

S414

5

2

S416

S417

1

4

S418

2

8

S419

4

16

S420

8

A

S417

PM

B

S418

T1

END

T3

S419

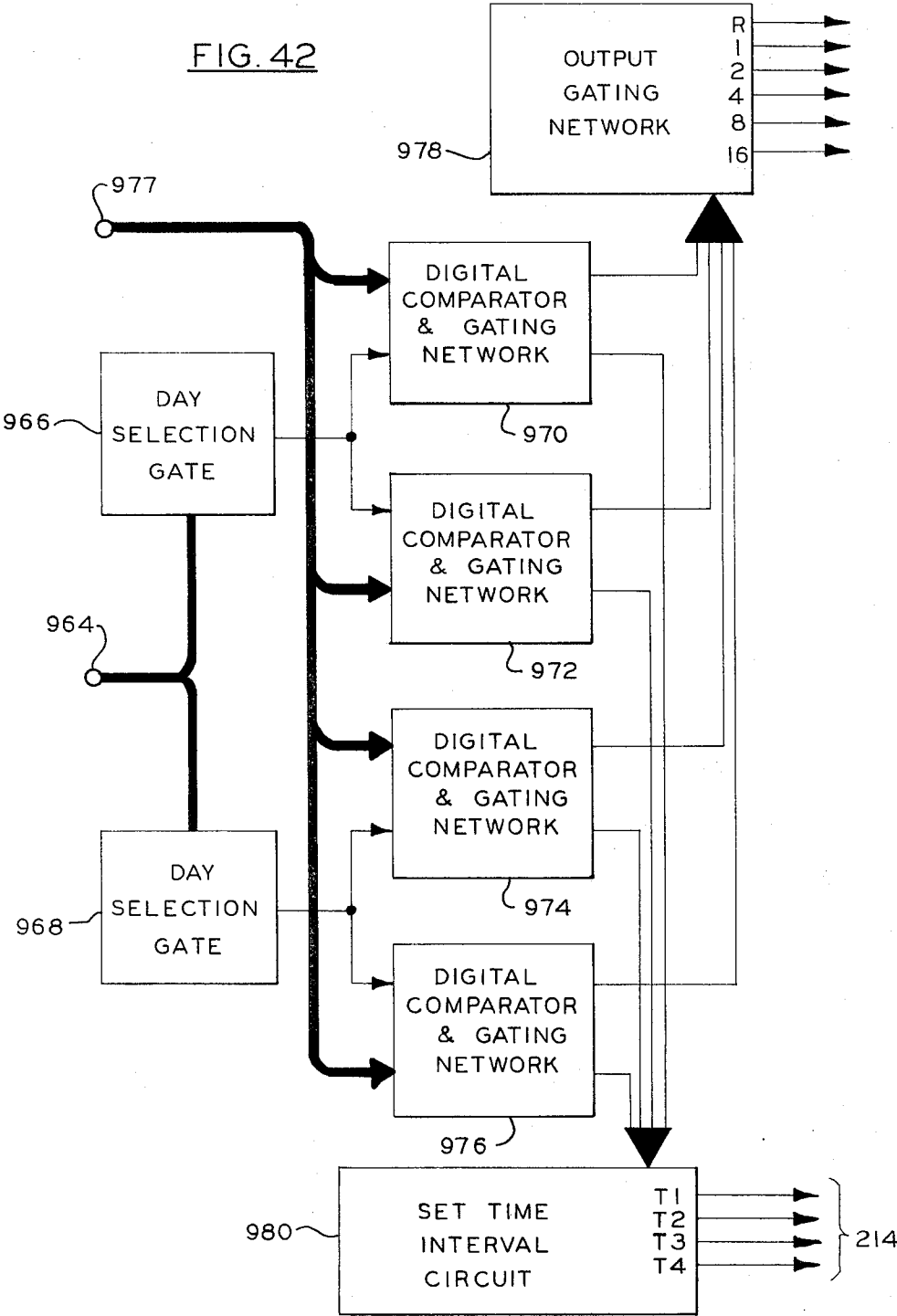
T2

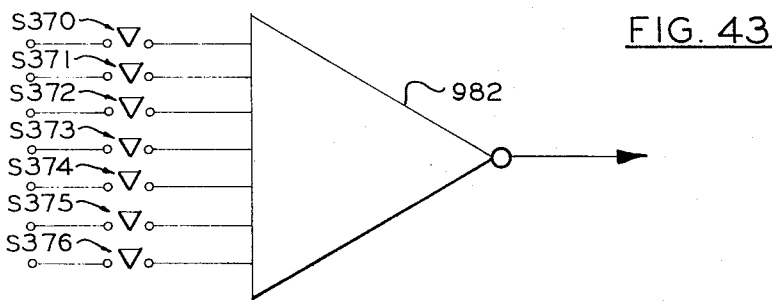
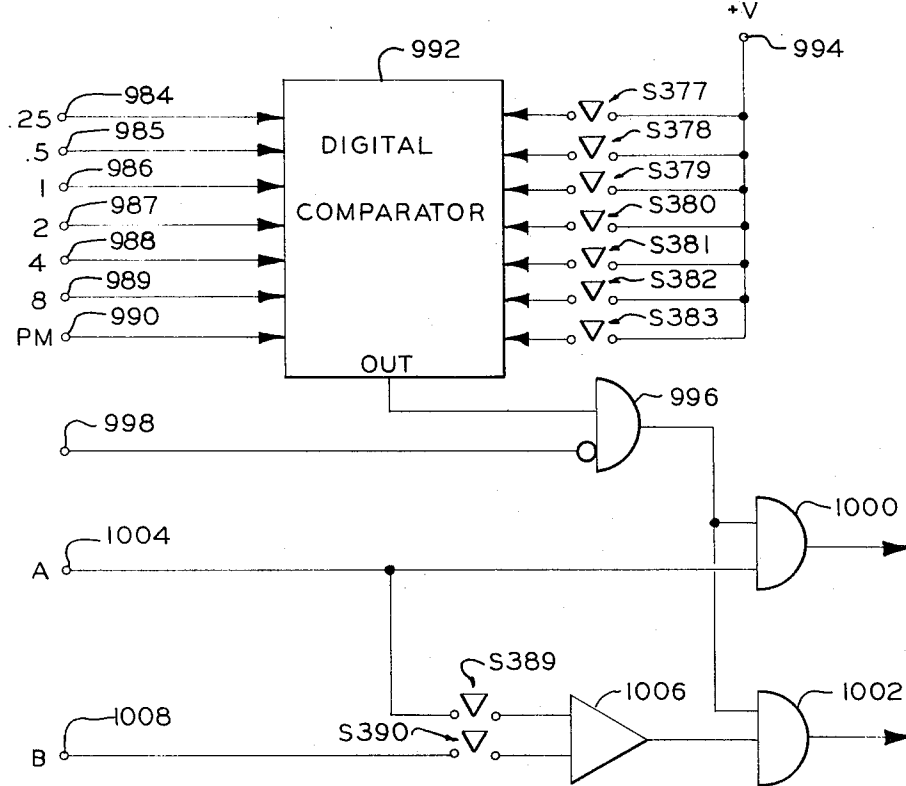
T4

962

FIG. 41

FIG. 42





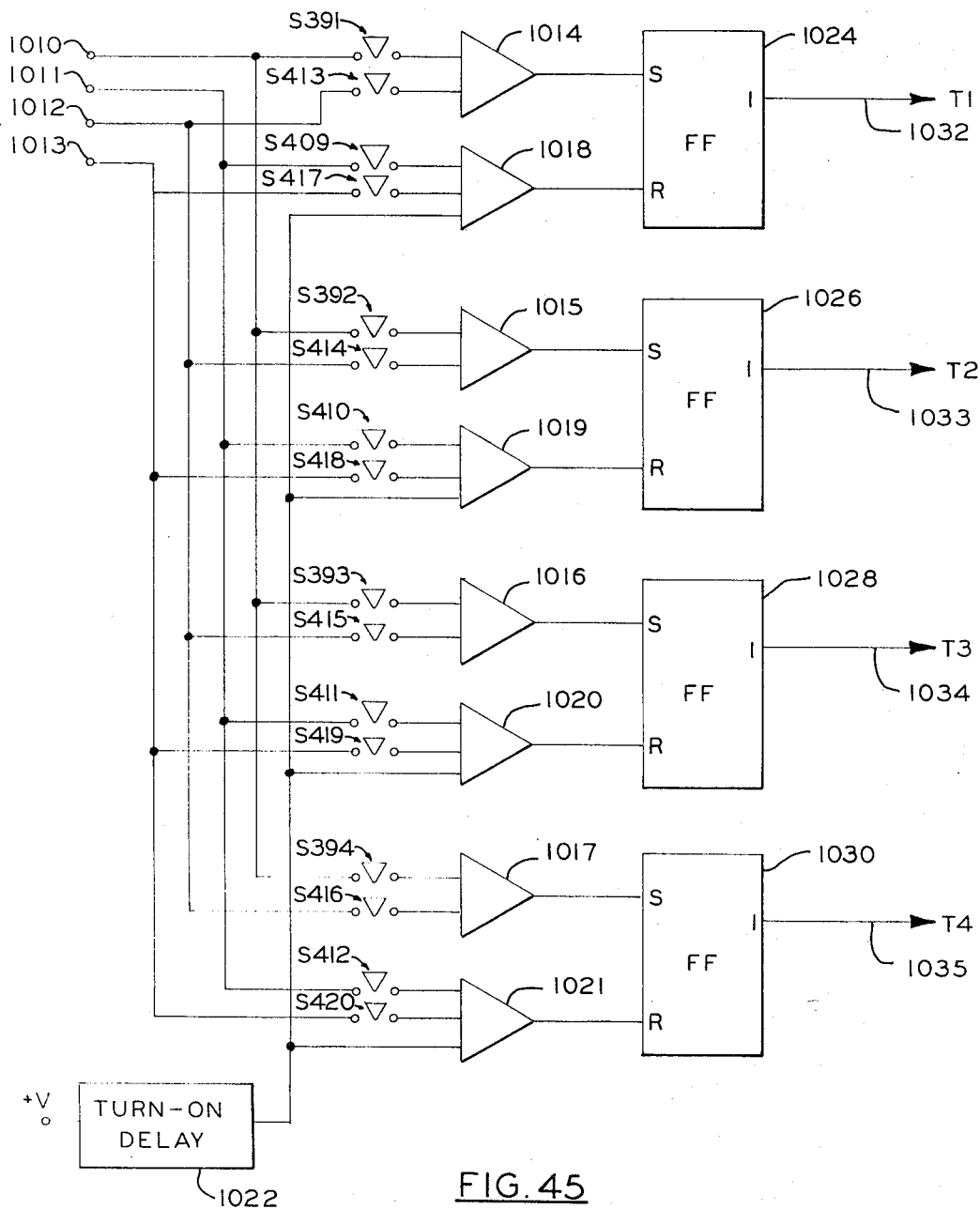


FIG. 45

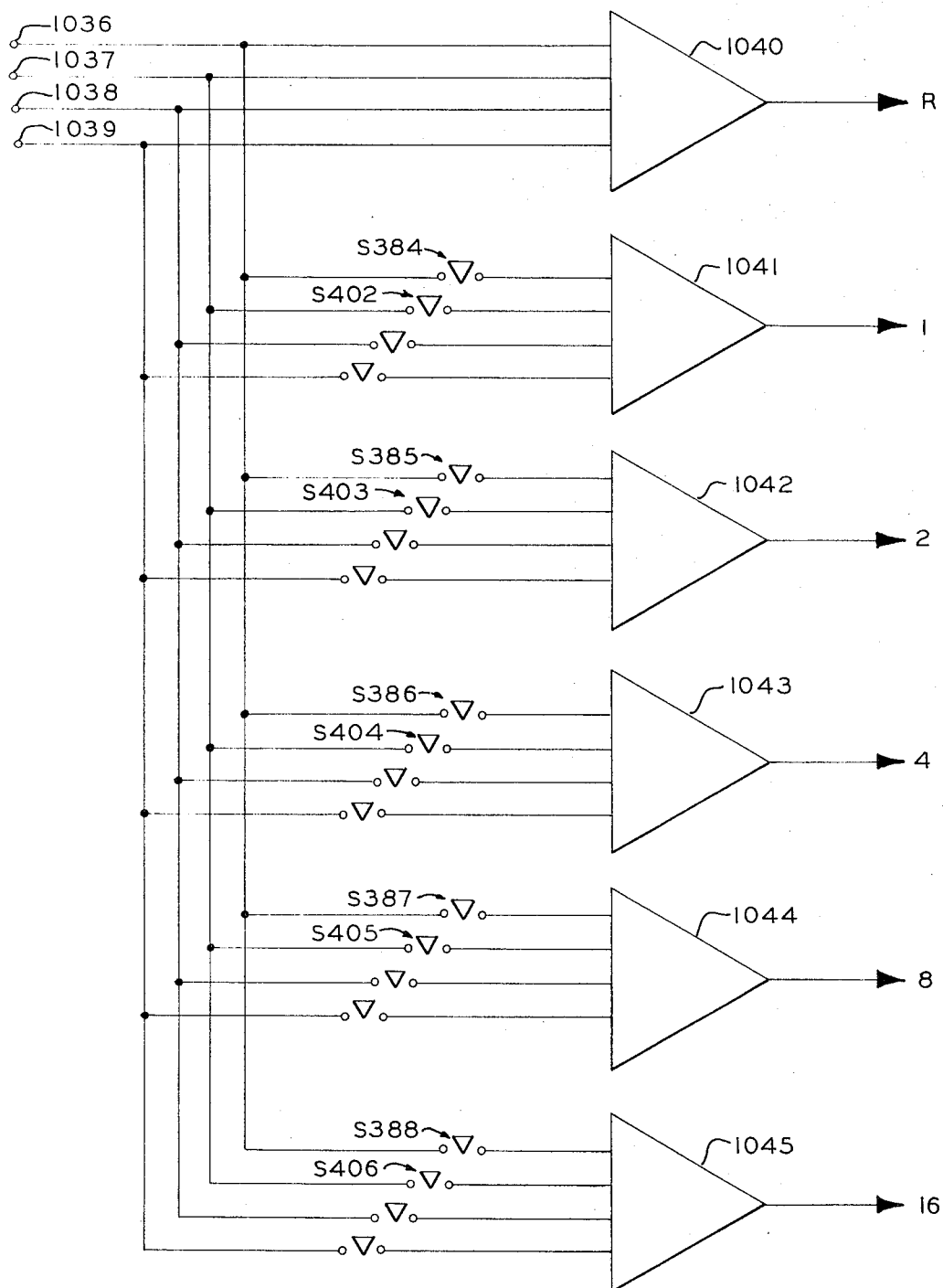


FIG. 46

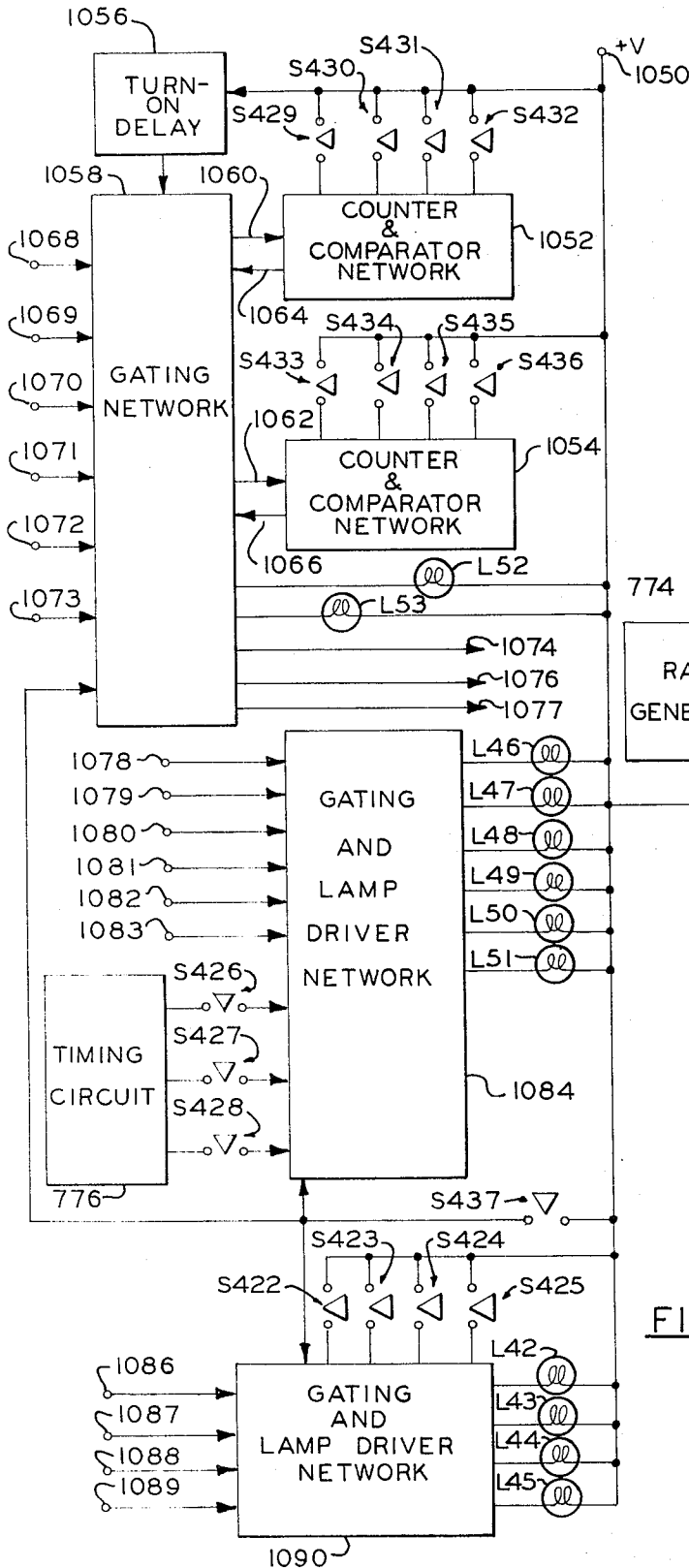
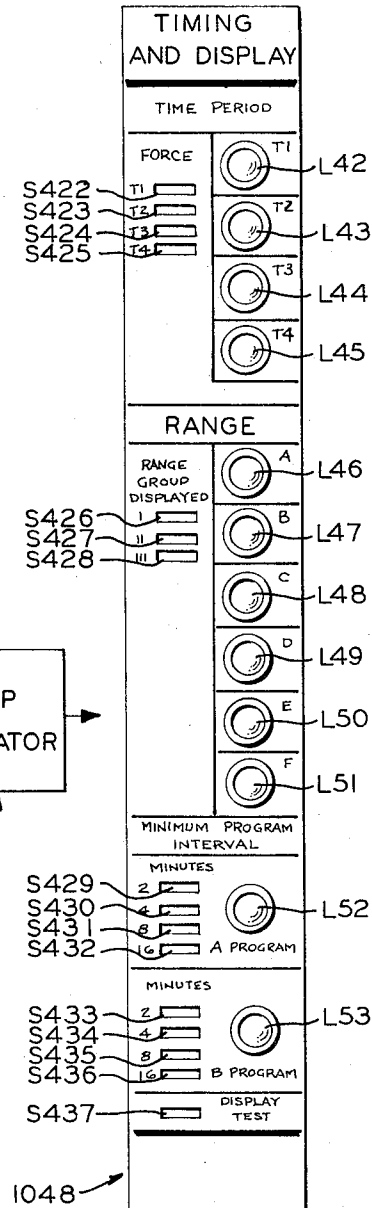


FIG. 47

FIG. 48

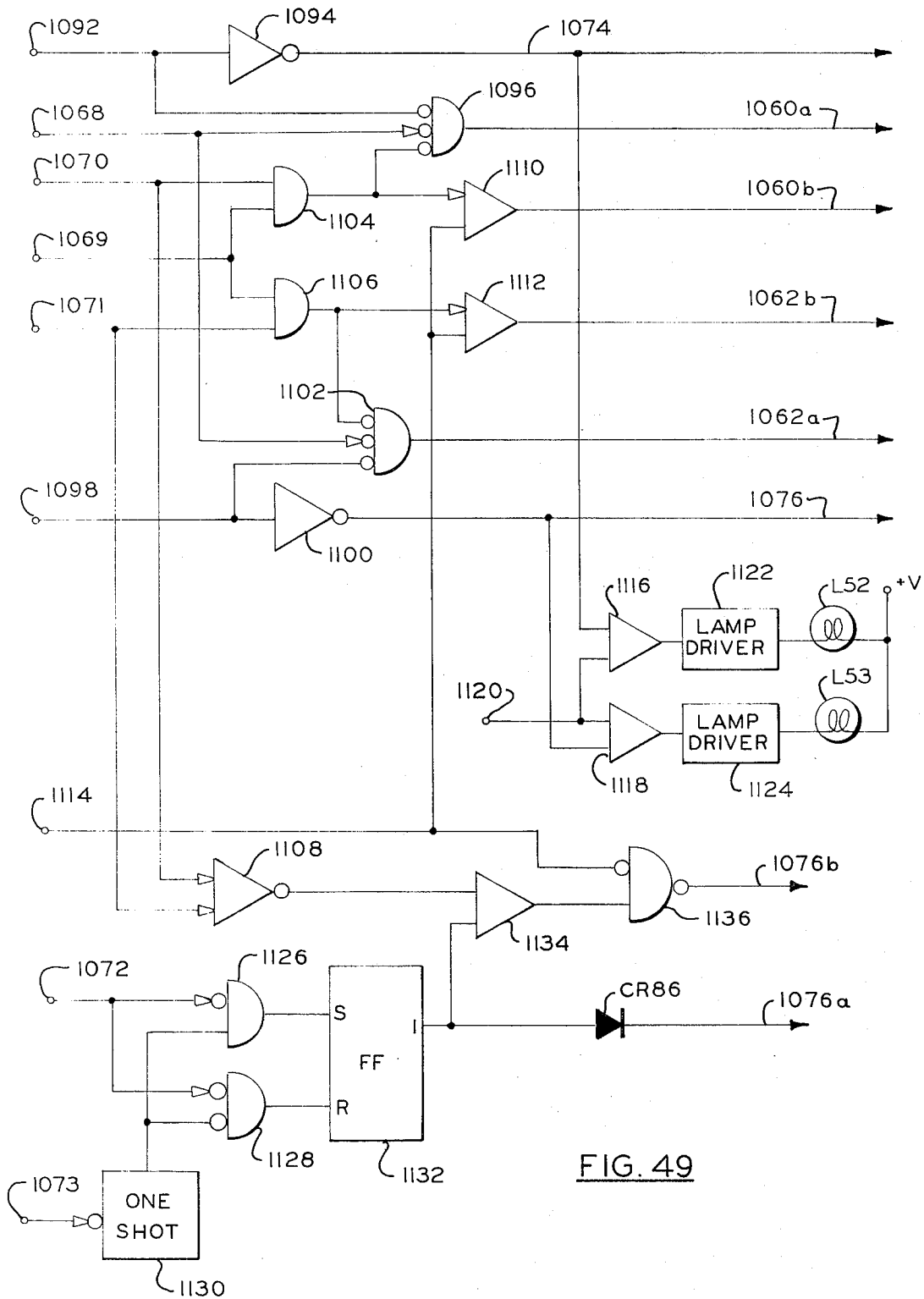
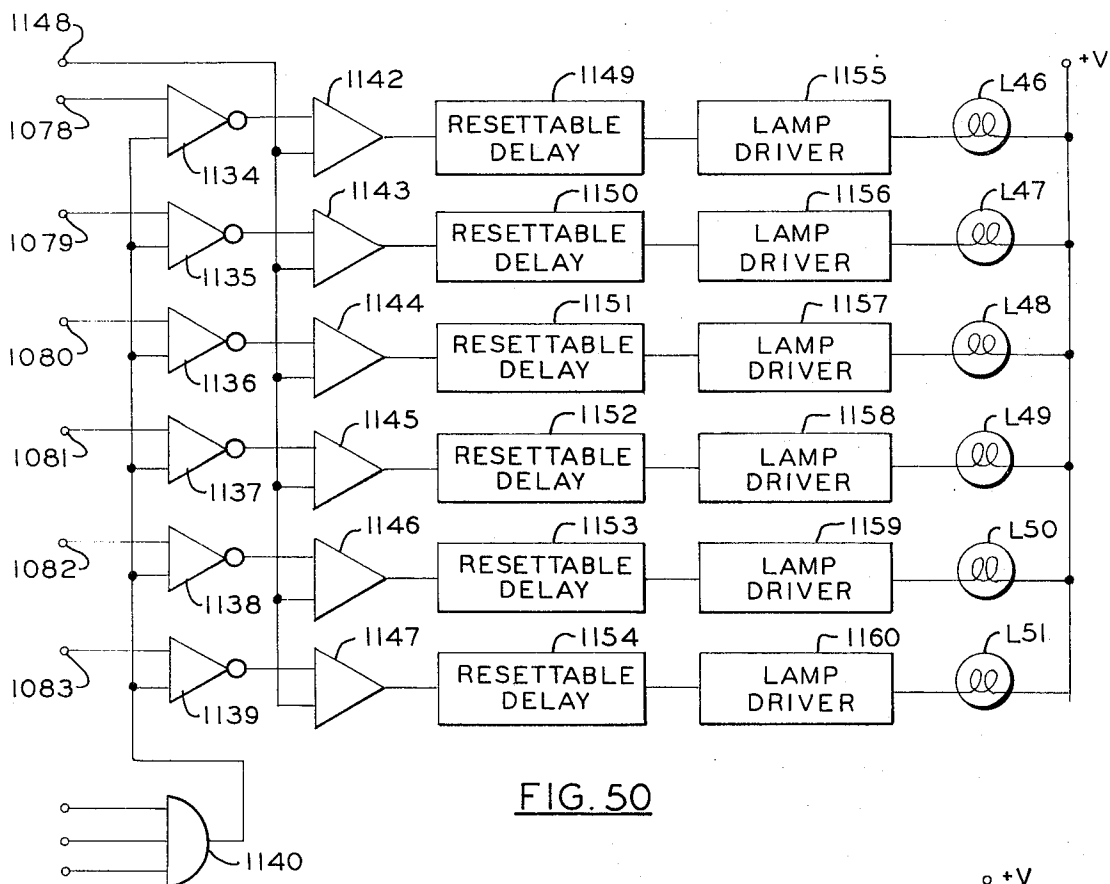
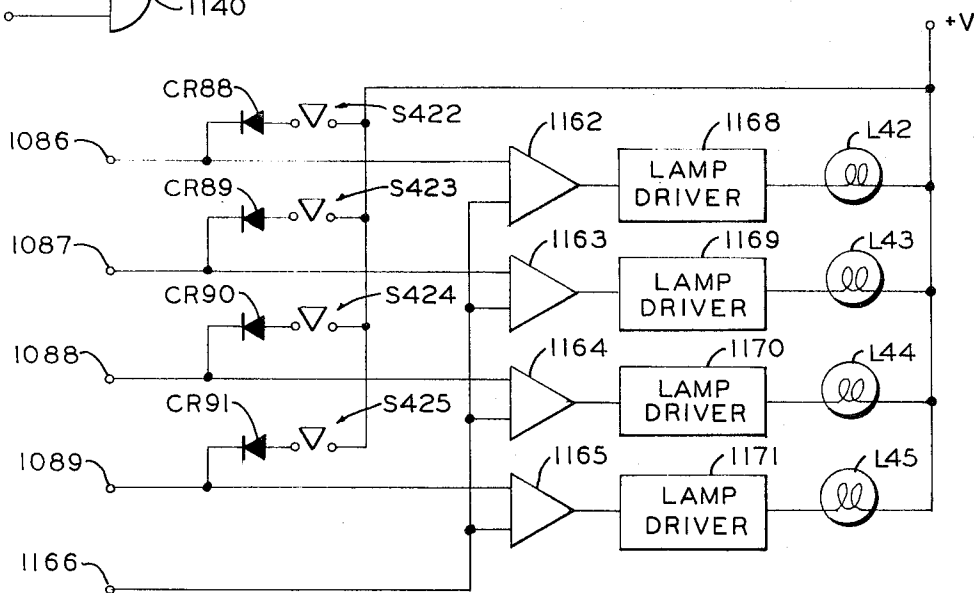


FIG. 49



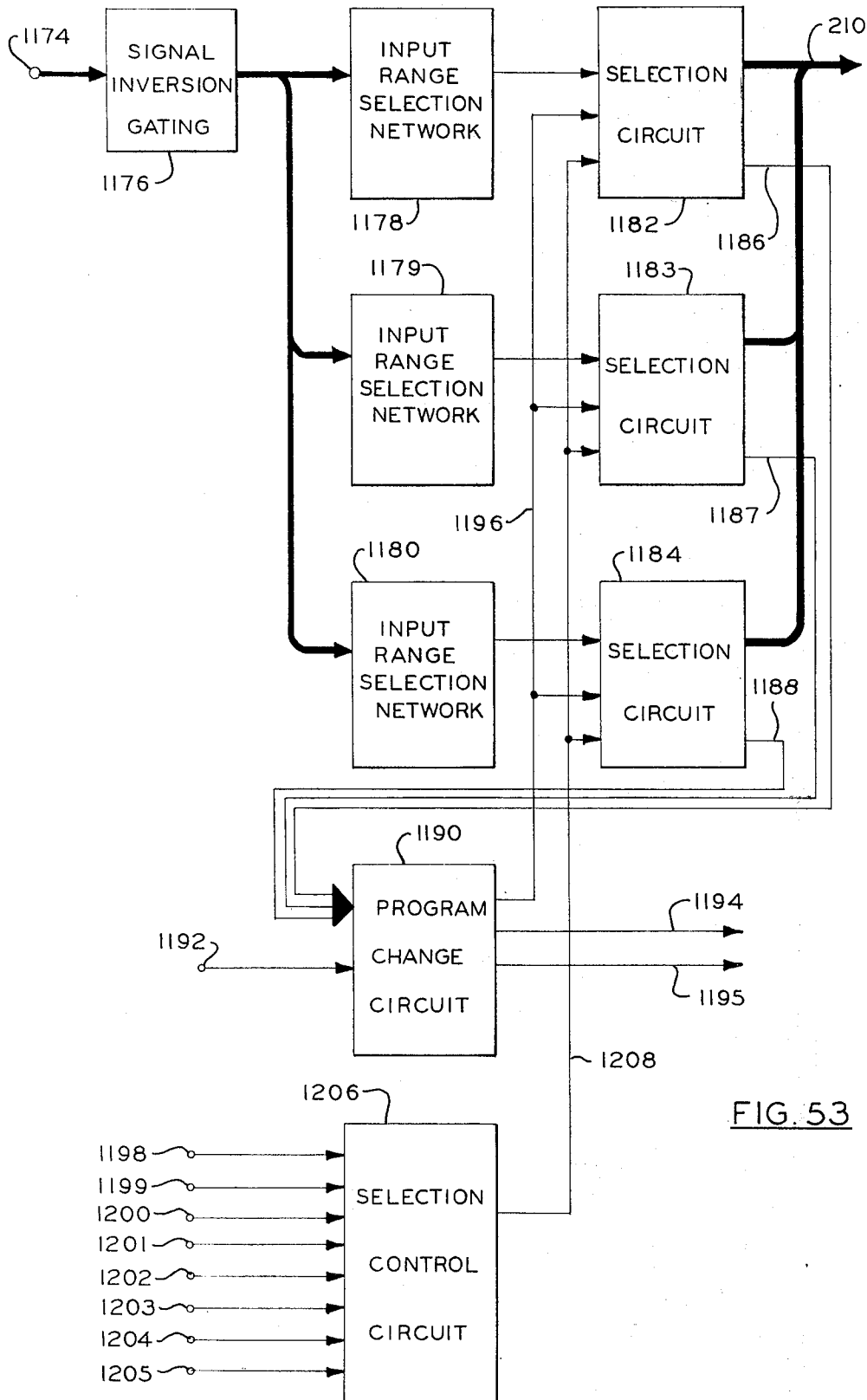


FIG. 53

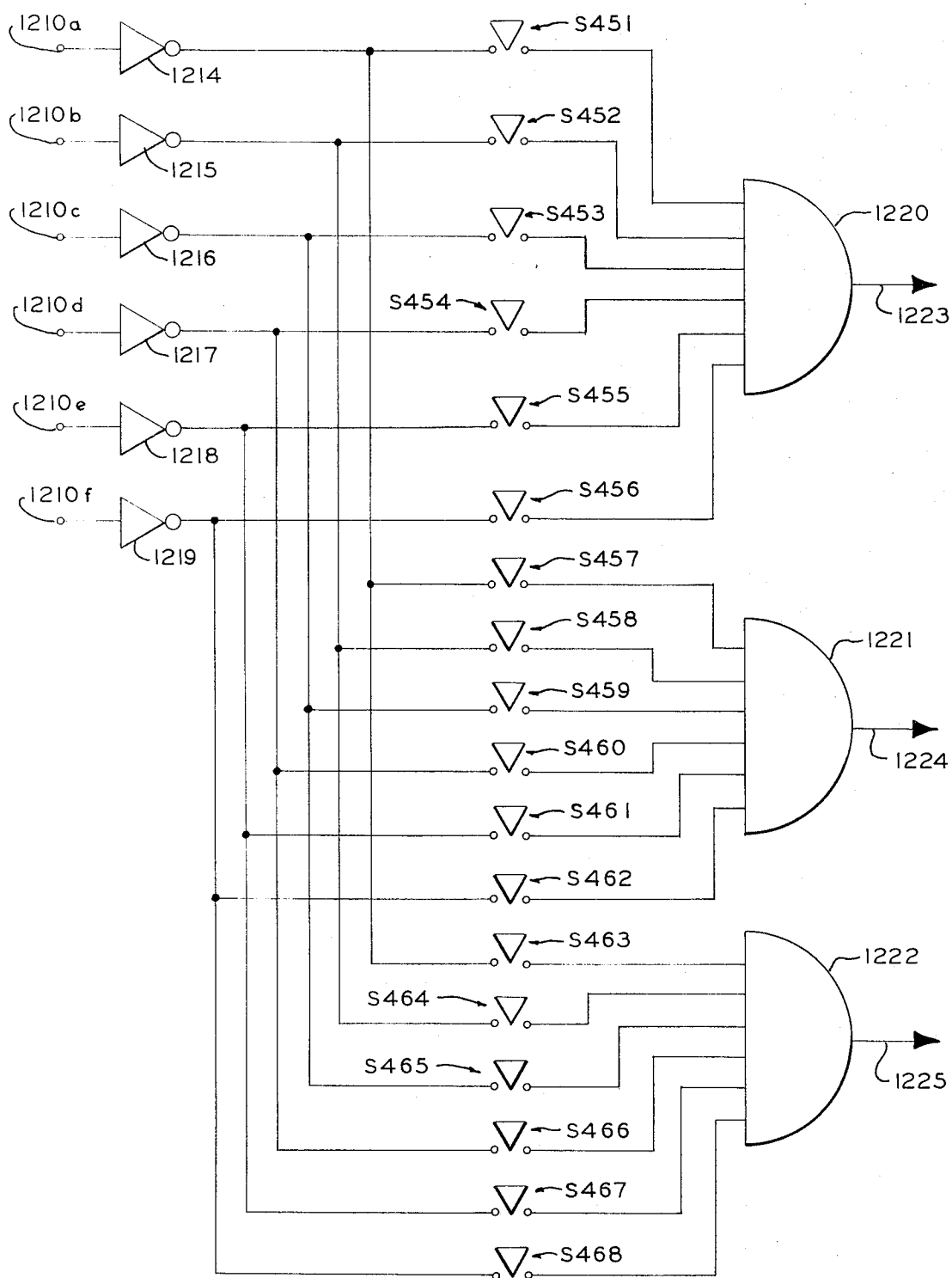


FIG. 54

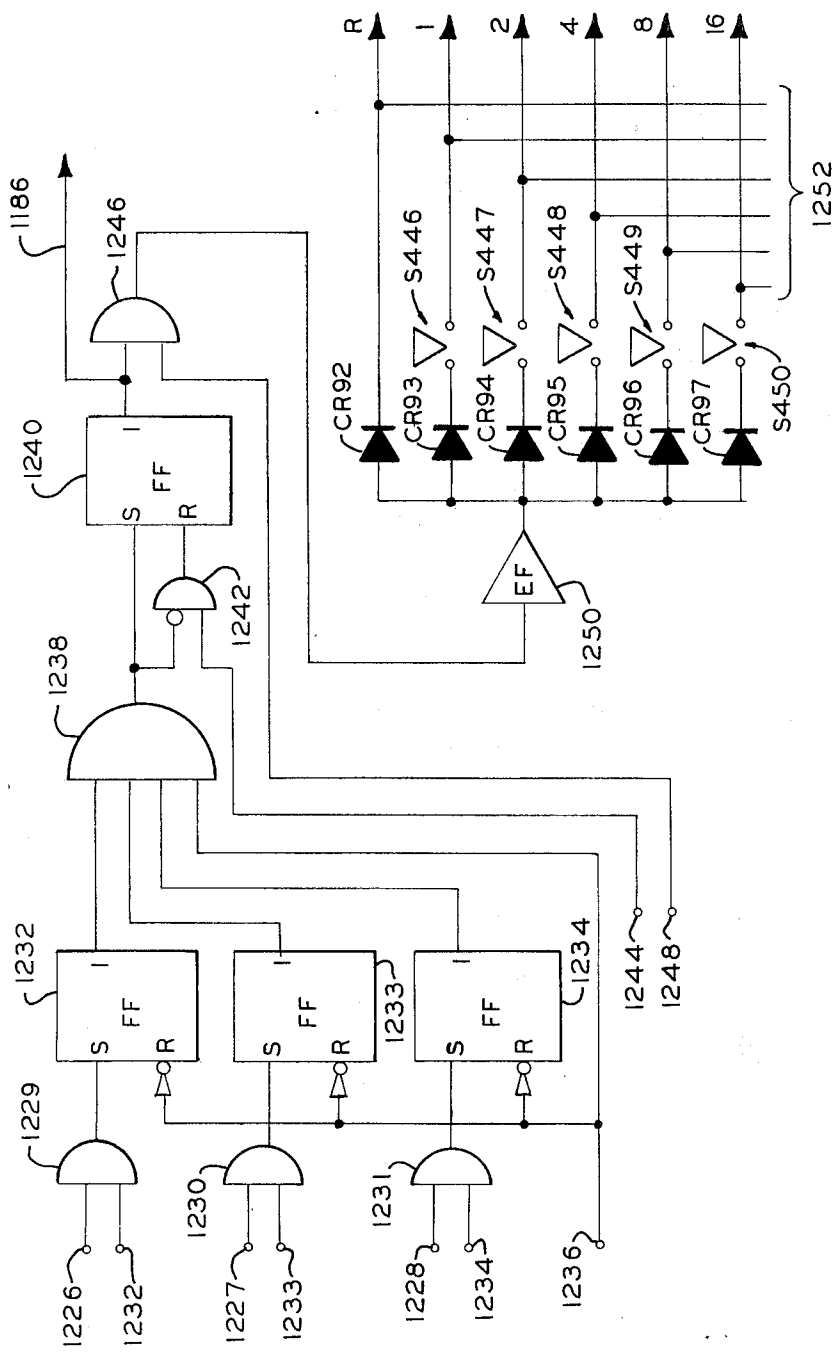


FIG. 55

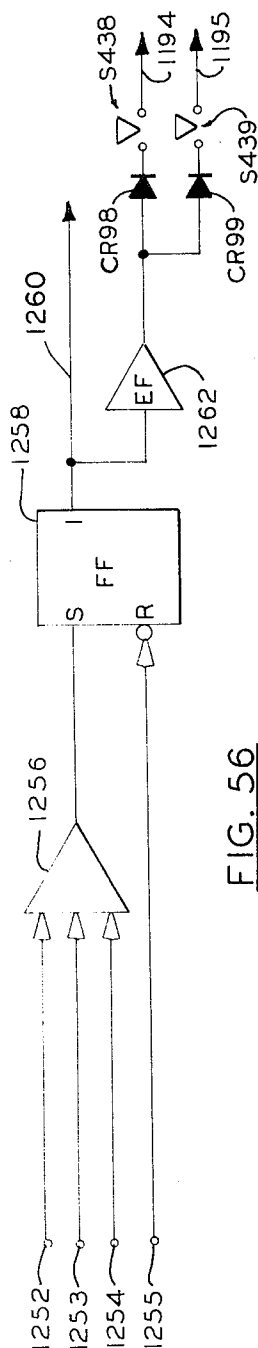


FIG. 56

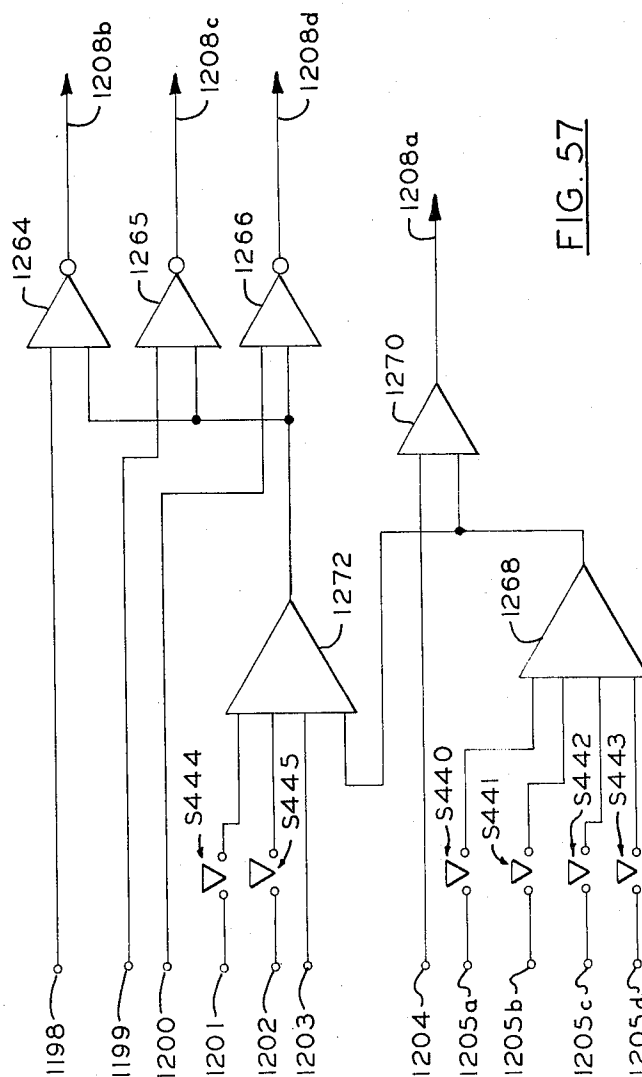


FIG. 57

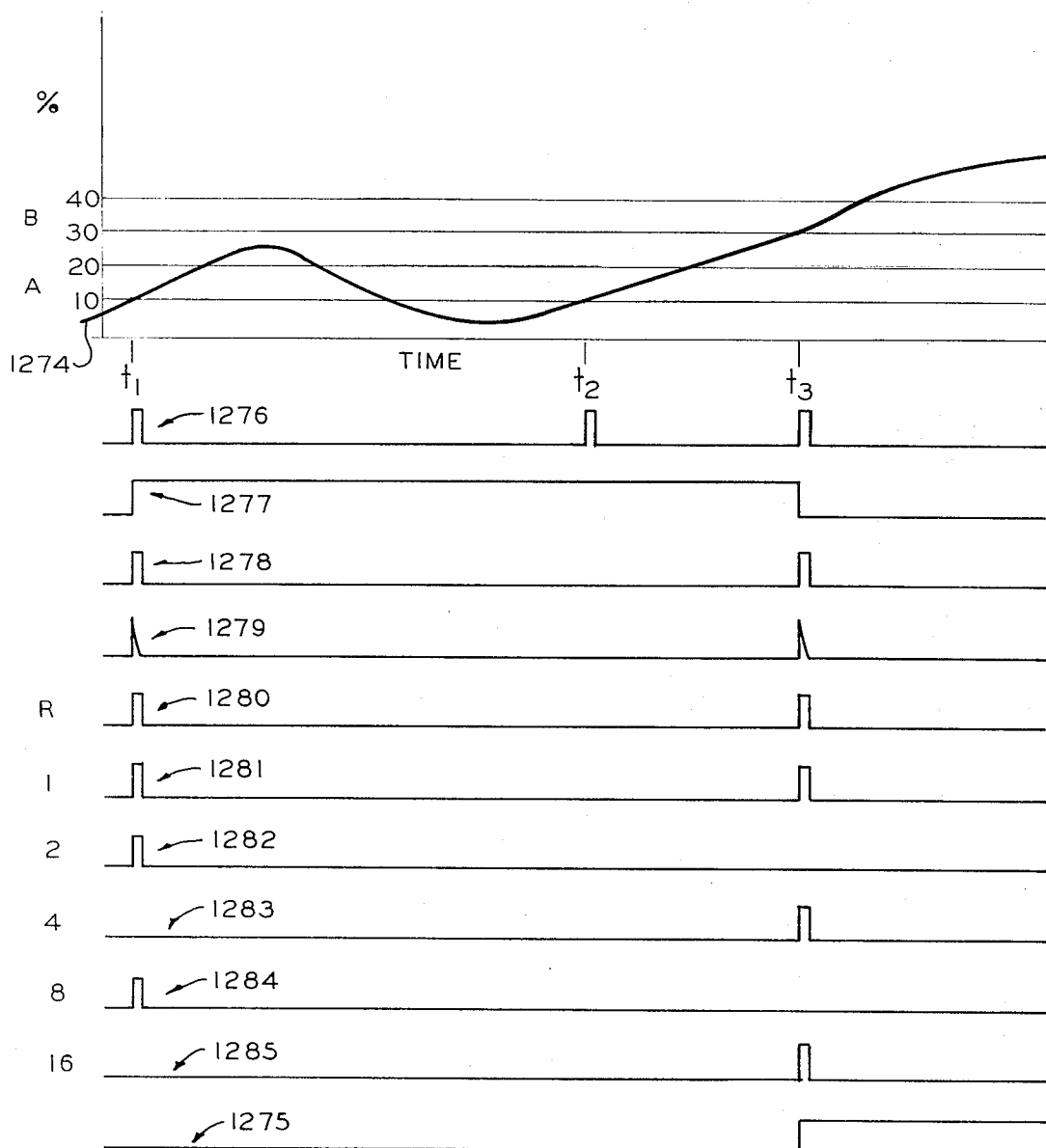


FIG. 58

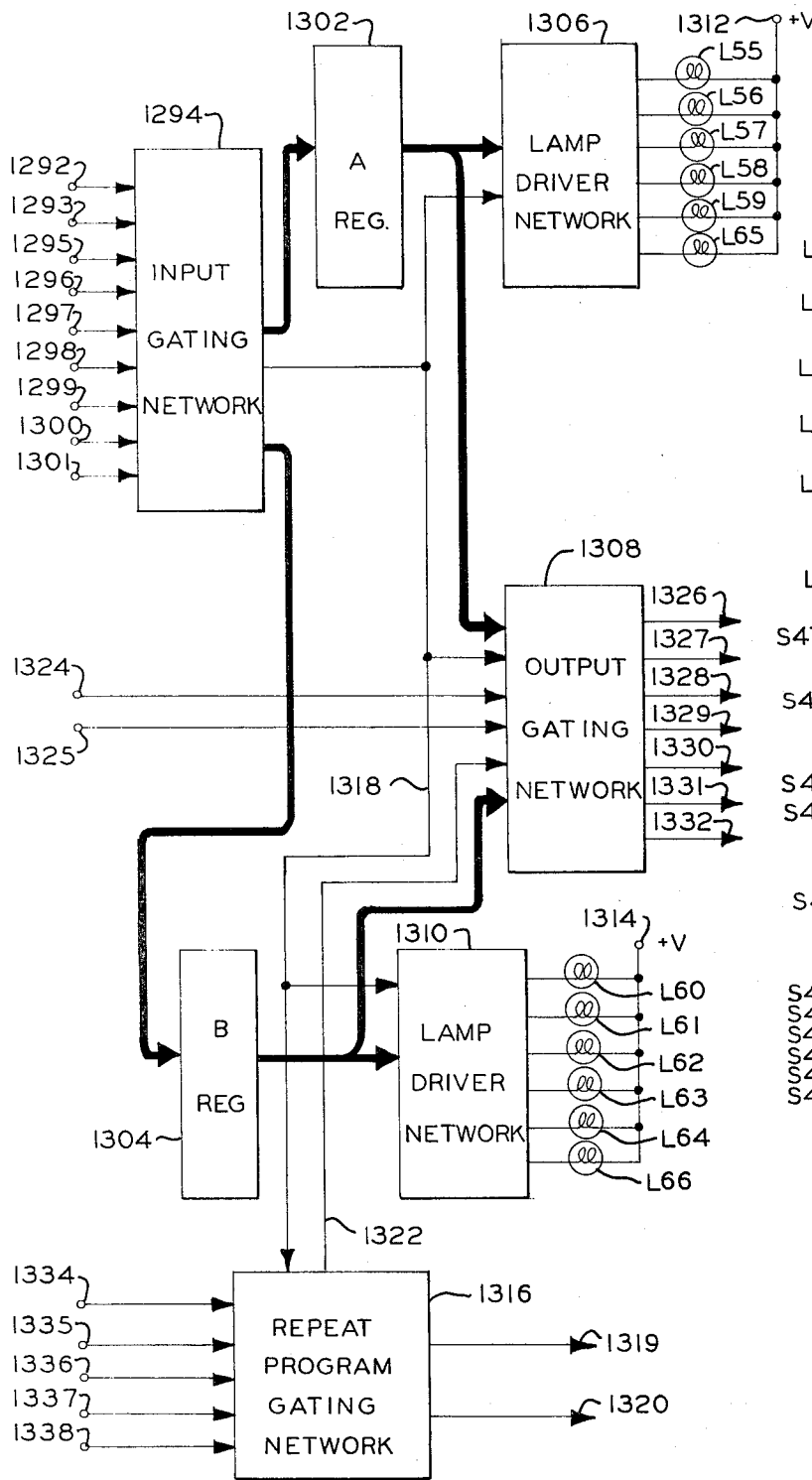


FIG. 60

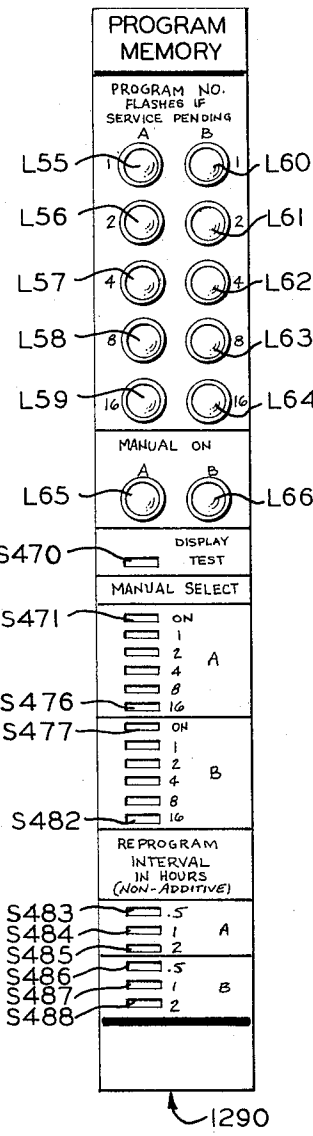
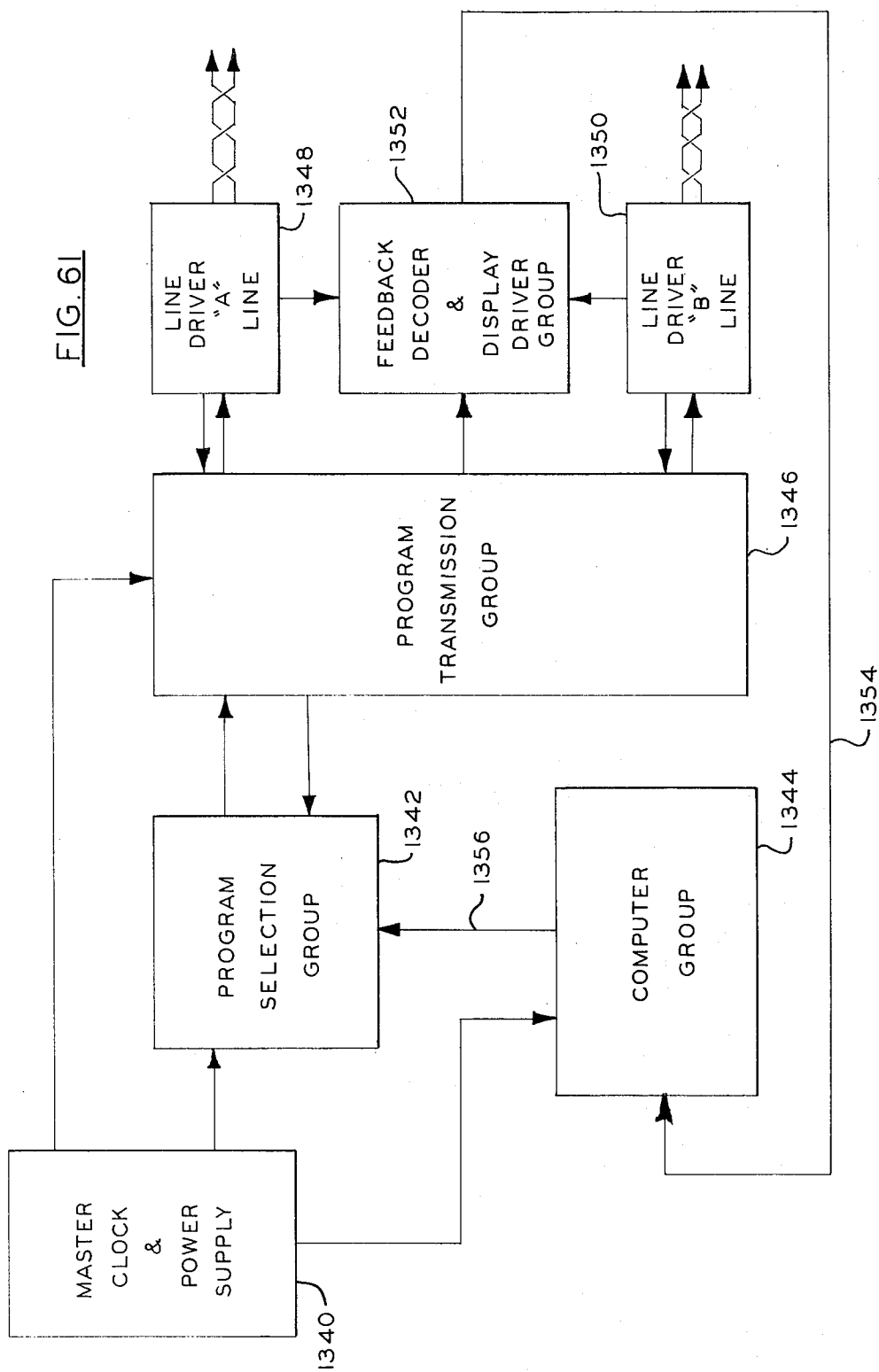


FIG. 59



MULTI-INTERSECTION TRAFFIC CONTROL SYSTEM

This application is a continuation-in-part of U.S. application Ser. No. 166,915 filed July 28, 1971.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to traffic control systems and, more specifically, to electronic computation and analysis of dynamic traffic parameters with means for effecting multi-intersection control based thereon.

2. Description of the Prior Art

As the number of motor vehicles on the streets and highways has increased over the years, the need for efficient control of traffic flow has become more pressing. The congestion on major city streets with numerous intersections, pedestrian crossings, and the like, is particularly acute. While the use of color-coded light as signals to control of traffic flow still represents the most efficient and satisfactory means of automatic control, optimum traffic flow can be achieved only through better means for timing the cycling of the traffic lights, both at individual intersections and at a plurality of consecutive or otherwise related intersections. Presently available systems include those in which cycling is under the control of an appropriate timing mechanism and those responsive to certain traffic parameters. For example, a traffic light at an intersection of a major thoroughfare and a less frequently used side street may be programmed to permit traffic flow on the main street at all times except for short intervals when the presence of a vehicle is indicated on the side street by appropriate presence detectors. Pedestrian signals at certain intersections commonly include a manual switch for operation by a person wishing to cross the street, thereby overriding the normal cycling of the lights for traffic control.

SUMMARY OF THE INVENTION

With the advances in computer technology it has become feasible to provide electronic numerical analysis of current traffic conditions over rather large areas and to utilize the results of such analysis for cooperative control of the cycling of traffic lights at numerous intersections. It has also been found expedient to utilize available magnetic or punched-tape apparatus for providing one or more predetermined sequences of electrical signals to control traffic light cycling or timing. The present invention combines the advantages of these two technical areas to control the operation of traffic signals at a plurality of intersections in response to a program recorded on punched tape, or the like, wherein the program is selected from several pre-recorded programs by computer analysis of existing traffic conditions.

In a general sense, the object of the present invention is to provide a master traffic control system for a plurality of intersections which promotes optimum, or acceptable, flow of traffic at all times, taking into account both economy of operation and required levels of sophistication for effecting operational changes in response to current analysis of traffic parameters. The term "traffic control system", as applied to the invention, is intended to include both the operational sequences, i.e., methods, employed in arriving at the timing or cycling of the traffic signals, and the assemblage

of circuitry and other hardware, or apparatus, used in effecting such control.

More specific objects are to provide a novel and efficient traffic control system wherein: time-averaged levels of traffic parameters such as density, speed and volume are sensed, computed, and used in selecting an optimum program of traffic control; the ratio of two or more current traffic parameters, such as density of opposing traffic flows, may be automatically computed and used as a means of controlling traffic signal timing; a plurality of traffic signal timing programs are pre-recorded and one program selected for use in response to actual traffic flow sensed and computed during the time a preceding program was in use; pre-selected ranges of traffic activity are used to control signal timing, after sensing and computation of such activity to determine within which range the activity falls over a given time period; pre-selected ranges of a number of different traffic parameters are established and a pre-recorded signal control program is selected and activated in response to one or more of such parameters changing from one range to another; metering and recording capability is provided for a plurality of sensed traffic parameters and pre-recorded control programs, e.g., automatically recording and visually indicating the identity of a particular program along with the time and date it was activated; a master time clock may be used to establish alternating periods of time-responsive and traffic-responsive signal control; and, periods may be established for effecting traffic-responsive signal control alternately for different traffic parameters or different ranges of the same or different parameters.

Other objects of the invention will in part be obvious and will in part appear hereinafter.

The invention accordingly comprises the several steps and the relation of one or more of such steps with respect to each of the others, and the apparatus embodying features of construction, combinations of elements and arrangement of parts which are adapted to effect such steps, all as exemplified in the following detailed disclosure, and the scope of the invention will be indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. 1 is a suggested arrangement of the front panel of a Master Traffic Controller with a plurality of diagrammatically indicated intersection traffic controllers, vehicle detectors and traffic signal lights connected thereto constituting a Multi-Intersection Traffic Control System;

FIG. 2 is a diagrammatic plan view of a plurality of street intersections arranged along two intersecting main streets;

FIG. 3 is provided to indicate continuity of the block diagram shown on the three sheets designated as FIGS. 3A, 3B and 3C;

FIGS. 3A, 3B and 3C are a single block diagram of the Multi-Intersection Traffic Control System constructed in accordance with the principles of the present invention;

FIG. 4 is a suggested layout of the front panel for the Master Clock Module;

FIG. 5 is a block diagram of the Master Clock Module;

FIG. 6 is a suggested layout of the front panel of the Detector Input Monitor Module;

FIG. 7 is a block diagram of the detector Input Monitor Module;

FIG. 8 is a combined block and logic diagram of a counter and comparator network employed within the Detector Input Monitor Module;

FIG. 9 is a timing diagram of the circuits contained within the Detector Input Monitor Module;

FIG. 10 is a logic diagram of a detector monitor circuit employed within the Detector Input Monitor Module;

FIG. 11 is a suggested layout of the front panel for the Density Computer Module;

FIG. 12 is a block diagram of the Density Computer Module;

FIG. 13 is a combined block and logic diagram of a response counter and comparator network contained within the Density Computer Module;

FIG. 14 is a combined block and logic diagram of the input circuit to a density computer contained within the Density Computer Module;

FIG. 15 is a schematic diagram of a density computer contained within the Density Computer Module;

FIG. 16 is a timing diagram of the density computer;

FIG. 17 is a suggested layout of the front panel for the Speed Computer Module;

FIG. 17A is a block diagram of the Speed Computer Module;

FIG. 17B is a block diagram of an individual speed computer;

FIG. 17C is a logic diagram of certain networks used within the speed computer;

FIG. 17D is a schematic diagram of other networks of the speed computer;

FIG. 17E and 17F are schematic-block diagrams of still further networks of the speed computer;

FIG. 17G is a timing diagram showing waveforms associated with the various networks of the speed computer;

FIG. 18 is a suggested layout of the front panel for the Volume Computer Module;

FIG. 18A is a block diagram of the Volume Computer Module;

FIG. 18B is a logic diagram of one of the circuits of FIG. 18A;

FIG. 18C is a block diagram of an individual volume computer;

FIG. 18D and 18E are schematic-block diagrams of networks within the volume computer;

FIG. 18F is a schematic diagram of other circuit elements of the volume computer;

FIG. 19 is a suggested layout of the front panel for the Traffic-Count Print Module;

FIG. 20 is a block diagram of the Traffic-Count Print Module;

FIG. 21 is a suggested layout of the front panel for the Ratio Computer Module;

FIG. 22 is a block diagram of the Ratio Computer Module;

FIG. 23 is a schematic diagram of an input network for the Ratio Computer Module;

FIG. 24 is a schematic diagram of an alternate embodiment of the input network of FIG. 23;

FIG. 25 is a combined block and schematic diagram of an analog computer employed within the Ratio Computer Module;

FIG. 26 is a logic diagram of a compute-cycle counter employed within the Ratio Computer Module;

FIG. 27 is a timing diagram of the circuits employed within the Ratio Computer Module;

FIG. 28 is a suggested layout of the front panel for the Meter-Record Output Module;

FIG. 29 is a block diagram of the output printer control circuit contained within the Meter-Record Output Module;

FIG. 30 is a block diagram of the meter drive circuit contained within the Meter-Record Output Module;

FIG. 31 is a suggested layout of the front panel for the Range Selection Module;

FIG. 32 is a block diagram of the Range Selection Module and a part of the Timing and Display Module;

FIG. 33 is a logic diagram of the timing circuit contained within the Timing and Display Module;

FIG. 34 is a timing diagram of the circuits employed within the timing circuit of FIG. 33.

FIG. 35 is a logic diagram of the counter and gating circuit of FIG. 32;

FIG. 36 is a schematic diagram of the ramp generator within the Timing and Display Module;

FIG. 37 is a timing diagram of the outputs of the circuits of FIGS. 35 and 36;

FIG. 38 is a block-logic diagram of the digital comparator and set range circuit of FIG. 32;

FIG. 39 is a logic diagram of the analog comparator and output gating network of FIG. 32;

FIG. 40 is a graphical summary of the operation of the Range Selection Module;

FIG. 41 is a suggested layout of the front panel for the Program-Time Selection Module;

FIG. 42 is a block diagram of the Program-Time Selection Module;

FIG. 43 is a schematic diagram of the day selection gate of FIG. 42;

FIG. 44 is a block-logic diagram of the digital comparator and gating network of FIG. 42;

FIG. 45 is a logic diagram of the set time interval circuit of FIG. 42;

FIG. 46 is a logic diagram of the output gating network of FIG. 42;

FIG. 47 is a suggested layout of the front panel for the Timing and Display Module;

FIG. 48 is a block diagram of the Timing and Display Module;

FIG. 49 is a logic diagram of the gating network of FIG. 48;

FIGS. 50 and 51 are block-logic diagrams of the gating and lamp driver networks for range-indicating and time-period indicating lamps, respectively, of FIGS. 47 and 48;

FIG. 52 is a suggested layout of the front panel for the Program-Range Selection Module;

FIG. 53 is a block diagram of the Program-Range Selection Module;

FIG. 54 is a logic diagram of the signal inversion gating and input range selection network of FIG. 53;

FIG. 55 is a logic diagram of the selection circuit of FIG. 53;

FIG. 56 is a logic diagram of the program change circuit of FIG. 53;

FIG. 57 is a logic diagram of the selection control circuit of FIG. 53;

FIG. 58 is a timing diagram of circuits within the Timing and Display, Program-Time Selection and Program Range Selection Modules;

FIG. 59 is a suggested layout of the front panel of the Program Memory Module;

FIG. 60 is a block diagram of the Program Memory Module; and

FIG. 61 is a block diagram summarizing the interconnection of major components of the system.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The final output element in any automatic traffic control system is, of course, the signal device which indicates to the vehicle operators a particular instruction. The present discussion will assume the use of the common three-color traffic light for indicating "stop", "go" and "caution" in the usual manner. The signal devices or lights are located in appropriate places at the point of desired traffic flow control, normally an intersection of two streets, and the electromechanical elements such as switches and relays, or equivalent electronic switching devices, for energizing or turning the individual lamps on and off are commonly located in a box near the intersection. Such boxes and their contents are referred to as intersection controllers and may contain additional elements for handling various electrical signals to provide a final output to the lamp circuits. Energizing signals for the intersection controllers may be provided by a timing mechanism internal or external to the intersection controller, from traffic actuated devices such as vehicle presence detectors, or from a remote master controller which provides such signals to a plurality of intersection controllers. The master controller may itself receive inputs from presence detectors, or the like, located at or near intersections or at other selected points along the route of the traffic to be controlled. The input devices used to sense and indicate vehicle presence will be assumed, in the present discussion, to be conventional loop-type detectors beneath the road surface which provide electrical signals (commonly a change in oscillator frequency) indicating vehicle presence in response to the change in reactance produced by the proximity of the large mass of metal in the vehicle.

The present invention is concerned with the entire traffic control system including the traffic lights, intersection controllers and vehicle detectors, as well as the master controller, but the principal features of the invention involving departure from prior art techniques and hardware are mostly embodied in the elements of the master controller. That is, the traffic lights, vehicle detectors and major portions of the intersection controllers, while necessary to the operation of the complete system, may be of conventional construction. An intersection controller which may be adapted for use with the present invention is disclosed in U.S. Patent application Ser. No. 302,041, filed Oct. 30, 1972, by Carlile R. Stevens for TRAFFIC CONTROL SYSTEM, which application is a continuation of Ser. No. 5,068, filed Jan. 22, 1970, now abandoned. The master controller, however, is almost entirely unique to the present invention and will therefore be the subject of the

bulk of the following disclosure. It is largely constructed in modular form with each module identified with a particular function performed within the control system. Thus, the disclosure may conveniently be divided into separate, detailed descriptions of each module with appropriate block diagrams to tie together the various modules, and other elements of the system.

FIG. 1

A typical front panel layout for the master controller is shown in FIG. 1, with diagrammatic indications of the remote elements of the system to which it is connected. The master controller is designated generally by the reference numeral 70 and is preferably enclosed in a single cabinet with a front panel containing various control and readout devices associated with operation of the system. Master controller 70 would normally be located in a police station, city hall, or the like, where surveillance and control of the entire system takes place, and is connected to a plurality of separate intersection controllers, indicated by the boxes numbered 72. In the disclosed embodiment, master controller 70 is connected to two separate groups of intersection controllers 72, each group being connected in parallel over separate single pairs of conductors designated lines A and B. Existing telephone lines may conveniently be used in some cases to provide some or all of the connections. As will become apparent, the system is not limited to the use of only two lines, nor is the number of intersection controllers connected in parallel on any one line limited by other than convenience or cost considerations; however, practical limitations exist due to loading factors.

Also diagrammatically indicated as connected to each of intersection controllers 72 are vehicle detectors 74 and traffic signal lights 76. This is not intended to imply that a single detector or signal light is connected to each intersection controller, as some controllers may be connected to more than one of each or have no vehicle detectors connected thereto. As vehicles pass in proximity to detectors 74 signals are generated to indicate vehicle presence in known manner, either by generating a single pulse for each vehicle sensed or a continuous signal for as long as a vehicle remains in proximity to the detector. The signals may be utilized exclusively within the intersection controller with which the detector is associated to effect changes in the cycling of the appropriate signal lights, or may be transmitted over line A or B back to master controller 70 and utilized in one or more ways described hereinafter in the master control system. Actual construction and operation of the signal lights and output switches therefor in the intersection controllers, as well as other circuits and mechanism in the intersection controllers, may be selected from a wide variety of suitable prior art devices and are not further described since the present invention is not directly concerned therewith. However, one such intersection controller adapted for use with the system of the present invention is disclosed in the aforementioned application.

Some of the features on the front panel of master controller 70 will be briefly described with the complete function and construction of all operational elements described later in detail. In the upper right portion of the front panel are a number of analog meter readouts, indicated collectively by reference numeral 78, which may comprise conventional ammeters of ap-

propriate scale to indicate current levels of selected traffic parameters in the system. A second group of meters 80 are arranged to drive pens on moving paper tapes to provide permanent records of the same or different traffic parameters. A pair of counter-printers 82 provide a digital meter readout and permanent digital record of such things as the identity of traffic control programs in use and traffic counts at specified times. Keyboard 84 provides actuating signals for tape punch apparatus 86 for recording pre-selected programs on paper tape in conventional fashion. Keyboard 84 may also be used for inserting manually the identity of a particular control program, a plurality of which have been recorded on tape 88, which is to be put into effect in response to such keyboard instruction. Alternatively, the control program in use may be automatically selected in response to current traffic parameters or to the time of day. The information on tape 88 is converted to electrical signals in conventional fashion by tape reader 90.

Section 92 of the front panel, below tape reader 90, is occupied by a group of individual panel faces of modules comprising circuitry and logic for accomplishing various functions within the master control system. Each panel layout and necessary details of the complete modules are separately described hereinafter. A pair of windows 94 above the tape reader are provided for observing digital meters which indicate offset time, i.e., the elapsed time from a beginning reference to the time when each successive signal light along the route turns green, for each of lines A and B. The upper left part of the front panel, indicated by reference numeral 96, is identical to the same portion of the master controller front panel disclosed in the aforementioned application. This section includes a number of push buttons, lamps, meters, and the like, for effecting certain tests and monitoring functions. Individual features of this section are not further described herein, being essentially identical to those shown and described in the aforementioned application, and are not directly concerned with the present invention.

FIG. 2

In FIG. 2 is shown a typical portion of a city street system wherein two essentially parallel arterial streets are connected by side streets, forming a grid pattern. All intersection controllers 72 along one arterial street, designated Street A, as well as the intersection controllers at those intersections on adjacent side streets having traffic signals, are connected by Line A to master controller 70. Intersection controllers 72 on Street B, and other streets in the general area, are connected to the master controller by Line B. Vehicle detectors 74 are located at desired points along both streets where traffic activity is to be sampled. Signals are transmitted over the lines connecting the individual detectors and signal lights to their respective intersection controllers, and between the latter and the master controller over lines A and B in conventional manner, using multiplexing techniques explained in the aforementioned application where appropriate. Various traffic parameters which may be calculated from the sensing of vehicles in the manner indicated will be explained at places in the present description where apparatus or functions associated with such parameters are taken up. FIG. 2 will be referred to in various places later where it is

helpful in explaining and understanding the overall system operation.

FIGS. 3, 3A, 3B and 3C

Before disclosing in detail the construction of the individual sections of the master controller, referred to herein as "modules", a block diagram indicating the interrelationship of all elements in the master controller will be considered. This block diagram is laid out on three sheets, designated as FIGS. 3A, 3B and 3C, with the relationship of the sheets to form a unitary diagram being indicated in FIG. 3. Everything in the block diagram may be, and preferably is, located in or on master controller 70. In general, the master controller is designed to do the following things:

1. Select the green timing for each traffic movement at each intersection it supervises.
2. Change this timing at preset times of the day, or when the value for selected traffic parameters resides within programmed ranges of values. The day of the week may also affect the time during the day when the program is changed.
3. Transmit to each intersection under its control the proper offset relationship the intersection is to maintain with the zero time reference point within the system.
4. Transmit to each intersection a once-per-cycle timing pulse from which the intersection may take its reference, thereby maintaining proper synchronization.
5. Receive information from each intersection indicating the status of the main traffic light at that intersection or any other information as may be desired, including vehicle detections.
6. (a) Display this information on a lighted map, or similar indicating display device, when desired.
(b) Use this data for traffic analysis and computation of parameters for selection of traffic responsive timing changes.
7. Display when desired a read-out indicating the number of seconds from the zero time reference point the system is at at all times.
8. Program any or all of its intersections via special instructions to operate in different modes; such as actuated (in response to local traffic demands), semi-actuated, fixed time or flash.

The above described operations are accomplished as follows: programs are stored on commercially available eight column punched tape, and are read by punch tape reader 90 (seen also in FIG. 1).

Sixty-four separate programs 32 for each of two systems, A and B) may be selected from the tape by scanning the tape for the appropriate program address. Each program contains sub-programming information for each intersection supervised by the master controller. The disclosed embodiment of master controller 70 is capable of supervising 110 intersection addresses, wherein a single address may include one or more intersections. Thus, the possible number of sub-programs that can be stored on a single tape would be the product of the number of programs times the number of intersections, i.e., 7040.

The program to be selected for a given period of the day, and day of the week, is determined by pin programming (as explained later herein) in the Program-Time Select Modules 98. Each module can select up to four different programs for different times. The output

of Master Clock 100 indicates to the Program-Time Select Modules the exact time and day of the week. A one pulse per second signal is also supplied from Master Clock 100 on line 101. Thus, when a particular preset time arrives, there will be an output from the Program-Time Select Module to Program Memory Module 102, which serves as an intermediate storage register to transfer program identities from the Program-Time Select Module to program number comparator 104. Here the identity of the desired program is compared with the program in position for use in reader 90. Power is supplied to a motor which drives the tape through the reader until the identities of the desired program and the one in position for use are matched.

The program identifications are broken down into two sections labelled A and B. The master controller is capable of transmitting programs over two separate output lines, previously identified as lines A and B. The block diagram is complete only for those functions performed in connection with the programs transmitted on line A. Block 106 in FIG. 3B indicates that the elements shown in the more detailed diagram provided for line A are duplicated for line B.

The elements within dashed line 108 control the operation of tape reader 90. When a change in program is desired on line A there is a momentary output on the line labelled "change program A" which sets program service flipflop 110. The "one" output of flipflop 110 is fed back to the Program Memory Module 102 on the line labelled "service A program". This prevents B program execution while an A program is being executed. Conversely, an A program cannot be executed while a B program is being executed. When the change-program-A line goes high, its signal is coupled through OR gate 112 to automatic tape control 114. Thus, the tape reader is caused to advance continuously at a high speed scan by a continuous signal on the "advance" line running to tape reader 90. This line also runs to reader power delay 116 which supplies power to tape reader 90.

The purpose of reader power delay 116 is to provide power to tape reader 90 only when needed, so that the motors and tape drive do not wear unnecessarily and the lamp that excites the photo cells will be extended in life. For each advance signal, power is applied to the tape reader and continues to be applied for a delay period which is reset each time a new advance signal arrives. Thus, if advance signals continue to come on a regular basis, the tape reader will get continuous power. However, if the advance signals stop for any length of time, such as occurs when the program has been concluded, the power is removed from the tape reader.

Following the program number or program address on the paper tape, there are intersection identification numbers. The first number indicates that the next line of data represents cycle length and is therefore to be entered into cycle length register 118. This is the cycle length (the time required for one complete cycle of all signal lights controlling an intersection) for all intersections in the entire system and is used to produce the reference time (T_r) for the entire system offset. The cycle length time for each of the two sections, A and B, may be of the same value, or of different values.

Each time a new intersection identification comes up on the tape, ID memory 120 is set to the corresponding number. A certain hole combination indicates that a

number is to be employed for identifying an intersection rather than data to be sent to an intersection. When ID memory 120 is set, its output is fed to ID comparator 122 which also receives an input from word counter 124 indicating which word is being generated. All data following a particular ID number is sent to the particular intersection identified until a new ID number is entered into ID memory 120.

The common function comparator 126, in combination with program service flipflop 110, supplies control signals to gates 128, allowing data from data shift register 130 to be transmitted via line 134 and transmit gates 128 to line transceiver 132. Data thus supplied to line transceiver 132 is transmitted thereby on line A to the respective intersection controllers in the A system. Certain lines of the 7-bit data represent the green timing for each traffic movement at an intersection controlled by the master controller 70, and other lines of the 7-bit data represent the proper offset relationship the intersection is to maintain with the zero time reference point within the system. Each line on the tape represents 7 bits of data. An 8th parity bit is generated in data shift register 130. Each time the tape advances, the 7 bits are entered into the data shift register. These 7 bits, plus the eighth parity bit, are shifted out one bit/frame by the end-of-frame pulse from word counter 124. In this manner the data is transferred from the tape to the data shift register and then shifted into an appropriate register in the intersection controller for controlling the green timing for each traffic movement at that intersection, or for maintaining the proper offset relationship.

Elements of a frame generator network are enclosed within dashed line 136 and include clock oscillator 138, word segment counter 140, word counter 124, one-shot 142, and frame counter 144. Clock oscillator 138 supplies pulses to word segment counter 140 at a rate of 2,850 Hz. Every fourth pulse is supplied to word counter 124, which again divides the pulses by 64. When the output of one shot 142 on line 146 goes to a high level in response to a pulse from word counter 124, operation of clock oscillator 138 is inhibited. When the pulse from one-shot 142 has decayed, clock oscillator 138 resumes the output of pulses to counter 140. The output of counter 140 is provided as a synchronization pulse to transmit gates 128, line transceiver 132 and receiver gates 146. The output of counter 124, in addition to triggering one-shot 142, is supplied to frame counter 144 and data shift register 130. Frame counter 144 is needed only when serial-data transmission requires the limiting of eight frame intervals before a new tape advance signal is provided by auto tape control 114.

Outputs of word counter 124 are likewise provided on the buss line indicated by the reference numeral 148 to ID comparator 122, auxiliary function comparator 150, common function comparator 126 and word decoder 152, as well as to corresponding networks in the B system. This insures proper identification of data within the words constituting a frame.

End of program AND gate 154 is connected to data buss line 156 to recognize an end of program code from reader 90, thereby resetting program service flipflop 110. The "zero" output of this flipflop then goes high and inhibits further operation of transmit gates 128.

The contents of cycle length register 118, provided from reader 90 as previously described, are supplied in

parallel to cycle counter 158. This counter is decremented by the one-pulse-per-second signal on line 101 from Master Clock 100. The purpose of counter 158 is to generate the reference time (T_r) at proper time intervals equal to the desired cycle length. The output of counter 158 is provided to common function comparator 126 and to offset display counter and lamp driver 160. The latter network provides interface to operate the digital display counter indicated in FIG. 1 by the reference numeral 94 which is also used to designate the block in FIG. 3B representing the display.

Lamp drivers 162 are used to detect and display on an optional, illuminated map the data transmitted to, or received from, the intersection controllers. The output of word decoder 152, besides providing data to the lamp drivers, is also provided on bus line 164 as an input to Detector Input Monitor Module 166 of FIG. 3C. The elements thus far described in FIGS. 3A and 3B are essentially disclosed in the aforementioned copending application. The elements which will now be discussed, shown in the FIG. 3C portion of the block diagram, are unique to the present system.

FIG. 3C illustrates in block diagram form the interconnection of a group of analog computer modules. It is the function of the computer modules to effect selection of program numbers, which are supplied to Program Memory Module 102 as a result of traffic actuation signals supplied to the computer modules. Traffic actuation signals from vehicle detectors located throughout the traffic control system are supplied to the master controller via the same transmission lines employed for sending data to the intersection traffic controllers located throughout the system. Word decoder 152 interprets the vehicle actuation signals and supplies this data on bus line 164 to Detector Input Monitor Module 166 via 12 terminals 168 through 179. The twelve output signals from Detector Input Monitor Module 166 are supplied, in parallel, to Traffic-Count Print Module 182, Density Computer Module 184, Volume Computer Module 186 and Speed Computer Module 188. Counter-printer device 82, shown also in FIG. 1 on the master controller front panel, is connected to the output of the Traffic-Count Print Module 182. The purpose of counter-printer 82 is to record the number of vehicles traversing designated vehicle detectors located throughout the traffic control system. Traffic-Count Print Module 182 acts as an interface between the signals supplied from Detector Input Monitor Module 166 and counter-printer device 82. Density Computer Module 184 determines traffic density by calculating the ratio of vehicle presence time to total time. For example, a continuous output from a vehicle detector will register 100 percent density, and no traffic actuations occurring during a given period of time will result in 0 percent density.

Volume Computer Module 186 calculates the number of vehicles in a given area of the traffic control system by automatically averaging multiple vehicle actuation signals supplied from Detector Input Monitor Module 166. Therefore, this module generates an analog output signal indicative of average traffic volume with respect to time. Speed Computer Module 188 calculates the average speed of traffic flow past one or more detectors, and thereby provides an analog output signal indicative of average speed with respect to time. The analog output signals supplied from the computer

modules will hereinafter be referred to generally as "traffic parameters".

The output of the Density Computer Module 184, Volume Computer Module 186, and Speed Computer Module 188 are each connected in parallel to 12 individual lines generally designated as bus line 190. Bus line 190 is connected to Ratio Computer Module 192. The function of the Ratio Computer Module is to calculate the expression $X/X+Y$, wherein X and Y represent two chosen analog signals of the same traffic parameter. To calculate the ratio, hereinafter referred to as RA, X and Y should both be selected from the same type of parameter, such as two density analog signals, two volume analog signals, two speed analog signals, or two aggregations of any of these analog signals. An example of the use of the expression $X/X+Y$ is to calculate the offset values for each of the intersections throughout the system. The variables X and Y would, therefore, be the traffic parameters for two opposing vehicular movements. Four output lines from Ratio Computer Module 192 are merged with bus line 190 and the combination is supplied, in parallel, to Meter-Record Output Module 194 and three Range Selection Modules 196, 197, and 198. Also, the program number, the program A, and the program B signals are supplied to inputs of the meter-record output module 194 from the program memory 102 via lines 195.

The outputs of Meter-Record Output Module 194 are connected to chart recorders 80, meters 78, and counter-printer 82a, of FIG. 1, to provide a graphical record of the magnitude of the traffic parameters on movable paper tape and provide a visual representation of the magnitude of the traffic parameters. It will be shown in the detailed description hereinafter of Meter-Record Output Module 194 that any of the parameters can be connected, via jumper lines, to any of meters 78. Also, a reference ramp is supplied to Range Selection Modules 196, 197, and 198 from a ramp generator circuit 200 contained within Timing and Display Module 202.

The outputs from Range Selection Modules 196, 197, and 198 are connected in parallel to Program-Range Selection Modules 204 via bus line 206. Also, this bus line is connected to range display circuit 208 contained within the Timing and Display Module 202. It is the function of the Range Selection Modules to systematize the signals supplied thereto into a hierarchy of discrete signals indicative of the magnitude of the analog signal occurring within a pre-selected "range". These discrete signals, hereinafter referred to as range-select signals, are employed within Program-Range Selection Modules 204 to thereby select a program number. The output signals from the Program-Range Selection Modules 204 are supplied to the Program Memory Module 102 on bus line 210.

Four signals (employed for inhibiting the selection of a traffic-actuated program) are supplied, in parallel, to Program-Range Selection Modules 204 and a display circuit 212 from Program-time Select Modules 98 on bus line 214. The display circuit 212 effects the illumination of an appropriate lamp during a time interval corresponding to the respective times for which each of the inhibit signals, designated T1, T2, T3 and T4, are in effect.

A second type of inhibit signal is supplied to Program-Range Selection Modules 204 to prevent the selection of two traffic-actuated programs in rapid suc-

cession. A minimum program interval timer 216 supplies these inhibit signals to Program-Range Selection Modules 204 via lines 218 and 219 for the A and B systems, respectively. Clock and timing signals are supplied to the complementary circuits of the computer group from clock generator and timing network 220 on line 222.

The following modules will be described individually in greater detail in the following order:

1. Master Clock
2. Detector Input Monitor
3. Density Computer
4. Speed Computer
5. Volume Computer
6. Traffic-Count Print
7. Ratio Computer
8. Meter-Record Output
9. Range Selection
10. Program-Time Selection
11. Timing and Display
12. Program-Range Selection
13. Program Memory

DETAILED DESCRIPTION OF THE MASTER CLOCK MODULE

FIGS. 4 AND 5

Master Clock Module 100 is a 7-day clock which supplies timing signals that can be employed in combinations to represent any time of day and the day of the week. A 60-cycle-per-second oscillator, synchronized to the AC supply voltage line, drives a series of counters which divide the oscillator output into seconds, minutes, hours, and ultimately days in a modified binary progression. A suggested layout of the master clock front panel, shown in FIG. 4 and designated generally by reference numeral 224, includes push-buttons for presetting the timing circuitry and also includes indicator lamps to provide a visual display of the time contained therein.

As shown on the front panel, four groups of indicator lamps are employed to represent minutes, hours, parts of a day, and days of the week. Lamps L10-L13 indicate minutes by the sum of the numbers adjacent each lamp illuminated. Lamps L14-L19 indicate hours in similar fashion. Lamps L20 and L21 are employed to indicate which half of the day is represented by the hours and minutes group of lamps. Lamps L22-L28 indicate the day of the week, Monday through Sunday, respectively. Also included on the front panel 224 are three push-buttons 226, 227 and 228 which are employed to actuate switches to advance the minutes counter, hours counter, and day counter, respectively. Thus, for example, Monday at 4:39 P.M. is represented by illumination of lamps L22, L18, L15, L13, L10 and L21. Each depression of the push-button 226 will advance the minutes counter by 1; each depression of push-button 227 will advance the hours counter by 1; and each depression of push-button 228 will advance the day counter by 1.

FIG. 5 illustrates Master Clock Module 100 in block diagram form. An AC input of 60 cycles per second is provided on a terminal 230 to oscillator 232. Provision for battery power (not shown) allows the oscillator to free-run about 5 percent slower than the 60 Hz line frequency during periods of AC power interruption. However, when AC power is restored, the oscillator is again synchronized to the line frequency and any necessary

adjustments may be effected by operation of push-buttons 226, 227 and 228. The output of oscillator 232 is applied to counter 234 which divides the signal applied thereto by 60 and produces a signal with a pulse repetition rate of 1 cycle per second on line 101. The 1-cycle-per-second signal on line 101 is supplied, simultaneously, to gating network 236 and a divide-by-60 counter 238. Counter 238 supplies a 1-cycle-per-minute output signal on line 240 which is applied simultaneously to counter 242 and counter and decoder network 244. Counter 242 divides the signal applied thereto by 2 and produces a signal on line 246 which has a pulse repetition rate of 1 cycle per 2 minutes. The minutes counter and decoder network 244 accepts the 1-cycle-per-minute timing signal on line 240 as an input, and produces a plurality of timing signals within the network which are supplied to output lines 248-253. The pulse repetition rate of the signals supplied to lines 248-253 are 1-cycle-per-2-minutes, respectively through 1-cycle-per-60-minutes. Lamps L10-L15 are connected between lines 248-253, respectively, and a source of positive voltage on terminal 254. Push-button 226 is connected as a second input to counter 244. Each operation of this push-button switch causes the minutes counter to advance by a count of one.

The signal supplied on the line 251, which corresponds to the 1-cycle-per-15-minute timing signal is also supplied as an input to the network 236. The combination of the two input signals applied to the network 236 will produce a half-second pulse on each of output lines 256 and 258 with their respective leading edges separated by a one-second interval every fifteen minutes. The signals on lines 256 and 258 are employed as strobe signals within the complementary modules of the master controller to differentiate A system data from B system data. Diodes are connected within gating network 236, and in series with the output lines 256 and 258, to allow the clamping of the output signals on these lines to positive potential by signals from complementary modules within the master controller.

The 1-cycle-per-60-minute signal supplied to the line 253 is supplied as an input to counter and decoder network 260. Network 260 divides the 1-cycle-per-60-minute signal, accordingly, to produce a plurality of timing signals on lines 262-267. These signals correspond to the 1-hour through 8-hour timing signals, plus the A.M. and P.M. signals. Lamps L16-L21 are connected between the lines 262-267, respectively, and a source of positive voltage. Push-button 227 is connected as a second input to network 260. Each operation of push-button 227 will advance the counter within network 260 by one.

The signal on line 267 that indicates the second half of a day (P.M.) is supplied as an input to counter and decoder network 268 which divides the one-half-a-day signal (P.M.) into timing signals which correspond to days of the week. The output of the network 268 is supplied on lines 270-276 to indicate the days Monday through Sunday, respectively. Lamps L22-L28 are connected between the lines 270-276, respectively, and a source of positive voltage on terminal 278. Push-button 228 is provided as a second input to counter and decoder network 268. Each operation of this push-button will advance the counter within network 268 by one.

DETAILED DESCRIPTION OF DETECTOR INPUT MONITOR MODULE

FIGS. 6, 7, 8, 9, AND 10

The primary purpose of the Detector Input Monitor Module is to accept signals from vehicle detectors located throughout the traffic control system. Normally, one such module would be provided for each of systems A and B. These actuation signals are transmitted from the respective intersection traffic controllers via the same transmission lines which the master controller employs to transmit data to the respective intersection controllers. The function of this module is to provide an interface between a number of detector channels (the disclosed embodiment shows 12 channels) to allow signals generated by the vehicle detectors to be periodically sampled for use by various computer modules, and to determine whether each individual vehicle detector is operating properly.

FIG. 6 illustrates a suggested layout for the front panel 280 of Detector Input Monitor Module 166. Connector 282 accepts bus line 164 which supplies the vehicle detector actuation signals from the respective intersection traffic controllers as mentioned hereinabove. Lamps L30-L41 indicate the status of the 12 detector channels. An illuminated lamp will indicate the presence of a vehicle at the respective vehicle detector. A flashing lamp will indicate a detector failure, or that no detections have been registered during the programmed sampling time, as explained further hereinafter. Each of the twelve detector input channels have two program pin slots designated ON and OFF. The earlier referenced U.S. application Ser. No. 5,068 contains a full disclosure of a convenient means for programming traffic control devices wherein programming networks are provided on printed circuit boards arranged in abutting relation to openings in a panel face. Pins having resilient, conducting end portions are inserted through selected openings to engage the edge of the printed circuit board, thereby acting as a switch to effect electrical connection between otherwise unconnected portions of the circuit thereon. Although not described further herein, it will be understood that references to program pins, slots and the switches provided thereby, denote the same structure and operation disclosed in the earlier application. Reference numerals S10-S21 designate the program pin slots shown in FIG. 6 and are also used to denote the schematic representation of program pin switches shown in FIG. 7 for the 12 channels. The ON program pin slot is used in testing or in simulating calls from the individual detectors. The OFF program pin slot has the capability of disabling the logic circuitry of an unused detector channel.

The primary purpose of Detector Input Monitor Module 166 is to allow automatic deletion from use in traffic activity calculations of vehicle detector inputs which do not change for prolonged periods. This may occur because of detection failure, a blocked traffic lane or a vehicle stalled over a detector. For example, a car stalled over a vehicle-detector loop will provide a continuous actuation signal, and a disconnected, or open, vehicle detector will not indicate any traffic activity. These two conditions will produce 100 percent or 0 percent vehicle density, respectively. Therefore, a provision is made in module 166 to program a time interval to periodically reset the detector monitor cir-

cuitry. This period of time is designated the ACTIVITY SAMPLE PERIOD herein. Switches S22-S25 are employed either individually or in combination to program the length of the ACTIVITY SAMPLE PERIOD (in minutes). Switch S26 is employed to double the ACTIVITY SAMPLE PERIOD of time, if desired.

FIG. 7 illustrates Detector Input Monitor Module 166 in block diagram form. A 1-cycle-per-2-minute timing signal, which is generated within Master Clock Module 100, is supplied to counter and comparator network 284 via line 246. Switches S22-S25, which program the ACTIVITY SAMPLE PERIOD, are shown as inputs to network 284 from a source of positive voltage. Switch S26, which doubles the ACTIVITY SAMPLE PERIOD, is also indicated as an input from a source of positive voltage. The output signal from network 284, which is the detector monitor circuit reset pulse, is supplied to circuits 286-297 on line 298. The 1-cycle-per-second signal which was produced within Master Clock Module 100, is supplied on line 101 and is connected in parallel to the detector monitor circuits 286-297. The 12 vehicle detector actuation signals are supplied as inputs to the detector monitor circuits 286-297 on lines 300-311, respectively.

The ON program pin for each of the detector input monitor channels may be connected between the input lines 300-311 and ground potential. The OFF program pin for each of the channels may be connected between circuits 286-297 and a source of positive voltage from terminal 312. Also, lamps L30-L41 are connected between the circuits 286-297 and terminal 312. The output from each of circuits 286-297 is supplied on lines 314-325, respectively. The operation of network 284 and circuits 286-297, with their complementary switches and lamps, will be more readily understood from the description of the logic illustrated in FIGS. 8, 9 and 10.

Counter and comparator network 284 is illustrated in the detailed logic diagram of FIG. 8. Switches S22-S25 are connected between a source of positive voltage and comparator circuit 326. Switch S26 is connected in series between a source of positive voltage and AND gates 328 and 330. The small circle on the input of gate 328 indicates that the negation of the signal applied thereto is required for operation of the input of the gate. The 1-cycle-per-2-minute timing signal, produced within Master Clock Module 100, is supplied on line 246 which is connected in parallel to the inputs of AND gates 328 and 330. The 1-cycle-per-2-minute signal on line 246 is also connected to the toggle input of flipflop 332. The 1 output of flipflop 332 is connected to a third input of AND gate 330. The outputs of AND gates 328 and 330 are connected, respectively, to the two inputs of an OR gate 334. The output of OR gate 334 is applied, in parallel, to the inputs of a pair of AND gates 336 and 338. The output of comparator network 326 is connected in parallel to an input of each of gates 336 and 338. The output of gate 336 is applied to the SET input of 4-bit counter 340. The output of gate 338 is applied to the toggle input of counter 340. The output of the flipflops contained within counter 340 are connected in parallel to comparator network 326.

In operation, assume that a program pin is inserted to effect closure of switch S25, thereby applying a positive voltage at an input, corresponding to 16 minutes, of the comparator network 326. Also assume that switches S22, S23, S24 and S26 are not connected. Therefore,

the input to gate 328 from switch S26 is placed into a true state since a false signal is required for operation of this gate. The 1-cycle-per-2-minute signal supplied on line 246 will pass through gate 328 to an input of OR gate 334. The input to gate 330 from switch S26 is in a false condition and will inhibit the operation of this gate. The signal supplied from the output of OR gate 334 will be identical to the signal applied to line 246, that is, 1-cycle-per-2-minutes. This signal is applied to gates 336 and 338. The second input to gates 336 and 338 is supplied from comparator network 326. The output signal from gate 336 is supplied to the set input of the first flipflop within counter 340. This signal is also employed within the detector monitor circuits 286-297 and is supplied on line 298.

In the example under discussion, let us assume that counter 340 has been placed into an initial condition by a signal from gate 336. A value of 16 minutes is represented as an input to one side of comparator network 326 by insertion of a program pin to close switch S25. A disparity of contents within comparator network 326 now exists, and the output signal therefrom is at a low level. Therefore, the input to gate 338 from comparator 326 is placed into a true condition, since an inverted signal is required for operation of the gate. The output of AND gate 338 will consist of the 1-cycle-per-2-minute signal from OR gate 334. Counter 340 will increment, over a period of time, until a count of 16 is reached, whereupon the disparity within comparator 326 will no longer exist. At this time, the output of the comparator will change to a true level and AND gate 338 will now be inhibited. However, AND gate 336 will be enabled and pass the 1-cycle-per-2-minute signal from OR gate 334. The period of time that AND gate 336 will be enabled is limited to one pulse, which is due to the fact that counter 340 is restored and a disparity of values contained within comparator 326 again exists. This cycle of operation will repeat itself ad infinitum unless changed by external means. Thus, the signal produced on line 398 is a short pulse having a repetition rate equal to that programmed by switches S22-S25.

If it is desired to double the activity sample period, a program pin is inserted into the proper slot to close switch S26 to apply a positive voltage to the inputs of AND gates 328 and 330. The input of AND gate 328, from switch S26, will disable this gate since the negation of the signal applied thereto is required. However, the input to AND gate 330 from switch S26 is in a true state. The 1-cycle-per-2-minute signal applied on line 246 is connected directly to a second input of AND gate 330. The toggle input "T" of flipflop 332 requires the negation of the signal on line 246 for operation thereof. Also, flipflop 332 will effectively divide the signal applied thereto by 2. Therefore, the output of flipflop 332 will have a pulse repetition rate of 1-cycle-per-4-minutes. The output of AND gate 330 will be a short pulse having a repetition rate of 1-cycle-per-4-minutes.

FIG. 9 illustrates the time relationship of the signals applied to AND gate 330 and the output therefrom. The timing signal applied on line 246 of 1-cycle-per-2-minutes is illustrated in FIG. 9 by the waveform 342. Since the toggle input to flipflop 332 requires an inversion of the signal applied thereto for operation thereof, the signal supplied at the output of flipflop 332 will be shifted in time by the duration of the timing pulse applied on line 246. The waveform 344 in FIG. 9 illus-

trates the 1-cycle-per-4-minute signal at the output of flipflop 332, which has been shifted in time by one pulse of waveform 342. The waveforms 342 and 344 represent the signals applied to two of the inputs of AND gate 330. The third input of AND gate 330 is at a constant high level due to closure of switch S26. Therefore, the output signal of gate 330 will have a pulse repetition rate of 1-cycle-per-4-minutes as illustrated by waveform 346. The signal from AND gate 330 will pass through OR gate 334 unaltered. The operation of counter 340, comparator 326 and AND gates 336 and 338 will be the same as discussed hereinabove. However, the time required for counter 340 to reach a state equal to that programmed in switches S22-S25 will be twice as long as the operation without the closure of switch S26.

FIG. 10 illustrates, in detailed logic form, an individual detector monitor circuit 286. The signal produced on line 298 from AND gate 336 is applied to the "reset" input of flipflop 348 and to AND gate 350. The reset input of flipflop 348 inverts the timing signal applied thereto. Also, a dynamic or transitional signal is required at each of the inputs to flipflop 348 for operation thereof. The act of resetting flipflop 348 resets the detector monitor circuit, which initiates the beginning of an ACTIVITY SAMPLE PERIOD.

A signal supplied from the individual vehicle detector in the first channel is applied on line 168 (FIG. 3C). Switch S10 which corresponds to the ON program pin for the first detector channel may be connected between line 168 and ground potential. Line 168 is connected in parallel to delay networks 352 and 354 which act to filter noise from signals applied thereto. Line 168 is also connected to the set input of flipflop 348, the function of which is to store vehicle detector signals in the flipflop. The outputs of delay networks 352 and 354 are applied, respectively, to two inverting inputs of AND gate 356. These two input signals are inverted, as indicated by the small circles. The third input of AND gate 356 is connected to latch 358, consisting of two NOR gates, 360 and 362. The 1 output of flipflop 348 is connected to an input of NOR gate 360. The 0 output of flipflop 348 is connected to the second input of AND gate 350. The output of AND gate 350 is connected to an input of NOR gate 362. The output of NOR gate 362 is connected to a second input of NOR gate 360. The output of NOR gate 360 is connected to a second input of NOR gate 362. The third inputs of NOR gates 360 and 362 are connected to switch S11, which corresponds to the OFF program pin of detector channel 1. Closure of switch S11 applies positive voltage to the inputs of NOR gates 360 and 362. The output of NOR gate 360 is also connected to an input of NOR gate 364 and to an input of AND gate 366. The second input to AND gate 366 is the 1-cycle-per-second timing signal which was produced within Master Clock Module 100 and supplied on line 101. The output of NOR gate 362 is the output of latch 358 which is connected to the third input of AND gate 356. The outputs of gates 356 and 364 are tied together via line 368. This line is also connected to an input of OR gate 370. The output of AND gate 366 is connected to the second input of OR gate 370. The output of OR gate 370 is connected to lamp driver 372 which is further connected to lamp L30 (shown also in FIGS. 6 and 7) and positive voltage. The output of detector monitor circuit 286 is supplied

on the line 314 which is connected to the common outputs of gates 356 and 364.

Detector monitor circuit 286, as shown in FIG. 10, operates from three individual input signals. The 1-cycle-per-second timing signal is supplied to gate 366, the reset timing pulse is supplied to the reset input of flipflop 348, and the actuation signals from a vehicle detector are supplied on line 168. The signal on line 168 is normally at a high level until a vehicle passes over the loop of the vehicle detector, whereupon the voltage level on this line drops to ground potential as indicated by the waveform above line 168 in FIG. 10. The delay network 352 acts to filter out any noise which may accompany the leading edge of the actuation signal. Simultaneously, trailing edge delay 354 will allow the actuation signal to pass unaltered. The actuation signal on line 168 is also applied as an input to flipflop 348. Since the set input to this flipflop requires a negative dynamic signal for operation thereof, the flipflop will be placed into a set condition as a result of the first negative transition of the actuation signal, and the 1 output will be at a high level.

Let us assume in the example under discussion that there is no program pin inserted into either switch S10 or S11. The high level of the 1 output of flipflop 348 will cause the output of NOR gate 360 to drop to a low level. The 0 output of flipflop 348 will drop to a low level and the output of AND gate 350 will also drop to a low level. Therefore, all three inputs to NOR gate 362 are at a low level and the output thereof will go to a high level. The high level output signal from NOR gate 362, in conjunction with a low level output from delay networks 352 and 354 will, in turn, enable AND gate 356. The output of this AND gate will rise to a high-level which will enable OR gate 370 and thereby operate lamp driver 372 to illuminate lamp L30. Simultaneously, the signal on line 314 goes to a high level.

The restoring signal from counter and comparator network 284 will place flipflop 348 into a reset state. The 0 output of the flipflop will now be at a high level, and one of the inputs to AND gate 350 will be in a true state. However, the second input to AND gate 350 will not be in a true state simultaneously with the first input. This condition will exist only when the flipflop was previously in a set state. If the flipflop was previously in a reset state, gate 350 would have been enabled at the time of the occurrence of the restoration pulse on line 298. The purpose of connecting gate 350 in this fashion is to change the state of latch 358 when no vehicle has been detected during the activity sample period.

Assume, for illustrative purposes, that no actuation signal had been received on line 168 between two consecutive reset pulses on a line 298. The 0 output of flipflop 348 would be at a high level, and coincidence of a true state on the two inputs to gate 350 would occur. The output of gate 350 would go to a high level which would cause the output of NOR gate 362 to go to a low level. Since the 1 output of flipflop 348 was at a low level (flipflop 348 was previously reset), and switch S11 was not connected, then the output of NOR gate 360 will go to a high level when the output of NOR gate 362 goes to a low level. A high level on the output of NOR gate 360 will cause the signal on line 314 to go to a low level. Inverter 364 is capable of producing a low-level output signal only. The input to AND gate 366 from NOR gate 360 will be at a high level, and the 1-cycle-per-second signal on line 101 will be passed

through gate 366. The 1-cycle-per-second signal is applied to OR gate 370 which will modulate lamp driver 372 and cause lamp L30 to blink. A subsequent actuation signal applied on line 168 will place circuit 286 back into a set condition, and a high level signal will be supplied on line 314.

If a program pin is inserted to close switch S10, circuit 286 will initially go into a set state. However, since the set input to flipflop 348 requires a transition of the signal applied thereto from a high level to a low level for operation, flipflop 348 will go into a set state only when a program pin is first inserted into switch S10. A reset signal on line 298 will reset flipflop 348 and operation of the circuit will continue as described hereinabove for as long as the program pin remains inserted in switch S10. Removal of the program pin will not affect the circuit 286.

A program pin inserted into switch S11 will apply positive voltage to an input of NOR gates 360 and 362. This, in turn, will cause the outputs of these NOR gates to go to a low level. The output of NOR gate 364 is incapable of producing a high-level output signal. Since the output of AND gate 356 is not high, and the output of NOR gate 364 is unable to produce a high-level signal, the voltage level on line 314 will "float" somewhere between a zero level and a high level. The purpose for this intermediate level signal on line 314 will be explained in greater detail in connection with the discussion of Density Computer Module 184. Since both inputs to OR gate 370 are low, lamp L30 will not be illuminated. This condition is designated OFF, and is employed to disable a detector monitor circuit when the detector channel is not in operation. This condition also exists when the circuit is operative, and a low-level signal does not exist at the input on line 168.

DETAILED DESCRIPTION OF THE DENSITY COMPUTER MODULE

FIGS. 11, 12, 13, 14, 15 AND 16

Density Computer Module 184 accepts actuation signals from the Detector Input Monitor Module 166 indicative of vehicle presence detection. The term "density" as used herein is defined as the ratio of the summation of the time during which a vehicle detector indicates presence to total elapsed time, i.e.,

$$d = (\Sigma \text{ Vehicle Presence Time}) / (\text{Total Time})$$

More particularly, the density figure represents a percentage of a time interval that an individual vehicle detector (or an aggregate of vehicle detectors) registers vehicle presence. The signal produced at an output of the Density Computer Module is an analog output voltage proportional to the traffic density.

FIG. 11 illustrates a typical front panel 374 of Density Computer Module 184. The twelve individual output signals of Detector Input Monitor Module 166 on lines 314-325 are supplied as inputs to the Density Computer Module, and are supplied to four groups of program pin switches on the face of panel 374. These program pin switches are designated S27-S38 for the first of four groups shown on the panel. The remaining three groups of program pin switches are indicated, in a similar fashion, by S39-S74.

Four individual density computer circuits are provided in the disclosed embodiment of Density Computer Module 184 and four program pin switches are disposed for connecting actuation signals as inputs to

each of the four density computers designated D1-D4. Density computer D1 has the four program pin switches S75-S78 as inputs thereto; density computer D2 has switches S79-S82 as inputs thereto; density computer D3 has switches S83-S86 as inputs thereto; and, density computer D4 has switches S87-S90 as inputs thereto. The output of the density computers D1, D2, D3, and D4 are represented by switches S91-S94. The 12 program pin switches S95-S106 are disposed for connecting, via jumper wires, signals from the density output switches S91-S94 to bus line 190 which connects to complementary modules of the master controller, as previously described.

The amount of time required for the density computer to "respond" to a change in the density of traffic is designated herein as RESPONSE TIME. Switches S107-S110 represent 1, 2, 4 and 8 minutes, respectively, of response time which can be programmed. The purpose of the program pin switches as shown in FIG. 11, will be more fully understood from the detailed description of the density computer hereinbelow.

FIG. 12 illustrates Density Computer Module 184 in block diagram form. Switches S107-S110 are connected, in parallel, between a source of positive voltage on terminal 376 and response counter and comparator network 378. The response counter is designed to reset to an initial value of 1 when a restoring signal is supplied thereto. Timing signals are supplied to terminal 380 which will act to increment the counter. This timing signal is designated clock 2, and has a square wave period of 2 milliseconds. The derivation of this timing signal will be described in greater detail hereinbelow. Output signals from response counter and comparator network 378 are supplied to density computers D1-D4 via the lines 382 and 384.

Each density computer D1-D4 employs a clock 1 timing signal which is supplied to a terminal 386. Clock 1 timing signal has a square wave period of 250 microseconds, and the derivation thereof will be described in greater detail hereinbelow. Switches S75-S90 are shown as input connections to density computers D1-D4, respectively. Switches S91-S94 are connected to outputs of the density computers D1-D4, respectively. The program pin switches under the headings of DETECTOR and LINE are not directly connected to the circuitry of Density Computer Module 184. Switches S27, S39, S51, and S63 are the first switches in each of the four groups, under the heading of DETECTOR in FIG. 11, and are all connected to line 314 of Detector Input Monitor Module 166. The remaining 11 switches in each group are connected, in groups of four corresponding switches, to lines 315-325. Switches S95-S106 are the 12 switches under the heading LINE in FIG. 11.

The program pins at the input and output of the Density Module are not employed in the same manner as those program pins used for other functions. These program pins are connected to a wire which can form a conductive "jumper" between two program pin switches. For example, the output of the Detector Input Monitor Module, indicative of vehicle actuation signals, is supplied to the first program pin under DETECTOR, i.e., S27. A flexible wire with program pins connected to both ends thereof can be employed to effect the conduction of the signal supplied from one of the detector input channels to one of the density computer input switches. More particularly, this jumper could be

employed to connect detector channel number 1 (wire 314) to the first switch (S75) of density computer D1. This connection will effect the conduction of vehicle detector actuation signals from detector channel number 1 to density computer D1 via the flexible conductor. A similar flexible conductor with program pins attached thereto may be employed to connect the output of density computer D1 to an output line such as Line 1 (S95). These jumpers are similar to patch cords except for the ability of the pin at either end to perform a single pole switch closure when inserted.

It should be pointed out that four detector input signals can be supplied to an individual density computer. These signals are summed within the respective density computers to generate one output signal therefrom. This feature provides the capability of summing all vehicle actuation signals on four lanes of traffic for one traffic thoroughfare. Program pins may be inserted in switches S107-S110 to provide for a response time desired by the programmer. This time is indicative of the rate at which the density computer output will respond to a change in the density of traffic. The function of these and the remaining program pins will be explained in greater detail hereinbelow.

Response counter and comparator 378 is illustrated in greater detail in FIG. 13. The 2 millisecond clock 2 timing pulse is applied as an input to two AND gates 388 and 390. As indicated by the arrowhead and small circle at the input of gate 390, the input supplied thereto must be a negative transitional signal for operation thereof. The output of AND gate 390 is supplied at the toggle input T to 4-bit binary counter 392. The output of AND gate 388 is also supplied on line 382. The negative transition of the signal on line 382 is passed through OR gate 394 to the set S1 input of counter 392. As was mentioned hereinabove, binary counter 392 is reset to an initial value of 1 when a restoring signal is applied thereto. The signal supplied to input S1 is the restoring signal mentioned earlier. The output of 4-bit binary counter 392 is supplied to one side of comparator network 396. Switches S107-S110 are connected in parallel between positive voltage from terminal 398 and the other side of comparator 396. The output of comparator 396 is supplied as the second input to AND gates 388 and 390. Also, the output of comparator 396 is supplied on line 388; the use of this signal will be explained in greater detail hereinbelow.

Assume, for example, that counter 392 is in a set condition (which is, by design, a binary count of 1). The output of comparator 396 will be low if a binary count other than 1 is programmed in the switches S107-S110. AND gate 390 will be enabled on the negative transitions of the clock 2 timing signal at terminal 380 which will increment counter 392. The contents of the counter will increase until a value is reached which equals that programmed in the switches S107-S110. When the output of comparator 396 goes high, AND gate 390 is disabled. However, AND gate 388 will now be enabled and the next clock 2 timing signal will pass therethrough. The first negative transition of the clock 2 signal will pass through the inverting OR gate 394 to set counter 392 to a value of 1. The output of comparator 396 will drop to a low level since counter 392 is restored. If no program pins were inserted into switches S107-S110, then it would require 16 negative transi-

tions of clock 2 before output signals would be supplied on lines 382 and 384.

The output signals on lines 382 and 384 of network 378 are transmitted to the density computer D1-D4 as shown in FIG. 12. The signal on output line 382 consists of a positive pulse with a repetition rate equal to the value programmed in the switches S107-S110, multiplied by 2 milliseconds. This is due to the fact that the counter is incremented to a count equal to that programmed in the switches by the clock 2 timing signal, which has a repetition rate of 2 milliseconds. The output signal on line 384 differs from the signal on line 382 in that it is not clocked. The signal on line 384 is the same as the output signal supplied from comparator 396. If a value of one is programmed in switches S107-S110, then the output of the comparator would be a continuous signal, since counter 392 is always reset to a value of 1.

FIG. 14 illustrates a portion of the density computer D1, in logic diagram form. This circuit has the function of sequentially sampling the four vehicle actuation inputs supplied to the density computer on switches S75-S78. The signal generated within response counter and comparator 378 on line 382 is supplied as an input to OR gate 400. Clock 1 timing signal, which has a pulse repetition rate of 250 microseconds, is supplied at terminal 386 as an input to AND gate 402. The second input of AND gate 402 is connected to the output of NOR gate 404.

The output of AND gate 402 is connected to the second input of OR gate 400. The output of OR gate 400 is connected to the toggle T input of 2-bit counter 406. The output of counter 406 is supplied in binary form on lines 408 to decoder 410, and the output of the decoder is connected to a plurality of AND gates for decoding the binary output. The output signal of the decoder on line 412 is indicative of a count of 1; the signal on line 413 is indicative of a count of 2; the signal on line 414 is indicative of a count of 3; and the signal on line 415 is indicative of a count of 4. These output lines are connected as inputs to two AND gates each.

The line 412 supplies an input enabling signal to AND gates 416 and 418. Line 413 supplies the input enabling signal to AND gates 420 and 422; line 414 supplies the input enabling signal to AND gates 424 and 426; and line 415 supplies the input enabling signal to AND gates 428 and 430. The outputs of AND gates 416, 420, 424 and 428 are connected as inputs to NOR gate 404.

Switch S75 is connected to the second input of AND gates 416 and 418; switch S76 is connected to the second input of AND gates 420 and 422; switch S77 is connected to the second input of AND gates 424 and 426; switch S78 is connected to the second input of AND gates 428 and 430. AND gates 418, 422, 426, and 430 require a higher minimum input voltage than AND gates 416, 420, 424, and 428 for operation thereof. The purpose for the differences in the input threshold levels for these AND gates will become evident from the description below. The outputs of AND gates 418, 422, 426 and 430 are connected to the input of NOR gate 432, and the output of NOR gate 432 is supplied on line 434.

The vehicle detectors employed in this traffic control system are of the loop type similar to that disclosed in U.S. Pat. No. 3,373,374 of G. Marosi. The nature of an actuation signal from the vehicle detector is ground po-

tential to represent vehicle presence and a high level signal to represent vehicle non-presence. It is an inherent characteristic of the vehicle detector to produce a constant actuation signal (ground potential) if a vehicle is stopped over the loop. However, it is pointed out that the vehicle detector actuation signals are inverted within the Detector Input Monitor circuitry. A high voltage level indicates vehicle presence, and an intermediate voltage level indicates vehicle non-presence. A low level signal, such as ground potential, indicates detector failure.

In operation, the output of decoder 410 enables a pair of AND gates sequentially. Assume, for example, that jumpers are connected between switches S27 (FIG. 12) and S75, switches S28 (FIG. 12) and S76, switches S29 (FIG. 12) and S77, and between switches S30 (FIG. 12) and S78. The first four actuation signals from Detector Input Monitor Module 166 will be applied to switches S75-S78, respectively. This could represent vehicle detectors located in four lanes of traffic traveling in one direction. Also, assume that counter 406 contains a binary count of 1, then decoder 410 will supply a high level signal on line 412. The first inputs to AND gates 416 and 418 are now at true state. If a vehicle actuation signal (a high level signal) is supplied to switch S75, gates 416 and 418 will be operative. The outputs of these gates will effect the generation of false outputs from NOR gates 404 and 432. If the output of NOR gate 404 is low, then AND gate 402 is disabled which will, in turn, disable the input to OR gate 400. This condition will remain unchanged until either the actuation signal disappears, or an advance pulse is supplied on line 382.

Since the inputs to AND gate 418 are connected in parallel with the inputs to gate 416, gate 418 will operate simultaneously with gate 416 for the example given herein. A vehicle actuation signal applied to switch S75 will cause the output of gate 418 to rise to a high level. This, in turn, will disable NOR gate 432 and cause the signal on line 434 to drop to a low level. As will be shown hereinbelow, a low level signal on line 434 will add to the density signal produced within the Density Module, and a high level signal on line 434 will subtract from the density signal produced herein.

If switches S75-S78 are connected in the same fashion as the example given hereinabove, the non-presence of an actuation signal will cause the signal level on line 434 to go to a high level state. As mentioned earlier, AND gates 418, 422, 430 have a higher minimum threshold voltage requirement for operation. An intermediate voltage level applied to switch S75 will enable AND gate 416, but will not enable AND gate 418. The output of AND gate 416 will be high which, in turn, will stop the incrementation of counter 406. The output of AND gate 418 will be low, and the output of gates 422, 426 and 430 will also be low which will, in turn, enable NOR gate 432 to produce a high level signal on line 434. If the vehicle detector supply actuation signals to switch S75 had failed, as detected by the Detector Input Monitor Module 166, a low level signal would be supplied to switch S75. This low level signal will disable AND gate 416 and will also disable AND gate 418. NOR gates 404 and 432 will both be enabled, and a clock 1 pulse on terminal 386 will step the counter to a value which will enable the next pair of AND gates. In effect, if a vehicle detector had failed, counter 406 with the accompanying circuitry will by-

pass this vehicle detector input. Switches S76, S77 and S78 with their respective AND gates operate in the same fashion as discussed hereinabove.

This operation, together with the operation of the response time logic described earlier, results in equal sampling of the state of all unfailed detector inputs which may have been connected to the four respective density computer inputs. The density value derived therefrom is proportional to the average of the individual detector densities.

FIG. 15 illustrates the density integrator circuit in schematic form. The signal supplied on line 434 (FIG. 14) is applied to terminal 436. A pair of resistors R12 and R14 are connected in series between terminal 436 and ground potential. A second pair of resistors R16 and R18 are connected in series between terminal 436 and a +15 volt supply on terminal 438. The base of an NPN transistor Q10 is connected to the junction of resistors R12 and R14. The emitter of Q10 is connected to ground potential, and the collector is connected to terminal 440. The base of PNP transistor Q12 is connected to the junction between R16 and R18. The emitter of Q12 is connected to terminal 438, and the collector is connected to terminal 440. Resistor R20 is connected in parallel with transistor Q10, more particularly, between the terminal 440 and ground potential.

Resistor R22 is connected between terminal 440 and the gate terminal (G) of a field effect transistor (FET) Q14. The drain terminal (D) of the FET Q14 is connected to terminal 440. The anode of diode CR10 is connected between the gate terminal of FET Q14 and the cathode thereof is connected to terminal 442. The anode of diode CR-12 is connected to line 384 and the cathode thereof is connected to terminal 442. Resistor R23 is connected between terminal 442 and the -15 volt supply on terminal 444. Rheostat R24 and Resistor R26 are connected in series between terminals 446 and the source terminal (S) of FET Q14. Capacitor C10 is connected between terminal 446 and ground potential. The positive input of a non-inverting voltage following amplifier A10 is connected to terminal 446. Resistor R28 is connected between the negative input terminal of amplifier A10 and ground potential. Amplifier A10 receives external power from the +15 volt supply via line 448 and from the -15 volt supply on line 450. The output of amplifier A10 is connected to switch S91, which is the output of density computer D1. Also, the output of amplifier A10 is fed back to the negative input thereof via rheostat R30.

The function of the circuit in FIG. 15 is to integrate the actuation signals supplied on terminal 436 and to supply on analog output signal commensurate with traffic density to switch S91. The ratio of the charge accumulated on capacitor C10 to the total supply voltage of 15 volts is employed herein to represent density. Capacitor C10 has a charge path through rheostat R24, resistor R26, FET Q14, and transistor Q12. Capacitor C10 discharges through rheostat R24, resistor R26, FET Q14, and transistor Q10. FET Q14 modifies the RC charge of discharge time constant. The signal produced within the counter and comparator 378, and provided on line 384, is supplied to the anode of diode CR 12. This signal acts to turn on FET Q14 to allow conduction between the drain and source terminals thereof. Since transistor Q12 is a PNP transistor and Q10 is an NPN transistor, when terminal 436 has a high

level signal applied thereto, transistor Q10 will turn on and transistor Q12 will turn off. This will provide a conductive path between the drain of FET Q14 and ground. If the signal applied to terminal 436 is a low level signal, transistor Q12 will turn on and Q10 will turn off. This will provide a conductive path between the +15 volt supply and the drain terminal of FET Q14. It can be seen from the explanation hereinabove that the output of NOR gate 432 controls the selection of either transistor Q10 or Q12. FET Q14 is turned on for a short period of time, 2 milliseconds, each time comparator 396 supplies a high level output signal.

The rate at which the charge accumulates on capacitor C10 is determined first by the frequency of pulses supplied on line 384, secondly by the setting of rheostat R24, and thirdly, by the state of the signal applied to terminal 436. More particularly, the response time of the computer is equal to one RC time constant, wherein the resistance consists of R24 and R26, and the capacitance consists of C10. The switching of FET Q14 multiplies the RC time by a factor dependent upon the response time programmed. The voltage potential between terminal 446 and ground potential is supplied to the positive input of amplifier A10. The output of amplifier A10 is a function of voltage with respect to time, wherein the voltage is representative of density over this period. Resistor R30 is employed to scale the voltage output of amplifier A10 to a desired range of operation.

FIG. 16 illustrates the timing relationship between the signals supplied to terminals 436 and line 384 to the charge that accumulates on capacitor C10. Waveform 452 illustrates a series of two millisecond pulses having a repetition rate determined by the value programmed in switches S107-S110, which is indicative of response time. This signal is supplied to line 384 and acts to switch FET Q14 on and off. Waveform 454 illustrates the signal supplied to terminal 436 which is an aggregate of the four vehicle actuation signals supplied to switches S75-S78. As was mentioned hereinabove, a low level signal supplied from NOR gate 432 to terminal 436 is indicative of vehicle presence, and a high level signal supplied therefrom is indicative of vehicle non-presence. The waveform 456 is purely random function due to the fact that vehicles crossing detector loops are a random function. Waveform 456 illustrates a function of voltage across C10 with respect to time. The vertical scale of waveform 456 and the horizontal scale of waveform 454 are exaggerated for illustrative purposes.

In operation, a low level signal supplied to terminal 436, as shown by waveform 454, at time t_1 will turn Q12 on. The timing pulse supplied on line 384, as shown by waveform 452, at time t_1 will turn FET Q14 on. Capacitor C10 has a charge path via the emitter to collector of Q12, the drain to source of FET Q14, and through resistor R26 and R24. As shown in waveform 456, the charge on capacitor C10 builds up at an exponential rate. At the end of the 2 millisecond timing pulse, Q14 is turned off and capacitor C10 has neither a charge nor discharge path (neglecting leakage and amplifier bias currents). Therefore, the charge will remain constant until the next timing pulse. As shown by the combination of waveforms 452 and 454, a charge is added to capacitor C10 at points t_2 , t_3 , and t_4 . At time t_5 a non-presence signal is supplied to terminal 436 as shown by waveform 454. At this time, transistor Q10

will be turned on and capacitor C10 will have a discharge path through resistors R24 and R26, source to drain of FET Q14, and collector to emitter of Q10. At time t_5 , waveform 456 shows an exponential decay of the charge across capacitor C10. A time t_6 , a vehicle non-presence signal is again supplied to terminal 436 and capacitor C10 will discharge additionally. Timing pulses on waveform 452 at times t_{20} through t_{24} are also shown, to indicate that the charge and discharge of capacitor C10 continues in a similar fashion.

The function of voltage versus time, as illustrated by waveform 456, is supplied to the non-inverting input of amplifier A10. The signal supplied to A10 is not inverted, but undergoes a small amount of amplification. Therefore, the signal supplied to switch S91 from amplifier A10 will have a shape as illustrated by waveform 456. This signal represents the analog output from the density integrator which is commensurate with vehicle density for the group of vehicle detectors supplying actuation signals to switches S75-S78.

DETAILED DESCRIPTION OF THE SPEED COMPUTER MODULE

FIGS. 17, 17A, 17B, 17C, 17D, 17E, 17F, AND 17G

It is the function of Speed Computer Module 188 to calculate vehicular speed, in either single detector or dual detector mode, and to produce an analog output signal that is proportional to the average speed. There are two independent speed computers, S1 and S2, within the Speed Computer Module.

FIG. 17 is a suggested layout of the front panel 458 for Speed Computer Module 188. Switches S112 through S115 are employed for selecting the response time, which is common to both speed computers. The amount of time required for the speed computer to respond to a change in the speed of vehicles passing through the system is designated herein as RESPONSE TIME. It is pointed out that response time was discussed under the description of the Density Computer Module hereinabove. More particularly, the value programmed for response time is the amount of time required for an exponential change of 63 percent of the difference between an initial analog output signal for speed and a new such signal as a result of a higher or lower speed.

Switches S116 and S117 are employed for overriding the RESPONSE TIME that is programmed in switches S112 through S115. This overriding feature will provide immediate readout of each new speed computation. Switch S116 is employed for speed computer S1, and switch S117 is employed for speed computer S2.

Vehicular speed may be computed by the Speed Computer Module with actuation signals from either one or two vehicle detector configurations. When one vehicle detector 74 (of FIG. 2) is employed, then the speed is computed on the basis of the time required for a vehicle to travel a given (fixed) distance while in the presence of the vehicle detector loop. In this configuration, an average distance of 25 feet is normally programmed for vehicle travel. An average vehicle length is assumed to be 19 feet, and the loop size is 6 feet. Since this distance is programmable, then it is possible to employ other values of loop size and vehicle length.

When two vehicle detectors are employed, the computing distance for speed is the distance between the

leading edges of two closely spaced detector loops along a lane of traffic flow. Likewise, this value is programmable and can vary from one vehicle detector configuration to another. The distance programmed for either single or dual detector operation will hereinafter be referred to as the "speed measuring interval."

Switches S118 through S122 are employed for programming the distance in feet over which the vehicle's speed is computed for speed computer S1. Likewise, switches S123 through S127 are employed for programming this distance in speed computer S2.

Switches S130 through S141 are internally connected to the 12 output channels of Detector Input Monitor Module 166 and serve both speed computers S1 and S2. Switches S128a and S128b are the two input connections to speed computer S1. Likewise, switches S129a and S129b are the two input connections to speed computer S2.

In operation, vehicle detector actuation signals are supplied to either one or both of the speed computer inputs by employing a jumper wire with program pins connected to each end. The program pin on one end of such a jumper wire is normally inserted into one of the DETECTOR switches, S130 through S141, and the other end of the jumper wire is inserted into a speed computer input, such as switch S128a. A second jumper wire is employed in a similar manner between another DETECTOR switch and switch S128b when employing actuation signals from two vehicle detectors to compute vehicle speed. Vehicle actuation signals are supplied in the same fashion to speed computer S2.

Switches S142 and S143 are internally connected to the outputs of speed computers S1 and S2, respectively. Switches S144 through S155 are internally connected to common bus line 190. In operation, the analog output signal from speed computer S1 is supplied to bus line 190 via a jumper wire connected between switch S142 and one of LINE switches S144 through S155. The output of speed computer S2 is connected in the same fashion from switch S143 to one of the LINE switches.

FIG. 17A is a block diagram of Speed Computer Module 188. A 2-millisecond period clock signal is applied on terminal 460 as an input to response counter and comparator network 461 to increment a counter contained therein. Switches S112 through S115 are connected between network 461 and a source of positive voltage on terminal 462. These switches are employed for programming the RESPONSE TIME for the Speed Computer Module. The network 461 is substantially the same as that shown and described in FIG. 13. The output of network 461 is supplied to speed computers S1 and S2.

Vehicle detector actuation signals are supplied as an input to the speed computers via switches S128a and S128b for S1 and switches S129a and S129b for S2. Switches S128b and S129b are connected to biasing resistors contained within the computers S1 and S2, respectively. The outputs from S1 and S2 are supplied to switches S142 and S143, respectively.

FIG. 17B is a block diagram of speed computer S1. Speed computer S2 is identical to S1. Switches S128a and S128b are connected to input switching network 463, the output of which is supplied, in parallel, to period integrator network 464 and sample and reset network 465. It is the function of network 463 to supply a digital signal which is at a high level when a vehicle

is sensed by a detector or is between two detectors where the time duration of the high-level digital signal is inversely proportional to vehicle speed. Period integrator network 464 converts the digital signal from network 463 to an analog signal, and generates a linear-ramp output signal during the time at which the digital signal is at a high level. Therefore, the highest amplitude reached by the linear-ramp signal is proportional to the amount of time required for a vehicle to pass through the speed measuring interval.

Switches S118 through S122 are connected, in parallel, between the output of an amplifier contained within network 464 and resistor scaling network 466. The output of network 466 is fed back to the input of the amplifier within network 464. Switches S118 through S122 are disposed for programming the speed measuring interval by altering the slope of the linear-ramp output voltage from network 464 in inverse proportion to the distance programmed.

The linear-ramp signal generated within network 464 is supplied to sample and hold network 467 where the maximum amplitude of the ramp is stored. The output voltage from network 467 remains essentially constant at a level which is inversely proportional to the speed of the last car that passed through the speed measuring interval. This voltage level will change when a subsequent car passes through the interval at a different speed.

Sample and reset network 465 supplies a SAMPLE signal to network 467 for transferring the highest amplitude of the ramp signal from network 464 into a sample and hold circuit within network 467. When the SAMPLE signal drops to a low level again, a RESET signal is supplied to network 464 for restoring the ramp generator to a zero voltage level. The SAMPLE signal is generated when the high-level digital signal from network 463 drops to a low level. The RESET signal is generated 50 milliseconds after the SAMPLE signal.

The voltage output from network 467 can be expressed by the following equation:

$$p = 35.2t/d$$

where p = output voltage in volts.

t = time duration of a high-level digital signal from network 463, d = programmed DISTANCE for the speed measuring interval, in feet, and

35.2 is a combined constant of the preceding circuits.

Since the equation above is expressed as a function of time per unit distance, and speed should be expressed by distance per unit of time, then, it is necessary to compute the reciprocal of the output voltage ($1/p$).

A reciprocal computing network 468 is provided after network 467 for performing the reciprocal operation. The output voltage from network 468 can be expressed by the following equation:

$$r = 3/p$$

where

r = output voltage in volts,

p = output voltage of network 467 in volts, and

3 is a combined constant of the preceding circuits.

The voltage from network 468 is supplied to output integrator 469 through response switch 470. Response switch 470 is operational when a RESPONSE signal is

supplied to terminal 471 from network 461 (FIG. 17a). Switch S116 is connected in parallel with switch 470. When a program pin is inserted into S116, switch 470 is by-passed and any RESPONSE TIME programmed in switches S112 through S115 is overridden. The purpose for bypassing switch 470 is to provide a fast response time, if desired.

Response switch 470 and output integrator 469 are substantially the same as that portion of the circuit of FIG. 15 which includes Q14, C10 and A10. This circuit was described in detail with the description of FIG. 15.

The structure and operation of the individual networks of the speed computers will now be described. FIG. 17C is a logic diagram of input switching network 463, and sample and reset network 465. Switch S128a is connected to AND gate 472, and is also connected to a dynamic input of NOR gate 473. Resistor R31 is connected between a source of positive voltage on terminal 474 and one side of switch S128b. The second side of switch S128b is connected to the second input (inverting input) of AND gate 472, and is also connected to a dynamic input and an inverting input of NOR gate 475.

The output of AND gate 472 is connected to a second input of NOR gate 473. The output of NOR gate 473 is connected to a third input of NOR gate 475, and is also connected to an inverter 476. The output of this inverter gate is the output of network 463, and is also connected to the input of a five-second delay circuit 477. The output of circuit 477 is connected to the fourth input (dynamic input) of NOR gate 475. The output of NOR gate 475 is connected back to the third input of NOR gate 473.

When a single vehicle detector is connected to speed computer S1, as, for example, when a program pin is inserted into switch S128a and no pin is inserted into switch S128b, the network 463 transfers vehicle actuation signals which are in phase with the input. That is, a high-level actuation signal (vehicle presence) on switch S128a will produce a high-level digital signal at the output of inverter 476. When an intermediate-level actuation signal (no vehicle presence) is supplied to S128a, then the output signal from inverter 476 will be at a low-level with a low-level signal supplied to S128a, which is indicative of no detector connection, or no traffic activity during a sampling period, the output signal from inverter 476 will likewise be at a low-level signal.

When two vehicle detectors are connected to speed computer S1, as, for example, when program pins are inserted into switches S128a and S128b, the output of inverter 476 will be high during the time a vehicle is between the leading edges of the loops of these detectors (extremities of the speed measuring interval).

The insertion of a program pin into S128b will supply the positive voltage from terminal 474 to the inverting input of AND gate 472, and to an inverting input plus a dynamic input of NOR gate 475. The leading edge of a vehicle actuation from S128b will active the dynamic input to NOR gate 475, and the high-level of the actuation signal will enable the inverting inputs to AND gate 475 and NOR gate 475. An intermediate-level signal, which is indicative of vehicle non-presence, will disable the inverting input of AND gate 472, but will enable the inverting input to NOR gate 475. A low-level actuation signal will disable both of these inverting inputs.

The output of the five-second delay circuit 477 is normally at a low-level.

With the conditions as described above, and no vehicles within the speed measuring interval, the output of NOR gate 475 is at a low-level, and the output of inverter 473 is at a high-level. The output of NOR gate 476 is at a low level.

When a vehicle enters the speed measuring interval, a high-level actuation signal is supplied to switch S128a which will cause the output of NOR gate 473 to drop to a low-level, thereby allowing the output of NOR gate 475 to go to high-level. The output of NOR gate 473 will remain at a low-level until a high-level actuation signal is supplied to switch S128b, or when the output of circuit 477 goes to high-level.

When a vehicle leaves the speed measuring interval, a high-level actuation signal is supplied to switch S128b and the output of NOR gate 475 will drop back to a low-level, thereby causing the output of NOR gate 473 to go to a high level. The output of inverter 476 will then drop to a low-level.

Therefore, it can be seen from the description hereinabove that a vehicle passing through the speed measuring interval will produce a digital high-level signal at the output of network 463 commensurate with the time that the vehicle was present within the interval. If a vehicle changes lanes, or otherwise leaves the speed measuring interval, the 5-second delay circuit will reset the network 463 for detection of a subsequent vehicle. The 5-second time limit is valid since this value corresponds to extremely low vehicle speeds, which are of no interest herein.

The sample and reset network 465 includes a 50-millisecond one-shot 478, and a flip-flop 479. The output of network 463 is connected to an inverting-dynamic input of one-shot 478 and to the reset input of flip-flop 479. The 0 output of one-shot 478 is connected to the set input of flip-flop 479. The 1 output of one-shot 478 is the SAMPLE signal which is supplied as an input to sample and hold network 467 (FIG. 17B). The 1 output of flip-flop 478 is the RESET signal which is supplied as an input to the period integrator 464 (FIG. 17B).

In operation, flip-flop 479 is reset by a high-level output signal from network 463, thereby removing the integrator RESET signal. When this output signal from network 463 drops to a low-level, one-shot 478 is activated. This produces the SAMPLE signal at the 1 output of the one-shot. Fifty-milliseconds after the one-shot is activated, the SAMPLE signal drops back to a low-level which sets flip-flop 479. This again produces the RESET signal at the output of the flip-flop.

FIG. 17D is a schematic diagram of period integrator network 464, AND resistor scaling network 466, with switches S118 through S122 connected therebetween. The signal from network 463 (FIG. 17B) is supplied on terminal 481. Resistors R32 and R33 are connected in series between terminal 481 and the inverting input of amplifier A12. Resistor R32 is a gain adjusting resistor that is employed for scaling network 464 in accordance with the constants of the equations discussed hereinabove. The non-inverting input of amplifier A12 is connected to ground potential.

Precision resistors R34a through R34e are each connected between one side of switches S118 through S122 and the inverting input of amplifier A12. The second side of each of switches S118 through S122 is con-

nected to the output terminal of amplifier A12. Resistor R35 is connected between the output of A12 and the inverting input of amplifier A13. The non-inverting input of A13 is connected to ground potential.

Capacitor C12 is connected between the output and inverting input terminal of amplifier A13. Reset switch 482 is connected in parallel with capacitor C12. Switch 482 is activated by the RESET signal which is supplied to terminal 483. Switch 482, when activated, shorts out capacitor C12 and discharges the voltage accumulated during the previous sample period.

When a high-level digital signal is supplied at the output of network 463 to terminal 481, the output of amplifier A12 drops to a negative voltage level. The magnitude of this negative voltage level is proportional to the amount of resistance connected, that is, by the insertion of program pins into switches S118 through S122, within the feedback path of A12. Also, the amount of resistance connected is inversely proportional to the distance of the speed measuring interval. For example, resistor R34a is 16 times greater in value than resistor R34e, and switch S118 corresponds to 1 foot of the distance while S122 corresponds to 16 feet of the distance. Therefore, it follows that the magnitude of the negative voltage present at the output of amplifier A12 is inversely proportional to the computed distance programmed.

The negative voltage level at the output of amplifier A12 will remain essentially constant for the time duration of the high-level digital signal that is supplied to terminal 481. This negative voltage level is supplied through R35 to the inverting input of amplifier A13 which will, in turn, cause the output voltage of A13 to increase positively at a linear rate. The rate of change of the voltage at the output of A13, with respect to time, is proportional to the magnitude of the negative voltage supplied to resistor R35. Therefore, the output voltage from A13 is an analog linear-ramp signal having a slope inversely proportional to the distance programmed.

When the digital signal supplied to terminal 481 drops to a low level (at the time that a vehicle leaves the speed measuring interval), the output of amplifier A12 returns to zero volts. The linear-ramp signal at the output of A13 will level off at the highest voltage reached, since capacitor C12 has accumulated a charge which is equal to this voltage. Simultaneously, the SAMPLE signal from network 465 is supplied to network 467, and 50 milliseconds thereafter the RESET signal is applied to terminal 483 which restores C12 to zero volts. The 50 millisecond time interval allows sufficient time for the voltage on C12 to be transferred to network 467 (FIG. 17B).

FIG. 17E is a schematic-block diagram of sample and hold network 467. The linear-ramp signal from network 464 is supplied to terminal 484, which is connected to the non-inverting input of amplifier A14. The output terminal of A14 is connected to sample switch 485, and the output of switch 485 is connected to the input of source follower 486. Source follower 486 is a high input impedance device which is employed to minimize any undesired discharge of voltage accumulated on C13. Capacitor C13 is connected between the output of switch 485 and ground potential. The SAMPLE signal is supplied to terminal 487, which is connected to the activation terminal of switch 485. The output of source follower 486 is connected to the output of net-

work 467, and is also connected to the inverting input of amplifier A14.

A sampling period for the speed computers, S1 and S2, consists of the time a vehicle is present within the speed measuring interval; this period varies in time with the difference between individual speeds. From the time a vehicle enters the speed measuring interval until the time the vehicle leaves this interval, the ramp signal produced within network 464 increases linearly from zero volts to a maximum positive voltage that is commensurate with the time duration required for the vehicle to pass through the interval. It is the function of network 467 to store this maximum positive voltage for use by the subsequent circuitry, such as network 468 and output integrator 469.

When a disparity of voltage levels exists between the two inputs of amplifier A14, an output voltage from A14 is supplied to switch 485. The SAMPLE signal activates switch 485 so that the output voltage from A14 will be transferred to capacitor C13. This voltage level is also transferred through source follower 486 to the output of network 467, and to the inverting input of amplifier A14. During the 50-millisecond time interval of the SAMPLE signal the disparity in voltage levels at the inputs of A14 will diminish, and capacitor C13 will accumulate a charge of voltage equal to that applied on terminal 484.

FIG. 17F is a schematic-block diagram of reciprocal computing network 468 (FIG. 17B). The output voltage from source follower 486 is supplied to terminal 488, which is connected to one of two inputs of analog multiplier 489. The analog multiplier may be, for example, a linear four-quadrant multiplier, e. g., Model Number MC1595L, manufactured by Motorola Semiconductors of PHOENIX, Ariz. The multiplier produces a differential output voltage which is proportional to the product of the two voltages supplied to its inputs. The two differential output terminals are connected to the inverting and non-inverting inputs, respectively, of amplifier A15. The output terminal of A15 is the output of network 468, and is also connected to the second input to multiplier 489.

Resistor R36 is connected between one of the differential output terminals of analog multiplier 489 and a source of positive voltage on terminal 490. Resistors R37 and R38 are connected in series between the second differential output terminal of the analog multiplier and terminal 490. R38 is an adjustable resistor, for which the purpose will become evident hereinbelow.

It is a property of the particular analog multiplier used that both output terminals are internally connected to a constant current source. Therefore, the sum of currents supplied through resistors R36 and R37-R38 to the output terminals is constant. By employing R37-R38 resistance which is higher than R36, it is assured that the amount of current through R36 will have to be greater by a fixed amount than that through R37-R38 in order to establish essentially zero volts differential at the input of A15.

The differential multiplier output voltage is thereby held at a constant current difference that must be maintained by generation of a voltage at the output of A15 which is fed back to the second multiplier input to compensate for any change in the voltage applied to the first multiplier input on terminal 488.

The transfer function of the multiplier follows the formula:

$$Z = k_1xy,$$

where

Z = differential output voltage

k_1 = proportionality constant

x = multiplicand input

y = multiplier input

Since the output is maintained at a constant value in this case, Z can be replaced by a second constant k_2 , yielding the relationship:

$$y = k_2/k_1x \text{ or } y = k_3/x,$$

wherein $k_3 = k_2/k_1$

From this relationship, it is evident that for any value of x (proportional to time required for a vehicle to pass through the speed measuring interval) a value of y is obtained which is inversely proportional to x (or directly proportional to the speed of the vehicle). This is the desired result. By adjustment of R38, the constant k_1 is chosen to cause the y values to correspond to the desired range of output voltages.

FIG. 17G is a timing diagram that illustrates the operation of speed computers S1 and S2. Waveform 492 represents the digital signal appearing at the output of network 463 as a result of vehicles passing through the speed measuring interval. Waveform 493 represents the output voltage from amplifier A12 within network 464. The amplitude of waveform 493 will vary with changes in the feedback resistance of A12 by the insertion of program pins in switches S118 through S122.

With reference to waveforms 492 and 493, the signal between times t_1 and t_2 represents a first vehicle passing through the speed measuring interval. The signal between times t_4 and t_5 represents a second vehicle passing through the interval at a speed slightly faster than the first vehicle. And the signal between times t_7 and t_8 represents a third vehicle passing through the interval at a speed slower than the first and second vehicles.

Waveform 494 represents the linear-ramp output voltage from network 464. The slope of the ramp is constant for a given distance of the speed measuring interval. When a vehicle leaves the speed measuring interval (at times t_2 , t_5 and t_8) the linear-ramp of waveform 494 levels off at the highest voltage reached. Also, the SAMPLE signal (not shown) is produced within network 465 at times t_2 , t_5 and t_8 to transfer this voltage level from network 464 (waveform 494) to network 467. Fifty milliseconds after the SAMPLE signal is produced, the RESET signal is supplied from network 46 to restore the voltage level stored within network 464 (waveform 494) to a zero value. This occurs at times t_3 , t_6 and t_9 .

Waveform 495 represents the output of network 467. At times t_2 , t_5 and t_8 the SAMPLE signal enables this network to accumulate a voltage on capacitor C13 which is commensurate with the magnitude of the voltage represented by waveform 494. The 50 millisecond time interval between the leading edge of the SAMPLE signal and the RESET signal is sufficient for network 467 to stabilize to a new voltage level as a result of a new vehicle speed.

The magnitude of waveform 495 is proportional to the amount of time required to travel a given distance. This signal is supplied to reciprocal computing network 468. Waveform 496 represents the output of network 468, and the magnitude thereof represents distance with respect to time; or vehicle speed. This signal is

supplied to output integrator 469, which is substantially the same as that shown in FIG. 15 and described therewith. If the signal is supplied through response switch 470 (i.e., with no program pin in S116) the analog signal at output switch S142 is representative of the cumulative average speed measured by the system, is illustrated by waveform 497. If, on the other hand, a signal representing in effect the instantaneous speed is desired, a program pin is inserted in switch S116 and waveform 497 (the output of integrator 469) will be essentially the same as waveform 496. The insertion of a program pin in switch S116 has the same effect with respect to the speed computer as bypassing FET Q14 in the circuit of FIG. 15.

DETAILED DESCRIPTION OF THE VOLUME COMPUTER MODULE

FIGS. 18, 18A, 18B, 18C, 18D, 18E, AND 18F

It is the function of the Volume Computer Module 186 to generate an analog voltage that is commensurate with traffic volume. Each volume computer circuit is capable of receiving actuation signals from four vehicle detector channels. When more than one vehicle detector channel is connected to a volume computer circuit, an average volume for two, three or four vehicle detector channels is calculated. A computer circuit generates an analog voltage as a function of the number of actuation signals with respect to time.

FIG. 18 is a suggested layout of front panel 510 of the Volume Computer Module, containing four individual volume computers V1, V2, V3 and V4. Switches S156-S159 are employed for programming the amount of time that is desired for the volume computer to respond to changes in traffic volume. Except for this common response setting, the four computers are independent.

Switches S160-S171 are connected to the 12 outputs of the Detector Input Monitor Module. Each output is representative of a lane of traffic. Switches S172 through S175 are connected to the four inputs of volume computer V1. Likewise, switches S176 through S187 are connected to four inputs of volume computers V2, V3 and V4, respectively. If more than one input signal (lane of traffic) is supplied to an individual volume computer, then the inputs connected are automatically averaged. That is, the average volume in two or more lanes may be computed by multiple input connections.

Switch S188-S192 are programmed to represent the number of vehicles, in hundreds, per hour, per lane that is required for a 100 percent volume output. It is pointed out that this is based on having a single detector per lane. Likewise, switches S193-S204, in groups of four, are employed in a similar manner as above for programming 100 percent volume for volume computers V2, V3 and V4, respectively.

Switches S205-S208 are connected to the outputs of the four volume computers V1, V2, V3 and V4, respectively. Finally, switches S209 through S220 are the twelve output switches connected to common buss line 190 accessible from the computer modules.

FIG. 18A illustrates Volume Computer Module 186 in block diagram form. One side of switches S156-S159 is connected to a source of positive voltage on terminal 512, and the other side is connected to response counter and comparator network 513. The network 513 is identical to network 378 which was de-

scribed in connection with FIGS. 12 and 13 hereinabove. Clock 2 timing signal, a square wave with a frequency of 500 cycles per second, is applied to terminal 514 to increment the counter within network 513. Output signals from network 513 are supplied to volume computers V1-V4 via line 515. Terminal 516 receives a one cycle per second pulse which is applied to SAMPLE and RESET circuit 517. Outputs from this circuit are applied via lines 518 and 519 to volume computers V1-V4.

In order to provide inputs to the volume computers from the detector inputs, a wire with a program pin attached to each end is employed for effecting an electrical connection by inserting one pin into one of switches S160-S171 and the other into one of switches S172-S187, the latter being contained within the volume computers V1 through V4, as shown and described in more detail later. In a similar manner, connections are made between the output switches S205-S208 and switches S209-S220 to supply the analog output signals from the volume computers to bus line 190.

FIG. 18B illustrates a logic diagram of sample and reset circuit 517. Terminal 516 is connected to the toggle input of flip-flop 520. The 1 output of flip-flop 520 is connected to the toggle input of flip-flop 521. The 1 output of flip-flop 521 is connected to the toggle input of flip-flop 522. The 1 output of flip-flop 522 is connected to both of one-shots 523 and 524. The output of one-shot 523 is connected to the input of one-shot 525. The output of one-shot 525 is connected to line 518. The output of one-shot 524 is connected to line 519.

The net effect of flip-flops 520, 521 and 522 is to divide the one cycle per second signal applied to terminal 516 by 8. Therefore, the signal supplied to the inputs of one-shots 523 and 524 has a pulse repetition rate of 1-cycle-per-8 seconds. The first negative transition occurring at the input of one-shot 524 will supply a positive-going signal on line 519. Likewise, the same negative transition supplied to the input of one-shot 523 will cause the output to go to a high level. One-shot 523 will cause the output to remain at a high level for approximately 35 milliseconds. The subsequent negative transition from the output of one-shot 523 will trigger one-shot 525, thereby producing a positive going signal on line 518. Accordingly, the positive-going signal on line 519 will occur earlier in time than the positive going signal on line 518. The purpose for the time delay between these two signals will be shown in greater detail hereinbelow.

FIG. 18C is a block diagram of an individual volume computer, such as V1. One side of switches S172-S175 is connected to resistor biasing network 527, and the second side is connected to both detector input averaging network 528 and detector accumulator and storage network 529. The output of network 528 is applied as an input to network 529. The signal on line 518, which will hereafter be referred to as RESET, is supplied to the terminal 530, which is connected as an input to network 529. The output of network 529 is applied as an input to resistor scaling network 531. The output of network 531 is supplied to sample switch 532. The signal on line 519, which will hereafter be referred to as SAMPLE, is supplied to terminal 533 which is connected as an input to sample switch 532.

The output of network 531 is also connected to sample and hold integrator 534 through switch 532 when a SAMPLE signal is supplied to terminal 533. The output of integrator 534 is connected to one side of switches S188-S192. The second side of switches S188-S192 is connected to resistor scaling network 531. Switches S188-S192 and the resistors in network 531 provide a feedback path for integrator 534.

The output of integrator 534 is also connected to response switch 535. The signal on line 515 from network 513 (FIG. 18a) is supplied to terminal 536 and is the controlling input of switch 535. The signal from integrator 534 is passed through switch 535 to output integrator 537 when a response signal is supplied to terminal 536. The output of integrator 537 is connected to one side of switch S205, the other side of which is connected to buss line 190.

In operation, vehicle detector actuation signals are supplied to switches S172-S175. The signals supplied to all switches containing a program pin are simultaneously applied to networks 528 and 529. It is pointed out that a vehicle actuation signal has three possible discrete voltage levels; first, a high level signal indicates vehicle presence; second, an intermediate voltage level indicates vehicle non-presence; and third, a low level signal indicates vehicle detector failure (or no activity during an activity sampling period).

It is the function of network 528 to average vehicle detector actuation signals when more than one switch is connected, and to supply an output voltage level to network 529 that is inversely proportional to the number of detector channels connected to input switches S172-S175. It is the function of network 529 to accumulate and store a voltage charge indicative of all vehicle actuation signals occurring during an eight second interval of sample time. The output signal from network 529 is passed through resistor scaling network 531 and is applied to one side of sample switch 532. This signal is passed through sample switch 532 when the SAMPLE signal is supplied to terminal 533. The period of the SAMPLE signal is less than 35 milliseconds. Approximately 35 milliseconds after the start of the SAMPLE signal (the time delay one-shot 523), when the SAMPLE signal is no longer present on terminal 533, the RESET signal is applied to terminal 530 to thereby reset network 529 to a zero analog voltage level.

The signal appearing at the output of integrator 534 is scaled by a factor which can be programmed by insertion of pins into switches S188-S192, to select the scale of the magnitude of the output signal.

Response switch 535 and output integrator 537 are identical to that portion of the circuit illustrated in FIG. 15 which includes FET Q14 and amplifier A10. Response switch 535 is essentially an FET connected in the same fashion as Q14 of FIG. 15. Output integrator 537 consists of an amplifier and capacitor connected in the same fashion as A10 and C10, respectively, of FIG. 15. The signal supplied to terminal 536 has a pulse repetition rate which is determined by the value selected via switches S156-S159, and determines the rate of charge of the capacitor included within integrator 537. The operation of the individual constituent networks of FIG. 18C will become more fully understood from the description which follows of the circuits employed within these networks.

FIG. 18D is a schematic-block diagram of detector input averaging network 528. Four individual circuits 538, 539, 540 and 541 are employed for switching feedback paths of an inverting amplifier as a result of vehicle actuation signals supplied to switches S172-S175, respectively. The output of each of these circuits is connected to the inverting input of amplifier A22. The output of amplifier A22 is fed back through each of the circuits 538-541, and also provides the output of network 528.

Circuit 538, which is illustrated within the dashed line, will be described in greater detail as representative of the feedback circuits 538-541. Input terminal 542 of circuit 538 is connected to switch S172, the remaining switches S173-S175 being respectively connected to input terminals of the other three feedback circuits. Resistor R40 is connected between the base of NPN transistor Q22 and terminal 542. Resistor R41 is connected between the base of Q22 and ground potential. The emitter terminal of Q22 is connected to ground potential, and the collector is connected to one side of resistor R42. The second side of transistor R42 is connected to the base terminal of PNP resistor Q23. Transistor R43 is connected between the emitter and base of Q23, the emitter also being connected to the output of amplifier A22. Resistor R44 is connected between the collector terminal of Q23 and the inverting input of amplifier of A22.

In operation, a high voltage level, indicative of vehicle presence, or an intermediate voltage level indicative of vehicle non-presence, at terminal 542 (switch S172) will cause a positive bias on the base of Q22 which all turn this transistor on. Transistor Q23 will also turn on by the application of a low voltage level, through transistor Q22, to the base of Q23. Precision resistor R44 will thereby be connected as a feedback resistor to A22. A low level signal, or no signal, supplied to terminal 542 indicative of a vehicle detector failure (or no activity during an activity sampling period) or no input connection, respectively, will turn transistor Q22 off. This will cause transistor Q23 to turn off. Resistor R44 will thereby be disconnected from the feedback circuit of A22, causing the output thereof to increase in value.

Resistor R45 is connected between the inverting input of amplifier A22 and circuit point 543. The cathode of zener diode CR25 is connected to ground potential, and the anode thereof is connected to circuit point 543. Resistor R46 is connected between circuit point 543 and terminal 544 to which a source of negative voltage is applied. The non-inverting input of amplifier A22 is connected to ground potential.

The function of the circuit that includes resistor R46 and zener diode CR25 is to provide a negative reference voltage to R45 at the inverting input of amplifier A22. The voltage appearing at the output of amplifier A22 is a positive voltage inversely proportional to the number of circuits (538-541) turned on by vehicle detector actuation signals supplied thereto. For example, when one of the four circuits is turned on the output of A22 could be exactly 10 volts. When a second circuit is turned on the output voltage will drop to one-half on 10 volts; when three circuits are turned on the output will be one-third of 10 volts; and when all four circuits are turned on the output will be one-fourth of 10 volts. This change is effected by switching of additional equal precision resistors in parallel with R44.

The feedback path from the output of amplifier A22 is through transistor Q23, when it is turned on, and resistor R44 to the inverting input of A22. Additional feedback paths are provided through a similar transistor and resistor in each of the circuits 539, 540 and 541. When a second feedback circuit is turned on, the output resistor thereof is connected in parallel with resistor R44 thereby reducing the feedback resistance by one-half. When the remaining two feedback circuits are turned on, their output resistors are likewise connected in parallel with R44 and reduce the feedback resistance to one-third and one-fourth, respectively, of the original value.

Accordingly, it can be seen that the voltage level appearing at the output of A22 will be inversely proportional to the number of feedback switching circuits (538-541) which are turned on. It will be shown in the detailed description of the circuits within network 529 that the voltage from A22 is applied across each of four equal value capacitors.

FIG. 18E is a schematic-block diagram of detection accumulator and storage network 529. Four individual circuits 545, 546, 547 and 548 are employed for storing a charge proportional to the voltage output of amplifier A22 and supplying this charge to an integrator upon activation by a vehicle actuation signal supplied from switches S172-S175, respectively. The output signal from each of the circuits 545-548 is connected to the inverting input of amplifier A23. The output of amplifier A22 is supplied to terminal 549 which is, in turn, connected to each of the circuits 545-548.

Circuit 545, which is illustrated within the dashed line, will be described in greater detail as representative of the individual circuits 545-548. Input terminal 550 of circuit 545 is connected to switch S172. Capacitor C25 is connected between terminal 550 and circuit point 551. Resistor R47 is connected between terminal 552 and circuit point 551, and terminal 552 is connected to a source of negative voltage. The cathode of diode CR26 is connected to circuit point 551, and the anode is connected to the gate terminal (G) of FET Q24. Resistor R48 is connected between the gate terminal of Q24 and ground potential. The source terminal (S) of Q24 is connected to the inverting input of amplifier A23. Resistor R49 is connected between the drain terminal (D) of Q24 and terminal 549. Capacitor C26 is connected between the drain terminal of Q24 and ground potential. Capacitor C26 is matched in capacitance to corresponding capacitors in circuits 546-548.

The voltage appearing at the output of amplifier A22 is applied on capacitor C26 for storage of a corresponding charge. This charge will be inversely proportional to the number of detector channels connected, and in response to the voltage supplied to the terminal 549. The discharge path of capacitor C26 is through Q24, when it is turned on, to the inverting input of amplifier A23. FET Q24 is normally turned off by the application of a negative voltage to its gate circuit supplied from terminal 552 through R47 and CR26. The positive transition of a vehicle actuation signal supplied to terminal 550 will reverse bias CR26 and turn on Q24 for a short period of time determined by the time constant of capacitor C25 and resistor R47.

Capacitor C27 has a capacitance value several times that of C26 and is connected between the output and inverting input terminals of A23. Reset switch 553 is

connected in parallel with capacitor C27. Terminal 530 is connected to the controlling input of reset switch 553. The non-inverting input terminal of amplifier A23 is connected to ground potential.

Capacitor C27 acts as a charge storage means across integrating amplifier A23. Reset switch 553 will effectively short out capacitor C27, when activated by the RESET signal, thereby restoring the voltage charge accumulated across capacitor C27 to a zero level.

Accordingly, it can be seen from the discussion hereinabove that each vehicle actuation signal supplied to terminal 550 will transfer a discrete amount of voltage charge across capacitor C27. When more than one vehicle detector channel is connected to the volume computer module, the charge transferred from an individual capacitor (e.g. C26) to capacitor C27 will be reduced proportionally to the number of channels connected. Therefore, if two vehicle detector channels are connected, then two actuation signals will be required to transfer a charge equivalent to the charge transferred by one actuation signal for one input connection; and, similarly, for three or four input connections three or four actuation signals will be required, respectively, to transfer an equivalent charge from the circuits 545-548 to the capacitor C27. The charge on capacitor C27 will be of such a polarity as to produce a negative voltage at the output of the amplifier A23 which is proportional to the average number of actuation signals received per input circuit.

It is the function of network 531, switch 532, and integrator 534 (all shown in FIG. 18C) to accept a negative voltage level from network 529 which is commensurate with the number of vehicle actuation signals received in an eight second interval; to scale this voltage in accordance with the value programmed in switches S188-S192; to store the scaled voltage, and to supply a positive voltage level to the input of sample switch 532.

FIG. 18F is a schematic diagram of resistor scaling network 531, sample switch 532, and sample and hold integrator 534. The output signal from network 529 is supplied to terminal 555. Resistor R50 is connected between terminal 555 and circuit point 556. The anode of diode CR27 is connected to circuit point 556, and the cathode is connected to ground potential. The cathode of diode CR28 is connected to circuit point 556, and the anode is connected to ground potential.

One side of each of resistors R51-R55 is connected to circuit point 556, and the other side of each of these resistors is connected to one side of switches S188-S192, respectively. The second sides of each of the switches S188-S192 are all connected to the output of amplifier A24. The drain terminal (D) of FET Q25 is connected to circuit point 556. Resistor R56 is connected between the drain and gate terminals (D and G, respectively) of Q25 to maintain a negative bias at the latter terminal. The source terminal (S) of Q25 is connected to the inverting input of A24.

Diodes CR27 and CR28 are provided for holding the drain terminal of Q25 within one forward voltage drop of ground potential. This is to assure that Q25 will be biased in the off state when the SAMPLE signal is not present on terminal 533.

Switches S188-S192 represent 100, 200, 400, 800, and 1,600 vehicles, respectively; in hundreds per hour, per lane that is required for 100 percent volume output. Resistors R51-R55 are in an inverse ratio to the

number of vehicles. For example, R51 has a resistance value 16 times that of R55; and the switch connected to R51 represents 100 vehicles where the switch connected to R55 represents 1,600 vehicles. Due to this inverse ratio, the higher the value of resistance in the feedback path, the larger the output voltage from A24, for a given input voltage.

The anode of diode CR29 is connected to the gate terminal (G) of Q25, and the cathode is connected to terminal 533. Diode CR29 is provided for isolating an individual circuit from other similar circuits in volume computers V2, V3, and V4 when the SAMPLE signal is present on terminal 533, i.e., when terminal 533 is released from a negative voltage source.

Capacitor C28 is connected between the inverting input and the output terminals of amplifier A24. Capacitor C28 acts as a voltage storage means between the SAMPLE signals which occur every 8 seconds. Amplifier A24 and C28 act essentially as an integrator between SAMPLE signals.

A new interim negative voltage level for computed volume will appear on terminal 555 from network 529 every 8 seconds. This voltage level is transferred to the integrator comprising A24 and C28 when Q25 is conducting, and will remain at the output of A24 until a new interim voltage level has been supplied to terminal 555. This process of updating the positive output voltage level of A24 occurs every 8 seconds. However, if no vehicle actuation signals are received within an 8 second interval, then the voltage level appearing at the output of A24 will drop to zero until a new voltage level representing vehicle actuations is supplied to terminal 555.

The positive voltage level output from A24 will be employed in integrator 537 for updating the average value for volume. In order to derive a time average of volume, the output of A24 is supplied to the integrator 537 (FIG. 18C) at a variable duty cycle, inversely proportional to the RESPONSE TIME. The 8 second sample period is a relatively short time in comparison to the RESPONSE TIME, which is in minutes. Therefore, minor fluctuations in the output caused by the 8 second sampling interval are small enough to be neglected for practical purposes.

DETAILED DESCRIPTION OF THE TRAFFIC-COUNT PRINT MODULE

FIGS. 19 AND 20

It is the function of Traffic-Count Print Module 182 to accept vehicle actuation signals; to accumulate a total of all such actuation signals; and to periodically print the total of the accumulated actuation signals. More than one vehicle actuation signal may occur simultaneously. Therefore, one analog accumulator circuit is employed as a memory element device for storing the vehicle actuation signals.

FIG. 19 is a suggested layout of front panel 570 for the Traffic-Count Print Module. Switches S233 through S244 are connected to the 12 outputs from Detector Input Monitor Module 166. These switches are disposed for connecting a detector output channel to a traffic counter.

Switches S245, S246 and S247 are provided for selecting the desired mode of operation. Switch S245 is closed to effect a counting of the actuation signals connected via switches S233 through S244. Switch S247 is closed to reset and counter following each print, and

switch S246 is closed when a reset is not desired with each printing.

Finally, switches S248 through S251 are employed for selecting a time interval between print cycles. Connector 572 is disposed for connecting the circuits of the Traffic-Count Print Module to the counter contained within the traffic counter and printer device 82.

FIG. 20 is a block diagram of Traffic-Count Print Module 182. Switches S233 through S244 are each shown connected in series between terminals 574 through 585 and detector input circuits 586. The circuits 586 are connected to analog memory circuit 588 via a line 590. Analog memory circuit 588 accumulates all vehicle actuation signals, even if they occur simultaneously, and stores these signals in the form of an analog voltage.

Analog memory circuit 588 applies this analog signal to count control gating 592. A count command signal is supplied, through switch S245, to the counter within the traffic counter and printer device 82, and a feedback signal is supplied to the analog memory circuit via line 594. This feedback signal subtracts an amount of voltage from the analog memory that is commensurate with the vehicle actuation signals fed out of the memory circuit.

Clock timing signals from Master Clock Module 100 are supplied to terminals 596 through 599. These timing signals are the 0.25 hour, 0.5 hour, 1 hour and 2 hour signals described hereinabove. Switches S248 through S251 are each connected in series between the terminals 596 through 599 and a print interval control circuit 600. Switch S252 is connected in series between ground potential and the circuit 600.

Circuit 600 supplies a print control signal to a print control circuit 602. Switches S246 and S247 are connected in series between positive voltage on a terminal 604 and the circuit 602.

A print command signal is supplied to the printer within the device 82 on a line 606. A counter reset signal is supplied to the counter within the device 82 on a line 608. A count inhibit signal is supplied to gating circuit 592 on line 610. Finally, an inhibit print signal is supplied to circuit 602 on line 612. The purpose for the inhibit count and inhibit print signals supplied on lines 610 and 612, respectively, is to prevent printing while a count operation is in progress and to prevent counting while a print operation is in progress.

DETAILED DESCRIPTION OF THE RATIO COMPUTER MODULE

FIGS. 21, 22, 23, 24, 25, 26, AND 27

The function of the Ratio Computer Module is to generate an analog signal that has a magnitude commensurate with the expression $X/(X+Y)$, where X and Y are individual or average traffic parameters such as density, volume, or speed. The traffic parameters are the result of computations performed by the computer modules such as the Density Computer, Volume Computer, or Speed Computer. For example, X and Y could be the output of two density computers indicative of traffic density for two opposing directions on the same street. In this example, the expression $X/(X+Y)$ would be useful in calculating the offset selections at the individual intersection controllers throughout the system. Another example, X could be the average density over a given segment of a main street and Y the average density over a given segment of a cross street in

that same vicinity. In this example, the expression $X/(X+Y)$ could be useful in selecting the time durations of the green lights for the individual controllers within that vicinity.

FIG. 21 illustrates the front panel 612 of Ratio Computer Module 192 which is divided into four individual ratio computers RA1, RA2, RA3 and RA4. Each ratio computer is divided into two sections, X and Y. The parameters, X and Y, as referred to herein, are the same as those employed in the expression $X/(X+Y)$. Each section within a ratio computer is divided into twelve individual lines, which are the same 12 lines which constitute buss line 190. Switches S254-S265 are employed to connect an input signal associated with a parameter on the respective line to ratio computer RA1 Section X. Switches S266-S277 are employed to connect the parameters to ratio computer RA1 Section Y. If more than one of the lines within a given section are connected to a particular input (X or Y), they are averaged. However, there is an alternate circuit that may be employed for the ratio computer which uses the largest input signal supplied thereto rather than the average input. Ratio computers RA2, RA3 and RA4 operate in a similar fashion.

FIG. 22 illustrates Ratio Computer Module 192 in block diagram form. Terminals 614-625 are connected to the twelve lines that constitute buss line 190. Input summing networks 626-629 are employed for combining the analog signals on those lines that are connected via program pins to ratio computers RA1 through RA4, respectively. Lines 630 and 632 supply the average X and Y values, respectively, to analog computer 634; lines 636 and 638 supply the average X and Y values, respectively, from network 627 to analog computer 640; lines 642 and 644 supply the average X and Y values, respectively, from network 628 to analog computer 646; lines 648 and 650 supply the average X and Y values, respectively, from network 629 to analog computer 652.

The ratio output signals supplied on lines 654-657 are employed within Range Selection Modules 196, 197 and 198 (FIG. 3C) and will be described in greater detail under the description of that module. A compute cycle counter 658 is employed for resetting the individual analog networks periodically. The clock 2 timing signal is supplied to terminal 660 for incrementation of the counter 658. The reset signals are supplied to analog computer networks 634, 640, 646, and 652 on a line 662.

FIG. 23 illustrates one of two types of input summing networks that can be employed within Ratio Computer Module 192. The signals on the twelve lines that correspond to the signals supplied to terminals 614-625 are shown herein as connected in parallel to two sets of program pins. These program pins correspond to switches S254-S265. Equal valued resistors R60-R71 are connected in series between switches S254-S265, respectively, and the non-inverting input of amplifier A30. These program pin switches connect the signals on those lines which are to be employed for the X parameter of the expression $X/(X+Y)$. Resistor R72 is employed as a feedback loop for amplifier A30, and is connected between the output and the inverting input thereof. The output of amplifier A30 is supplied on the line 630.

Resistors R73-R84 are connected in series between switches S266-S277, respectively, and the non-

inverting input of amplifier A32. Resistor R85 is employed as a feedback loop for amplifier A32, and is connected between the output and the inverting input thereof. The output of amplifier A32 is supplied on the line 632. The resistors R60-R85 have a small resistance value when compared to the amplifier input impedance. Therefore, the input impedance of the amplifier can be ignored for all practical purposes. Amplifiers A30 and A32 function as voltage followers to buffer the voltage at the junction of the respective input resistors.

Assume, for example, that program pins are inserted into switches S254 and S255. Then, resistors R60 and R61 will act as a voltage divider network for the voltage supplied on terminals 614 and 615. Also assume that no program pins are inserted into switches S256-S265. Since all the input resistors are of equal value, the voltage applied to the non-inverting input of amplifier A30 will be the average of the voltage supplied between terminals 614 and 615. If three or more resistors are connected in a similar fashion, then the same voltage averaging will occur at the input of the amplifiers. The average value of all the individual signals supplied to A30 through the switches and resistors will appear at the output on line 630.

FIG. 24 shows an alternate circuit for the input summing networks 626-629 which has the capability of selecting the highest voltage from a plurality of inputs. Diodes CR30-CR76 are employed in lieu of resistors R60-R71 and R73-R84, respectively. A negative voltage is supplied to terminal 664 for applying a forward bias to diodes CR30-CR52 through a resistor R86, and to diodes CR54-CR76, through a resistor R87. The circuit point between the connection of the cathodes of diodes CR30-CR52 and the resistor R86 is also connected to the non-inverting input of amplifier A30a, the output of which is supplied on the line 630a. The circuit point between the cathodes of CR54-CR76 and the resistor R87 is also connected to the non-inverting input of amplifier A32a, the output of which is supplied on the line 632a.

Input signals are supplied to the circuit in FIG. 24 on the terminals 614a-625a. Program pin switches S254a-S265a are employed for connecting signals supplied to the input terminals to the anodes of the diodes. Diode CR78 is connected between the output of amplifier A30a and the inverting input thereof. The anode of CR78 is connected to the output of A30a. Resistor R88 is also connected between the inverting input of A30a and negative voltage on terminal 664 to forward bias diode CR78. Diode CR80 is connected between the output of amplifier A32a and the inverting input thereof. The anode of CR80 is connected to the output of A32a. Resistor R89 is also connected between the inverting input of A32a and the negative voltage on terminal 664, which provides forward bias on CR80. The purpose for employing diodes CR78 and CR80 in lieu of a feedback resistor will be more fully understood from the following detailed description of the circuit operation.

Assume, for example, that a +5 volt signal is supplied to terminal 614a and a +6 volt signal is supplied to terminal 615a. Also assume that program pins are inserted into switches S254a and S255a only. Diode CR32 will have a voltage on the cathode 0.7 volts less than the voltage supplied to the anode. Therefore, the voltage on the cathodes of CR30 and CR32 will be 5.3 volts.

Since the voltage on the cathode of CR32 is greater than that applied on the anode thereof, then CR30 will be back biased and the voltage supplied to terminal 614a will not be supplied to the input of A30a. The remaining diodes with their accompanying switches operate in a similar fashion. Diode CR78 will compensate for the 0.7 volt drop across the input diodes to supply an output voltage on line 630a equal to the highest input voltage.

FIG. 25 shows the analog networks 634, 640, 646 and 652 all of FIG. 22. For illustrative purposes, assume that the circuit in FIG. 25 is the analog network 634 of FIG. 22. The signals on lines 630 and 632 are supplied to a pair of terminals 666 and 668, respectively. A pair of equal valued resistors R90 and R91 are connected in series between the terminals 666 and 668. Terminal 666 is also connected to the inverting input of an amplifier A34. The circuit point between resistors R90 and R91 is connected to a voltage-to-current converter 670. This circuit is similar to a Bipolar Current Source illustrated in the *Electronic Engineer* of April 1969 on Page 78, Number 912 of Richard C. Gerdes. The output of converter 670 is supplied to the non-inverting input of amplifier A34. It is pointed out that the connection of amplifier A34 effects a comparison operation in lieu of an amplification operation. More particularly, the input signal supplied to terminal 666 and connected to the inverting input of amplifier A34 is compared to the signal supplied to the non-inverting input from converter 670.

Capacitor C30 is connected between the non-inverting input of amplifier A34 and ground potential. A transistor Q30 is also connected between the non-inverting input of A34 and ground potential, more particularly in parallel with capacitor C30. The emitter of Q30 is connected to ground potential, and the collector thereof is connected to the non-inverting input of A34. The base of Q30 is connected to a terminal 672 through a resistor R92. The output of amplifier A34 is connected to the set input of flipflop 674, the reset input of which is connected to terminal 672. The 1 output of flipflop 674 is supplied to a gated constant current source 676. The constant current source is gated on or off by signals supplied from flipflop 674. When the flipflop is reset, source 676 is supplying current to capacitor C32. When flipflop 674 is set, then source 676 is turned off. The output of the gated constant current source is supplied as an input to peak sample and hold circuit 678. This circuit is essentially a peak memory circuit which has the characteristic of rapid charge time with a very slow discharge time. The purpose of this circuit is to store the highest value of voltage developed across CR32 during a given cycle. As shown, capacitor C32 is connected between the input of circuit 678 and ground potential. Transistor Q32 is connected in parallel with capacitor C32. The emitter of Q32 is connected to ground potential, and the collector is connected to the input of circuit 678. The base of Q32 is connected through resistor R93 to terminal 672. The output of peak sample and hold circuit 678 is supplied on line 654, which is the output of ratio computer RA1. The operation of the circuit illustrated in FIG. 25 will be described following the description of the circuit in FIG. 26, and in conjunction with the timing diagram shown in FIG. 27.

Compute cycle counter 658 is shown in FIG. 26 in logic diagram form. Three flipflops 680, 681, and 682

are connected in a binary counter form. The 1 output of flipflop 681 and the 1 output of flipflop 682 are connected to NOR gate 684. The output of NOR gate 684 is the reset signal supplied on line 662, which is also supplied to terminal 672 of FIG. 25. The clock 2 timing signal has a repetition rate of 2 milliseconds, and is represented in FIG. 27 by the waveform 686. The 1 output of flipflop 681 has a pulse repetition rate of 8 milliseconds and has a shape as illustrated by waveform 688. The 1 output of flipflop 682 has a repetition rate of 16 milliseconds and has a shape as illustrated by waveform 690. It can be seen by the combination of waveforms 688 and 690, which are supplied as input signals to NOR gate 684, that a coincidence exists every 16 milliseconds for a period of 4 milliseconds. Waveform 692 illustrates the reset timing signals supplied on the line 662.

The timing signal supplied by the counter 658 (FIG. 22) is supplied to terminal 672 of the circuit in FIG. 25. When the timing signal supplied to terminal 672 is high, flipflop 674 is reset, and transistors Q30 and Q32 are turned on. The conduction of transistors Q30 and Q32 will act to discharge the capacitors C30 and C32, respectively. As long as these two transistors are conducting, no charge can accumulate on the capacitors.

The signals supplied to terminals 666 and 658 are combined at the junction of R90 and R91 as an input to converter 670. This voltage controls the rate at which current is supplied from converter 670 to capacitor C30. Waveform 694 of FIG. 27 illustrates the charging of capacitor C30. (The amplitude of the waveforms in FIGS. 27 is exaggerated for illustrative purposes and is not drawn to any particular scale.) It is pointed out that the ramp of waveform 694 does not begin until the reset signal of waveform 692 drops to a low level. This is due to the fact that transistor Q30 is on and will discharge any voltage developed across C30. When the signal on line 662, as indicated by waveform 692, drops to a low level transistor Q30 turns off and the buildup of a charge on C30 is at a linear rate, and will continue to increase until a subsequent reset pulse is applied to terminal 672.

Waveform 696 illustrates a typical waveform which may be applied to terminal 666. This could be indicative of the traffic density from the density computer. Amplifier A34 compares the two inputs which are indicated by waveforms 694 and 696. When these input signals reach an equal value, an output signal is supplied from A34. Waveform 698 illustrates the output signal from amplifier A34. Flipflop 674 is set by the output signal from A34 which will, in turn, inhibit gated constant current source 676. It is pointed out that the charge on capacitor C32 from current source 676 began at the same time that the reset signal, as illustrated by waveform 692, dropped to a low level. It is also pointed out that the slope of waveform 694 is a result of the summation of the X and Y signals supplied on terminals 666 and 668, respectively. The slope of the charge curve of capacitor C32, as indicated by waveform 700, is the same following each reset since it is determined by a constant current supply.

Accordingly, it can be appreciated that the changing slope of waveform 694 will determine the time interval between the end of the reset pulse 692 and the time an output is produced from amplifier A34. More particularly, the time interval is the result of the time required for capacitor C30 to develop a voltage across the plates

thereof that is equal to the voltage applied on terminal 666. The amount of the time delay is controlled inversely by the slope of the ramp voltage illustrated in waveform 694. The slope of this ramp, in turn, is controlled by the sum of the parameters X and Y.

The time required for the voltages supplied at the inputs of amplifier A34 to reach equal values is directly proportional to the value of X since the comparison will not be effected until the voltage on capacitor C30 has reached a value equal to X. Accordingly, the final value of the voltage developed across the plates of C32 within a given compute cycle will also be directly proportional to X and inversely proportional to (X+Y).

Peak sample and hold circuit 678 stores the highest value of voltage developed across the plates of C32. Waveform 700 illustrates the function of voltage versus time which is supplied as an input signal to circuit 678. Waveform 702 illustrates the function of voltage versus time supplied as an output signal from circuit 678. By appropriate selection of components within circuit 678 the output signal supplied on line 654 is made equal to the expression $X/(X+Y)$. The first cycle of operation will produce an output signal on line 654 that builds up as illustrated by the initial portion 702a of waveform 702. However, the amplitude of this output signal will not change by any appreciable amount between compute cycles as illustrated by the later portion 702b of waveform 702.

DETAILED DESCRIPTION OF THE METER-RECORD OUTPUT MODULE

FIGS. 28, 29, AND 30

It is a function of Meter-Record Output Module 194 to supply to a counter-printer the next program number to be executed. This counter-printer is one of those indicated in FIG. 1 by the reference numeral 82 and is shown in the system block diagram in FIG. 3C where it is numbered 82a. The counter-printer 82a contains an impulse counter which is incremented by a count of one each time a pulse is supplied thereto from Meter-Record Output Module 194. Since the program number is supplied from Program Memory Module 102 in the form of simultaneous pulses on parallel lines in binary combinations, commonly referred to as parallel-by-bit, it is necessary to perform a parallel-to-serial conversion of the program number. It will be shown in the block diagram description hereinbelow that this conversion is performed by impulsing the counter within printer-counter 82a a number of times equal to the value of the program number.

It is also a function of Meter-Record Output Module 194 to provide interfacing circuits between the traffic parameter analog signals supplied on the output lines constituting bus line 190, plus the lines 654-657 from Ratio Computer Module 192, and either indicating meters or chart records, or both. Five summing networks are provided for combining two to four of the traffic parameter signals, if desired, to thereby drive a chart recorder.

FIG. 28 suggest a possible layout of the front panel 704 for Meter-Record Output Module 194. Switches S280-S299, which are located under the heading AVERAGER INPUT, are the input connections to the five summing networks (four switches per network). Switches S300-S311 are connected to the 12 output lines common to each of the computer modules, and switches S312-S315 are connected to the four output

lines from Ratio Computer Module 192. Switches S300-S315 are located under the heading LINE.

The outputs of the summing networks are disposed for connections at switches S316-S325. Switches S326-S335, which are located under the heading OUTPUT CHANNEL, are provided for either connecting one of the computer output lines or an output from one of the summing networks to an indicating meter. Connector 705 is employed for coupling the signals supplied at switches S326-S335 to indicating meters 78 and chart recorders 80.

The printing function portion of Module 194 is illustrated in block diagram form in FIG. 29. Terminals 706 and 708, which are provided with the program A and program B signals, respectively, from the program service flipflop, are connected to input gating network 710. An output of network 710 is supplied on line 712 to print output gating network 714, counter 716, and comparator 718. The contents of counter 716 are supplied in parallel to one set of inputs of comparator 718. Terminals 720-724, which are provided with the program number from Program Memory Module 102, via lines 95, are connected to the second set of inputs of the comparator. The output of comparator 718 is connected to network 714 and output gating network 726 via line 728.

Terminal 730, which is provided with the A or $\bar{A}$ signal from Program Memory Module 102, is connected as an input to network 726. The toggle input of counter 716 is supplied from an oscillator contained in network 710 via line 732 through gating within network 726, and line 734. The print output gating network supplies an inhibit count signal to network 726 on line 736.

Network 714 supplies a print command to counter-printer device 82a on line 738. Network 726 supplies a count, reset and an A or B command signal to counter-printer device 82a on lines 740, 742 and 744, respectively.

The application of a program A or a program B signal, which is supplied from program service flipflop 111 (FIG. 3B) via the program memory 102 (FIG. 3A) and lines 195 (FIG. 3C), to either terminal 706 or 708, will thereby remove an inhibit signal, which is normally present on line 712, to network 714, counter 716, and comparator 718. Simultaneously, the program number stored with Program Memory Module 102 is applied via line 95 to terminals 720-724, and 730. Due to a disparity in the binary values applied to either side of comparator 718, a low level output signal is supplied on line 728 to networks 714 and 726. A print command signal is inhibited within network 714. With the conditions set up as stated hereinabove, oscillator pulses will be supplied to network 726 to supply advance pulses simultaneously to electronic counter 716 on line 734, and to the mechanical counter contained within counter-printer device 82a on line 740. Electronic counter 716 will advance to a binary value equal to the binary value of the program number applied to terminals 720-724. When an equal binary value is detected within comparator 718, a high-level output signal is supplied on line 728 whereupon a print command is provided from network 714 on line 738. Also, an inhibit count signal is supplied from network 714 on line 736. A short time later, which is determined by a one-shot contained within network 714, a reset command is supplied on line 742 to thereby restore the mechanical counter to a zero value.

The state of the signal supplied on terminal 730 will determine the state of the A or B signal supplied on line 744. The purpose for this is to set a print wheel within the counter-printer device 82a to either A or B, depending on the application of either a program A or a program B signal to terminals 706 or 708, respectively.

FIG. 30 illustrates the program pin connections for the switches of Meter-Record Output Module 194. Switches S280-S299, which are the AVERAGER INPUT switches, are the input connections to averaging circuit 746, which contains five summing networks. Each summing network has the capability of combining four signals supplied thereto. Switches S316-S325, which are the AVERAGER OUTPUT switches, are the output connections for the five summing networks. Switches S326-S335, which are the OUTPUT CHANNEL switches, are the input connections for scale adjusting circuit 748. Potentiometers are provided within circuit 748 to adjust the meter scale to a desired range of operation. Output lines from circuit 748 (which are numbered 1-10) are connected to connector 705. These lines are disposed for supplying control signals to Chart Recorder 80, and meters 78.

DETAILED DESCRIPTION OF THE RANGE SELECTION MODULES

FIGS. 31, 32, 33, 34, 35, 36, 37, 38, 39 AND 40

It is a function of Range Selection Modules 196, 197 and 198 to accept one or more of the analog signals from any one of the computer modules, and to systematize an aggregation of these analog signals into a hierarchy of six discrete ranges. The term "range" as used herein refers to the full extent over which the aggregation of the input analog signals may vary between programmed limits. It will be shown in the description of the circuitry hereinbelow that groups of program pins are provided for the selection of the minimum and maximum limits of a given range. Each Range Selection Module has provisions for supplying six individual ranges. The input analog signals are supplied on 16 individual parallel lines, which may be signals produced within the Density Computer Module, the Volume Computer Module, the Speed Computer Module, or the Ratio Computer Module. Program pins are provided for connecting one or more of these lines to the input terminals of the Range Selection Module.

The magnitude of the analog signals from each of the computer modules is interpreted herein as a percentage of the amplitude that corresponds to the anticipated normal traffic activity. Zero percent corresponds to no traffic activity, and 100 percent corresponds to maximum normal activity. Abnormally high levels of traffic activity are interpreted by a percentage greater than 100 percent, but not to exceed a maximum limit of 160 percent. The programmable limits for each of the six ranges within the Range Selection Module are expressed in percentages as discussed herein.

FIG. 31 shows the front panel 750 of the Range Selection Module in an elevational view. Separate but identical front panels are provided on the master controller for each of the three Range Selection Modules. Switches S336 and S337 are provided for identifying the particular Range Selection Module with which the respective face panels are associated. Closure of switches S336 and S337 individually or simultaneously allows the circuitry associated therewith to identify

strobe signals unique to the respective Range Selection Modules, as will be described hereinafter. In the ensuing description it will be assumed that face panel 750 shown in FIG. 31 is programmed to be associated with Range Selection Module 196, the other two modules being identical therewith in all material respects.

Switches S338-S349 are provided for connecting one or a combination of the twelve output lines from buss line 190 as inputs to Range Selection Module 196. Switches S350-S353 are provided for connecting the output lines from ratio computers RA1 through RA4, respectively, as additional inputs to Range Selection Module 196.

Switches S354-S359 are employed for selecting the lower limit for the first of the six ranges, Range A. Switches S360-S365 are employed for programming the upper limit for Range A. The remaining groups of switches, both minimum and maximum, for Ranges B, C, D, E, and F are identical to that discussed for Range A.

FIG. 32 illustrates Range Selection Module 196 in block diagram form. Terminals 752-763 are connected to the twelve lines in buss line 190. Terminals 764-767 are connected to the outputs of the four ratio computers RA1 through RA4. Switches S338-S353 are shown connected in series between the terminals 752-762, respectively, and input averaging network 768. This network is identical to network 626 of FIG. 23, described earlier herein. It is pointed out that an alternate circuit, which has also been described hereinabove, and is illustrated in FIG. 24, may be employed for selecting the input signal with the highest amplitude from a plurality of input signals supplied thereto in lieu of averaging the input signals.

The aggregation of all input signals, or the signal with the highest amplitude, is supplied to analog comparator and output gating network 770 via line 772. Some circuits that are included within Timing and Display Module 202, which will be described in greater detail hereinbelow, are required to explain the operation of Range Selection Module 196. The area enclosed within the dashed line in FIG. 32 represents a portion of Timing and Display Module 202. Ramp generator circuit 774 produces a ramp output signal that is employed for an amplitude comparison operation which will be explained in greater detail hereinbelow. Timing circuit 776 supplies the clock 1 and clock 2 timing signals, as employed in some of the circuits discussed hereinabove, and three readout strobes for synchronization of operation when three Range Selection Modules are used within one master controller.

Ramp generator 774 and timing circuit 776 supply a reference voltage and timing signal, respectively, to network 770 and to counter and gating circuit 778 via line 780. Counter and gating circuit 778 supplies a "clear" signal to ramp generator 774 and network 770 via line 782. The counter and gating circuit contains a 6-bit binary counter, the contents of which are supplied to digital comparator and set range circuit 784 via line 786. Circuit 784 contains the program pin switches that correspond to minimum and maximum range percentage values as discussed hereinabove. Circuit 784 supplies six output signals therefrom via the line 788 to network 770. The output signals from network 770 are supplied on lines 790-795, which correspond to ranges A through F, respectively.

In operation either the aggregation of all signals supplied to network 768, or the signal with the highest amplitude, is supplied to network 770 via line 772 for comparison therein. The ramp signal from generator 774 is also supplied to network 770 via line 782 as an amplitude reference signal for the comparison operation.

Counter and gating circuit 778 produces a clear signal on line 782 which synchronizes the generation of the ramp voltage from generator 774. Therefore, the ramp voltage is synchronized to counter 778. More particularly, one incrementation of the counter within circuit 778 is equal to 2.5 percent of the amplitude of the ramp voltage that corresponds to normal traffic activity. The maximum amplitude of the ramp signal corresponds to 160 percent of normal traffic activity. Individual flipflops contained within the circuit 784 are set, and subsequently reset, when the counter reaches a value which corresponds to the minimum and maximum percentage, respectively, for each range. The analog comparator contained within network 770 enables the output gating network when an equal comparison of the amplitude of signals supplied to the comparator is detected. If an individual flipflop is set within circuit 784 at the time the comparator enables the output gating within network 770, then a signal is supplied on the line corresponding to the range flipflop which is set. The function of Range Selection Module 196 and the individual circuits will become more evident from the detailed description hereinbelow.

FIG. 33 illustrates timing signal generator circuit 778 in greater detail. An 8 KHz clock 796 is provided with positive voltage from terminal 798. A timing signal is supplied from clock 796 with a pulse repetition rate of 8 KHz. This signal is supplied to the toggle input of flipflop 800. As indicated by the small circle adjacent to the toggle input of flipflop 800, the negative transition of the signal supplied thereto is required for operation thereof. The output signal of flipflop 800, which is the clock 1 timing signal, has a pulse repetition rate of 4 KHz, or a period of 250 microseconds. Three flipflops 802, 804 and 806 are connected in a binary counter fashion. The clock 1 timing signal from flipflop 800 is connected to the toggle input of flipflop 802. The 1 output of flipflop 802 is connected to the toggle input of flipflop 804. The 1 output of flipflop 804 is connected to the toggle input of flipflop 806. The output signal from flipflop 806 has a pulse repetition rate equal to that of the clock 1 timing signal divided by 8, which produces a 500 Hz timing signal. This is the clock 2 timing signal, which has a period of 2 milliseconds.

The clock 1 timing signal is also connected to a first input of three NOR gates 808, 810 and 812. The 1 output of flipflop 802 is connected to a second input of NOR gates 808 and 812. The 0 output of flipflop 802 is connected to a second input of NOR gate 810. The 1 output of flipflop 804 is connected to the third input of NOR gates 808 and 810. The 0 output of flipflop 804 is connected to a third input of NOR gate 812. The 1 output of flipflop 806, which corresponds to the clock 2 timing signal, is connected to the fourth input of NOR gates 808, 810 and 812. The output of NOR gate 808 is connected as an input to NOR gate 814; the output of NOR gate 810 is connected as an input to NOR gate 816; and, the output of NOR gate 812 is connected as an input to NOR gate 818. The outputs of gates 814,

816 and 818 are supplied on lines 820, 822 and 824, respectively.

The operation of the circuit illustrated in FIG. 33 will be more fully understood from the timing diagram of FIG. 34. Waveform 826 is the clock 1 timing signal produced at the output of flipflop 800. Waveforms 828, 830, and 832 represent the timing signals produced at the one outputs of flipflops 802, 804, and 806, respectively. It is pointed out that waveform 832 is the clock 2 timing signal. The signal at the output of NOR gate 808 will be at a high level when the 1 outputs of flipflops 800, 802, 804 and 806 are in a low state. Therefore, it can be seen by observing coincident low level signals on waveforms 826, 828, 830 and 832 that the output of gate 808 will be high at time t_1 . NOR gate 814 will invert the output from NOR gate 808. Waveform 834 illustrates the output signal of NOR gate 814. The input connections to NOR gate 810 require that flipflops 800, 804 and 806 be reset, and that flipflop 802 be set. By observing the waveforms 826, 828, 830 and 832 it can be seen that at time t_2 this condition is satisfied. Waveform 836 represents the output of NOR gate 816. NOR gate 812 requires that flipflops 800, 802 and 806 be in a reset condition, and that flipflop 804 be in a set condition. Likewise, by observing waveforms 826, 828, 830 and 832, it can be seen that the conditions required for the output of NOR gate 812 to go to a high level are satisfied at time t_3 . Waveform 838 represents the output of NOR gate 818. The timing signals represented by waveforms 834, 836 and 838 (supplied on lines 820, 822 and 824) are employed within the Range Selection Modules as readout strobes, ROI, ROII, and ROIII.

FIG. 35 illustrates, in logic diagram form, counter and gating circuit 778 that is employed for sequencing the operations within Range Selection Module 196. As shown therein, the clock 2 timing signal is supplied to one of the two inputs of AND gate 840, and to the reset input of flipflop 842. It is pointed out that the negative transition of the clock 2 timing signal is required to reset flipflop 842. The output of AND gate 840 is connected to the toggle input of 6-bit binary counter 844. The toggle input of counter 844 requires, for incrementation thereof, the negative transition of the output signal from gate 840. The six output signals supplied from counter 844, indicative of a count of 1, 2, 4, 8, 16, and 32, are supplied on lines 845-850, respectively. Also, these lines are connected in parallel as the six input signals to NOR gate 852. The output signals supplied from NOR gate 852 will be high when all of the input signals supplied thereto are low. Therefore, it can be seen that the output signal from gate 852 will be indicative of a "counter-0" signal.

Line 850 is connected as an input signal to the set input of flipflop 842. It is pointed out that the set input of flipflop 842 requires the negative transition of the signals supplied thereto for operation thereof. The 0 output of flipflop 842 is connected as an input to NAND gate 854. It will be shown in the discussion hereinbelow that the signal supplied from NAND gate 854 is a clear signal employed for resetting the circuitry employed within the Range Selection Module. The clear signal is also connected to the reset input of counter 844, and the negation of this signal is supplied to the second input of AND gate 840.

Switches S336 and S337 are each connected in series between ground potential and each of the two respec-

tive inputs of AND gate 856. The output of gate 856 is connected to the second input of NAND gate 854. The insertion or non-insertion of a program pin into switches S336 and S337 serves to identify the one of the Range Selection Modules with which the circuits associated with a particular panel face are adapted to operate, as pointed out earlier; such insertion or non-insertion is also supplied to other circuitry, that will be discussed hereinbelow, on lines 858 and 860.

In operation, clock 2 timing signals are passed through AND gate 840 when the clear signal is at a low level. The negative transitions of the clock 2 timing signals will increment counter 844. When counter 844 reaches a count of 63, a high level signal will be supplied to the set input of flipflop 842. However, flipflop 842 will not set until the signal drops to a low level as a result of the subsequent clock 2 timing pulse, whereupon the reset output of flipflop 842 will drop to a low level. If a program pin is inserted into switch S336 and no program pin is inserted into switch S337, then the output of AND gate 856 will be at a high level. The two inputs to NAND gate 854 are at a NOT-AND condition, which is the requirement for supplying a high level output signal therefrom. Therefore, the clear signal will be supplied to the reset terminal of counter 844 and simultaneously inhibit the operation of AND gate 840. The subsequent negative transition of clock 2 will reset flipflop 842. The output of flipflop 842 will, in turn, rise to a high level and cause the output signal from NAND gate 854 to drop to a low level.

Counter 844 requires 63 clock 2 pulses to reach a count of 63 therein. The subsequent negative transition of clock 2 will cause the high level signal on line 850 to drop from a high level to a low level, which will thereby set flipflop 842. The 0 output of flipflop 842 will drop to a low level, and if the second input to NAND gate 854 is high, then the clear output signal will rise to a high level. The next subsequent clock 2 pulse, which corresponds to a count of 64, will reset flipflop 842 and cause the output of NAND gate 854 to drop back to a low level. Therefore, the time duration of a clear pulse is equal to one clock 2 pulse, or 2 milliseconds.

Switches S336 and S337 are connected as inputs to AND gate 856 to inhibit the output of NAND gate 854 for Range Selection Modules programmed as II and III (i.e., Modules 197 and 198 in FIG. 3C). This is due to the fact that one clear signal is employed for all three Range Selection Modules to effect a synchronous operation.

FIG. 36 is a schematic diagram of a ramp generator that is located within Timing and Display Module 202 and is employed within Range Selection Modules as an amplitude reference signal. A constant current source 862 is supplied with positive voltage from a terminal 864. The output of source 862 is supplied to the non-inverting input of amplifier A36. A feedback loop is provided between the output of A36 and the inverting input thereof via the line 866. A capacitor C34 is connected between the non-inverting input of amplifier A36 and ground potential. The collector of a transistor Q34 is also connected to the non-inverting input of amplifier A36, and the emitter thereof is connected to ground potential. More particularly, the transistor Q34 is connected in parallel with capacitor C34. Resistor R95 is connected between terminal 868 and the base

of Q34. Resistor R96 is connected between the terminals 864 and 868.

In operation, the constant current source 862 supplies a current which charges capacitor C34. The voltage developed across the plates of C34 as a result of this supply of current, is applied to the non-inverting input of A36. A voltage will continue to develop across the plates of C34 until transistor Q34 is turned on to discharge the capacitor. Waveform 870, in FIG. 37, illustrates the clear signal supplied from NAND gate 854. Each pulse is 2 milliseconds long and there is a 128-millisecond time interval between pulses. Waveform 872 illustrates the ramp voltage supplied at the output of A36. It is pointed out that the waveform 872 illustrates the discharge of C34 during the clear pulse, and a linear increase in amplitude following the clear pulse. The clear signal is synchronized to counter 844, and the ramp voltage is synchronized to the clear signal. Therefore, the ramp voltage is synchronized to counter 844.

FIG. 38 illustrates digital comparator and set range circuit 784 in logic diagram form. The output signals from 6-bit binary counter 844 are supplied to terminals 874-879 which are connected to one side of a group of twelve digital comparators 880-891, only the first two and last two of which are shown. Switches S354-S359, which define the minimum percentage for Range A, are each connected in series between a source of positive voltage on terminal 892 and the opposite side of digital comparator 880. The output of comparator 880 is connected to one of the two inputs of AND gate 894. The second input of AND gate 894 is connected to terminal 896. The output of AND gate 894 is connected to the set input of flipflop 898.

Switches S360-S365 are each connected in series between terminal 892 and comparator 881. The output of comparator 881 is connected to OR gate 900. The second input of OR gate 900 is connected to terminal 902.

The output of OR gate 900 is connected to the reset input of flipflop 898.

The output of comparator 890 is connected to one of the inputs of AND gate 904. The second input of AND gate 904 is connected to terminal 896. The output of AND gate 904 is connected to the set input of flipflop 906. The output of comparator 891 is connected to OR gate 908. The second input of OR gate 908 is connected to terminal 902. The output of OR gate 908 is connected to the reset terminal of flipflop 906. The AND gates, OR gates, and flipflops associated with the comparators 882-889 are connected in the same fashion as those discussed hereinabove. The output of flipflop 898 is associated with Range A; the output of flipflop 906 is associated with Range F; and, the flipflops which are connected to the comparators 882-889 (not shown) are associated with Ranges B, C, D, and E, respectively.

In operation, an output signal is produced from the comparator 880 when the combination of signals supplied from the terminals 874-879 is identical to the combination of program pins inserted into switches S354-S359. The signal supplied on terminal 896 is the counter 0 signal from NOR gate 852 (FIG. 35). This input to AND gate 894 will inhibit the setting of flipflop 898 when the counter is in a 0 state and no program pins are inserted to close any of switches S354-S359. Comparator 881 operates in the same fashion, and effects the resetting of flipflop 898 through OR gate 900.

The signal supplied to terminal 902 is the clear signal and will reset all of the output flipflops.

Assume, for example, that a program pin is inserted into switches S355 and S363. When counter 844 reaches a count of 2, an output signal would be supplied from comparator 880 and AND gate 894. The counter, of course, is not at a count of zero and the output signal from AND gate 894 will set flipflop 898. Counter 844 will continue to increment, and when it reaches a count of 4, the output from comparator 881 will be passed through OR gate 900 to reset flipflop 898. The clear signal supplied to terminal 902 assures that all flipflops will be reset at the beginning of a cycle of operation.

FIG. 39 illustrates analog comparator and output gating network 770 in logic diagram form. The signal supplied from network 768 on line 772 is supplied to terminal 910. This terminal, in turn, is connected to the non-inverting input of an amplifier A38. The reference ramp voltage from generator 774 is supplied to terminal 912. This terminal is connected to the inverting input of the amplifier A38. It can be seen from the connection of amplifier A38 (no feedback loop) that a comparison operation of the input voltages is effected therein. The output of amplifier A38 is connected to one of the three inputs of AND gate 914. The second input of AND gate 914 is connected to terminal 916. The output of AND gate 914 is connected to the set input of flipflop 918. The reset input of flipflop 918 is connected to terminal 920. The 0 output of flipflop 918 is connected to the third input of AND gate 914. Also, the 0 output of flipflop 918 is connected to the set input of flipflop 922. The reset input of flipflop 922 is connected to terminal 916. The 0 output of flipflop 922 is connected to an input of AND gates 924-929.

The second input of each of the AND gates 924-929 is connected to terminals 930-935, respectively. The output of AND gates 924-929 is connected to an input of NAND gates 936-941, respectively. The second inputs of NAND gates 936-941 are connected in parallel to the output of NOR gate 942. The three inputs to gate 942 are supplied from the outputs of NOR gates 944, 946 and 948. The three inputs to NOR gate 944 are connected to terminals 950, 952 and 954, respectively. The two inputs of NOR gate 946 are connected to terminals 952 and 956. The three inputs to NOR gate 948 are connected to terminals 952, 954 and 958.

In operation, the output signal from amplifier A38 will drop to a low level when the two analog inputs on terminals 910 and 912 are equal in amplitude. The clock 2 timing signal is supplied on terminal 916. If flipflop 918 is in a reset state when the output signal from amplifier A38 drops to a low level, then the output of AND gate 914 will rise to a high level. When the clock 2 timing signal cycles to the subsequent low level, then the output of AND gate 914 will, in turn, drop to a low level signal. As indicated by the small circle and arrow at the set input of flipflop 918, a negative transition of the signal supplied thereto is required for operation thereof. Therefore, when the output of AND gate 914 drops back to a low level, the flipflop 918 will set and the signal on the 0 output will drop to a low level. The negative transition of the signal at the 0 output of flipflop 918 will set flipflop 922. The 1 output of flipflop 922 will, in turn, enable one of the inputs to each of AND gates 924-929.

If flipflop 898 is set by comparator 880 (FIG. 38), then a high level signal will be supplied at the 1 output thereof. This signal is supplied to terminal 930 of FIG. 39. If flipflop 922 is set at the same time that flipflop 898 of FIG. 38 is set, then the output of AND gate 924 will rise to a high level. If the second input of NAND gate 936 is high at this time, the output thereof will drop to a low level.

Line 858 from switch S336 in FIG. 35 is connected to terminal 952. Line 860 from switch S337 is connected to terminal 954. Line 820 from the output of NOR gate 814 in FIG. 33 is connected to terminal 958; line 822 from the output of NOR gate 816 is connected to terminal 956; line 824 from the output of NOR gate 818 is connected to terminal 950. The output signals supplied on the lines 820, 822, and 824 are the readout strobes ROI, ROII, and ROIII, respectively.

Assume, for example, that a program pin is inserted into switch S336, establishing the subject module as Range Selection Module I (196). Therefore, terminal 952 will be at a low level and terminal 954 will be high. NOR gate 944 will be disabled due to the fact that a signal from terminal 954 is high. NOR gate 946 will be disabled due to the fact that the inversion of the signal supplied to terminal 952 is required for operation thereof. However, NOR gate 948 is enabled and the ROI supplied to terminal 958 will pass through the NOR gate to one of the three inputs of NOR gate 942. NOR gate 942 is enabled due to the fact that the second and third inputs thereof are at a low level. The output signal from NOR gate 942 will correspond to an inversion of waveform 843 illustrated in FIG. 34.

Accordingly, it can be seen that the information contained within the flipflops as illustrated in FIG. 38 will be passed through AND gates 924-929 when the two signals supplied to terminals 910 and 912 are equal in amplitude. It can also be seen that ROII will pass through NOR gate 946 when the subject module is programmed as Module II (197), and NOR gate 944 will pass strobe ROIII therethrough when the subject module is programmed as Module III (198). It is pointed out that the outputs of NAND gates 936-941 of one Range Selection Module are connected in parallel by buss line 206 to the respective outputs of a second and third Range Selection Module when three modules are employed in one master controller. The readout strobes are used to distinguish the signals of an individual module from signals of the other Range Selection Modules.

FIG. 40 is a graphical summary of the procedure employed within the Range Selection Module for systematizing the analog signal supplied to the module into discrete ranges. Waveform 960 represents an aggregation of signals supplied from one of the computer modules to the Range Selection Modules which is programmed to accept such signals. It is pointed out that the vertical scale of the graph in FIG. 40 represents percentages on the left side and voltage on the right side. The divisions along the horizontal axis represent the 130-millisecond time intervals between the clear pulses, as indicated by waveform 870 in FIG. 37. It is also pointed out that the amplitude variations illustrated by waveform 960 are exaggerated over the time interval represented by the graph. The two horizontal lines at 60 percent and 42.5 percent represent the upper and lower percentage values, respectively, for a selected exemplary range. The time span between time

t_6 and t_7 is amplified for illustrative purposes. Waveform 960a is the portion of waveform 960 between times t_6 and t_7 .

Assume, for example, that the horizontal lines at 60 percent and 42.5 percent represent the maximum and minimum percentages, respectively, for Range A. When the counter reaches a count which is equal in magnitude to that represented by the combination of program pins inserted into switches S354-S359, then AND gate 894 will be enabled and flipflop 898 will be set. It is pointed out that waveform 872 is synchronized to the counter; therefore, flipflop 898 will be set at a time which will coincide with the time at which the amplitude of waveform 872 is equal to 42.5 percent. It can be seen in the amplified portion of the waveforms that flipflop 898 will be set at the time corresponding to t_8 (representing set time). Simultaneously, the amplitude of waveform 960 is compared to the amplitude of waveform 872 by amplifier A38, and time t_c represents the time at which an equality of the amplitudes is detected. The flipflop will be reset at time t_r .

DETAILED DESCRIPTION OF THE PROGRAM-TIME SELECTION MODULE

FIGS. 41, 42, 43, 44, 45, AND 46

It is the function of Program-Time Selection Module 98 to select a block of data at a designated time of day from an input device, such as a paper tape reader, wherein the block of data corresponds to binary-coded timing data to be transmitted to an individual intersection of a traffic control system. Henceforth, "program" will be used in this description to mean the block of data that corresponds to this stored timing information. The selection of a program is effected by comparing the time of day with the combination of pins inserted into groups of switches.

FIG. 41 illustrates a suggested layout of front panel 962 of Program-Time Selection Module 98. Four individual programs can be selected from one module. Switches S370-S376 are employed for selecting the day of the week that the first two programs are to be selected. Switches S377-S383 are employed for selecting the hour in which the first program is to be selected. Switches S384-S388 are employed for selecting the program number corresponding to the first set of program pins. Switches S389 and S390 are employed for designating this program number a part of system A or system B, respectively. Switches S391-S394 are employed for starting an override time interval which will be explained in greater detail hereinbelow. It is pointed out that the switches S384-S394 are operable only at the time selected by switches S377-S383 and for the day which is selected by switches S370-S376.

Switches S395-S401 select the time of that day programmed by switches S370-S376 for initiating a second program number selected by switches S402-S406. Switches S407 and S408 are employed for designating the program number selected by switches S402-S406 as a part of system A or system B, respectively. Switches S409-S412 are employed for ending the override time interval initiated by switches S391-S394. The remaining groups of program slots on front panel 962 are identical to those discussed hereinabove. Switches S413-S416 initiate a second override time interval, and switches S417-S420 terminate this second override time interval.

FIG. 42 illustrates the Program-Time Selection Module in block diagram form. Signals indicative of the day of the week from the day counter and decoder network 268, as shown in FIG. 5 and discussed hereinabove, are supplied to terminal 964, which is connected to two day selection gates 966 and 968. The output signal from gate 966 is connected in parallel to two digital comparator and gating networks 970 and 972. The output of gate 968 is connected to two additional digital comparator and gating networks 974 and 976. Timing signals from the hours counter and decoder network 260, as shown in FIG. 5, are supplied to terminal 977, which is connected in parallel to four networks 970, 972, 974 and 976. One of two outputs from each of these networks is supplied in parallel to gating network 978. The six output signals from gating network 978 are indicative of the program number selected by Program-Time Selection Module 98. The second output from each of these networks is supplied in parallel to a set time interval circuit 980. The four output signals from circuit 980 are indicative of the override timing intervals T1, T2, T3, and T4 which are supplied on lines 214.

The gate 966 supplies a comparison input signal to networks 970 and 972. Switches S370-S376 are employed within gate 966 to select the day of the week. Switches S377-S383 and switches S389 and S390 are employed within network 978 to select the time of the day for the first two program numbers. Switches S384-S388 are employed within network 978 to select the program number desired for the corresponding time of the day and day of the week. All timing interval programs included in Program-Time Selection Module 98 for establishing a program time, and which override a traffic-actuated program selection, are provided within the circuit 980.

In operation, digital comparator and gating network 970 compares the value represented by the combination of pins inserted into switches S377-S383, and the day of the week determined by the gate 966 and program pins inserted therein; and network supplies two output signals therefrom which are employed within network 978 and the circuit 980, respectively. These signals occur only when an equal comparison is detected within network 970 and differ primarily by gating circuits which will be explained in greater detail hereinbelow. The output gating network supplies a high-level signal on each output line that is connected via the switches S384-S388 contained thereon. The combination of pins inserted represents the program number desired when an equal comparison is detected in network 970.

The set time interval circuit 980 contains four flip-flops that supply the four output signals, T1, T2, T3 and T4. It will be shown in the detailed description of the Program-Range Selection Module how the override timing signals T1, T2, T3 and T4 are employed. Switches S391-S394 effect the connection of the input signals supplied to circuit 980 to the set input of each of the four flipflops contained therein. Switches S409-S412 effect the connection of the input signals supplied to circuit 980 to the reset input of each of the four flipflops contained therein.

The day selection gates 966 and 968 are essentially a NOR gate with seven switches connected in series with each of the seven inputs thereto. FIG. 43 illustrates a NOR gate 982 with the switches S370-S376

connected in series with each of the inputs to the gate. The output of NOR gate 982 is connected to two of the digital comparator and gating networks. If no program pins are inserted into switches S370-S376, then the output of NOR gate 982 will be high at all times. As will be shown in the discussion hereinbelow, it is required that the output of gate 982 be at a low level for the comparator networks to operate. If, for example, a program pin is inserted into switch S373, which would correspond to Thursday, the output of NOR gate 982 will go to a low level when the signal supplied to switch S373 goes to a high level.

FIG. 44 illustrates digital comparator and gating network 970 in logic diagram form. The time of day, expressed in hours, is supplied to the terminals 984-990 from Master Clock Module 100. Terminals 984-990 are connected to digital comparator 992. Switches S377-S383 are connected in series between a source of positive voltage on terminal 994 and comparator 992. The output of comparator 992 is connected to one of the two inputs of AND gate 996. The second input of AND gate 996 is connected to terminal 998, which is connected to the output of NOR gate 982 in FIG. 43. The output of AND gate 996 is connected to two AND gates 1000 and 1002. The second input of AND gate 1000 is connected to terminal 1004. The second input of AND gate 1002 is connected to the output of OR gate 1006. Switch S389 is connected in series between terminal 1004 and one of two inputs to OR gate 1006. Switch S390 is connected in series between the second input of OR gate 1006 and terminal 1008. As indicated in FIG. 5, the output on line 256 of gating network 236 is connected to terminal 1004. Line 258 from gating network 236 is connected to terminal 1008. The output of AND gate 1000 is connected to set time interval circuit 980. The output of AND gate 1002 is connected to output gating network 978.

In operation, an output signal is produced from digital comparator 992 when the combination of signals supplied to the terminals 984-990 coincide with the combination of program pins inserted into switches S337-S383. AND gate 996 requires a high level signal from comparator 992 and a low level signal from NOR gate 982. Therefore, it can be seen that the output of AND gate 996 will be high when NOR gate 982 has a low level output, and digital comparator 992 has a high level output. This combination of signals will occur when the output of the delay counter and decoder network 268 coincides with the program pins inserted into switches S370-S376, and the output of networks 244 and 260 coincides with the programming of switches S377-S383. The signals supplied to terminals 1004 and 1008 are the two half-second pulses having each of their respective leading edges separated by a 1-second interval occurring every 15 minutes.

When the output of AND gate 996 is high, the output of AND gate 1000 will also be high for the half-second pulse duration of the signal supplied on terminal 1004. It will be shown in the description hereinbelow that the signal supplied from AND gate 1000 is employed in the set time interval circuit 980 for setting one of the four flipflops contained therein. A program pin is inserted into either switch S389 or S390 to indicate that the program number selected by Program-Time Selection Module 98 is to be used in system A or system B, respectively. If a program pin is inserted into switch S389, the output signal from AND gate 1002 will occur

when the output of AND gate 996 is high and for the half-second time duration of the pulse supplied on terminal 1004. In a similar manner, the output of AND gate 1002 can occur when the signal supplied on terminal 1008 occurs, and a program pin is inserted into switch S390 instead of S389.

FIG. 45 illustrates set time interval circuit 980 in logic diagram form. The output of AND gate 1000 is connected to terminal 1010. The output of an AND gate, connected in a similar fashion to gate 1000 and contained within networks 972, 974 and 976 are connected to terminals 1011, 1012 and 1013, respectively. Switches S391-S394 are connected in series between terminal 1010 and OR gates 1014-1017, respectively. Switches S409-S412 are connected in series between terminal 1011 and OR gates 1018-1021. Switches S413-S416 are connected in series between terminal 1012 and OR gates 1018-1021. Switches S417-S420 are connected in series between terminal 1013 and OR gates 1018-1021. The third input to OR gates 1018-1021 is connected in parallel to turn-on delay network 1022.

The output of OR gate 1014 is connected to the set input of flipflop 1024. The output of OR gate 1018 is connected to the reset input of flipflop 1024. The output of OR gate 1015 is connected to a set input of flipflop 1026. The output of OR gate 1019 is connected to the reset input of flipflop 1026. The output of OR gate 1016 is connected to the set input of flipflop 1028, and the output of OR gate 1020 is connected to the reset input of the flipflop 1028. The output of OR gate 1017 is connected to the set input of flipflop 1030, and the output of OR gate 1021 is connected to the reset input of the flipflop 1030. The 1 output of flipflops 1024, 1026, 1028 and 1030 is supplied on lines 1032-1035, respectively. These outputs correspond to the signals required for the override time intervals T1, T2, T3 and T4. It is pointed out that flipflops 1024, 1026, 1028 and 1030 contain a diode in series with the output to enable signals from other modules to override the output signals from these flipflops.

In operation, flipflop 1024 can be set when the day of the week and the time of day programmed occurs, which produces a high level signal on terminal 1010 (and a program pin is inserted into switch S391). In a similar fashion, flipflops 1026, 1028 and 1030 may be set by insertion of a program pin into switches S392, S393 and S394, respectively. Flipflop 1024 can be reset by the occurrence of a timing pulse on terminal 1011 when a program pin is inserted into switch S409. The remaining switches operate in a similar fashion. The purpose of the turn-on delay network 1022 is to reset all flipflops when an initial power turn-on occurs.

FIG. 46 illustrates output gating network 978 in logic diagram form. The output of AND gate 1002 is connected to terminal 1036. Similar AND gate connections in networks 972, 974 and 976 are connected to terminals 1037, 1038 and 1039, respectively. Terminals 1036-1039, respectively, are connected in parallel to the four inputs of OR gate 1040. Switches S384-S388 are connected in series between terminal 1036 and one of four inputs to OR gates 1041-1045. Switches S402-S406 are connected in series between terminal 1037 and a second input to OR gates 1041-1045. The remaining groups of program pins illustrated in FIG. 41 under PROGRAM NUMBER are connected in a similar fashion to the remaining inputs

of OR gates 1041-1045. The output of OR gates 1041-1045 correspond to the binary count of 1, 2, 4, 8, and 16, respectively. The output of OR gate 1040 is a reset pulse which will be explained in greater detail hereinbelow. It is pointed out that the OR gates 1040-1045 contain a diode in series with the output to enable signals from other modules to override the output signals from these OR gates.

DETAILED DESCRIPTION OF THE TIMING AND DISPLAY MODULE

FIGS. 47, 48, 49, 50, AND 51

Timing and Display Module 202 provides: a display function for Program-Time Selection Module 98 and Program-Range Selection Modules 204, a timing function for several modules within the master controller, and a sequencing function for the selection of a program via either the Program-Time Selection Module or the Program-Range Selection Module. FIG. 47 illustrates the Timing and Display Module panel face 1048. Lamps L42-L45 are provided for indicating the status of set time interval circuit 980 as shown in FIG. 42. Four switches S422-S425 are provided for selectively generating one of the timing override signals to make the selection of programs time responsive.

Lamps L46-L51 are provided for indicating the status of the six range select output signals from Range Selection Modules 196, 197 and 198. Switches S426, S427 and S428 are provided to select the Range Selection Module (I, II or III) for which the lamps provide a display. Closure of switch S426 will cause the lamps L46-L51 to indicate the status of the six respective ranges selected by Range Selection Module 196. Likewise, closure of switch S427 or S428 will cause the lamps to indicate the status of the range select output signals from Range Selection Modules 197 and 198, respectively.

When a block of timing data is selected for transmission to the intersection traffic controllers throughout the traffic control system, a time delay will exist between the selection of these blocks of data due to the fact that they are selected at prescribed times of the day. However, when programs are selected on the basis of accumulated vehicle detections, such as traffic actuation, two separate programs could be selected in rapid succession. Therefore, a provision is made for generating a minimum time interval between programs selected via traffic actuations. This time interval is labeled on the face 1048 of the Timing and Display Module as "minimum program interval". The amount of time desired for this time interval for the A program may be selected by insertion of program pins into switches S429-S432 in desired combinations thereof. Likewise, switches S433-S436 are provided for selecting the minimum program interval for the B program. Lamp L52, when illuminated, indicates that the minimum program interval for the A system is in a count-down status. Lamp L53, likewise, when illuminated, indicates that the minimum program interval for the B system is in a count-down status. Switch S437 is provided for testing the condition of all display lamps L42-L53 on Timing and Display Module front panel 1048.

FIG. 48 shows the Timing and Display Module in block diagram form. Switches S429-S432 are connected between terminal 1050 and counter and comparator network 1052. Terminal 1050 is connected to

a source of positive voltage. Switches S433-S436 are connected between terminal 1050 and counter and comparator network 1054. Turn-on delay network 1056 is connected to positive voltage on terminal 1050.

The output of turn-on delay 1056 is connected to gating network 1058. Lamps L52 and L53 are connected between gating network 1058 and positive voltage on terminal 1050. Control signals are supplied to network 1052 from network 1058 via line 1060. Also, control signals are supplied to network 1054 from network 1058 via line 1062. The output from the comparator within network 1052 is supplied to network 1058 via line 1064, and the output of the comparator within network 1054 is supplied to network 1058 via line 1066. Six control and timing signals are supplied from the complementary modules to terminals 1068-1073, which are thereby connected in parallel to network 1058.

Gating network 1058 receives control and timing signals on terminals 1068-1073 in addition to comparator output signals on lines 1064 and 1066, and thereby supplies control signals, which are employed within the Program-Range Selection and Program Memory Modules, on line 1074 for the A system and line 1076 for the B system. Program clearing signals for both the A and B systems are supplied on the line 1077. The operation of the circuits contained within gating network 1058 will be more fully understood from the detailed description accompanying FIG. 49.

The six output lines 790-795 of analog comparator and output gating network 770, as shown in FIG. 32, are connected to terminals 1078-1083, respectively, which are, in turn, connected to gating and lamp driver network 1084. Switches S426-S428 are each connected in series between timing circuit 776 and network 1084. Timing circuit 776 is the circuit that was described in detail in FIG. 33 hereinabove. It is pointed out that the three timing signals from timing circuit 776 are the three readout strobes ROI, ROII and ROIII, which are illustrated by waveforms 834, 836 and 838 in FIG. 34. Lamps L46-L51 are connected between network 1084 and positive voltage on terminal 1050.

The four override timing signals from set time interval circuit 980, as shown in FIG. 42, are connected to terminals 1086-1089, respectively, which are connected to gating and lamp driver network 1090. Switches S422-S425 are each connected in series between terminal 1050 and network 1090. Lamps L42-L45 are connected between network 1090 and positive voltage on terminal 1050. Switch S437 is connected between the terminal 1050 and networks 1084, 1090 and 1058. Closure of switch S437 will effect the illumination of all lamps L42-L53 for testing purposes. Ramp generator 774, as illustrated in FIG. 36 and described in the accompanying text hereinabove, is connected to positive voltage on terminal 1050. Ramp generator 774 and timing circuit 776 are a part of Timing and Display Module 202, which are shown in block diagram form in this Figure for illustrative purposes only, and will not be further discussed.

FIG. 49 illustrates gating network 1058 in logic diagram form. Counter and comparator network 1052 is identical to those discussed earlier and will not be discussed in greater detail herein. The output of the comparator, which is supplied on line 1064 (FIG. 48), is connected to terminal 1092, which is, in turn, connected to the input of NOR gate 1094 and one of three

inputs to AND gate 1096. The output of NOR gate 1094 is connected to line 1074. The comparator output signal from network 1054, which is supplied on line 1066 (FIG. 48), is connected to terminal 1098, which is, in turn, connected to the input of NOR gate 1100 and also to one of three inputs of AND gate 1102. The 2-minute clock signal which is supplied from the Master Clock Module 100, is connected to terminal 1068, which is, in turn, connected to the second input of AND gates 1096 and 1102. The reset signal, which is supplied from the output of OR gate 1040 in the Program-Time Selection Module 98, is supplied to terminal 1069, which is, in turn, connected to an input of each of two AND gates 1104 and 1106. Line 256 from gating network 236 (FIG. 5) is connected to terminal 1070. Line 258 of gating network 236 is connected to terminal 1071 which is, in turn, connected to the second input of AND gate 1104 and one of two inputs to NOR gate 1108. Terminal 1071 is connected to the second input of AND gate 1106 and to the second input of NOR gate 1108.

The output of AND gate 1104 is connected to the third input of AND gate 1096 and to one of two inputs of OR gate 1110. The output of AND gate 1106 is connected to the third input of AND gate 1102 and to one of two inputs of OR gate 1112. The signal from turn-on delay network 1056 is supplied to terminal 1114, which is thereby connected to the second input of OR gates 1110 and 1112. The output of AND gate 1096 is the toggle input to the counter contained within network 1052 and is designated line 1060a since it is a part of line 1060 in FIG. 48. The output of OR gate 1110 is the reset input to the counter in network 1052 and is designated herein as line 1060b. The output of AND gate 1102 is the toggle input to the counter contained within network 1054 and is designated herein as line 1062a. The output of OR gate 1112 is the reset input to the counter in network 1054 and is designated herein as line 1062b. The output of NOR gate 1100 is the control signal supplied on line 1076.

Line 1074 is connected to one of two inputs of OR gate 1116. Line 1076 is connected to one of two inputs of OR gate 1118. The second input to each of the OR gates 1116 and 1118 is connected to terminal 1120, which is, in turn, connected to switch S437 (not shown). Switch S437 is employed for testing the status of the display lamps. The output of OR gate 1116 is connected to an input of lamp driver 1122. Lamp L52 is connected between positive voltage and lamp driver 1122. The output of OR gate 1118 is connected to an input of lamp driver 1124. Lamp L53 is connected between positive voltage and lamp driver 1124. Lamp L52 is illuminated by the application of a high-level signal to either of the inputs of OR gate 1116. Likewise, lamp L53 is illuminated by the application of a high-level signal to one of the two inputs of OR gate 1118.

The output signal from NAND gate 854 of FIG. 35, which is designated the clear signal, is connected to terminal 1072 which is, in turn, connected to one of two inputs of AND gate 1126, and is also connected to one of the two inputs of AND gate 1128. It is pointed out that the negative transition of the clear signal is required for operation of AND gates 1126 and 1128. Output line 251 from network 244 is connected to terminal 1073. The signal supplied on this line from Master Clock Module 100 is the 8-minute clock signal. Ter-

minal 1073 is connected to the input of one-shot 1130. The negative transition of the 8-minute clock signal supplied to terminal 1073 is required for operation of one-shot 1130. The output of one-shot 1130 is connected to the second input of AND gate 1126 and the second input of AND gate 1128. The input to AND gate 1128 from one-shot 1130 requires the inversion of the signal supplied thereto for operation thereof.

The output of AND gate 1126 is connected to the set input of flipflop 1132. The output of AND gate 1128 is connected to the reset input of flipflop 1132. The 1 output of flipflop 1132 is supplied through diode CR86 on line 1076a, which is a part of the line 1076 from network 1058. The 1 output of flipflop 1132 is also connected to one of two inputs of OR gate 1134. The output of NOR gate 1108 is connected to the second input of OR gate 1134, the output of which is connected to one of two inputs of NAND gate 1136. The second input of NAND gate 1136 is connected to terminal 1114. It is pointed out that the inversion of the signal supplied to terminal 1114 is required for operation of NAND gate 1136. The output of NAND gate 1136 is supplied on line 1076b, which is a part of line 1076 from network 1058.

In operation, the signal supplied on line 1074 will act upon circuitry within the Program-Range Selection Module (to be discussed in greater detail hereinbelow) to inhibit the selection of a new program for the A system for as long as the signal supplied on this line is at a high level. A high-level signal is supplied on line 1074 when the signal supplied to terminal 1092 is at a low level. This will occur when the contents of the counter within network 1052 does not equal the value selected by the combination of program pins inserted into switches S429-S432. However, when the contents of the counter advances to the value represented by the inserted program pins, the output of the comparator will go to a high level and the output signal on line 1074 will thereby drop to a low level. Lamp L52 will be illuminated each time the signal on line 1074 is high due to the fact that the signal supplied from line 1074 to OR gate 1116 passes therethrough to operate lamp driver 1122. A signal is supplied to the B system on line 1076 in the same fashion as described hereinabove by the application of a comparator output signal to terminal 1098 to operate NOR gate 1100. Lamp L53 is illuminated in the same fashion.

If the contents of the counter within the network 1052 does not equal the value selected by the program pins, then the input signal to AND gate 1096, which is connected to terminal 1092, is at the desired low level for operation. If a new program is not selected by Program-Time Selection Module 98 at this time, the signal supplied to terminal 1069 will be at a low level which will disable the operation of AND gate 1104. Therefore, the output of AND gate 1104 will be at a low level and the third input of AND gate 1096 will be at the desired low level for operation thereof. With the condition stated herein, the negative transitions of the 2-minute clock signal supplied to terminal 1068 will be passed through AND gate 1096. These negative transitions will be supplied on line 1060a to the network 1052 for incrementation of the counter contained therein.

The counter within network 1052 will advance until it reaches a state equal to the value represented by the inserted program pins into switches S429-S432. A

high-level output signal will be supplied from the comparator, also contained therein, to disable AND gate 1096 and cause the output of NOR gate 1094 to drop to a low-level signal. The contents of the counter within the network 1052 will remain the same until a reset signal is supplied to the counter on line 1060b. This signal is produced by the operation of AND gate 1104. AND gate 1102 operates in the same fashion as AND gate 1104 to supply an incrementation signal to the counter contained within network 1054 on line 1062a. The reset signal to network 1054 is supplied from the output of AND gate 1106 and passed through OR gate 1112 in the same fashion as the reset signal for the A system.

The signal supplied on line 1076b from NAND gate 1136 is employed within Program-Range Selection Module 204 as a "program clear" signal. The application of an A system or B system timing signal to terminal 1070 or 1071, respectively, will cause the output of NOR gate 1108 to momentarily drop to a low level. This signal will, in turn, pass through OR gate 1134 to the input of NAND gate 1136. If a turn-on delay signal is not present on terminal 1114, then a low-level signal is required on the second input of NAND gate 1136 for operation thereof. Therefore, the negative spike from NOR gate 1108, which passes through OR gate 1134, will cause a positive spike to be produced at the output of NAND gate 1136. It is pointed out that the application of a high-level signal to terminal 1114 when the output of OR gate 1134 is low will also produce a high-level output signal on line 1076b. The signal on line 1076b will not go to a high level as a result of the signal on line 1076a going high due to the provision of diode CR86. It will be shown in the discussion of the Program-Range Selection Module as to how this signal is employed.

Flipflop 1132 will be set when a clear signal drops to a low level and the output of one-shot 1130 is high. When the output of the one-shot is low, then flipflop 1132 will reset when the clear signal drops to a low level. The purpose for the signal supplied on line 1076a will be more fully understood following the detailed description of the Program-Range Selection Module.

FIG. 50 illustrates the gating and lamp driver network 1084 in logic diagram form. Terminals 1078-1083 are connected to an input of NOR gates 1134-1139. The signals from switches S426, S427 and S428 are supplied to the three inputs of AND gate 1140, the output of which is connected to the second input of each of NOR gates 1134-1139. The outputs of the NOR gates 1134-1139 are connected to an input of OR gates 1142-1147. Switch S437 is connected to terminal 1148, which is connected to the second input of each of OR gates 1142-1147. The output of OR gates 1142-1147 are connected to resettable delays 1149-1154, respectively. The outputs of the delays are connected to lamp drivers 1155-1160, respectively. Lamps L46-L51 are each connected in series between positive voltage and lamp drivers 1155-1160, respectively.

The function of the circuit illustrated in FIG. 50 is to illuminate lamps L46-L51 in accordance with the input signals supplied thereto. The signal supplied to terminal 1148 is the display test from switch S437, and will cause lamps L46-L51 to illuminate when a high-level signal is supplied thereto. AND gate 1140 is employed for selecting a particular Range Selection Module for

which the lamps L46-L51 are to represent output signals. The signal supplied to terminals 1078-1083 are the six output signals corresponding to the six ranges A through F of the Range Selection Modules.

If the circuit illustrated in FIG. 50 is selected to display the status of the six output signals from Range Selection Module 196, then a program pin is inserted into switch S426. The signal illustrated by waveform 834 of FIG. 34 will be applied to the first input of AND gate 1140. The second two inputs of AND gate 1140 will not be at a low level, since these inputs are biased at a high level. The output of AND gate 1140 will be high, and this, in turn, will disable NOR gates 1134-1139. However, when the signal applied to the first input of AND gate 1140 through switch S426 drops to a low level, as illustrated by waveform 834, then the output of AND gate 1140 will drop to a low level. This will enable each of the NOR gates to pass a low-level signal therethrough from any of the terminals 1078-1083. The high-level output signal from NOR gates 1134-1139 will pass through OR gates 1142-1147 to illuminate lamps L46-L51. It is pointed out that the signal supplied from the outputs of NOR gates 1134-1139 will be of a very short time duration due to the short pulse supplied to the first input of AND gate 1140. Therefore, the resettable delay networks 1149-1154 effect a time delay sufficient to view the illuminated lamps.

FIG. 51 illustrates gating and lamp driver network 1090 in logic diagram form. Terminals 1086-1089 are connected to an input of OR gates 1162-1165. The signal from switch S437 is supplied to terminal 1166, which is connected to the second input of OR gates 1162-1165, the outputs of which are connected to inputs of lamp drivers 1168-1171. Lamps L42-L45 are connected between a source of positive voltage and lamp drivers 1168-1171. Accordingly, it can be seen that a high-level signal supplied to terminal 1166 will cause lamps L42-L45 to illuminate simultaneously.

Diodes CR88-CR91 are each connected in series between switches S422-S425 and terminals 1086-1089, respectively. A high-level signal supplied to terminal 1086 will pass through OR gate 1162 to cause lamp L42 to illuminate. A high-level signal supplied to terminals 1087, 1088 or 1089 will likewise cause lamps L43, L44 or L45, respectively, to illuminate. Also, closure of switch S422 will supply a high-level signal to terminal 1086 which will likewise cause lamp L42 to illuminate. The switches S422-S425 are illustrated herein a second time to point out that terminals 1086-1089 are output terminals as well as inputs to buss line 214 (FIGS. 3A and 3C). The closure of switch S422 will not only effect the illumination of lamp L42, but will also supply a high-level signal to the Program-Range Selection Module corresponding to the time interval T1. These signals will be explained in greater detail hereinbelow.

DETAILED DESCRIPTION OF THE PROGRAM-RANGE SELECTION MODULE

FIGS. 52, 53, 54, 55, 56, 57, AND 58

It is the function of Program-Range Selection Modules 204 to accept the six discrete range signals from Range Selection Modules 196, 197 and 198 and to supply a program number to the Program Memory Module. An individual Program-Range Selection Module can select three separate program numbers; and range-select signals from three separate Range Selection

Modules can be accepted to select each of these three program numbers. Also, the Program-Range Selection Modules can be programmed to operate for either the A or B traffic control system.

FIG. 52 shows a suggested layout of front panel 1172 of a Program-Range Selection Module. Switches S438 and S439 are provided for designating the program numbers selected by a Program-Range Selection Module as part of either the A or B traffic control system. Switches S440-S443 are provided for selecting the override timing interval, as discussed in conjunction with the description of the Program-Time Selection Module 98, to inhibit the selection of a program number by this Program-Range Selection Module. Switches S444 and S445 are provided for inhibiting the selection of a program number by this module when a minimum program interval, as supplied from Timing and Display Module 202, is timing out.

Switches S446-S450 are provided for selecting the first of the three program numbers which can be selected from an individual Program-Range Selection Module. Switches S451-S456 are provided for selecting the range signal, from Range Selection Module 196, which will effect the transmission of the program number selected by switches S446-S450 to the Program Memory Module. Switches S457-S468 are provided for selecting the range signal from Range Selection Modules 197 and 198 to thereby transmit the program number selected by switches S446-S450 to the Program Memory Module. The remaining groups of switches under PROGRAM NUMBER and RANGES are provided for selecting the second two program numbers in the same fashion as discussed hereinabove for switches S446-S468. The operation of these switches and the function of the Program-Range Selection Modules 204 will become clearer from the detailed description provided hereinbelow.

FIG. 53 shows a Program-Range Selection Module in block diagram form. The six discrete range signals from the Range Selection Module are supplied on buss line 206 to terminal 1174, which is, in turn, connected to signal inversion gate 1176. Gate 1176 is essentially a NOR gate connected in series with each of the six lines from terminal 1174. The output from gate 1176 is supplied, in parallel, to three input range selection networks 1178, 1179 and 1180. The outputs of these networks are each connected to selection circuits 1182, 1183, and 1184, respectively. The six output lines from the selection circuits 1182-1184 are each connected in parallel to provide six output lines from Program-Range Selection Modules 204 on buss line 210, which are provided as inputs to Program Memory Module 102 to be discussed in greater detail hereinbelow.

A separate output signal is supplied from each of the selection circuits 1182, 1183 and 1184 on lines 1186, 1187, and 1188, respectively. These output lines are connected as an input to program change circuit 1190. Also, the clear signal, as discussed hereinabove, is supplied to terminal 1192 which is also connected as an input to program change circuit 1190. Two signals are supplied from the program change circuit that are supplied to lines external to the Program Range Selection Module. The first of these two signals is supplied on a line 1194 and is connected to the output of gating network 236 of FIG. 5. Therefore, line 1194 is connected to line 256. Likewise, a second line 1195 is connected to line 258. The signals supplied on these lines are des-

ignated A and B, respectively. A third output from circuit 1190 is connected as an input to circuits 1182, 1183 and 1184 on line 1196. Terminals 1198-1205 are connected as inputs to a selection control circuit 1206. The outputs from circuit 1206 are supplied to circuits 1182, 1183, and 1184 on a line 1208.

Switches S451-S468 are contained within network 1178. The remaining two groups of switches located under RANGES are contained within networks 1179 and 1180, respectively. Switches S446-S450 are contained within circuit 1182. Switches S438 and S439 are contained within program change circuit 1190. Finally, switches S440-S445 are contained within circuit 1206.

In operation, the six discrete range signals from a Range Selection Module are supplied to terminal 1174, and gate 1176 inverts the signals for use within the Program-Range Selection Modules 204. Networks 1178, 1179, and 1180 provide output signals to circuits 1182, 1183, and 1184, respectively, as a result of transmitting therethrough range signals on those lines connected via program pins. Selection circuits 1182, 1183, and 1184 select program numbers as a result of input signals from the networks 1178, 1179, and 1180. However, the transmission of these program numbers to a Program Memory Module are controlled by program change circuit 1190 and selection control circuit 1206. These operations will be more fully understood from the detailed description of each of the networks and circuits hereinbelow.

FIG. 54 illustrates, in logic diagram form, an individual input range selection network such as network 1178. Terminals 1210a-1210f are the six inputs from the Range Selection Module representing the respective ranges A - F. Terminals 1210a-1210f are connected to be input of NOR gates 1214-1219, respectively, and the outputs of which are connected to three groups of switches containing six switches per group. Switches S451-S456 are connected in series between the output of NOR gates 1214-1219 and six respective inputs of AND gate 1220; switches S457-S462 are each connected in series between the outputs of NOR gates 1214-1219 and six inputs of AND gate 1221; and, switches S463-S468 are each connected in series between the outputs of NOR gates 1214-1219 and the six inputs of AND gate 1222. The output of AND gates 1220, 1221, and 1222 are supplied on lines 1223, 1224, and 1225, respectively.

In operation, the signals supplied on terminals 1210a-1210f are inverted from a high level to a low level, and vice versa, via NOR gates 1214-1219. AND gate 1220 will supply a high-level output on line 1223 if all of the inputs are at a high level. The biasing for each of the inputs to AND gate 1220 is connected in such a manner that a high-level signal will be supplied to each input if no signal is supplied thereto. Therefore, if no program pins are inserted into switches S451-S456, then the output of AND gate 1220 on line 1223 will be high. If one of switches S451-S456 has a program pin inserted therein, then a low-level signal will be supplied on the respective input to AND gate 1220. Assume, for example, that a program pin is inserted into switch S453. A high-level signal supplied to terminal 1210c will cause the output of NOR gate 1216 to drop to a low level which will thereby be transmitted to the input of AND gate 1220. Therefore, the output on line 1223 will be at a low level. However, if the sig-

nal supplied to terminal 1210c drops to a low level (which is the case when a signal is supplied from the Range Selection Module), then a high-level signal will be supplied through switch S453 to the input of AND gate 1220. Also assume that no other program pins are inserted into switches S451, S452, S454, S455, and S456. Then the only time at which the output of AND gate 1220 will go to a high level is when a low-level signal is supplied to terminal 1210c. The operation of switches S457-S462 as inputs to AND gate 1221 and switches S463-S468 as inputs to AND gate 1222 operate in the same fashion as discussed hereinabove.

FIG. 55 is a logic diagram of a selection circuit such as circuit 1182. The output signals from AND gates 1220, 1221, and 1222 on lines 1223, 1224, and 1225, respectively, are supplied to terminals 1226, 1227, and 1228. These terminals are, in turn, connected to one of the two inputs of AND gates 1229, 1230, and 1231. The second input to each of these AND gates is connected to terminals 1232, 1233, and 1234, respectively. The output of each of AND gates 1229, 1230, and 1231 is connected to the set input of each of flipflops 1232, 1233, and 1234, respectively. The clear signal as discussed hereinabove is supplied to terminal 1236 which is, in turn, connected to the reset input of flipflops 1232, 1233, and 1234. It is pointed out that the negative transition of the clear signal is required to reset these flipflops. Terminal 1236 is also connected to one of four inputs of AND gate 1238. The 1 output of each of flipflops 1232, 1233, and 1234 is connected to an input of AND gate 1238, the output of which is connected to the set input of flipflop 1240. The inversion of the output from AND gate 1238 is connected as one of two inputs to AND gate 1242, the second input of which is connected to terminal 1244. The output of AND gate 1242 is connected to the reset input of flipflop 1240. The 1 output of flipflop 1240 is connected to one of two inputs of AND gate 1246. Also, the 1 output of flipflop 1240 is output line 1186 from circuit 1182. The second input of AND gate 1246 is connected to terminal 1248. The output of AND gate 1246 is connected to the input of emitter follower 1250, the output of which supplies the output program number which is, in turn, supplied as an input to the Program Memory Module. Each of the six output lines has a diode connected in series therewith. Diodes CR92-CR97 are connected in series with the R, 1, 2, 4, 8, and 16 output lines. The anodes of these diodes are connected to the common point which is the output of emitter follower 1250. Switches S446-S450 are each connected in series between the cathode of diodes CR93-CR97, respectively, and the output lines 1, 2, 4, 8 and 16. The group of lines designated by the reference numeral 1252 indicates the connection to selection circuits 1183 and 1184.

In operation, each of flipflops 1232, 1233, and 1234 must be set simultaneously with the presence of the clear signal on terminal 1236 to operate AND gate 1238. It is pointed out that flipflop 1232 corresponds to range parameter I; flipflop 1233 corresponds to range parameter II; and flipflop 1234 corresponds to range parameter III. The signals supplied to terminals 1232, 1233, and 1234 have a short time duration equal to that of the read-out strobes ROI, ROII, and ROIII. The presence of a signal on terminals 1226, 1227, and 1228 from AND gates 1220, 1221, and 1222 as discussed hereinabove, simultaneously with a read-out

strobe, will set flipflops 1232, 1233, and 1234. Since the negative transition of the clear signal resets these flipflops, then the output of AND gate 1238 is substantially the same time duration as the clear signal.

The output signal from AND gate 1238 sets flipflop 1240. If a high-level signal is present on terminal 1248 when flipflop 1240 is set, then the output of AND gate 1246 will go to a high level and an output will be supplied on the reset line through diode CR92 and those output lines which have a program pin inserted into the respective slot to close the switches. If a high-level signal is present on terminal 1244 and the output of AND gate 1238 is low, then flipflop 1240 will be reset by the operation of AND gate 1242.

FIG. 56 illustrates program change circuit 1190 in logic diagram form. The output signals from selection circuits 1182, 1183, and 1184, which are supplied on the lines 1186, 1187, and 1188, respectively, are connected to terminals 1252, 1253, and 1254. These terminals are, in turn, connected to the three inputs of OR gate 1256. The output of OR gate 1256 is connected to the set input of flipflop 1258. The clear signal is supplied to terminal 1255 which is connected to the reset input of flipflop 1258. The negative transition of the clear signal is required to reset flipflop 1258. The 1 output of flipflop 1258 is supplied on line 1260. Also, the 1 output of flipflop 1258 is connected to emitter follower 1262, the output of which is supplied through diodes CR98 and CR99. The anodes of these diodes are connected to the output of emitter follower 1262. Switch S438 is connected in series between the cathode of diode CR98 and the output line 1195, which supplies the A signal. Switch S439 is connected in series between the cathode of diode CR99 and the output line 1195, which supplies the B timing signal.

In operation, the positive transition of a signal present on any of the terminals 1252, 1253, and 1254 will set flipflop 1258 through OR gate 1256. Line 1186 is connected to terminal 1252, and will be at a high level at the beginning of the clear signal provided that the desired range signal inputs have been received at one of the input range selection networks 1178, 1179, and 1180 during the previous 130-millisecond range-selection cycle. The line 1260 is connected to terminal 1248 which enables AND gate 1246, and thereby supplies a high-level signal at the output of emitter follower 1250. It is pointed out that the high-level signal supplied at the output of emitter follower 1250 is of a short time duration, which is determined by the time duration of the clear signal (2 milliseconds). The timing relationship of the circuits described herein will be more fully understood from the detailed description of the timing diagram shown in FIG. 58.

FIG. 57 illustrates the selection control circuit 1206 in logic diagram form. Terminals 1198, 1199, and 1200 are, in turn, connected to one of the two inputs of NOR gates 1264, 1265, and 1266. Switches S440-S443 are connected in series between terminals 1205a-1205d, respectively, and the four inputs to OR gate 1268, the output of which is connected to one of two inputs of OR gate 1270 and to one of four inputs of OR gate 1272. The second input to OR gate 1270 is connected to terminal 1204, and the output is supplied on line 1208a. Terminal 1203 is connected to a second input of OR gate 1272. Switches S444 and S445 are each connected in series between terminals 1201 and 1202, respectively, and the second two inputs of OR gate

1272. The output of OR gate 1272 is connected to the second input of each of NOR gates 1264, 1265, and 1266. The output of these NOR gates is supplied on lines 1208b, 1208c, and 1208d, respectively.

The three read-out strobes, ROI, ROII, and ROIII are supplied to the terminals 1198, 1199, and 1200, respectively. These strobes are passed through gates 1264, 1265, and 1266 when the output signal from OR gate 1272 is at a low level. The signals supplied to terminals 1201 and 1202 are the minimum program interval timing signals which are supplied from Timing and Display Module 202 as discussed hereinabove. These signals can be supplied to the inputs of OR gate 1272 only when a program pin is inserted into either of the switches S444 or S445. The signal supplied to terminal 1203 is that signal which is supplied on the line 1076a of FIG. 49, and is designated PRGA + PRGB. The signals supplied to terminals 1205a-1205d are the timing override signals T1, T2, T3, and T4 which are supplied from the Program-Time Selection Module 98.

In operation, the output of OR gate 1268 will be at a low level if no program pins are inserted into the switches S440-S443, or if no timing override signals are present on terminals 1205a-1205d when program pins are inserted into the switches. The signal supplied to terminal 1204 is a program clear signal which is further supplied on line 1076b within Timing and Display Module 202. It is pointed out that the program clear signal is present for a short time duration (approximately 50 microseconds) as a result of either the A or B system timing signals being present on terminals 1070 or 1071, respectively, in FIG. 49.

FIG. 58 is a graphical summary of the timing relationship of signals controlling the operation of the Range Selection Modules, Timing and Display Module, Program-Range Selection Modules, and Program Memory Module. Waveform 1274 represents the output from one of the computers, such as the Density Computer. The change in the waveform with respect to time is exaggerated for illustrative purposes. Assume, for example, that range A has a minimum value of 10 percent and a maximum value of 20 percent. Therefore, the two horizontal lines corresponding to 10 and 20 on the vertical scale represent the low and upper percentages, respectively, programmed for range A. Likewise, range B is programmed to have a minimum value of 30 percent and a maximum value of 40 percent. It is pointed out that, in this example, a gap exists between 20 percent and 30 percent, more particularly, between the programmed limits of the programmed bands of ranges A and B.

Waveform 1276 represents the clear signal, which originates within Range Selection Module 196. This waveform does not show all of the positive pulses, to avoid ambiguity. Waveform 1277 represents the output of flipflop 1240 in FIG. 55. Waveform 1278 represents the 1 output of flipflop 1258 in FIG. 56. Waveform 1279 represents the program clear signal, which is produced within the Timing and Display Module.

In operation, the signal represented by waveform 1274 intercepts the minimum value for range A, which thereby selects the program number designated for range A. The first pulse of the clear signal that occurs after the intersection of waveform 1274 with the minimum value for range A effects the setting of flipflop 1240 by the application of the clear signal to terminal 1236. Waveform 1277 illustrates the 1 output of flip-

flop 1240. Line 1186 is connected to terminal 1252. Therefore, when a signal is supplied from the 1 output of flipflop 1240 the positive transition of this signal is supplied to the set input of flipflop 1258. Waveform 1278 shows that the 1 output of flipflop 1258 goes to a high level at this time. The negative transition of the clear signal supplied to terminal 1192 resets flipflop 1258. Waveform 1278 shows that the output drops back to a low level following the negative transition of waveform 1276, which is the clear signal.

Assume, for example, that a program pin is inserted into switch S438. Therefore, when flipflop 1258 is set a signal is supplied on the line 1194 through switch S438. Line 1194 is connected to terminal 1070 of FIG. 49. Therefore, the positive transition of the output signal from flipflop 1258, as illustrated by waveform 1278, effects a positive pulse on line 1076b from NAND gate 1136 via NOR gate 1108 and OR gate 1134. This signal is illustrated by waveform 1279 and is designated program clear signal. The program clear signal, which has a time duration of 50 microseconds, is supplied to terminal 1244 in selection circuit 1182, and to an identical terminal in selection circuits 1183 and 1184. Also, this signal is common to any additional Program-Range Selection Modules connected in parallel with this module. It is pointed out that the output of AND gate 1238 is at a high level for the duration of the clear pulse. Therefore, the application of the program clear signal to terminal 1244 will not reset flipflop 1240 at this time.

Waveform 1274 intercepts the horizontal band programmed for range A at time T_1 and again at time T_2 . However, at time t_2 flipflop 1240 has not been reset and the 1 output therefrom will remain at a high level state, as shown by waveform 1277. Therefore, flipflop 1258 will not set since a positive transition is required at the input of OR gate 1256 for operation thereof to thereby set the flipflop. Waveform 1275 represents the output of a flipflop contained within selection circuit 1183 that is connected in the same manner as that shown for the connection of flipflop 1240 in FIG. 55. Accordingly, it can be appreciated from the discussion hereinabove that the same program number will not be re-transmitted to the Program Memory Module twice in succession when an input signal, such as represented by waveform 1274, passes into and out of and then back into the programmed range. The input signal must intercept a different programmed range to effect the transmission of a program number to the Program Memory Module.

Due to the exclusive programming of ranges, which requires that no two ranges can overlap in percentage values, only one circuit can impulse the output diodes at a time. Therefore, when flipflop 1240 is set and flipflop 1258 is also set, an output signal will appear at the anode of diodes CR92-CR97. Assume, for example, that the circuit illustrated in FIG. 55 is programmed to select a program number 11. Therefore, a program pin is inserted into switches S446, S447, and S449. Waveforms 1280-1285 represent the output signals appearing on the buss lines R, 1, 2, 4, 8, and 16 (210). It is pointed out that the time duration of this output signal is equal to that of the clear signal. At time t_3 a new program number is transmitted to the Program Memory Module. Waveforms 1280-1285 illustrate the transmission of number 21. The reset signal, as shown by waveform 1280, is always transmitted with the program

number; and its use in the Program Memory Module will be described in greater detail hereinbelow.

There are two different types of override signals provided for inhibiting the generation of a program number on the output buss lines. The first of these override timing signals is produced within the circuit 980 of FIG. 42. These signals are supplied to terminals 1205a-1205d. The selection of one of these override timing signals is effected by inserting a program pin into one of the switches S440-S443. The output of OR gate 1268 supplies this selected override timing signal to OR gates 1270 and 1272. If the output of OR gate 1272 is high, this will inhibit the operation of NOR gates 1264, 1265, and 1266. Therefore, any range selection signal supplied to terminals 1210a-1210f will not appear at the input to networks 1178, 1179, and 1180. The implication of this condition is that the conditions for the range selection circuits, such as illustrated in FIG. 55, will not be satisfied during the duration of the timing override signals. At the same time the output of OR gate 1268 will cause the output of OR gate 1270 to go high which will, in turn, cause flipflop 1240 to be reset via gate 1242. This first type of override timing signal inhibits the selection of a new range by inhibiting NOR gates 1264, 1265, and 1266 in addition to resetting any previously-remembered traffic responsive program selection.

The second type of override timing signal is of a temporary nature which effects only the selection of a range from the signals supplied to terminals 1210a-1210f. This type of override timing signal is supplied to terminals 1201, 1202, and 1203. The signals supplied to terminals 1201 and 1202 are the minimum program intervals discussed hereinabove. The signal supplied to terminal 1203 is the PRGA + PRGB signal. This signal is at a high level when a previously selected program is being executed by the Master Controller. This signal is also at a high level for a short time duration every 15 minutes out of each hour. The signal supplied to terminal 1203 delays the recognition of range selection signals supplied to AND gates 1229, 1230 and 1231. The purpose for this signal is to prevent the A and B line pull-up from Master Clock Module 100 from being interpreted as a new traffic-actuated program. This will be more fully understood from the detail description of the Program Memory Module.

DETAILED DESCRIPTION OF THE PROGRAM MEMORY MODULE

FIGS. 59 and 60

It is the function of the Program Memory Module to accept program numbers supplied thereto from either the Program-Time Selection Module 98 or the Program Range Selection Modules; to store this program member within a register contained therein, and to supply this program number to a comparator 104 upon command by a signal from the program service flipflop 110. Also, the Program Memory Module displays the contents of the program number registers contained therein by lamps provided on front panel 1290, shown in FIG. 59. Additional programming features are provided within the Program Memory Module to supply the program number stored within the registers periodically, wherein the time interval between such transmissions of program numbers is selectable via program pins.

Lamps L55-L59 are provided for displaying the contents of a register containing the A system program number. Likewise, lamps L60-L64 are provided for displaying the contents of the B register contained within the module. Lamps L65 and L66 are provided for displaying manual selection of a program number for either the A or B system, respectively, from program pin selections to be discussed hereinbelow. Switch S470 is provided for manually forcing all lamps to illuminate for test purposes.

As alluded to earlier, a program number can be manually selected from the program pin slots on panel 1290 of the Program Memory Module. Switches S471-S482 are provided for manually selecting a program number for either the A or the B system.

The program numbers stored within the registers contained within the Module can be supplied to the program number comparator 104 periodically by selecting a PROGRAM INTERVAL in hours via switches S483-S485 for the A system, and switches S486-S488 for the B system.

FIG. 60 illustrates the Program Memory Module in block diagram form. The A system timing signal, which is produced within Master Clock Module 100 on line 256, and also from the Program-Range Selection Module 204 on line 1194, is supplied to terminal 1292. Likewise, the B system timing signal, which is also produced within the Master Clock Module and in the Program-Range Selection Module, is supplied to terminal 1293. Terminals 1292 and 1293 are connected, in parallel, to input gating network 1294. The six parallel lines from output gating network 978 of the Program-Time Selection Module are connected to terminals 1295-1300. The six parallel output lines from the Program-Range Selection Module are also connected to terminals 1295-1300. It is pointed out that these six parallel outputs correspond to the lines designated R, 1, 2, 4, 8, and 16, which are provided for supplying the program number selection. The one-cycle-per-second timing signal from the Master Clock Module is supplied to terminal 1301 to effect blinking of the display lamps at certain times, to be explained in greater detail hereinbelow.

Input gating network 1294 accepts the program number that is supplied to terminals 1295-1300 from either the Program-Time Selection Module or the Program-Range Selection Module, and further supplies this number to A register 1302, or to a B register 1304. The selection of the register that will receive the input signals for the program number is determined by either an A or B system timing signal that is supplied to either terminal 1292 or 1293, respectively. The contents of A register 1302 are supplied, in parallel, to lamp driver network 1306 and to output gating network 1308. The contents of the B register are supplied, in parallel, to lamp driver network 1310 and to output gating network 1308. Lamps L55-L59 and lamp L65 are each connected in series between a source of positive voltage on terminal 1312 and lamp driver network 1306. Lamps L60-L64 and lamp L66 are each connected in series between a source of positive voltage on terminal 1314 and lamp driver network 1310.

Control signals are supplied from input gating network 1294 to lamp driver networks 1306 and 1310, network 1308, and to repeat program gating network 1316 on line 1318. The output from network 1316, which is provided on line 1319, is supplied to the set

input of program service flipflop 110 of FIG. 3B. Output line 1320 from network 1316 is supplied to the program service flipflop for the B system. A signal is supplied on line 1319 to thereby set the program service flipflop, shown in FIG. 3B by the line labelled "change program A."

An output-control signal is supplied to output gating network 1308 on line 1322 from repeat program gating network 1316. The output signal from program service flipflop for the A system is returned to the Program Memory Module via the line labelled Service A program in FIG. 3A, and is supplied to terminal 1324 of FIG. 60. Likewise, the output of the Program Service Module for the B system is supplied to terminal 1325. Terminals 1324 and 1325 are, in turn, connected to inputs of output gating network 1308. Six parallel output lines 1326-1331 from output gating network 1308 are connected as an input to the program number comparator 104 (FIG. 3A). Output line 1332 from network 1308 supplies the PRGA + PRGB signal discussed hereinabove. This signal is present when a signal is supplied to either terminal 1324 or 1325 from the program service flipflops for System A or System B, respectively.

The minimum program interval timing signals produced within Timing and Display Module 202 are supplied to terminals 1334 and 1335, respectively. The presence of an inhibit signal on either of these terminals will supply a signal on line 1322 to network 1308 that will prevent the transmission of a program number therefrom. Timing signals from the Master Clock Module are supplied to terminals 1336, 1337, and 1338. The signals supplied to these terminals are the 0.25 hour, 0.5 hour and 1 hour timing signals, respectively. These timing signals are employed within the repeat gating network to supply input signals for selecting the program interval employed for repeating the transmission of a program number from output gating network 1308.

In operation, the signals supplied on terminals 1295-1300, corresponding to the program number, are entered into either A register 1302 or B register 1304 in accordance with the presence of a timing pulse on either terminal 1292 or 1293, respectively. The A system timing signal goes to a high level if a program pin is inserted into switch S438 on the Program-Range Selection Module. Likewise, the B system timing signal goes to a high level if a program pin is inserted into switch S439. The A and B system timing signals are also supplied from the Master Clock Module every quarter hour on the lines 256 and 258 from the network 236 (FIG. 5). The presence of these timing signals at the respective terminals of the Program Memory Module could cause the interpretation of noise which may be supplied on the lines connected to terminals 1295-1300, and thereby create an erroneous loading of program numbers into the registers 1302 and 1304. One shot 1130, AND gates 1126 and 1128, and flipflop 1132 of FIG. 49 are provided to eliminate this problem.

Referring again to FIG. 49, the signal supplied to terminal 1072 is the clear signal and the signal supplied to terminal 1073 is the 8-minute clock signal. It is pointed out that the A and B system timing signals, which are produced within the network 236, are likewise synchronized to the 8-minute clock. The one shot 1130 is operated on the negative transition of the 8-minute

clock signal. A negative transition of the clear signal occurring at the time the one shot 1136 is in operation will set flipflop 1132 through AND gate 1126. The one output of flipflop 1132 is supplied as an input to OR gate 1134. The output of OR gate 1134 is supplied to one input of NAND gate 1136. A high-level signal at the output of OR gate 1134 will cause the output signal on line 1076b to drop to a low level, assuming that a turn-on delay signal is not supplied to terminal 1114 at this time. Therefore, a program clear signal is not supplied to terminal 1204 of FIG. 57, but the PRGA + PRGB is supplied to terminal 1203. Therefore, the output of OR gate 1272 will be at a high level and thereby inhibit the operation of NOR gates 1264, 1265, and 1266. This operation will not allow the recognition of range selection signals at the input of AND gates 1229, 1230, and 1231. Accordingly, it can be appreciated from the discussion hereinabove that occurrence of the A and B system timing signals every quarter hour are prevented from effecting an erroneous recognition of a new traffic actuated program number from the Program-Range Selection Module.

Switches S471 through S482 are contained within the output gating network 1308. A program pin inserted into either switch S471 or switch S477 will inhibit the recognition of a program number from either the Program-Time Selection Module or the Program-Range Selection Module. If a program number is manually selected via switches S471 through S482, then this number will be supplied on lines 1326-1331 and will have precedence over the contents of registers 1302 and 1304.

Lamp drivers 1306 and 1310 indicate the contents of A register 1302 and B register 1304, respectively, at all times. If a program number has been manually selected, then display lamps L55-L64 will blink on and off while displaying the contents of each of the registers. The display lamps will also blink during the time interval between the loading of program numbers into the registers and the time the programs are initiated by the data transmission circuitry.

The program numbers selected by either switches S471-S482, or the contents of A register 1302 and B register 1304 can be retransmitted on lines 1326-1331, periodically, by the insertion of a program pin into one of the switches located under PROGRAM INTERVAL. These switches are located within repeat program gating network 1316. A signal present on either line 1319 or 1320 will set the program service flipflop for either the A or B system, respectively. Therefore, the repeat program gating network has the capability of inhibiting program selection signals on line 1318 if a PROGRAM INTERVAL is programmed.

Accordingly, it can be appreciated from the discussion hereinabove that a program number can be loaded into either A register 1302 or B register 1304 by supplying a combination of signals which correspond to a program number to terminals 1295 through 1300 in conjunction with an A system or B system timing signal to terminal 1292 or 1293, respectively. The contents of the registers are always displayed by the lamps; however, the contents are not transmitted on output lines 1326-1331 until a signal is supplied to either terminal 1324 for A system or 1325 for B system. These signals are supplied to terminals 1324 and 1325 as a result of a change-program-A signal on line 1319 or a change-program-B signal on line 1320. Under normal opera-

tions, such as when no program interval is programmed, a signal is supplied on lines 1319 and 1320 as a result of a signal supplied from input gating network 1294 to the network 1316 via line 1318.

BRIEF SUMMARY

FIG. 61

FIG. 61 is a consolidated block diagram of the master controller which will be helpful in summarizing the operation of the Multi-Intersection Traffic Control System disclosed hereinabove. Master Clock Module 100 and a conventional power supply (not further described) are contained within the block indicated as Program Selection Group 1342 which groups further includes Program-Time Selection 98, Program Memory 102, Range Selection 196-198, Program-Range Selection 204, and Timing and Display 202. The following modules are contained within the block indicated as Computer Group 1344: Detector Input Monitor 166, Density Computer 184, Volume Computer 188, Speed Computer 188, and Ratio Computer 192.

Program Transmission Group 1346 contains the tape reader 90 and the following circuits: tape reader control, frame generator, cycle counter, and offset counter. Program service flipflop 110, transmit gates 128, and line transceiver 132 are all contained within Line-Driver 1348. Corresponding circuits for the B system are contained within Line-driver 1350. Receiver gates 146, word decoder 152, and lamp drivers 160 are all contained within Feedback Decoder and Display Driver Group 1352.

Timing signals and power are supplied to groups 1342, 1344 and 1346 from circuits 1340. Vehicle actuation signals for the A and B systems are supplied to Computer Group 1344 via Line-Drivers 1348 and 1350, respectively, group 1352, and line 1354.

Computer Group 1344 supplies analog signals having values corresponding to parameters which have been calculated therein to Program Selection Group 1342 on line 1356. Group 1342 selects a program number from a plurality thereof in accordance with the analog signal value, and supplies signals to Program Transmission Group 1346 to effect transmission of a block of data identified by the program number selected by Group 1342. Data blocks (programs) identified for the A system are transmitted, via Line-Driver 1348, to the insertion controllers connected to Line A. Also, Group 1346 effects the transmission of data blocks identified for the B system, via Line Driver 1350, over Line B intersection controller connected thereto. Feedback signals appearing on either Line A or Line B interpreted by Group 1352 to supply traffic actuation signals to Computer Group 1344. Also, Group 1352 may provide signals to a visual display, such as a map, (not shown) to indicate the status of intersections throughout the system.

Referring back to FIG. 2, intersections 1360-1365 are controlled by data supplied on Line A, intersections 1366-1370 are controlled by data supplied on Line B from master controller 70. Streets A and B are two main arteries of east-west traffic flow. Vehicle detectors 74 located at intersections 1360 and 1366 sense the eastbound traffic activity on Streets A and B, respectively, and the vehicle detectors located at intersections 1365 and 1370 sense the westbound traffic activity on Streets A and B, respectively. The vehicle detectors located at intersections 1362 and 1368 can be

employed for sensing the differences in westbound traffic activity caused by additions and subtractions of vehicles at intersections 1364 and 1370, respectively.

The offset timing for traffic flow along a street is favored for the heaviest traffic activity. In the example illustrated in FIG. 2, offset timing of lights 76 along Street A or Street B could be favored for either eastbound or westbound traffic flow, depending on the values of traffic parameters, computed as described herein, from signals received from the various vehicle detectors. A program of signals to control the cycling time of a related group of traffic lights to promote optimum traffic flow may thus be provided, either in response to currently computed traffic parameters or as a function of the time of day.

What is claimed is:

1. A method of changing timing of energization of a plurality of traffic signal devices located throughout an area of related traffic movement, wherein the timing of energization of said signal devices is controlled by a timing apparatus at selected locations in said area said method comprising:

- a. storing a plurality of different data blocks representative of time duration in a storage medium for transmission in the form of electrical signals commensurate with the time duration in any of said data blocks;
- b. electrically indicating the presence of vehicles at selected locations in said area;
- c. computing a traffic flow parameter value derived from the indication of vehicle presence at one or more of said selected locations over a selected time period;
- d. generating a time-related analog signal having a magnitude variable in response to the value of said computed parameter;
- e. selecting one of said data blocks as a function of said analog signal magnitude; and
- f. transmitting said selected data block to said timing apparatus for changing the timing of energization of said traffic signal devices to that of said selected data block.

2. The invention according to claim 1 and further including the steps of establishing a plurality of discrete ranges into which the value of said analog signal magnitude may fall, determining the one of said ranges into which said value does fall, and selecting one of said time duration data blocks for transmission in accordance with said one range.

3. The invention according to claim 2 wherein digital signals are provided to indicate the range into which the value of said analog signal magnitude falls.

4. The invention according to claim 1 wherein said parameter is traffic density.

5. The invention according to claim 4 wherein vehicle presence is indicated by switching an electrical indicating signal between a first and a second level, respectively, when vehicles are and are not in one of said selected locations, whereby traffic density at said one location over a selected time period may be computed by calculating the percentage of said time period for which said indicating signal is at said first level.

6. The invention according to claim 5 and further including the step of averaging a plurality of said indicating signals from a corresponding plurality of said selected locations to provide an average value of traffic density over said plurality of locations.

7. The invention according to claim 1 and further including the steps of electrically indicating the presence of vehicles in two separate groups of selected locations in said area, computing separate parameters and generating separate analog signals for each of said groups, and selecting a separate one of said time duration data blocks for controlling energization of said traffic signal devices in each of said groups of locations.

8. The invention according to claim 1 and further including the step of computing an additional parameter value commensurate with said vehicle presence indications, the additional parameter being related to but different than the first-mentioned parameter, and calculating the ratio of one of said parameter values to the sum of the two parameter values, and selecting said time duration data block for transmission as a function of said ratio.

9. The invention according to claim 8 and further including the steps of establishing a plurality of discrete ranges into which the value of said ratio may fall, determining the one of said ranges into which said ratio does fall, and selecting one of said data blocks for transmission in accordance with said one range.

10. The invention according to claim 1 and further including the step of selecting one of said data blocks for transmission at a preselected time of day, while inhibiting transmission of any of said data blocks selected as a function of said analog signal magnitude.

11. A method of monitoring input signals from a plurality of vehicle presence detectors at selected locations in a traffic sampling area, said method comprising:

- a. providing a first indication signal level during the time a vehicle is present at any one of said selected locations;
- b. providing a second indication signal level during the time no vehicle is present at any one of said selected locations;
- c. periodically determining whether said indication signal level has changed between said first and second levels during the period; and
- d. providing a third indication signal level in response to a determination that no change between said first and second levels has occurred during said period.

12. The invention according to claim 11 and further including the step of calculating from said indication signals a traffic parameter based on the presence of vehicles at said selected locations.

13. The invention according to claim 12 wherein the calculation of said parameter is based only on said first and second indication signal levels, any third indication signal levels being disregarded.

14. The invention according to claim 13 wherein separate indication signals are provided from each of a plurality of vehicle presence detectors at different selected locations, and further including the step of averaging said indication signals in calculating said parameter.

15. The invention according to claim 11 wherein said period may be selectively varied.

16. In a multi-intersection traffic control system including at preselected locations,

- a. traffic signal devices;
- b. vehicle presence detectors; and
- c. intersection controllers having a timing apparatus to control energization of said signal devices in pre-

determined cycles, wherein the improvement comprises a master control apparatus for accepting actuation signals from said detectors and providing time duration data for changing said predetermined cycles of said timing apparatus, said control apparatus further including:

- d. storage means for a plurality of discrete programs of time duration data, each associated with said predetermined cycles;
- e. computer means for calculating from said vehicle actuation signals at least one parameter having a value derived therefrom, and representing said parameter by an analog signal;
- f. first selection means responsive to at least one of said analog signals to select one of said discrete programs in accordance with the value thereof; and
- g. means for transmitting the time duration data of said selected program to said timing apparatus to thereby change the predetermined cycles for controlling the energization of said signal devices.

17. The invention according to claim 16 wherein said storage means comprises a punched tape and said transmitting means comprises means for generating electrical signals related to the position of holes punched in said tape.

18. The invention according to claim 16 and further including clock means for generating electrical pulses in predetermined time sequences and second selection means to select and transmit the data of one of said discrete programs in accordance with a preselected combination of said pulses and to inhibit the simultaneous transmission of programs selected by said first selection means.

19. The invention according to claim 18 and further including input circuitry for receiving said vehicle actuation signals and supplying same to said computer means, and means for periodically determining whether any of said vehicle presence detectors have failed to register a change in their respective actuation signals during a preselected time interval.

20. The invention according to claim 19 wherein selected pulses from said clock means are applied to said input circuitry to establish said time interval.

21. The invention according to claim 20 and further including means for inhibiting transmission to said computer means of said vehicle actuation signals from detectors which have failed to register a change in actuation signals during one of said time intervals.

22. The invention according to claim 18, wherein said first selection means includes:

- a. a number N of program selection means responsive to predefined amplitudes of said analog signals; and

- b. means for rendering inoperative N-1 of said program selection means, said means for rendering inoperative being controlled in accordance with preselected states of said clock means, whereby one of said discrete programs is selected by the operative program selection means.

23. The invention according to claim 22 wherein said meters include means providing a permanent record of continuous variations in said parameters.

24. The invention according to claim 16 and further including circuit means for determining into which one of a plurality of preselected ranges of values the value of said analog signal falls, and said first selection means

is responsive to said one range to select said program in accordance therewith.

25. The invention according to claim 16 wherein said computer means is adapted to compute first and second parameter values associated with related but different groups of said vehicle actuation signals. 5

26. The invention according to claim 25 wherein said first and second parameter values are averaged in arriving at said analog signal.

27. The invention according to claim 25 and further including means for computing the ratio of said first parameter value to the sum of said first and second parameter values. 10

28. The invention according to claim 16 and further including a plurality of output meters for visually indicating the value of one or more of said parameters. 15

29. The invention according to claim 16 and further including means for providing a permanent record of the identification of selected blocks of time duration data transmitted to said timing apparatus together with the time and date of transmission thereof. 20

30. In a traffic control system, an apparatus for receiving input signals from a plurality of sensing devices, said input signals changing between high and low levels in response to random actuations of said sensing devices, said apparatus comprising, in combination: 25

- a. means providing a first level output signal in response to a high level input signal;
- b. means providing a second level output signal in response to a low level input signal;
- c. timing means periodically providing electrical timing signals to establish repetitive time intervals; and

- d. means providing a third level output signal in response to one of said timing signals when said input signal has remained at one of said high and low levels during said time interval preceding said one timing signal.

31. The invention according to claim 30 wherein said apparatus receives said input signals from a plurality of separate vehicle presence detectors which provide high and low signals in response to the presence or non-presence of a vehicle at the respective detector locations.

32. The invention according to claim 30 and further including means for selectively varying the duration of said timing intervals.

33. The invention according to claim 30 and further including bistable switching means and gating means, said bistable means being turned on by said timing signals and off by said input signals, and said gating means being enabled by a previously established on state of said bistable means to pass one of said timing signals, said third level signal being provided in response to the passing of one of said timing signals by said gating means.

34. The invention according to claim 33 wherein said bistable means comprises a flipflop having said input signals as a set input and said timing signals as a reset input.

35. The invention according to claim 34 and further including electronic latch means intermediate of said flipflop and gating means and the output of said apparatus.

* * * * *

35

40

45

50

55

60

65