United States Patent

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Paris, France
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[33] **France**
[31] **51,268**

[54] **METHOD AND SYSTEM FOR FINDING OR PLOTTING AN OPTIMUM PATH**

18 Claims, 6 Drawing Figs.

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[51] **Int. Cl.** **G06g 7/48,** G06g 7/62, G06j 1/00
[50] **Field of Search** 235/185, 180; 35/24

[56] **References Cited**

UNITED STATES PATENTS

3,474,240	10/1969	Marquis et al.	235/185
3,053,453	9/1962	Bock et al.	235/185
3,250,902	5/1966	Mauchly	235/185
3,289,323	12/1966	Fondahl	35/24
3,380,177	4/1968	Wagner	35/24

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ABSTRACT: Nodal and link elements are arranged to simulate a system between which a path is to be formed, the link element including, selectively, time delays in accordance with characteristics of the interconnections between nodal points of the system. A point, or set of points forms a departure point, and a single, or a set of points forms an arrival point. A signal applied (under control of a clock) to a node will propagate along the links from node-to-node, in accordance with the timing of the delaying circuits on the links. Once a signal is applied to the node, the node is inhibited from accepting other signals, so that the shortest (smallest delay) path from a departure to an arrival point is established. A tracing signal is then propagated along a parallel path from the departure to the arrival point, so that the path can be displayed.

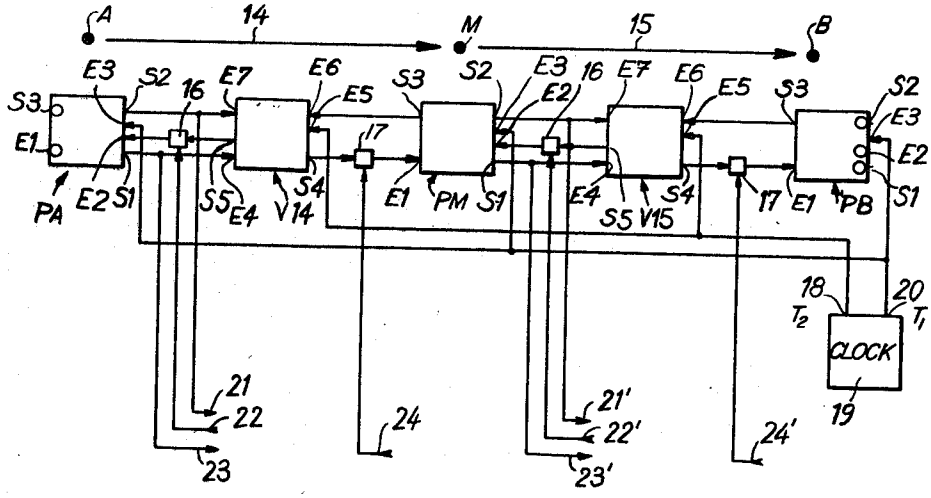


Fig. 1

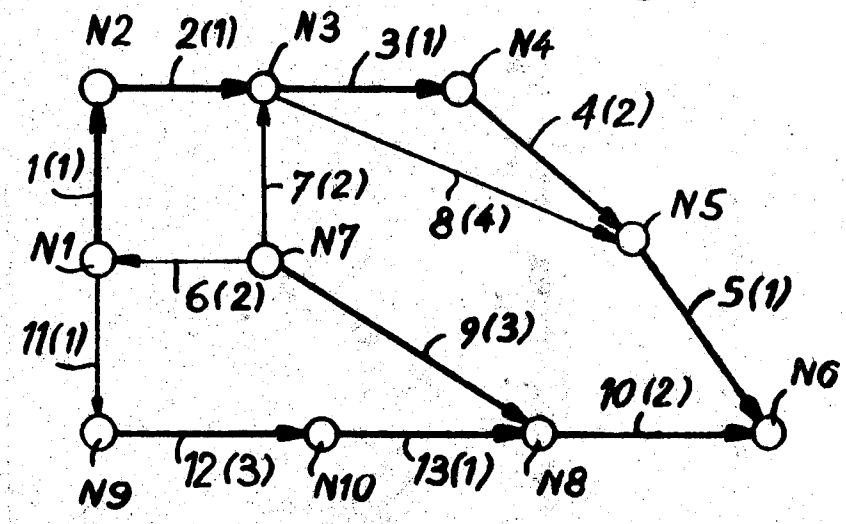
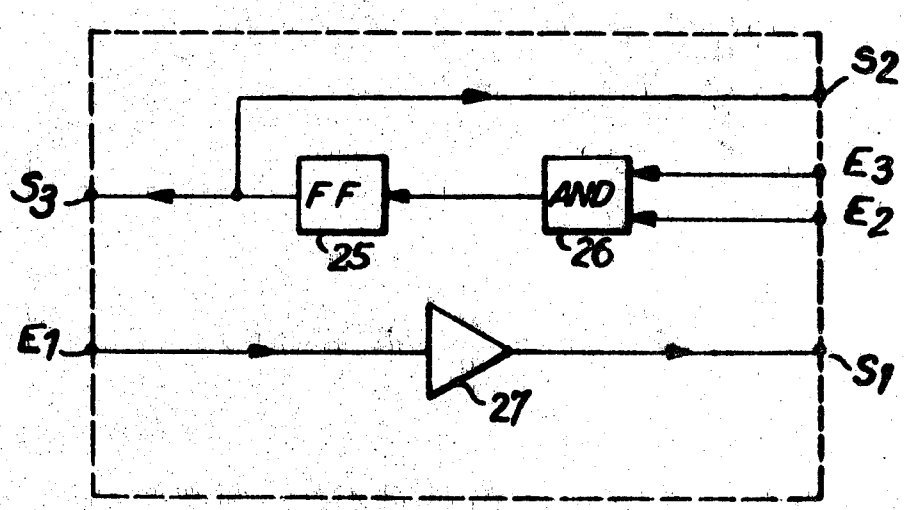

N2
2(1)
N3
3(1)
N4
4(2)
1(1)
7(2)
8(4)
N5
N1
N7
6(2)
5(1)
11(1)
9(3)
10(2)
N6
N9
12(3)
N10
13(1)
N8

Fig. 3


S2
E3
E2
S3
FF
AND
25
26
E1
S1
27

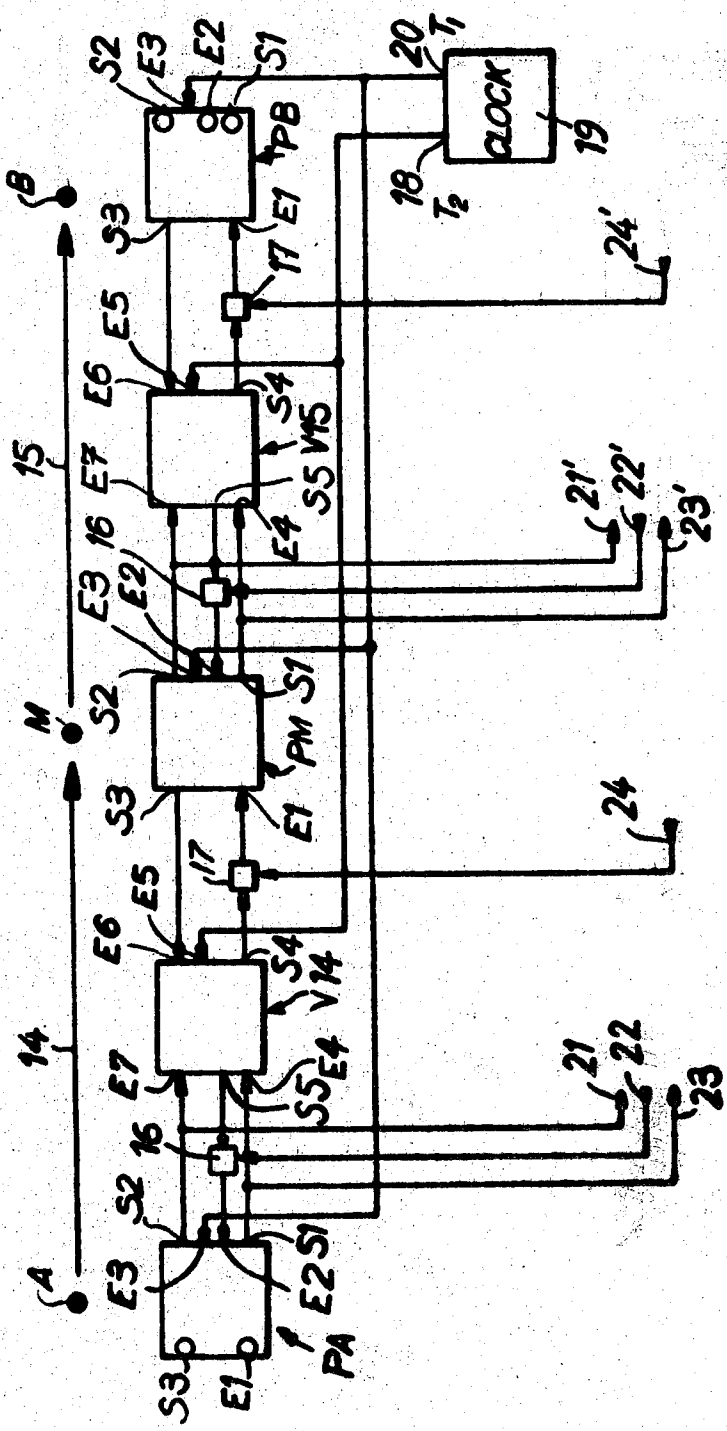

B
M
A
15
14
S2
E3
E2
S1
PB
E1
S3
17
E5
E6
S4
V15
E7
S5
E4
16
PM
V14
PA
20
T_1
CLOCK
19
18
T_2
24'
21'
22'
23'
24
21
22
23

Fig. 2

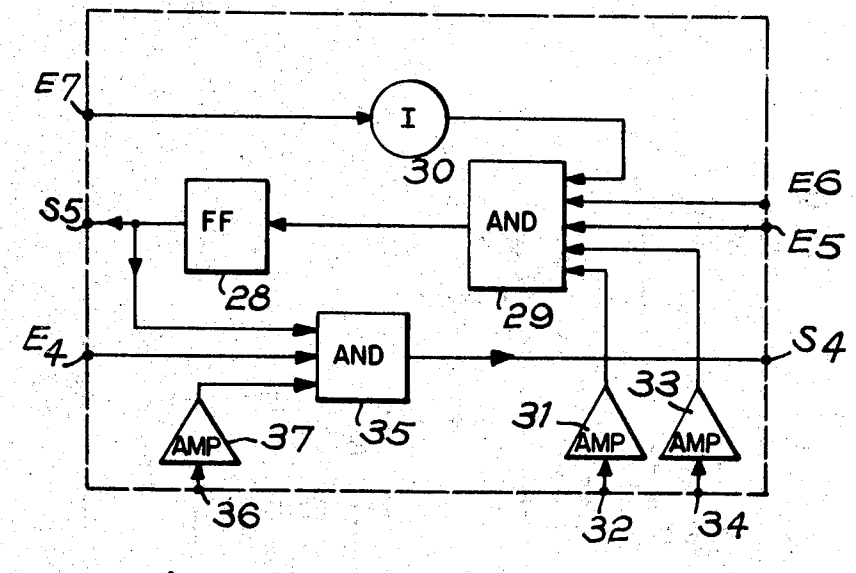

E7
I
30
E6
S5
FF
28
AND
29
E5
E4
AND
35
S4
33
31
AMP
37
AMP
AMP
36
32
34

Fig. 4

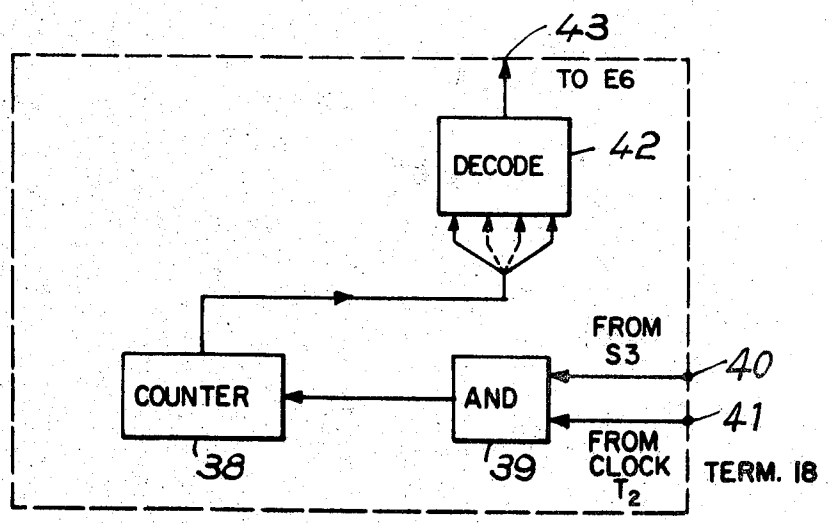

43
TO E6
DECODE
42
FROM
S3
40
COUNTER
AND
41
38
39
FROM
CLOCK
T_2
TERM. 18

Fig. 5

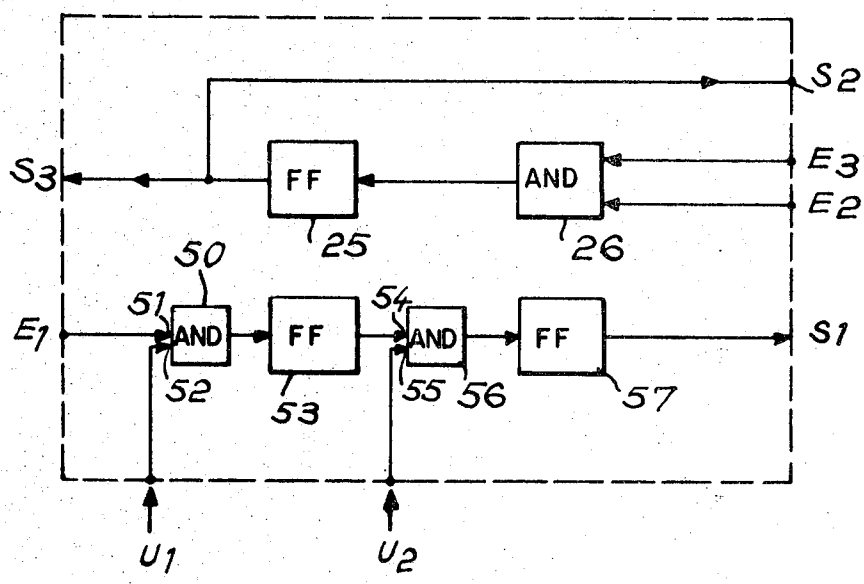

S2
S3
FF
AND
E3
E2
25
26
50
51
E1
AND
FF
54
AND
FF
S1
52
53
55
56
57
U1
U2

Fig. 6

METHOD AND SYSTEM FOR FINDING OR PLOTTING AN OPTIMUM PATH

The present invention relates to apparatus to solve the problem of determining the optimum path between states of a certain system. This system is entirely defined by a predetermined number of variables (which may include time). For each state of the system, each of the variables takes a predetermined value and the state is defined by all said values. Each of these possible states can be represented in a geometrical space having the same number of dimensions as the system includes variables. A state is then defined by a point in this space.

The geometrical space in question is instrumented by devising an analogue network. The points of the space will be represented by the nodes of the network, and the connections between these points will be represented by connecting links forming the mesh of the network; in the described embodiment of the network is electrical.

More precisely, two subsets are defined in a set of points, one of which constitutes a first family of points, known as departure points, and the other a second family of points, known as arrival points. As each of the points of the first family can be connected to each of the points of the second family by a large number of paths, it is a specific object of the invention to determine the optimum path coupling a departure to a point of arrival.

For certain applications, the family of departure points as well as that of the arrival points can be reduced to one point only.

For other applications, a departure point may also function as an arrival point.

The problem as set out above is very general. By way of particular examples, it may relate to urban traffic, the solution of problems of distribution of products or services, or the calculations of the shortest routes in transoceanic flights.

SUBJECT MATTER OF THE INVENTION

An interconnected mesh network is provided whose nodes correspond to points, all representative of states of a system with a plurality of variables in a geometrical space having the same number of dimensions as the system comprises variables, and whose mesh lines with different weightings, correspond to all the conceivable elementary passages between the different nodes. According to the invention, a group of nodes representing a first family of points, and another group of nodes representing a second family of points, known as arrival points are selected and their addresses stored; during a first stage, emitted simultaneously from all the arrival nodes selected initially, signals progress along the lines of the interconnecting mesh, leaving nodes and progressing towards the intermediate nodes which thus in turn become selected. The selection of a node has the effect that during this stage the reception of other signals at the selected node is inhibited. Additionally, the step-by-step progression of the signals from the selected nodes is enabled and further, a connection through the interconnecting line over which the selection of the node occurred, is established. From intermediate nodes thus selected new signals are emitted as above, and so on. The interconnection line to the departure node over which one of these signals first reaches the departure node, is determined and the progression of the signals is then stopped. In a second stage, a connection is established from this departure node over the path thus determined, terminating at the arrival node from which the signal originated.

The invention also consists in a system for carrying out this method.

The essential characteristics of the method and of the system of the invention will clearly appear from the following description, referring to the accompanying drawings in which:

FIG. 1 represents a network developed in a two-dimensional space and representative of a particular problem to be solved,

FIG. 2 schematically shows an embodiment of the circuits enabling the nodes and the connecting links of the network of FIG. 1,

FIG. 3 represents an embodiment of a "nodal element" corresponding to a node of the network,

FIG. 4 represents an embodiment of a cone connecting link termed a "loop element,"

FIG. 5 represents an embodiment of an element for weighting the connection links of the network, and

FIG. 6 represents a modification of the circuit displaying the optimum path of the system according to the invention.

Referring now to the drawings, FIG. 1 shows a network in a two-dimensional space.

In this network, the nodes N1 to N10 represent different states considered in a given problem, whilst the interconnecting lines, also called loops 1 to 13 constitute paths permitting passage of signals from one node to another node, or progressible change of state in the problem.

The connection lines are oriented and thus reproduce the sense of the connections between the various states in the problem in question. In FIG. 1, all the loops are in one direction; however, they could also be in two directions by arranging two lines in parallel oriented in opposite direction.

For purposes of initial explanation, let N1 be the departure node and N2 the arrival node.

At the side of each reference for the loops, a weighting applied to each of the loops has been indicated in parentheses. Thus it is that the connection 1 is not weighted and consequently has weighting ratio of 1. On the other hand, the connection 4 has a weighting ratio of 2, corresponding to two progression times of the step-by-step progression over line 4 between N4 and N5, whilst the loop 9 has a weighting ratio of 3 corresponding to three progression times of the step-by-step progression over line 9 between N7 and N8.

FIG. 2 shows, in enlarged scale and greater detail, a departure node A, an arrival node B and an intermediate node M. The two elementary paths permitting passage from the node A to node B are shown by the loops 14 and 15.

The nodes A, B and M are represented respectively by "nodal elements" PA, PB and PM which are identical, whilst the loops 14 and 15 are shown respectively by "loop elements" V14 and V15 are also identical.

Each "nodal element" comprises three outputs S1, S2 and S3 and three inputs E1, E2 and E3. Each connection line ("loop element") comprises two outputs S4 and S5 connected respectively to the input E1 of the "nodal element" end of the connection through an OR gate 17 and to the input E2 of the "nodal element" forming the origin for the signals in the line through an OR gate 16. Four additional inputs E4, E5, E6 and E7 are provided.

The inputs E4 and E7 are respectively connected to the outputs S1 and S2 of the sending (origin of signals) "nodal element." The inputs E3 and E5 are respectively connected to the outputs 20 and 18 of a clock 19. Input E6 is connected to the output S3 of the receiving nodal element.

In the case where any one of the nodes A, B and M are, additionally, connected to other connection lines (e.g. node N3, FIG. 1), the "loop elements" corresponding to these additional connections are connected in a manner identical to the connection of "loop element" V15 to the "nodal element" PM. Thus, the supplementary terminals 21, 22 and 23 will be connected respectively to the input E7, to the output S5 and to the input E4 of each of the additional "loop elements" forming part of another connection link, or loop from the same original "nodal element"; in FIG. 2, nodal element PA. Lines 21', 22', 23' may form an additional connection to nodal point PM.

Similarly, in the case where the nodes A, B and M are ends of other lines (e.g. node N5, FIG. 1), the lines 24, 24' to the gates 17 may form a second input connected to the output S4 of each of the additional connecting "loop elements" relatively to the same end "nodal element."

FIG. 3 shows the circuit of a "nodal element." This nodal element is composed of a bistable memory **25** whose output is connected to S3 and whose input is connected to an AND gate **26** comprising two inputs located at E2 and at E3 and a noninverting amplifier **27** whose input is located at E1 and its output at S1. In addition, the output of the memory **25** includes a shunt located at S2.

FIG. 4 shows the circuit of a connection link, or "loop element." This "loop element" comprises a bistable memory **28** whose output is located at S5 and whose input is connected to an AND gate **29** with five inputs, two of which are located at E5 and E6; an inverting amplifier **30** whose input is located at E7 and whose output is connected to one of the inputs of the AND gate **29**; a noninverting amplifier **31** whose input **32** is connected, if desired, to a weighting element and whose output is connected to one of the inputs of the AND gate **29**; a second noninverting amplifier **33** whose input is located at **34** and whose output is connected to one of the inputs of the AND gate **29**; and an AND gate **35** whose output is located at S4 and whose three inputs are connected, one to the output of the bistable memory **28**, the other to the input E4 and the third to a supplementary input terminal **36** through a noninverting amplifier **37**.

FIG. 5 shows the circuit of a weighting element intended to weight a connecting link, or "loop element." This weighting element essentially comprises a binary counter **38** whose input is connected to an AND gate **39** whose two inputs, located at **40** and **41**, can be connected on the one hand to the output S3 of the "nodal element" end of the "loop element" to be weighted and on the other hand to the terminal **18** of the clock **19**, whilst the output of the binary counter **38** is connected to the *n* inputs of a decoding or coincidence gate **42** preset for a predetermined number of counts, depending on the weighting factor, whose output **43** can be connected to the input **32** of the "loop element" to be weighted.

The operation of the above described system is as follows:

Let us firstly consider the circuit represented in FIG. **2** by the "nodal elements" PA, PB and PM and the "loop elements" V14 and V15.

The path to be recognized is that permitting the passage from the node A, termed the departure (or origin) node, to the node B, termed the receiving or arrival node. It passes through the intermediate or connecting node M.

A node becomes the departure node A when a peripheral device (not shown) applies a continuous "send" or "departure" activation or addressing signal to the input terminal E1 of a "nodal element"; in FIG. **2**, nodal element PA. A node becomes an arrival node B, when a a peripheral device (not shown) applies an appropriate continuous "arrival" activation signal to the input terminal E2 of a "nodal element"; in FIG. **2**, nodal element PB.

During the whole time of operation, the clock **19** alternately and continuously supplies two signals T1 and T2. Signal T1 is applied to the output **20** and T2 to the output **18**.

The initial state of the memory **25** (FIG. **3**) of the nodal elements is such that an inhibiting signal appears on the outputs S2 and S3 of these nodal elements before these memories are triggered (so that bistable memory **25** will change state). The initial state of the memory **28** of the "loop elements" (FIG. **4**) is such that an inhibiting signal appears on the output S5 of these "loop elements" before these memories are triggered to change state.

During the operation, the "nodal element" PB recognizes the appearance of the first signal T1 from clock **19**, on line **20**, connected to terminal E3 (FIG. **3**). AND gate **26** (FIG. **3**) is now activated (T1 on E3, and E2 by the "arrival" activation signal from the peripheral device). This "nodal element" is the only one in the mesh network which has its memory triggered, since the inputs E2 of the other nodal elements do not receive an activating signal.

At the moment, the memory **25** of the "nodal element" PB triggers, the output S3 of this element activates one of the inputs of the AND gate **29** of the "loop element" V15, through the input E6 (FIG. **4**).

Upon the following signal T2, in the absence of inhibition applied to the AND gate **29** through the lack of input **34**, the AND gate **29** has all its inputs active.

It has been assumed in this example that the "loop elements" do not comprise weighting elements and that consequently no inhibition is applied through the input **32** to the AND gate **29**. AND gate **29** also has an active input at E7 since the "nodal element" PM, the origin of the "loop element" V15 does not yet store any signal. Memory **25** of element PM has not yet been triggered, and the output S2 of this "nodal element" delivers an inhibit signal which, inverted by the inverter **30** of the "loop element" V15, permits activation of AND gate **29**.

The first clock signal T2 (subsequent to clock T1) thus causes storage of a condition in the "loop element" V15. Additionally, change of state of element **28** activates one of the inputs of the AND gate **35** and also, by means of the output S5 over OR gate **16**, input E2 of the AND gate **26** of the "nodal element" PM.

The second signal T1 completes the activation of AND gate **26** of the "nodal element" PM; this "nodal element" is for its turn memorized (that is, stores a condition) and activates, upon change of state of its element **25**, through its output S3, the input E6 of the AND gate **29** of the "loop element" V14.

The series of operations for passing from the node M to node A is repeated in the same manner as during the passage from node B to node M. Thus it is that the next (second) signal T2 will activate the "loop element" V14; the third T1 signal finally activates one of the inputs of its gate **35** and, through its output S5 and the input E2 of the "nodal element" PA one of the inputs of the gate **26** of this element.

At the moment when the memory **28** of a "loop element" connected to the "departure" node B has been triggered, the "send" or "departure" activation signal has been applied to the input E1 of the "nodal element" PA by the peripheral device, as referred to above.

This signal is present at the output S1 of the "nodal element" PA and activates input E4 of the AND gate **35** of the "loop element" V14. Gate **35** is entirely activated if no nonvalidating signal (which is normally the case) is applied through the input **36** and memory **28** has triggered. The use of signals to terminals **36**, **32** and **34** will be described below. The "send" signal passes through the AND gate **35**, is present at the output S4 of the "loop element" V14, passes through OR gate **17**, terminals E1, amplifier **27** and terminal S1 of "nodal element" PM, passes through the "loop element" V15 and the "nodal element" PB in order to appear at the output S1 thereof.

The setup of a continuous circuit path running from A to B is thus effected by guiding the starting send signal through the outputs S1 of the "nodal elements" PA, PM and PB, and the outputs S4 of the "loop elements" V14 and V15.

The device to be described plots in a single operation, for the purpose of exploration, the desired passage between the point of departure and point of arrival. For certain uses it may be useful or necessary that this passage appears step-by-step either at a given rhythm, or in reply to successive orders sent to said device.

This modification is obtained by replacing the amplifier **27** in the "nodal element" (FIG. **3**) by a "master-slave" circuit, or by a circuit as shown in FIG. **6**. Instead of amplifier **27**, a first logic AND gate **50** having two inputs **51** and **52** controls a first bistable circuit **53**; the output of this first bistable circuit **53** feeds an input **54** of a second AND gate **56**. The output of AND gate **56** is connected to a second bistable circuit **57** whose output constitutes the output S_1 of the "nodal element."

The operation of this circuit is such that the signal intended to mark the different stages of the path can progress only from one "nodal element" to the following "nodal element" during a cycle of signals U_1 connected to input **52** of AND gate **50** and U_2 connected to input **55** of AND gate **56**, which are exclusive of one another and which control the propagation of a signal in this circuit.

When it is a question of circuits known as "master-slave," the cycle of signals if formed by the succession of the two voltage levels which can be applied to the corresponding input of these well known circuits. When it is a question of the present circuit with double bistable circuits, the progression of the display signal is obtained by applying a first signal U1 to the input 52 of the first AND gate 50, this causing the input signal present on the input E1 of the "nodal element" to progress and to be memorized in the bistable circuit 53. This signal cannot go any further if, the second signal U2 is absent. When it is desired to cause the signal to progress, the first signal U1 is terminated and the second signal U2 is applied to the input 55 of the AND gate 56. The other input 54 of this gate being activated by the triggered bistable circuit 53, bistable circuit 57 triggers in turn. Thus, the signal appears at the outputs S1 of the "nodal element" and after having cleared a "loop element," appears at the input E1 of the following "nodal element." There it is stopped by the AND gate 50 of this "nodal element," which is not activated in the absence of a signal U1. The progression of the display signal will thus be effected at the rhythm of the signals U1, U2. The setup of the path is backwards, but the signal which must pass through the path leaves from the point of origin to the end point so that the path is defined in correct order. One of the bistable circuits of each "nodal element" can be used for making the path. According to whether the bistable circuits will be returned to zero, or if they remain triggered, the path can be indicated step-by-step or any previous steps may be indicated. If with an arrangement of FIG. 6, it is desired to have the path established in a single step, it is only necessary to apply the signals U1 and U2 simultaneously. This is not possible with the "master-slave" circuit.

Reference will now again be made to FIG. 1. Let N1 be the departure node, and the node N6 the arrival node. The problem to be solved is the determination of the shortest path between nodes N1 and N6. Contrary to the arrangement in the preceding example, the "loop elements" here are weighted, according to a ratio indicated in parentheses, as follows:

It has been seen in the preceding example that the storing of a path, which may be termed memorization of a "loop element" is effected by a signal T2, that is by an activating signal delivered to the output 18 of the clock 19 when the "nodal element" end of the "loop element" in question has been activated. In order to weight a "loop element," it will thus be sufficient to control the memorization of this element, no longer at the first signal delivered to the output 18 of the clock 19 and according to the memorization of the "nodal element" end of said "loop element," but at the second, the third, or the *n*th clock output at 18, according to the weighting ratio.

To this end, the binary counter 38 (FIG. 5) of a weighting element associated with the "loop element" to be weighted, counts, by means of the terminal 41 connected to the output 18 of the clock 19, the number of signals emitted on the output 18 of the clock 19. As long as the desired number of these signals is not reached, the weighting element maintains through its output 43, connected to the input 32 of the "loop element," an inhibiting signal on the AND gate 29.

When the number of the signals emitted by the output 18 of the clock 19, corresponding to the weighting of the "loop element" in question, diminished by one, is reached, the weighting element lifts this inhibition and the "loop element" can be memorized at the following signal if no other inhibition appears before this instant.

In FIG. 1, the loops whose weighting ratio is 1 correspond to "loop elements" comprising no weighting elements, whilst the loops 4 and 9 correspond to "loop elements" comprising weighting elements with 1 and 2 steps respectively.

Upon addressing nodes H1 and N6, that is, after the departure nodes N1 and arrival nodes N6 have been activated, the first of the signals T1 delivered by the output 20 of the clock 19 sets, or activates the arrival node N6. Then, the first of the signals T2 delivered by the output 18 of the clock 19 and following the above defined signals T1 memorizes the link 5 alone since the link 10 is weighted 2.

At the second signal T1 the node N5 is memorized. At the second signal T2 it is only the link 10 which is memorized and links 4 and 8 will have their counters 35 stepped one unit. Then at a third signal T1, the node N8 is memorized and at a third signal T2, the link 13 is memorized as well as link 4, while link 8 will have its counter 38 stepped by 2; and so on according to the rhythm of the signals T1 and T2.

At the fifth signal T1, the node N3 is memorized, and the memorization of the link 8 is inhibited.

Link 8, highly weighted represents, for joining the nodes N3 and N5, a longer passage than the passage constituted by the links 3 and 4; thus, link 8 will not be activated.

At the fifth T2 signal, the link 2 is memorized as well as link 9.

At the sixth signal T1, the nodes N2 and N7 are memorized, this preventing the memorization of the link 6 and 7 issuing from the node N7 and at a sixth signal T2, the loops 1 and 12 are memorized.

Finally, at the seventh signal T1, the nodes N1 and N9 are memorized.

At this moment, the departure node N1 being reached, the signals T1 and T2 are blocked and a signal is sent to the input E1 of the departure "nodal element" and will instantaneously pass through the noninverting amplifiers 27 of the "nodal elements" constituting the nodes N1, N2, N3, N4, N5 and N6 and the AND gates 35 of the loop elements constituting the links 1,2,3,4 and 5. This signal will permit the display of the itinerary constituted by the links 1 to 5 and shown in thick lines in FIG. 1 and it only, since, as the links 6,7,8 and 11 are not memorized, the AND gates 35 associated with the "loop elements" representing the links 6,7,8 and 11 are inhibited.

In this same figure, the loops 9 and 10 on the one hand and 12. 13 and 10 on the other hand have been shown by thick lines. These links constitute two itineraries which do not reach the node N1 for the following reasons: the itinerary of the links 9 and 10 does not reach the node N1 due to the orientation of the link 6 whose memorization is prohibited by reason of the memorization of the original node N7, whilst the path over links 12, 13 and 10 does not reach the node N1 due to the fact that the link 1 is memorized before the link 11 and that consequently the itineary of the links 11, 12, 13 and 10 is longer than the itinerary of the links 1 to 5.

Thus, only the shortest path permitting the passage from the node N1 to the node N6 will be followed and may be displayed.

In certain cases there may exist between two nodes two lengths presenting the same number of steps (one step corresponding to the emission of a signal T2) and that this number of steps is minimum. These two paths can either be between departure nodes and arrival nodes, or between intermediate nodes.

In such a case, the device displays the two equal lengths, or the double portion of the length. However, it is possible to eliminate, if necessary, one of the two lengths by giving preference to the other.

To this end, in these two lengths, the two "loop elements" issuing from the same "nodal element" and constituting the branching in question are considered and preference is given to one of the two "loop elements" by connecting the output S5 (FIG. 4) of the preferred "loop elements" to the input 36 of the nonpreferred "loop element" so that its AND gate 35 is inhibited.

Moreover, one may at any moment temporarily or continuously eliminate certain links from the network by applying an inhibiting signal to the input 34 of the "loop elements" in question.

Moreover, as indicated above, two nodes can be connected together by two links oriented in opposite direction possibly with two different weightings.

The weighting of the links can also be modified by controlling the weighting elements.

The system not only enables problems of single point connections to be solved, but also general problems to be solved

including a first family of points, known as the departure family, and a second family of points known as the arrival family, whatever may be the number of points of these families. It is possible to select from a plurality of departure nodes and a single arrival node, the particular departure node which can connect with the arrival node with the minimum number of steps, and to indicate the appropriate itinerary or itineraries.

Conversely, the system, assuming a single departure node and a plurality of arrival nodes, permits those arrival nodes to be found which can be reached with the minimum number of steps and the appropriate itinerary or itineraries to be indicated.

Finally, assuming a plurality of departures nodes and a plurality of arrival nodes, the system enables solving of the problem "of the affinity of one assembly for another assembly" by plotting the "departure node and arrival node" pairs separated by the minimum of steps and by indicating the appropriate itinerary or itineraries. In this case, as in the two preceding cases, it is understood that the family of points in question can be reduced to one, so that the case then becomes analogous to that of the example described above in connection with FIG. 1.

Such a system can be used in various fields of application, for example that of regulating urban traffic.

In this case, the problem is to guide the drivers on the road in a major center towards their destinations starting from traffic centers. This guiding is effected according to the variable itineraries, determined periodically and taking into account at each instant, the state of congestion at the different arterial highways, the regulations in force and unforeseeable elements such as accidents, roadworks etc. For each of these operations, a group of itineraries can be established between the traffic centers in question. At the end of the signal cycle, the optimized assembly of the guiding itineraries has been defined.

Each central traffic point or intersection of the network of streets is represented by a "nodal element." Streets or parts of the streets joining two adjacent intersections are represented by two parallel "loop elements" of opposite direction in order possibly to represent the two possible directions of traffic.

Weighting elements can be associated with each "loop element" in order to confer thereto a weighting ratio dependent upon the criteria adopted (kind of street possible obstacles, traffic lights, limited speed, possible congestion, etc.).

A cyclic device successively sets up each central point as an arrival point, all the other central points then being set up as departure points. All that remains is to inform the drivers of the optimized itineraries by means of luminous or electromechanical signals placed before each crossroads and controlled from the terminal S4 of the "loop elements."

The system according to the invention may also be used for the purpose of increasing the speeds of certain public services, such as that of fire engines for example, and also to optimize the problem of evacuations in the case of emergency.

From among other possible applications, the calculation of the minimum path itineraries in transoceanic flights, and the problem of dynamic programmation and the plotting of the critical paths are referred to.

Finally, such a system can constitute a subassembly "Center of Inscription" (of which it only presents a simplified embodiment) of a complex polyvalent memory as described in French Pat. No. 1,381,212 of the 30th Sept. 1961, filed in the name of one of the inventors of the present application, and one of the functions of which is the plotting of the shortest sequence of intermediate actions between two situations.

The present invention is not limited to the described and shown embodiment but covers all relevant modifications thereto; the system may be instrumented according to various technologies which could utilize, for example electronic, electromechanical, mechanical, hydraulic or pneumatic circuits, with elements having the same logic functions.

We claim:

1. Method of determining the shortest interconnection between a first point, or set of points, to a second point, or set of points, said points being located in a mesh network having interconnecting links, connecting said points together, comprising:

applying addressing signals to first and second points to identify and select said first and second points within the points of the mesh network;

applying tracing signals emanating from said second addressed point to all interconnecting links connected thereto;

conducting said tracing signals from said links to all points connected to said links, other than said second point, and, during said conducting step;

timing the progression of said tracing signals through all said links in accordance with predetermined characteristics of said links;

passing said tracing signals through said points connected to said links and inhibiting said points, having said tracing signals passed therethrough, from accepting tracing signals from other links connected to respective points, at subsequent periods of time;

repetitively applying said tracing signals from said points to subsequent links connected thereto;

inhibiting the first addressed point, first reached by a tracing signal from a connecting link, from accepting subsequent tracing signals from other links connected thereto;

establishing through those points and links, through which a tracing signal passed, a continuous closed connection, to establish a continuous circuit between said first and second points; and

identifying those points and interconnecting links through which the tracing signal has passed and which are a part of said continuous, closed connection between said first and second points.

2. Method according to claim 1 wherein the step of timing the progression of the tracing signal comprises the step of controlling the timing of progression of said tracing signals in discrete timed steps, and controlling the number of steps required for passing of a signal through a link.

3. Method according to claim 1 further comprising the steps of:

generating control signals in those interconnecting links which are part of said continuous closed connection between said first and second points; and

controlling the continuity of a second circuit path through those points and those interconnecting links, by said control signals.

4. System to trace the shortest path from a first point, or set of points to a second point, or set of points, said points being located within a network of points, said network having interconnecting links emanating from said points and interconnecting said points in a predetermined pattern, comprising:

a source of clock pulses (19);

a plurality of similar nodal circuit elements (FIG. 3) forming nodal points in the system, said nodal circuit elements having input and output terminals and means (26), controlled by said clock pulses and by signals applied to at least one of said terminals, to establish a circuit path between said input and output terminals;

a plurality of similar link circuit elements (FIG. 4) forming interconnecting links in the system, said link circuit elements being connected to said nodal circuit elements in accordance with the pattern of the network, said link elements having input and output terminals and means, controlled by said clock pulses and by signals applied to at least one of said terminals, establishing a circuit path between said input and output terminals;

at least one time delay element (FIG. 5) selectively associated with, and connected to a link circuit element, said time delay element being connected to, and controlled by said source of clock pulses and having means delaying signals passing through the circuit path of said

link element by a preselected number of clock pulses, the number of pulses of delay being determined by a characteristic of said delay element, whereby the output signals from the link elements having said time delay element associated therewith will appear at a time delayed with respect to the clock pulses controlling said circuit path;

said circuit elements additionally comprising means (FIG. 3: 25–S2; FIG. 4: E7–30–29) inhibiting establishment of a circuit path through a preceding link element connected to a nodal element when a circuit path has already been established from another link element to said nodal element;

means applying an addressing signal to one of said nodal circuit elements at a location in said network of points corresponding to said second point, said addressing signal controlling said nodal circuit element to enable application of said clock pulses to an output terminal, and hence to any link circuit element connected thereto;

means applying an addressing signal to another one of said nodal circuit elements elements at another location in said network of points, corresponding to said first point, said second addressing signal inhibiting progression of a clock pulse applied to said second nodal element from any link circuit element to a further connected link circuit element; and

whereby the circuit path requiring the least number of clock pulses between said one nodal circuit element, and said other nodal circuit element, over said link circuits, will be established between said one and said other nodal circuit elements.

5. System according to claim **4** wherein said time delay (FIG. **5**) element includes a pulse counter (**38**) connected to have said clock pulses applied thereto, the delay time being a whole number of clock pulses.

6. System according to claim **4** wherein said circuit elements have a pair of parallel circuit paths, each path passing signals in opposite direction.

7. System according to claim **4** wherein said nodal circuit elements comprise a bistable memory (**25**) and an AND gate (**26**), said AND gate (**26**) being controlled by a conjunction of timing signals from said clock pulse source (**16**) and said addressing signal, or by an output from a link circuit element being connected to said nodal circuit element; and interconnecting means controlling change of state of said memory (**25**) upon appearance of an output from said AND gate.

8. System according to claim **7**, including a second circuit in parallel with said bistable memory (**25**) and said AND gate (**26**), said second circuit passing signals in a direction opposite to the signal paths through said bistable memory.

9. System according to claim **7**, wherein said link elements are oriented, each including a circuit comprising: a bistable memory (**28**), and an AND gate (**29**) having an output connected to control said bistable memory;

an OR gate (**16**);

the output (**S5**) of said memory (**28**) and a first input (**E6**) of said AND gate being respectively connected, through said OR gate (**16**) to an input (**E2**) of the AND gate (**26**) of the nodal element forming a connection to the link element; and

said link element further including an inverter (**30**) connected to the output (**S2**) of the bistable memory (**26**) of the next nodal element, said inverter having a further output connected to the AND gate (**29**) of the link element.

10. System according to claim **9**, wherein said time delay element comprises: a binary counter (**38**); and an AND gate (**39**) controlling said counter, one of the inputs (**40**) of said AND gate (**39**) is connected to the output (**S3**) of the bistable memory (**25**) of the nodal element in advance of the link element with which the time delay element is associated;

a decoding circuit (**42**);

the output of the counter (**38**) being applied to said decoding circuit, said decoding circuit being preset to provide an output pulse only after a predetermined number of input pulses from said counter have been counted to define said characteristic of the delay element; and

the output, after decoding, being applied to an additional input (**31**, **32**) to the AND gate **29** of the link element to which the delay element is connected.

11. System according to claim **9**, wherein said link element is oriented and comprises an inhibiting circuit (**34**) including an amplifier (**33**), the output of said amplifier being connected to an additional input of the AND gate (**29**) of the link element.

12. System according to claim **4**, wherein said source of clock pulses supplied a pair of pulse output signals (**T1**, **T2**), one of which (**T7**) is connected (**20–E3**) to control the nodal elements (FIG. **3**) and the other (**T2**) is connected (**18–E5**) to control the link elements (FIG. **4**).

13. System according to claim **9**, wherein: said circuit path establishing a selected itinerary between departure and arrival nodes includes an amplifier (**27**) associated with each of the nodal elements;

an OR gate (**17**);

an AND gate (**35**) associated with each of said link elements, the output of said AND gate (**35**) being connected (**S4**) through said OR gate (**17**) to the input of the amplifier (**27**) associated with the nodal element next connected to the link element;

said AND gate (**35**) having additional inputs connected to the output of the bistable memory (**28**) of the link element.

14. System according to claim **12**, including: an additional AND gate (**35**) included in said circuit path; an inhibiting amplifier (**37**);

said additional AND gate (**35**) being controlled by said inhibiting amplifier (**37**); and

means (**36**) controlling the operation of said inhibiting amplifier to inhibit progression of signals in said path.

15. System according to claim **4**, wherein: the circuit path establishing the selected itinerary, or itineraries, between departure and arrival nodes includes a circuit (FIG. **6**) associated with each of said nodal elements and successively comprising a first AND gate (**50**) with two inputs;

a first bistable trigger circuit (**53**);

a second AND gate (**56**) with two inputs;

a second bistable trigger circuit (**57**); and

one of the inputs of said first and the second AND gates being connected to receive, at one of the their inputs (**52**, **55**), each successively or simultaneously, an activation signal (U_1, U_2) respectively and an other input of said first and second AND gates being connected in said circuit path to control propagation of a signal along said path.

16. System according to claim **4** wherein said nodal circuit elements (FIG. **3**) and said link circuit elements (FIG. **4**) each includes a controllable bistable circuit (**25**, **28**) and a conjunctive logic circuit (**26**, **29**) controlling the state of said bistable circuit in the respective circuit element, one of the inputs of the conjunctive logic circuit being connected to said clock pulse source and the other input being connected to the output from a connected circuit element and to said means applying an addressing signal.

17. System according to claim **16** wherein each said link elements has a time delay element (FIG. **5**) associated therewith, said time delay element including a settable pulse counter (**38–43**) connected to said clock pulse source (**19**) and delaying transmission of pulses by said link elements under control of the count setting of the pulse counter.

18. System according to claim **16** wherein each said circuit element has a pair of independent, parallel circuit paths, passing signals in opposite direction; and one of said independent circuit paths in the link circuit (FIG. **4**) includes a control element (**35**) closing said independent circuit path under control of the state of said bistable circuit (**28**).