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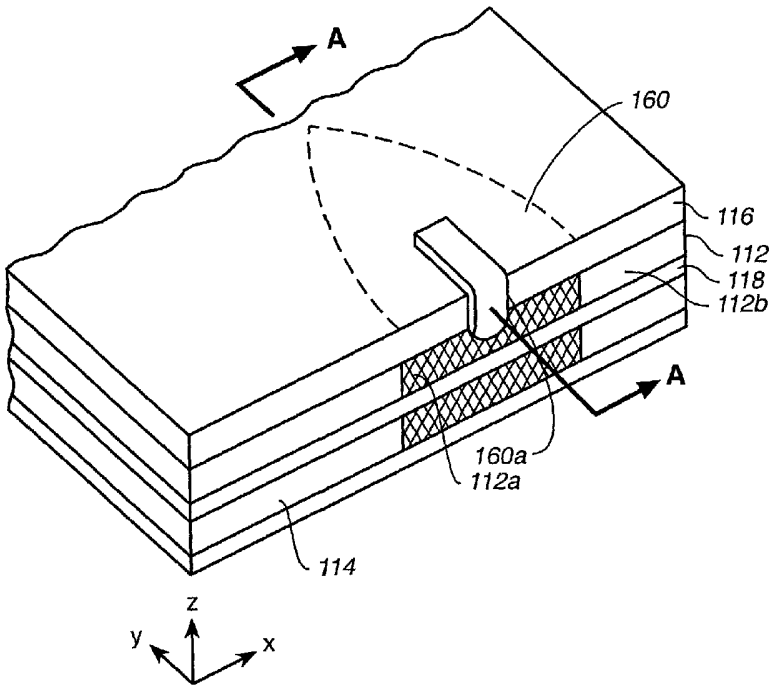
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(54) Title: CARD MANUFACTURING TECHNIQUE AND RESULTING CARD




(57) Abstract: A card manufacturing technique and the resulting card are provided. The card has a ground and/or power layer (112) extending to the edges of a circuit board for electrostatic discharge protection but also has gaps (112a) at the edge of the ground and/or power layer (112) to avoid short circuiting with conductive segments (160) of another layer deformed when the card is trimmed during manufacture.

WO 03/015484 A1

# CARD MANUFACTURING TECHNIQUE AND RESULTING CARD

## FIELD OF THE INVENTION

The invention relates generally to circuit boards, a method of making a memory card integrating a circuit board, and the resulting memory card.

## BACKGROUND OF THE INVENTION

This invention relates generally to circuit boards, and more specifically to circuit boards of memory cards utilized in portable devices to store data. Although the invention has application to a wide variety of circuit boards, it is described herein to be implemented in a memory card, specifically a portable memory card having flash electrically-erasable and programmable read-only memory (flash EEPROM).

In recent years, devices such as digital cameras, digital audio players, and personal digital assistants have become popular. These devices require a large amount of storage capacity in a small and rugged package. Memory cards utilizing high density non-volatile memory are frequently inserted and removed from these devices and printers or external readers attached to personal computers. The frequent handling of these cards results in a high risk of electrostatic discharge.

Thus, it is desired to have a small thin memory card that is immune from electrostatic discharge yet simple to manufacture and assemble.

## SUMMARY OF THE INVENTION

Memory cards are getting smaller and thinner, yet the capacity is increasing and they are also becoming more densely packaged. Frequent handling of these cards results in a high risk of electrostatic discharge (ESD).

A memory card and a method of making a memory card resistant to damage from electrostatic discharge and less prone to short circuiting of the multiple conductive layers of the card is described. The memory card is formed by encapsulating or placing a circuit board into a plastic cover. At a junction between the plastic cover and an edge of the circuit board there is a gap where an electrostatic discharge is prone to enter and damage the circuit components of the memory card. The ground and power layer extend to the edge of the circuit board and along the junction between the circuit board and the memory card. Thus any electrostatic discharge is absorbed by either of these layers and damage to the other circuit components from the high voltage discharge is avoided. A prior method of avoiding short circuits due to the trimming process involved pulling back the entire edge of the conductive layer away from the edge of the circuit board, however this method affords little if any ESD protection to the susceptible components of the memory card.

During the manufacturing of the memory card, the circuit board is trimmed to its final dimensions. Conductive segments of a metallic layer that are located at the edge of the circuit board are deformed during the trimming process and can extend over an insulating layer and contact a second metallic layer, in this case either the ground or power layer, thus resulting a short circuit. As previously mentioned, it is desirous to extend the ground and/or power layer to the junction of the card for electrostatic discharge purposes. Therefore, in order to avoid short circuiting yet

preserve maximum ESD protection, small gaps are formed at the edge of the second conductive layer that are vertically aligned with the conductive segments such that any deformation that may occur during the trimming process will not result in a short circuit. The deformation of the conductive segments will fall into the gap at the edge of the second conductive layer rather than making contact with the layer. The size of the gaps is small in relation to the remaining edge of the ground and/or power layer at the junction of the circuit board and the cover, thus ensuring a high level of ESD protection while avoiding short circuits from the trimming of the board.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a top view of the memory card exemplifying the present invention.

FIG. 2 is a cross-sectional view of the memory card exemplifying the present invention.

FIG. 3 is a perspective exploded view showing the conductive layers of the card.

FIG.4 is a perspective exploded view showing the conductive layers of the card during manufacturing.

FIG. 5a is an enlarged perspective view of an edge of the memory card.

FIG. 5b is an enlarged perspective view of another example of an edge of the memory card.

FIG. 5c is an enlarged perspective view of another example of an edge of the memory card.

FIG. 6a is a cross-sectional view along section A-A of the card shown in FIGS. 4 and 5a.

FIG. 6c is a cross-sectional view along section A-A of the card shown in FIGS. 4 and 5c.

FIG 7 is a top view of a gap of FIGS. 3-5.

FIG. 8 is a top view of examples of gaps in the conductive layer of the card.

## DESCRIPTION OF EXEMPLARY EMBODIMENTS

Figure 1 shows the rear side of a memory card exemplifying the present invention. The memory card 100 comprises a circuit board 110 having an exposed rear side with terminals 140 and a covered front side (not shown). The covered side comprises at least one integrated circuit including flash memory, circuit traces, and passive components, which are not shown. Cover 120 covers over the front side and edges of the circuit board, such that the rear side of the circuit board is exposed to form substantially all of the rear side of the memory card. A narrow gap 130 at the junction between the edges of circuit board 110 and cover 120 exists. An electrostatic discharge 150 is shown entering the narrow gap 130 at the junction between the edges of circuit board 110 and cover 120. U.S. Patent No. 6,040,622 to Wallace, entitled "Semiconductor Package Using Terminals Formed on a Conductive Layer of a Circuit Board" describes in detail the construction of a memory package in detail and is hereby incorporated by reference in its entirety.

Figure 2 shows the gap 130 between circuit board 110 and cover 120 highly exaggerated for illustrative purposes. Conductive layers 112 and 114 extend to the edge of circuit board 110. The gap is quite small, but large enough that an electrostatic discharge (ESD) 150 can reach conductive layer 112 or 114. The conductive layers can be either the ground layer or power layer. In the case of an ESD, the ESD will be absorbed by the conductive layers 112 and 114, rather than by any of the circuit components on the front side 180 of circuit board 110. The front side 180 has at least one integrated circuit including flash memory, circuit traces, and passive components.

Figure 3 shows the bottom of the circuit board 110 with segments 160 of a conductive layer. These segments may be part of circuit traces on the front side of the circuit board, may be segments that were used for electroplating purposes on either the front or the back of the circuit board, or may be test leads that are not needed after a testing or burn in period of the board. During the production of the circuit board, it is cut or sheared to its final dimensions and placed into a plastic cover or encapsulated as seen in Figure 1. The final shearing or cutting is performed in a direction from the front side 180 to the rear side 190 such that any deformation from the process would extend along edges of circuit board 110 from the covered front side 180 down to the exposed rear side 190. Thus for the purposes of describing the relation of the component parts during the shearing or cutting process, the conductive layers 112 or 114 are described as below the conductive segments 160 seen on the covered front side 180 of the circuit board.

Figure 4 illustrates an intermediate stage in the production of the circuit board. At this stage, segments 160 are connected to bus 165. Segments 160 and bus 165 are part of the same conductive layer before circuit board 180 is trimmed to its final dimensions. The segments in this intermediate example may be circuit traces used in electroplating on either the front or back of the circuit board, or as in Figure 3 may be functional circuit elements or test leads. The present invention protects against short circuiting of any conductive segments of a conductive layer positioned above another conductive layer during a cutting or shearing operation.

Figure 5a is an enlarged view of an edge of some of the layers of the circuit board after shearing showing only one gap or slot for illustrative purposes. Figure 5a shows conductive layer 112 positioned below the conductive segments 160. An insulating layer 116 is positioned between the conductive segments 160 and the

conductive layer 112. Conductive layer 112 has gaps 112a and edge portions 112b. Gaps 112a are wider (i.e. larger in the X direction) than segments 160 and any deformation of segments 160 that may reach the plane of conductive layer 112 during the shearing or cutting process will arrive at gap 112a rather than contact any portion of the conductive layer 112, thus avoiding a short circuit. Note that edge portions 112b of circuit board 110 are located at the junction 130 between circuit board 110 and cover 120 as seen in Figure 1. Thus a rather large part of the conductive layer is positioned at the edge of the circuit board to attract any ESD which may occur, while at the same time any potential short circuit resulting from contact of segments 160 with layer 112 or 114 is avoided.

Figure 6a is a cross sectional view taken along section A-A of the circuit board shown in Figure 5a. Conductive segment 160 on insulating layer 116 has been deformed during the shearing or cutting operation such that deformation 160a of segment 160 extends down the edge of the circuit board. The amount of deformation and thus size of deformation 160a depend on the shearing force, the geometry of the shearing instrument, and the elasticity of the metal of the conductive segment. It is foreseen that the deformation may extend down the edge of the circuit board, i.e. in the Z direction, into or away from the edge of the board, i.e. in the Y direction, and across the edge of the board, i.e. in the X direction. Thus the gap 112a is made sufficiently wide enough that any amount of deformation in the X direction will fall into the gap and not contact edge portions 112b. Gap 112a is also sufficiently deep enough that any deformation that extends into the gap, or in the Y direction, will likewise not contact conductive layer 112. Conductive layer 114 is fashioned in the same method and has the same structure as layer 112. Layer 112 or 114 may respectively be either the ground or power layer. Figure 7 shows the relative width,

or size of the gap and the segment in the X and Y directions. The size of the conductive segments can vary widely depending on the function of the segment, but generally range from about one mil (0.001") up to about 50 mils (0.05"), and the width and depth of the gap are sized proportionally to the segment with sufficient tolerance such that any deformation will enter the gap and not make contact with the conductive layer. In one example, the width *csw* of conductive segment 160a of Figure 7 is 4 mils wide (i.e. in the X direction), and the width *gw* of gap 112a is 40 mills from edge to edge (i.e. in the X direction) while the depth *gd* is 60 mills (i.e, in the Y direction).

Figure 5b is an enlarged view of another example of an edge of the circuit board. This figure illustrates possible deformation patterns of segment 160. Deformation 160a may extend not only in the Z direction as illustrated by Figure 5a, but also laterally along the X axis and into the gaps 112a along the Y axis as a result of the trimming of the circuit board. Gap 112a is made wide enough (i.e. along the X axis) such that any deformation 160a will fall into gap 112a or 114a and not make contact with edge portions 112b of conductive layer 112 or 114. Likewise, it is deep enough (i.e. along the Y axis) such that any deformation into memory card 100 will fall into gap 112a or 114a and not make contact with layer 112 or layer 114. In Fig. 5b deformations 160a are only shown extending to layer 112. However deformation 160a may extend to layer 114 and would thus fall into gap 114a rather than make contact with edge portions 114b.

Figure 5c is an enlarged view of another example of an edge of the circuit board. In this example, all of the layers of the circuit board are slotted at the edge of the circuit board. A slot 116c, 112c, and 114c is formed in insulating layer 116, conductive layer 112, and conductive layer 114 respectively. The slot runs through

all of the layers of the circuit board including the layers that are not shown and the layers that are not numbered. Slots 116c, 112c, and 114c are smaller in both the X and Y direction than the gaps 112a and 114a in conductive layers 112 and 114. Thus, the gaps 112a and 114a extend laterally (i.e. in the X direction) on either side of slots 112c and 114c. The gaps 112a and 114a also extend deeper (i.e. in the Y direction) than slots 112c and 114c. Thus the slots are formed within the gaps and are completely surrounded by the gaps. As with the previous examples of Figures 5a and 5b, any deformation 160a that may occur will fall into gaps 112a and 114a rather than make contact with edge portions 112b or 114b of conductive layers 112 and 114. Thus, short circuiting is avoided. There can be many different variations in the geometry of the edge, and in particular the slots 116, 112, and 114 so long the gaps in the conductive layers 112 and 114 are larger in the X and Y direction than the conductive segments 160 that they are aligned with.

Figure 6c is a cross sectional view taken along section A-A of the circuit board shown in Figure 5c. As described above regarding Fig. 6a, conductive segment 160 on insulating layer 116 has been deformed during the shearing or cutting operation such that deformation 160a of segment 160 extends down the edge of the circuit board. The amount of deformation and thus size of deformation 160a depend on the shearing force, the geometry of the shearing instrument, and the elasticity of the metal of the conductive segment. It is foreseen that the deformation may extend down the edge of the circuit board, i.e. in the Z direction, into or away from the edge of the board, i.e. in the Y direction, and across the edge of the board, i.e. in the X direction. Thus the gap 112a is made sufficiently wide enough that any amount of deformation in the X direction will fall into the gap and not contact edge portions 112b or 114b. Gap 112a is also sufficiently deep enough that any deformation that extends into the

gap, or in the Y direction, will likewise not contact conductive layer 112 or conductive layer 114.

Figure 8 shows some of the various shapes that gap 112a may have. Gap 112a may have many different sizes and shapes, all of which are proportionately large enough to avoid any short circuit between deformation 160a and conductive layer 112 or 114.

While an illustrative example of the invention has been shown and described, it will be apparent that other modifications, alterations and variations may be made by and will occur to those skilled in the art to which this invention pertains.

It is therefore contemplated that the present invention is not limited to the embodiments shown and described and that any such modifications and other embodiments as incorporate those features which constitute the essential features of the invention are considered equivalents and within the true spirit and scope of the present invention.

IT IS CLAIMED:

1. A circuit board having at least one peripheral edge comprising:

a first conductive layer having conductive segments at the edge of the circuit board;

a first insulative layer;

a second conductive layer separated from the first conductive layer by the first insulative layer, positioned below the first conductive layer, and extending to the edge of the circuit board, the second conductive layer having gaps at the edge of the circuit board, one or more of the gaps aligned with the conductive segments whereby any deformation of the conductive segments that extends over the edge to the plane of the second layer extends within the gaps and does not contact the second conductive layer.

2. The circuit board of claim 1 wherein the gaps are slots.

3. The circuit board of claim 1 wherein the gaps are notches.

4. The circuit board of claim 1 wherein the width of the gap is smaller away from the edge than it is at the edge of the circuit board.

5. The circuit board of claim 1 wherein the second conductive layer is the ground or power layer.

6. The circuit board of claim 1 further comprising a third conductive layer, the third conductive layer having gaps at the edge of the circuit board, the gaps aligned with the conductive segments whereby any deformation of the conductive segments that extends to the plane of the third layer extends within the gaps and does not contact the third conductive layer.

7. The circuit board of claim 6 wherein the third conductive layer is the ground or power layer.

8. A method of making a multi-layer circuit board:

forming a first conductive layer having conductive segments positioned along at least one edge of the circuit board;

forming an insulative layer below the first conductive layer

forming a second conductive layer below the first conductive layer and the insulative layer, said second conductive layer having gaps positioned along the at least one edge of the circuit board, at least one of said gaps larger than said conductive segments and aligned with said conductive segments;

trimming the circuit board and the conductive segments such that any deformation of the segments extends into the gaps and does not make contact with the second conductive layer.

9. The method of claim 8 wherein the step of trimming the circuit board comprises the step of shearing the circuit board.

10. The method of claim 9 wherein the first conductive layer is sheared before the second conductive layer.

11. A circuit board having at least one edge comprising:

a power layer extending to the at least one edge;

a ground layer extending to the at least one edge; and

at least one additional layer having metallic segments at the at least one edge of the circuit board, the at least one additional layer separated from the ground or power layer by an insulating layer;

wherein portions of the ground or power layer positioned under the metallic segments at the at least one edge are slotted whereby any deformation of the metallic segments at said at least one edge does not contact the ground or power layer.

12. The circuit board of claim 11 wherein the metallic segments connect to a bus which is also trimmed from the circuit board.

13. The circuit board of claim 11 wherein the metallic segments are circuit traces.

14. The circuit board of claim 11 wherein the metallic segments are test leads.

15. A structure comprising:

a metallic layer comprising at least one bus, a first area, and segments connecting the at least one bus to the first area; and

a circuit board comprising:

at least one edge, wherein the first area of the metallic layer forms a first layer of the circuit board and wherein the segments connecting the bus to the first area are positioned at the at least one edge of the circuit board and extend over the at least one edge of the circuit board to the at least one bus;

an insulative layer below the metallic layer; and

a second conductive layer positioned below the metallic layer and the insulative layer and extending to the at least one edge, the second conductive layer having gaps at the at least one edge of the circuit board, whereby at least one of the gaps is aligned with at least one of the segments.

16. The structure of claim 15 whereby any deformation of the conductive segments that extends over the at least one edge to the plane of the second conductive layer extends within the gaps and does not contact the second conductive layer.

17. A method of making a memory storage device comprising a circuit board, a cover, and a junction between an edge of the circuit board and the cover comprising:

forming a first metallic layer comprising a first area, a bus, and a plurality of segments connecting the first area to the bus at the edge of the circuit board, the first area positioned within the circuit board, the bus positioned without the circuit board;

forming an insulating layer below the first area of the first metallic layer;

forming a second metallic layer below the insulating layer and separated from the first metallic layer by the insulating layer, the second metallic layer extending to the edge of the circuit board and having a plurality of gaps at the edge of the circuit board positioned below the plurality of segments;

shearing the plurality of segments at the edge of the circuit board and removing the bus such that any deformation of the segments falls within the gaps of the second metallic layer.

18. The method of claim 17 further comprising placing the circuit board into the cover such that the edge of the circuit board and of the second metallic layer is at the junction between the cover and the circuit board.

19. The circuit board of claim 1 further comprising at least one integrated circuit including flash memory, circuit traces, and passive components.

20. The circuit board of 11 further comprising at least one integrated circuit including flash memory, circuit traces, and passive components.

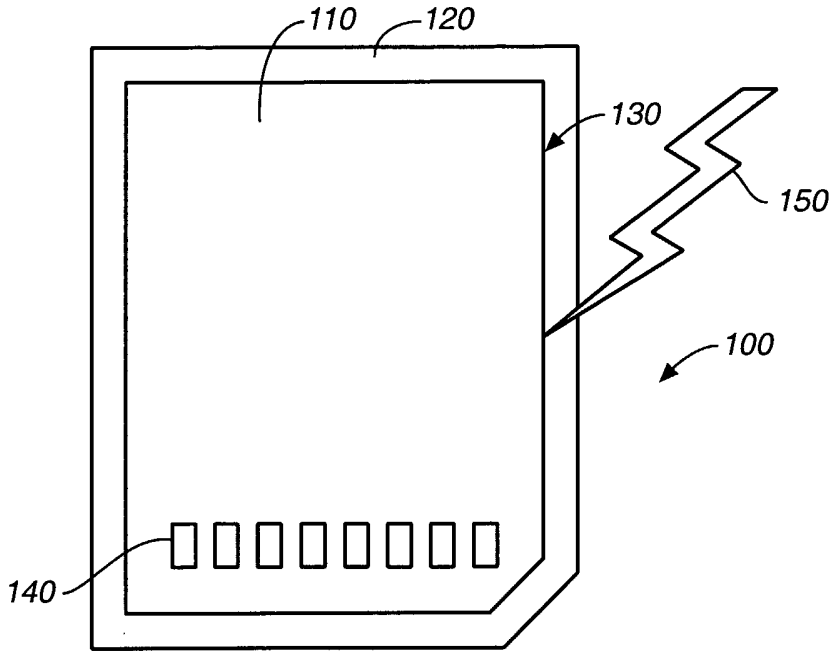



FIG._1

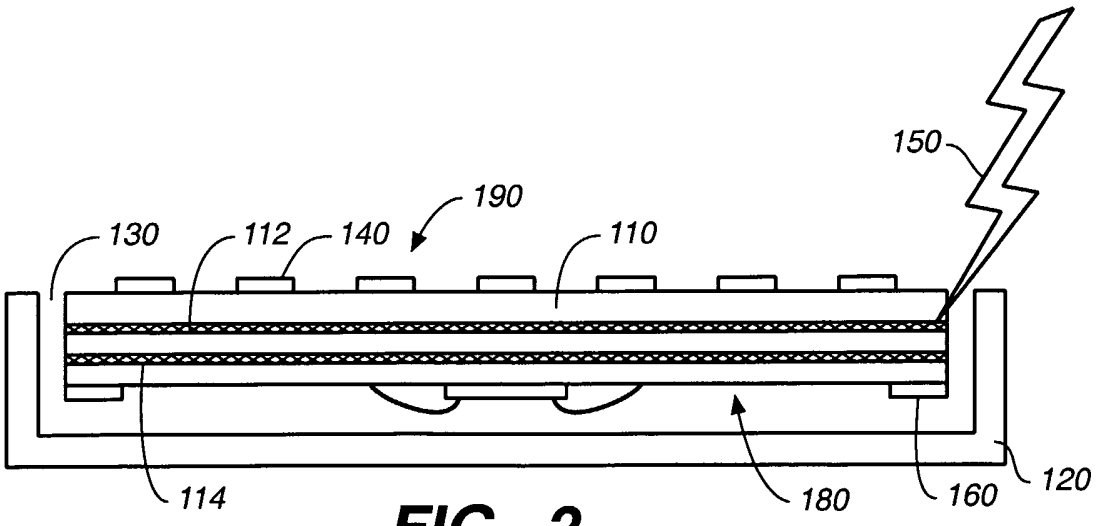
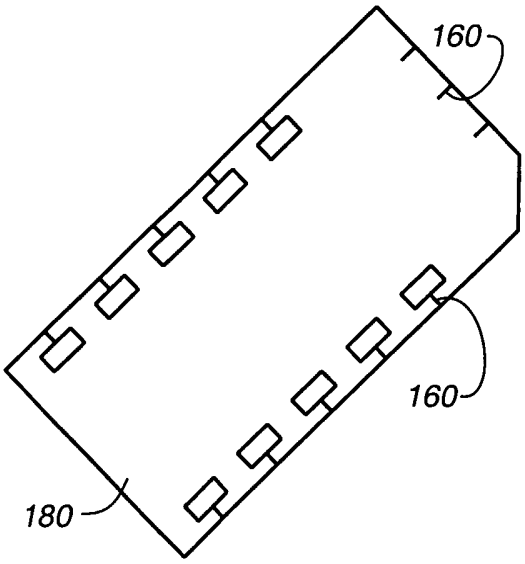



FIG._2



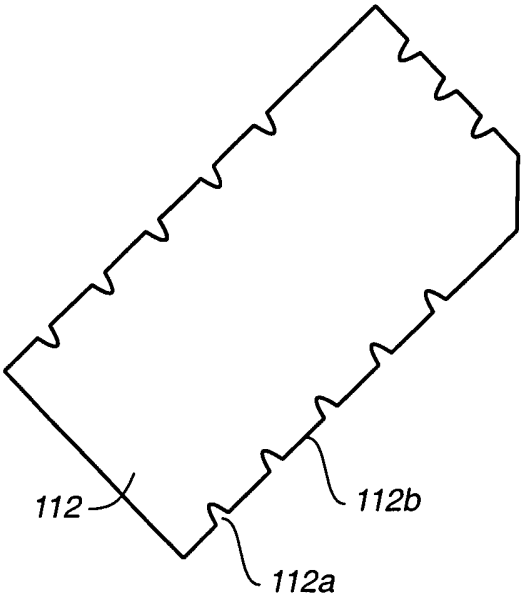
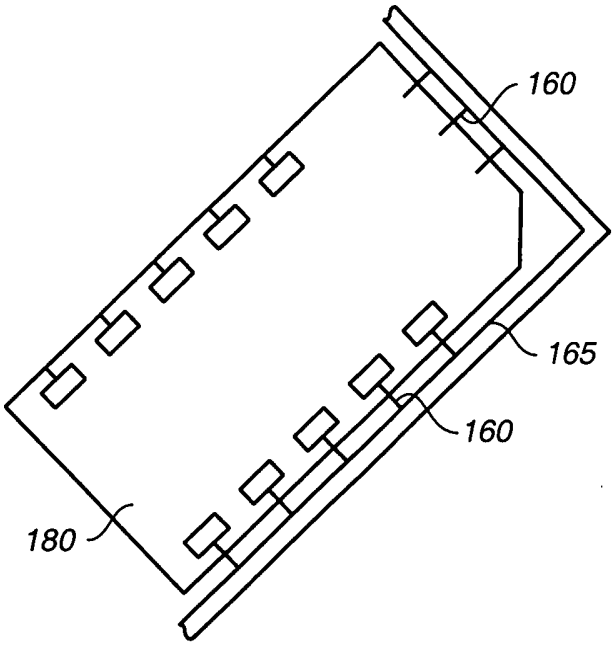




FIG._3



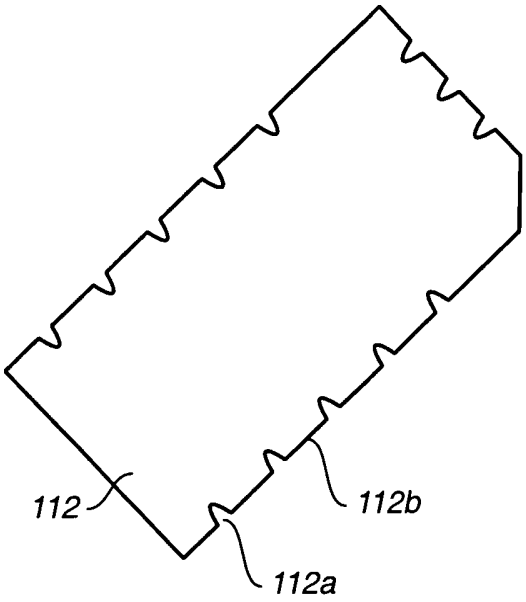




FIG._4

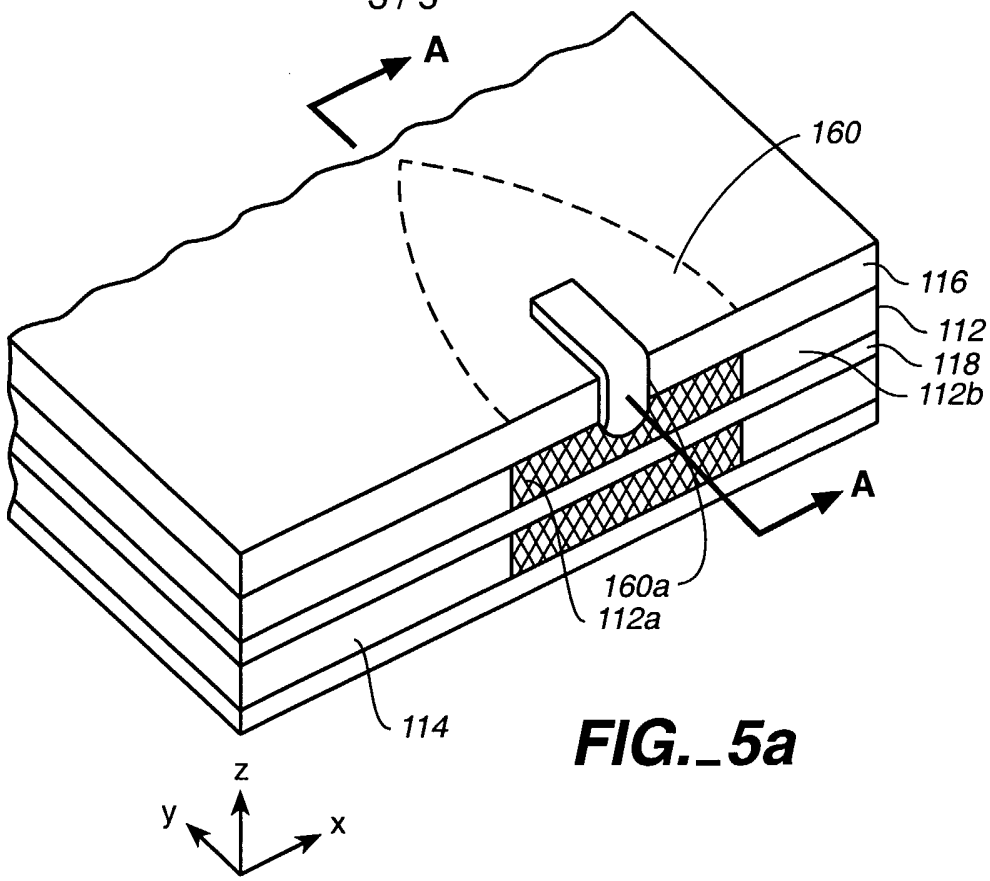

A
160
116
112
118
112b
A
160a
112a
114
z
y
x

FIG._5a

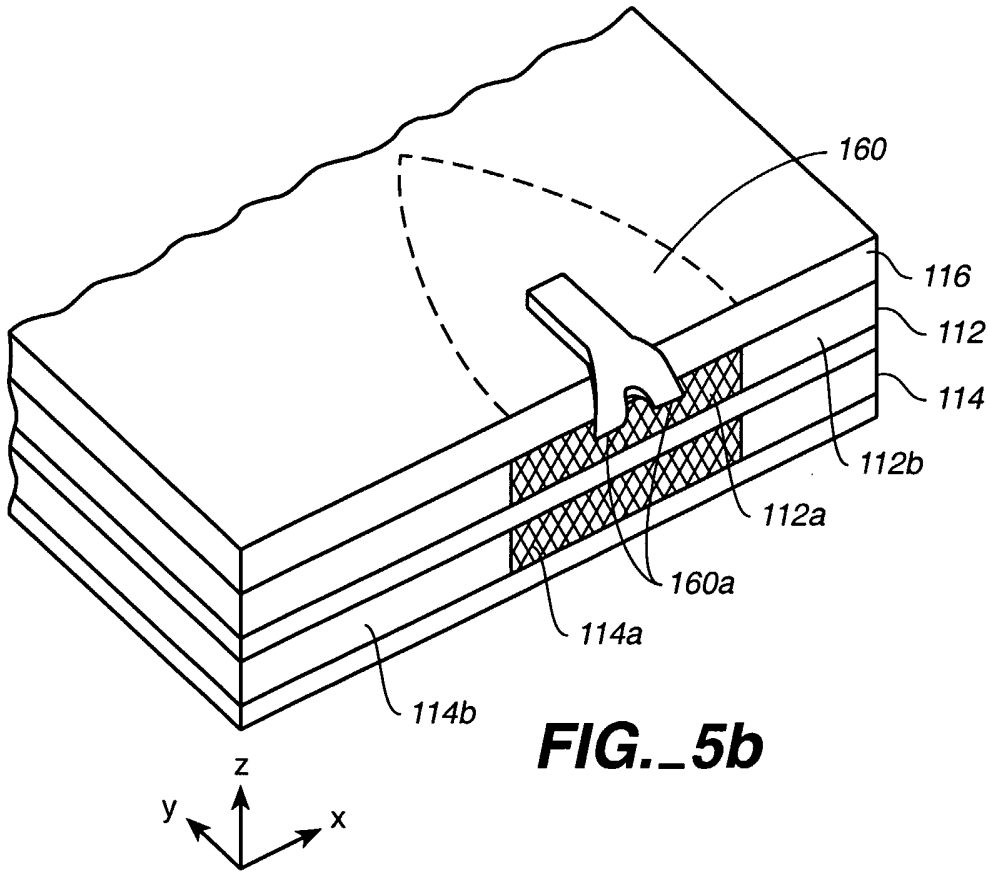

160
116
112
114
112b
112a
160a
114a
114b
z
y
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FIG._5b

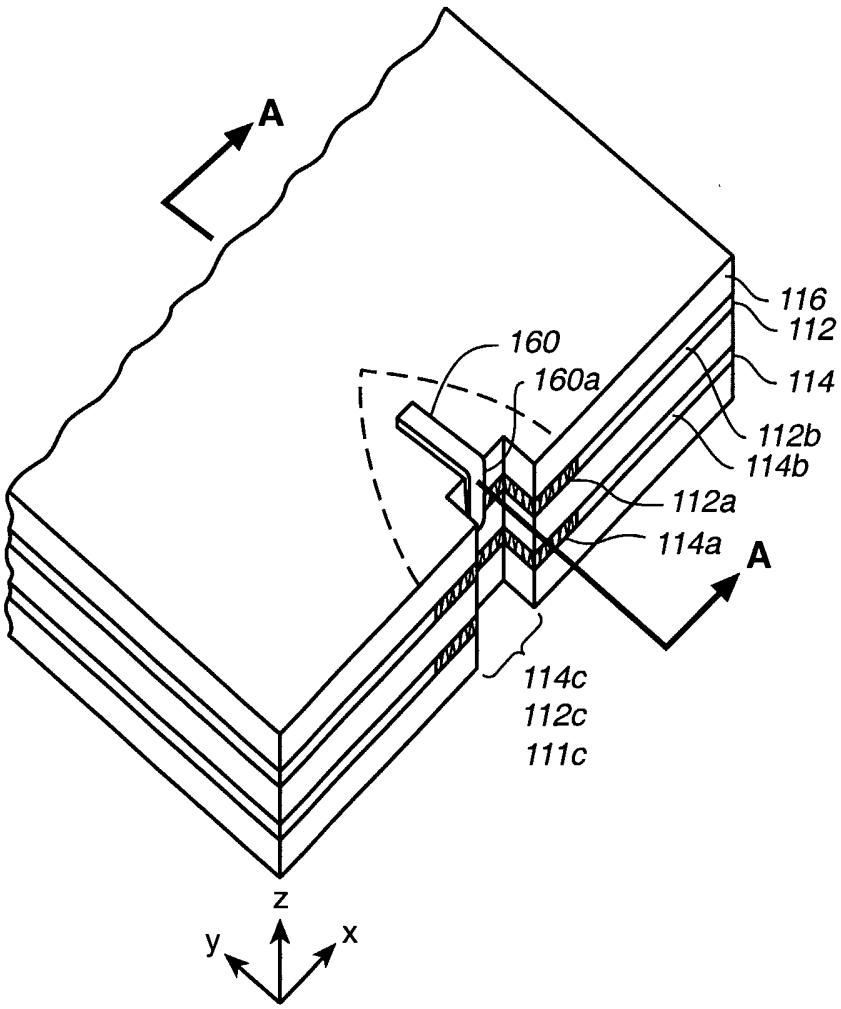



FIG._5c

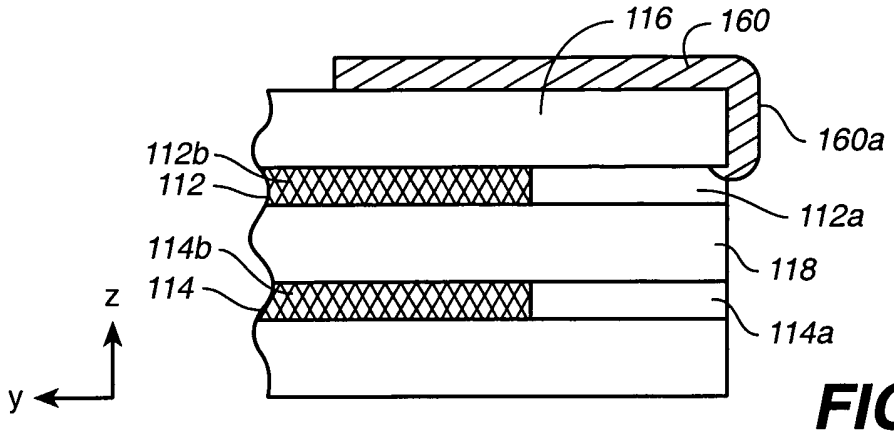



FIG._6a

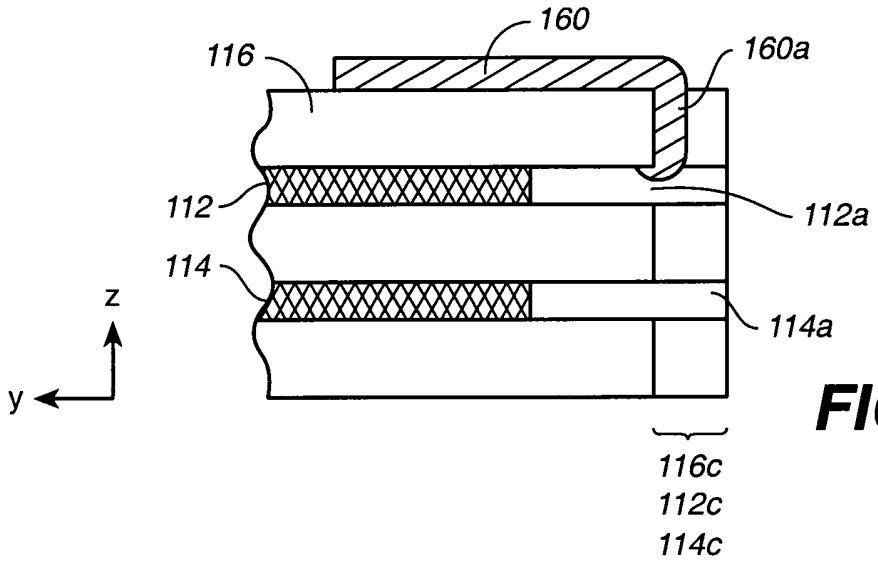



FIG._6c

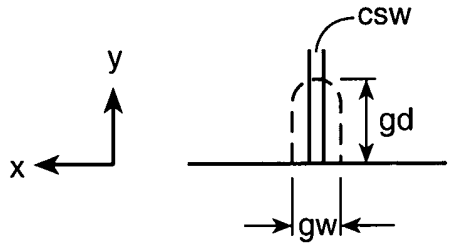



FIG._7

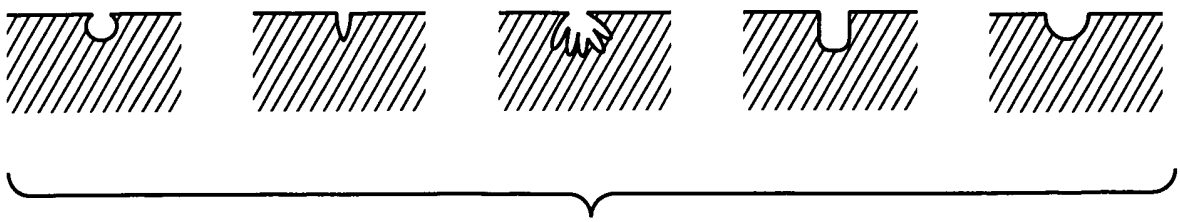


FIG._8

# INTERNATIONAL SEARCH REPORT

PCT/US 02/24535

**A. CLASSIFICATION OF SUBJECT MATTER**
IPC 7 H05K1/11 H05K1/02

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
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**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1998, no. 14,<br>31 December 1998 (1998-12-31)<br>& JP 10 242608 A (NITTETSU SEMICONDUCTOR KK), 11 September 1998 (1998-09-11)<br>abstract<br>--- | 1,2,5-7 |
| A | HOSSEINI S: "THE ELECTRICAL INSULATION OF ELECTROPLATING BUS BARS IN FLEXES"<br>MOTOROLA TECHNICAL DEVELOPMENTS, MOTOROLA INC. SCHAUMBURG, ILLINOIS, US,<br>vol. 15, 1 May 1992 (1992-05-01), page 39<br>XP000305735<br>ISSN: 0887-5286<br>the whole document<br>---<br>-/-- | 1 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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