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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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(54) **Title**: LED WITH SHAPED GROWTH SUBSTRATE FOR SIDE EMISSION

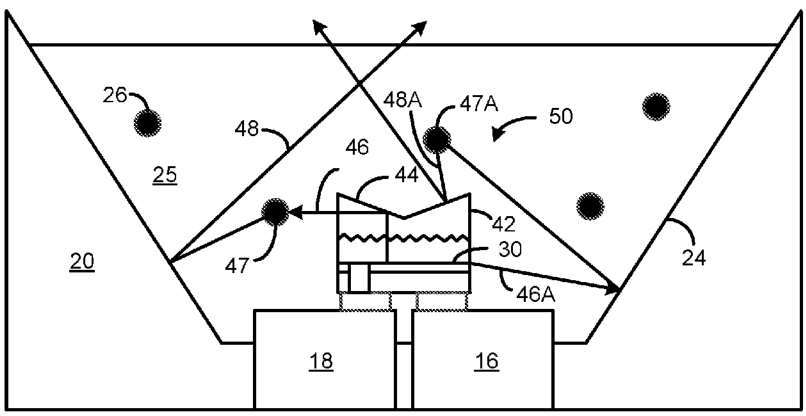

Fig. 5

(57) **Abstract**: An array of optical features is formed in a surface of a relatively thick growth substrate wafer. LED layers are epitaxially grown over the opposite surface of the growth substrate wafer. The LED layers include an active layer that emits light towards the growth substrate wafer. The resulting LED wafer is singulated to form individual LED dies having a growth substrate portion, wherein each growth substrate portion has at least one of the optical features. The optical features redirect a majority of light emitted from the active layer to exit the LED die through sidewalls of the growth substrate portion. The side-emitting LED die is mounted in a reflective cup and encapsulated with a phosphor material. The LED light thus energizes phosphor grains that are not overlying the LED die, so less phosphor light is absorbed by the LED die and efficiency is improved.

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LED WITH SHAPED GROWTH SUBSTRATE FOR SIDE EMISSION

Mark Butterworth

FIELD OF THE INVENTION

This invention relates to light emitting diodes (LEDs) and, in particular, to a technique for causing an LED to have enhanced side emission.

BACKGROUND

A vast majority of all light emitted from an LED die is from its top surface, opposite the LED's mounting surface. This essentially creates a pin point of light, since the top surface area is on the order of 1 mm^2.

Fig. 1 represents a common use for an LED, where the LED is located in a reflective cup for directing light in a particular direction, such as for an LED flash in a smartphone camera. Fig. 1 is a cross-sectional view of a typical flip-chip LED die 10 having its anode contact 12 and its cathode contact 14 formed on the bottom surface of the die 10. The contacts 12 and 14 take up a large area of the bottom surface of the LED die 10 and are reflective. The die 10 may optionally be mounted on a submount having more robust metal pads for bonding to the electrodes of a package 20.

The contacts 12 and 14 are bonded to electrodes 16 and 18 in a package 20. The package electrodes 16 and 18 may then be connected to any other terminals, such as to metal pads on a printed circuit board, a substrate, elongated pins for insertion into a socket, etc.

The LED die 10 is located in a reflective cup 22. The reflective walls 24 of the reflective cup 22 may be coated with a reflective metal or paint, or the cup 22 itself may be formed of a reflective material.

The LED die 10 may be GaN based and emit blue light. The cup 22 is filled with a material comprising phosphor powder 26 infused in silicone, epoxy, or other encapsulating binder material 25. The phosphor powder 26 may be YAG (emits yellow-green light), or a mixture or red and green phosphor powders, or any other type of phosphor(s). Some blue light escapes, and the resulting mixture of blue light and phosphor light create white light or any other color of light, depending on the phosphor type and density of the phosphor.

The LED die 10, in its simplified example of Fig. 1, has an n-type semiconductor layer 28, an active layer 30, and a p-type semiconductor layer 32. There are typically many other layers in a heterojunction GaN LED. The LED layers are epitaxially grown over a growth substrate. A conductor 34 extends through the p-type semiconductor layer 32 and active layer 30 to connect the cathode contact 14 to the n-type semiconductor layer 28. In the example of Fig. 1, the growth substrate, such as sapphire, has been removed.

Generally, the LED die 10 absorbs about 15% of the visible light that impinges on it. In the example of Fig. 1, a blue light ray 36 from the LED die 10 energizes a particular grain 38 of the phosphor powder 26, and the light (e.g., yellow light) emitted from the grain 38 is emitted in all directions. One of the emitted rays 40 is shown coming back toward the LED die 10, where about 15% of the light is absorbed by the LED die 10.

Since the vast majority of all light emitted by the LED die 10 is through its top surface, and almost half of the light emitted by the phosphor above the LED die 10 is downward toward the LED die 10, there is a significant amount of light absorbed by the LED die 10, lowering the efficiency of the LED module.

What is needed is an inexpensive technique for improving the efficiency of LED modules, such as an LED die in a reflective cup.

SUMMARY

In one embodiment, a transparent growth substrate wafer, such as sapphire, SiC, GaN, or other growth substrate wafer is patterned, by masking and etching or any other suitable method, to have optical features with angled sides that reflect a majority of the LED light sideways so that a majority of the LED light is emitted from the sidewalls of the LED. The optical features are formed opposite the growth surface (i.e., on the outside of the complete LED). Since there may be many thousands of LEDs grown on a single growth substrate wafer, there will be thousands of the optical features formed in the substrate. In one embodiment, the optical features are concave cones or dimples having a vertex

approximately centered with respect to its associated LED. Other optical feature shapes are also envisioned.

The growth substrate wafer is preferably much thicker than a conventional growth substrate wafer. For example, conventional growth substrate wafers are typically less than 100 microns (ideally, the minimum thickness to achieve the desired mechanical support during processing). To achieve the desired depths of the optical features (e.g., cones) and to create a relatively large surface area for the sidewalls, the growth substrate wafer may be greater than twice the thickness of a conventional growth substrate wafer, such as 0.5 mm-1 mm.

The angled sides of the optical features may reflect the LED light by total internal reflection (TIR), or a thin reflective metal layer may be deposited over the growth substrate wafer to coat the outer surface of the optical features. The etching of the growth substrate wafer is preferably performed prior to the LED semiconductor layers being grown to avoid damage to the LEDs. It will be assumed that the LED is a GaN based LED emitting blue light or ultraviolet light. After the LEDs are formed over the growth substrate wafer, the wafer is singulated to form individual side-emitting LED dies.

Accordingly, a majority of all the light emitted by the LED die’s active layer will be reflected sideways by the optical features.

When the resulting LED die is mounted in a reflective cup, and the cup is filled with a phosphor material, the phosphor grains that are energized by the blue light will not be over the LED die, but will be over a reflective surface of the cup. Therefore, when the grains emit light in all directions, a smaller percentage of the phosphor light will impinge on the active layer and be absorbed by the LED and a larger percentage will be reflected upward by the cup’s reflective walls surface. This greatly increases the light output of the LED module and improves efficiency with very little additional cost.

The invention is not limited to flip-chip LEDs, and vertical LEDs or LEDs with top contacts may be used instead of flip-chip LEDs.

It is known to create a side-emitting LED, such as for use in backlights, by affixing a separate side-emitting lens over the top of an LED die. However, the present technique obviates such a side-emitting lens. Since no separate side-emitting lens is used, the cost for the lenses and extra processing steps are avoided, and the LED module can be made shallower. Reflecting the LED light using optical features in the growth substrate is also more optically efficient than using a side-emitting lens.

Various other embodiments are disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional simplified view of a prior art blue or UV flip-chip LED die mounted in a reflective cup filled with a phosphor material.

Fig. 2 is a cross-sectional view of a small portion of a relatively thick transparent growth substrate wafer.

Fig. 3 illustrates the wafer of Fig. 2 after the bottom surface is roughened to improve light extraction and after the top surface is formed to have optical features to cause the LED to be a side-emitting LED.

Fig. 4 is a cross-sectional view of two simplified LEDs formed on the growth substrate wafer of Fig. 3.

Fig. 5 is a cross-sectional view of a singulated LED die mounted in a reflective cup filled with a phosphor material, where the phosphor grains emit light away from the top surface of the LED die to reduce the amount of absorption by the LED die.

Fig. 6 illustrates the structure of Fig. 5 but with the addition of an LED submount.

Fig. 7 is a cross-sectional view of another embodiment of an LED die, where the optical feature formed in the growth substrate has a bowl or parabolic shape.

Fig. 8 is a cross-sectional view of another embodiment of an LED die, where the optical feature formed in the growth substrate has a dome shape for refracting light away from over the top surface of the LED die.

Elements that are the same or similar are labeled with the same numeral.

DETAILED DESCRIPTION

The present inventive technique may be applicable to many types of different LEDs, and one example of an LED structure will be described to illustrate the invention's application. In the example, the LED is a GaN based LED that emits blue light. A suitable transparent growth substrate for a GaN based LED is typically sapphire, SiC, or GaN.

Fig. 2 illustrates a sapphire growth substrate wafer 42. Such wafers are available between 2-6 inches in diameter, although larger wafers are anticipated and included within the scope of the invention. Since a typical LED is only about 1 mm^2, many thousands of LEDs may be formed on a single wafer 42. The conventional thickness of such a wafer is less than 100 microns, or what the manufacturer believes is the minimum thickness needed for mechanical support of the LED layers during processing. However, in the present process, a much thicker wafer 42 is used to accommodate the depth of the side-emitting optical features and to create a large sidewall surface area. In one embodiment, the thickness of the wafer 42 is about 0.3 mm-1 mm, and preferably greater than 0.5 mm.

The bottom surface 43 (the GaN growth surface) of the wafer 42 is roughened to increase light extraction by reducing total internal reflection (TIR). Such roughening is conventional and may be performed by grinding, chemical etching, plasma etching, etc.

In one embodiment, the top surface of the wafer 42 is masked, using a metal (Ni) mask or a photoresist mask, and chemically etched to form thousands of optical features 44, one for each LED to be formed. In one embodiment, the wafer 42 surface is patterned with a Ni mask and a chlorine-based inductively coupled plasma-RIE process is used to form conical optical features. The thickness of the Ni mask creates a shadow effect near the edges of each mask opening so that the etching rate progressively diminishes towards the edges of the Ni openings. Etching features in sapphire is known. A laser or grinding tool may also be used to etch the wafer 42. A cross section of a conical optical feature 44 is shown in Fig. 3 although many other suitable features may be formed. Figs. 6 and 7 illustrate some other optical features.

The depth of the optical features 44 may exceed one half the width of the singulated LED for a 45 degree angle cone to achieve a wide TIR angle. For example, the depth of the cone may be about 0.5 mm. Other shapes of optical features may be made shallower and utilize a thinner wafer 42.

In one embodiment, the reflection by the optical features 44 is by TIR. In another embodiment, a thin layer of reflective metal, such as silver or aluminum, is deposited (e.g., by sputtering) over the optical features 44. The reflective metal may only be a few microns thick. In such a case, the growth substrate wafer 42 may be thinner. Dielectric layers may also be formed as a Bragg reflector over the optical features 44 to act as a mirror.

As shown in Fig. 4, the LED semiconductor layers may then be epitaxially grown over the roughened surface 43 using conventional techniques. Such a GaN based LED may have the same layers 28, 30, and 32 as described with respect to Fig. 1. The metal conductor 34, anode contact 12, and cathode contact 14 are then formed to form a flip-chip LED.

The resulting LED wafer is then singulated by, for example, laser etching or scribing followed by breaking. Singulation lines 48, including the kerf, are shown in Fig. 4. Many suitable ways of singulating an LED wafer are known.

As shown in Fig. 5, the resulting LED dies 50 are mounted in a reflective cup 20, as described with respect to Fig. 1. The bare LED dies 50 may optionally be mounted on a robust submount 51, shown in Fig. 6, prior to be mounted in the cup 20. The submount 51 acts as a heat spreader and provides much larger and robust bottom contacts 52 for attachment to the cup electrodes 16 and 18. Such a submount 51 however adds height and cost to the module.

The cup 20 is then filled with a material comprising phosphor powder 26 infused in a transparent or translucent encapsulant binder material 25 such as silicone or an epoxy. The material 25 is then cured. The type(s) of phosphor powder(s), the density of the phosphor powder 26, and the thickness of the phosphor layer determine the overall color emitted by the combination of the LED light and phosphor light.

As shown in Fig. 5, the optical feature 44 will cause most of the LED light emitted from the active layer 30 to be reflected out the relatively large sidewalls of the LED die 50. Thus, most of the LED die's emitted light will energize phosphor grains that are over the reflective cup surface rather than over the LED die 50. When these grains emit light in all directions, a vast majority of the emitted light will either be emitted upward, out the top surface of the module, or be reflected upwards by the reflective cup. Only a small percentage of the emitted light will impinge the active layer 30 of the LED die 50, where about 15% of the light will be absorbed by the active layer 30. A light ray 46 emitted by the active layer 30 is shown being reflected by the optical feature 44 and energizing a phosphor grain 47, where the grain 47 emits a light ray 48 that is reflected upward by the cup's reflective wall 24.

Additionally, if the top of the wafer 42 is coated with a reflective film, such as a reflective metal, any light emitted by the phosphor grains that impinges on the reflective film will be redirected away from the LED die 50 and not be absorbed. This further increases the efficiency of the structure of Fig. 5. In Fig. 5, this is illustrated by the light ray 46A energizing a phosphor grain 47A, which emits a light ray 48A that reflects off a reflective film on the wafer 42.

Thus, compared to the conventional structure of Fig. 1, there is a large reduction in the absorption of light by the active layer 30, and efficiency is improved at very little additional cost.

The side-emitting LED die 50 is also useful for backlighting liquid crystal displays (LCDs) by more evenly spreading light into a light guide, where the light guide has prisms or a roughened surface for redirecting the light toward the LCD screen. Since the side-emitting LED die is very shallow, the light guide may be very thin. The LED dies may be mounted in holes in the light guide or along its edges.

Many other optical features besides cones may be formed in the growth substrate wafer. For example, a dimple having a vertex and a symmetrical asymptotic or parabolic shape may be used.

Fig. 7 illustrates how the optical feature may be a bowl shape 56, which may be easier to form than a cone shape. Reflection may be by TIR, or a reflective metal may be deposited in the bowl. A reflected light ray 57 is shown.

Fig. 8 illustrates how the optical feature may be a convex dome shape 58. In such a case, the LED light is refracted away from over the LED top surface. A refracted light ray 59 is shown.

In another embodiment, the LED die 50 is not a flip-chip.

In another embodiment, the wavelength conversion material in the reflective cup is other than phosphor, such as a quantum dot material.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.

CLAIMS

What is claimed is:

1. A light emitting structure comprising:

a light emitting diode (LED) die comprising:

a growth substrate having a first surface and a second surface opposite the first surface; and

semiconductor layers, including an active layer that emits light, epitaxially grown over the first surface of the growth substrate, the active layer having a third surface facing the growth substrate, wherein the second surface of the growth substrate has formed in it at least one optical feature that redirects at least a portion of the light emitted from the third surface of the active layer to exit the LED die through sidewalls of the growth substrate.

2. The structure of Claim 1 wherein the at least one optical feature is covered with a reflective layer that reflects the portion of the light emitted from the third surface of the active layer to exit the LED die through the sidewalls of the growth substrate.

3. The structure of Claim 1 wherein the at least one optical feature has an angled surface that redirects light toward the sidewalls of the growth substrate.

4. The structure of Claim 1 wherein the at least one optical feature comprises a concave, substantially conical shape formed in the growth substrate.

5. The structure of Claim 1 wherein the at least one optical feature comprises a concave rounded shape formed in the growth substrate.

6. The structure of Claim 1 wherein the at least one optical feature comprises a convex rounded shape that refracts the light towards the sidewalls of the growth substrate.

7. The structure of Claim 1 wherein the growth substrate comprises sapphire.

8. The structure of Claim 1 wherein the growth substrate is greater than 200 microns thick.

9. The structure of Claim 1 wherein the growth substrate is greater than 500 microns thick.

10. The structure of Claim 1 further comprising:

a reflective cup in which the LED die is mounted; and

a wavelength conversion material in the cup covering a top and sides of the LED die.

11. The structure of Claim 10 wherein the wavelength conversion material comprises phosphor grains infused in a binder material, and wherein at least a portion of the light emitted from the sidewalls of the growth substrate energize phosphor grains that are not overlying the LED die.

12. The structure of Claim 1 further comprising a phosphor material covering a top and sides of the LED die, wherein the LED die emits blue light and the phosphor material emits phosphor light that combines with the blue light.

13. The structure of Claim 1 wherein the at least one optical feature redirects a majority of the light emitted from the third surface of the active layer to exit the LED die through sidewalls of the growth substrate.

14. A method of forming a light emitting structure comprising:

providing a growth substrate wafer having a first surface and a second surface opposite the first surface;

forming a plurality of optical features in the second surface of the growth substrate wafer;

after forming the plurality of optical features, growing epitaxial layers over the first surface of the growth substrate wafer to form a light emitting diode (LED), the LED having an active layer that emits light, the active layer having a third surface facing the growth substrate wafer; and

singulating the growth substrate wafer to form individual LED dies having a growth substrate portion, wherein each growth substrate portion has at least one of the optical features, the least one of the optical features redirecting a majority of light emitted from the third surface of the active layer to exit the LED die through sidewalls of the growth substrate portion.

15. The method of Claim 14 further comprising:

mounting one of the LED dies in a reflective cup; and

depositing a wavelength conversion material in the cup covering a top and sides of the LED die.

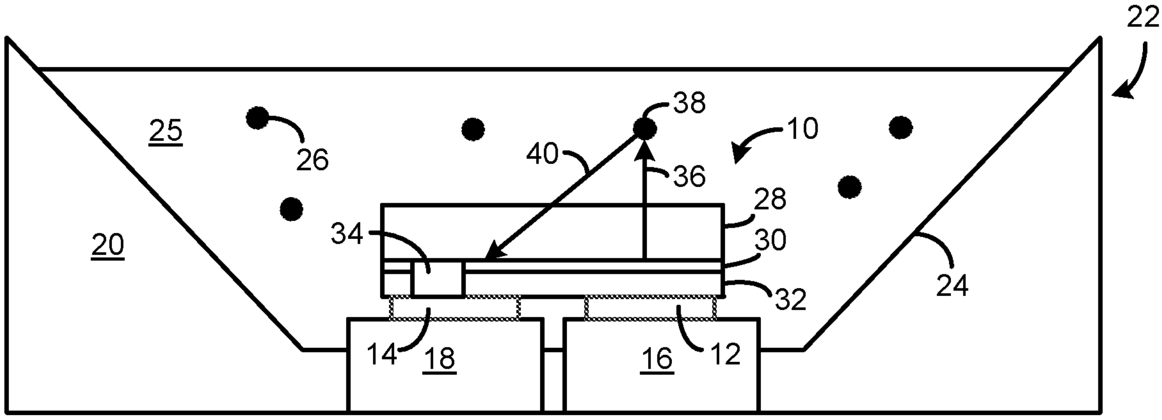

Fig. 1 (prior art)

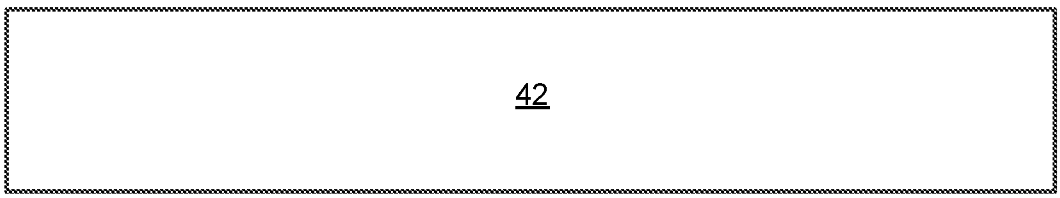

Fig. 2

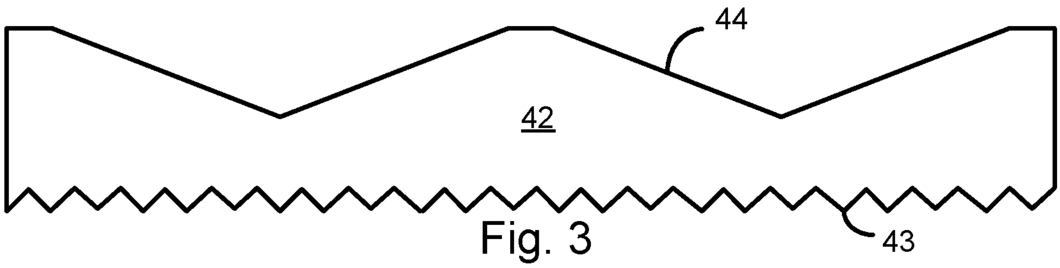

Fig. 3

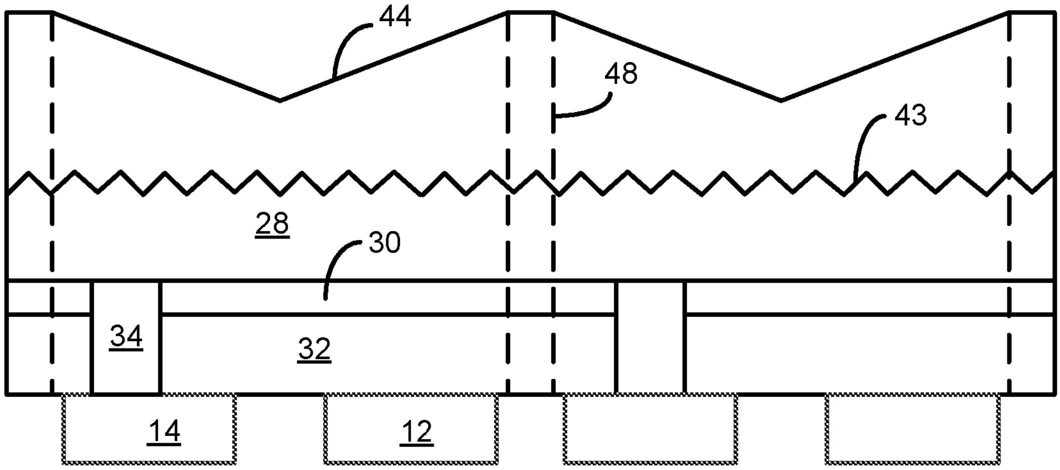

Fig. 4

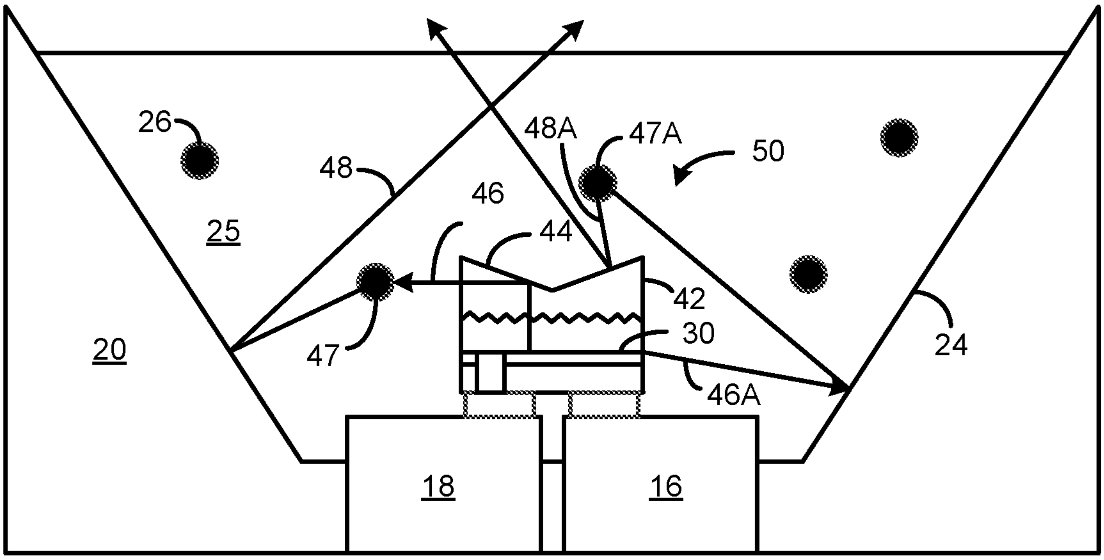
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Fig. 5

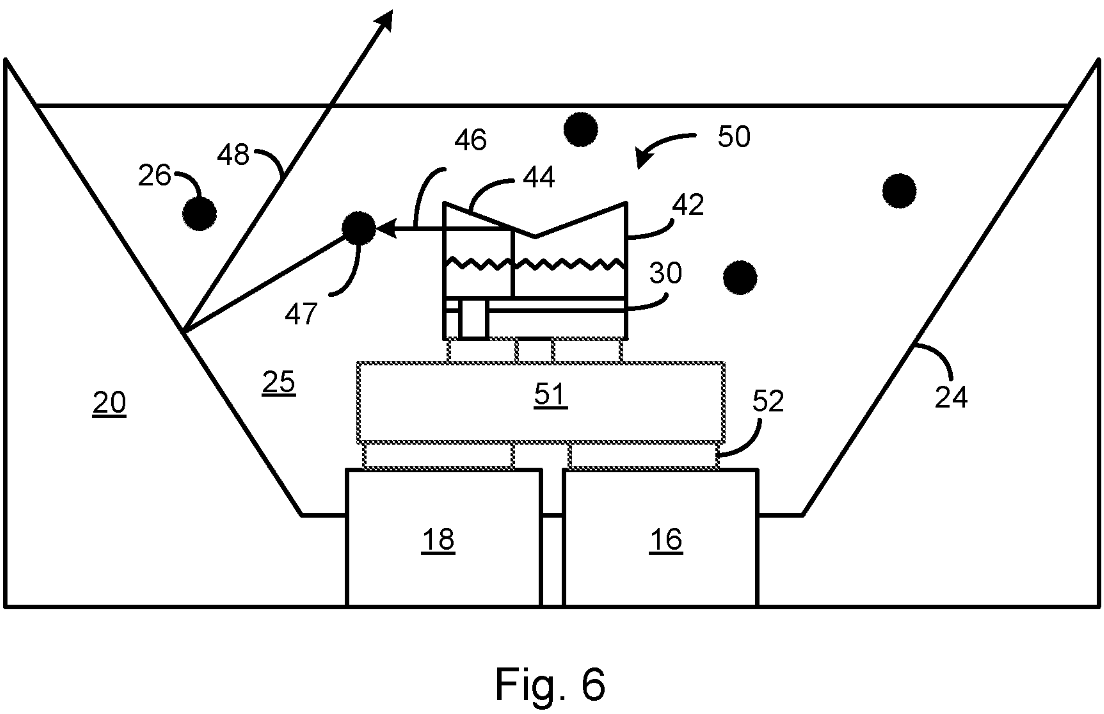
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Fig. 6

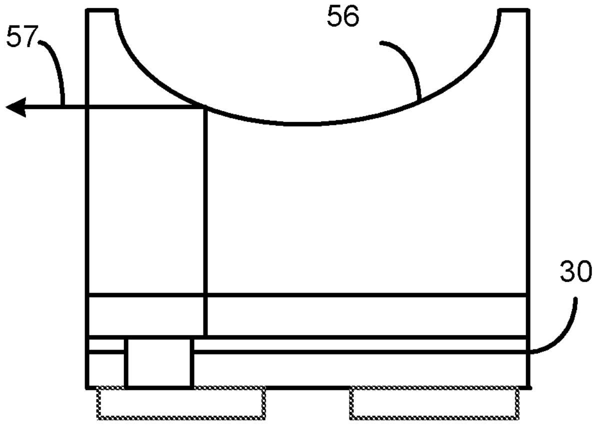

Fig. 7

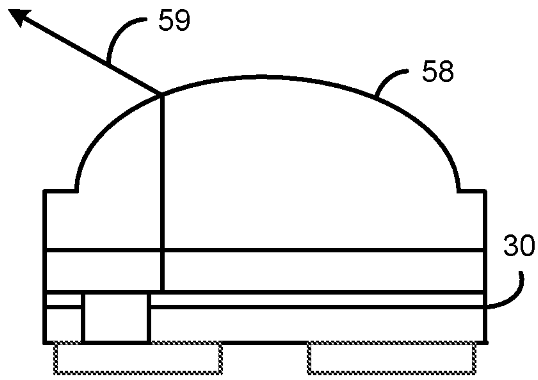

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2014/058077

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/00 H01L33/20 H01L33/46
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
14 April 2014	24/04/2014

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

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