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(74) Agents: STEFFEY, Charles E. et al.; Schwegman, Lund-
berg & Woessner, P.A., P.O. Box 2938, Minneapolis, Min-
nesota 55402 (US).

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(71) Applicant (for all designated States except US): LAM
RESEARCH CORPORATION [US/US]; 4650 Cushing
Parkway, Fremont, California 94538 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): MAKHRATCHEV,
Konstantin [RU/US]; 3412 Manchester CMN, Fremont,
California 94536 (US). MCMILLIN, Brian [US/US];
5408 Quebec Common, Fremont, California 94555 (US).

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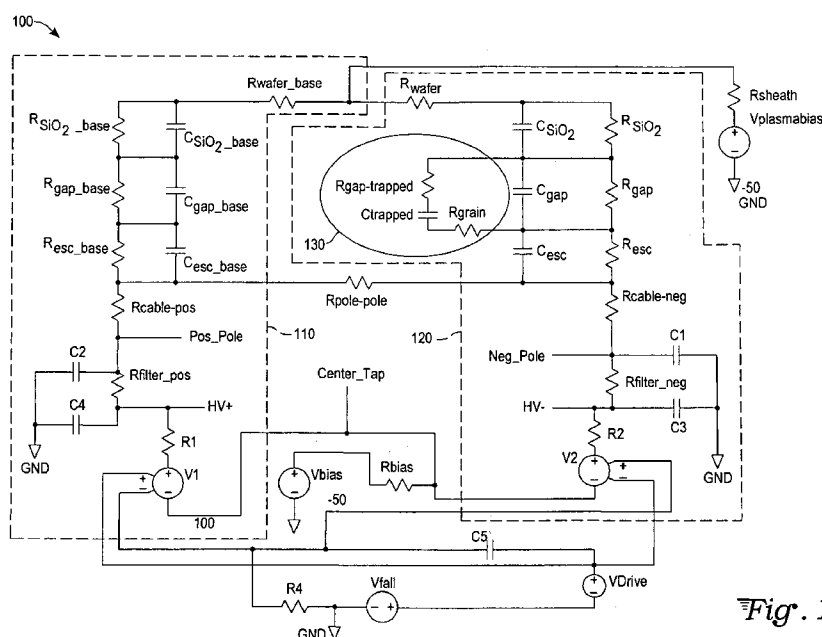


Fig. 1

(57) Abstract: A method for simulating the effect of trapped charge in an electrostatic chuck on the chuck performance comprises creating a trapped-charge electrical model having a trapped-charge capacitor and a gap-trapped resistor, and coupling the model to a plurality of voltage sources. The trapped-charge capacitor and the gap-trapped resistor may be varied in relation to a plurality of electrostatic chuck physical parameters.

METHOD FOR USING AN RC CIRCUIT TO MODEL TRAPPED CHARGE IN AN ELECTROSTATIC CHUCK

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of United States Provisional Application Serial No. 61/013,596 filed December 13, 2007 and entitled “Method For Using an RC Circuit to Model Trapped Charge in an Electrostatic
10 Chuck,” the content of which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

The present invention is related to the design and simulation of an electrostatic chuck, commonly employed in semiconductor processing equipment
15 for holding a substrate. More specifically, the present invention provides an improved method and model for the simulation of trapped charge in an electrostatic chuck in order to estimate effects of trapped charge on chuck performance. By application of the model and simulation method, the effects of specific operating parameters such as effective clamp voltage and leakage
20 current, can be determined, enabling the design of an electrostatic chuck having desirable operating characteristics.

BACKGROUND ART

Electrostatic chucks are increasingly employed in semiconductor
25 processing equipment as a means for holding a substrate, such as a silicon wafer, in position while undergoing a fabrication process. Skilled artisans will appreciate that electrostatic chucks have a variety of benefits such as an ability to hold a substrate securely in a vacuum chamber where conventional vacuum chucks are inappropriate. An electrostatic chuck can retain a wafer without a

need for mechanical retention devices like clips, which can interfere with process conditions, damage the wafer surface, or exclude a portion of the wafer surface from receiving a desired process treatment.

Electrostatic chucks operate by inducing opposing charges on the
5 substrate and the chuck resulting in an electrostatic attraction between the chuck and the substrate. The degree of attraction is dependent on an amount of charge induced as well as a rate at which the charge dissipates due to conductive effects. Voltage biasing is employed to induce and control the electrostatic force and may be applied for only a portion of a processing cycle, e.g., just after a substrate
10 is transferred to the chuck. Alternately, voltage biasing may be applied continuously throughout a processing cycle. For example, using the conduction properties of a plasma can provide a means of electrical connection to one terminal of a substrate and wafer system.

The design and simulation of an electrostatic chuck requires an
15 estimation of several parameters. In particular, the amount of charge which is accumulated between the substrate and the chuck is an important parameter. This charge, known as gap charge, is retained in regions where the substrate and the chuck are not in physical contact. Another important parameter is the electrical resistance between the substrate and the chuck. This resistance, known
20 as gap resistance, is associated with numerous points of contact between the chuck and the substrate. (Skilled artisans will appreciate surface roughness present on both the substrate and the chuck produces a microscopic chuck/substrate interface having many discrete points of physical connection in association with numerous gaps, despite a macroscopic appearance of direct
25 contact.) The gap charge is directly related to the attractive force between the chuck and the substrate, while the gap resistance determines how quickly the attractive force diminishes with time if not maintained by a voltage bias.

When applying a bias to the substrate/chuck system, the gap charge will be affected by charge which is trapped in the chuck itself. This trapped charge is
30 determined by the physical design of the electrostatic chuck in addition to its chemical composition. The trapped charge will further be determined by electrical characteristics of the chuck. In particular, ceramics commonly used by

skilled artisans for electrostatic chucks have a grain structure which can provide a resistive path for electrical conduction through the chuck. Additionally, a gap-trapped resistance between the chuck and the substrate can provide an electrical path for trapped charge in the chuck to pass into or out of the substrate according to voltage bias conditions. Finally, the substrate itself will possess a resistance which can affect the charge distribution and time-varying characteristics of the substrate/chuck system.

The design and simulation of electrostatic chucks typically involves the use of experimentally determined values for key design parameters, in particular for the measurements of the charge trapped in the chuck (which will be referred to herein as C_{trapped}). In order to model the performance of a chuck having altered design parameters, for example, a different area, new measurements are typically made on a physical system. Furthermore, trade publications and technical articles typically employ simple electrical models for the apparatus used to bias the chuck. These models are usually based on a single constant voltage source and on/off switch with only two resistors and two capacitors.

What is needed is an improved means for electrically modeling the trapped charge in an electrostatic chuck and a method for simulating the effect of trapped charge on electrical parameters which relate to desirable performance characteristics of the chuck such as adhesive force.

SUMMARY OF THE INVENTION

These needs have been met in the present invention which presents a method and an apparatus for modeling the trapped charge in an electrostatic chuck by means of a combination of resistance and capacitance values. This combination, known as an RC model, is employed in a circuit which incorporates other electrical models relevant to the electrostatic chuck performance (e.g., a resistance value associated with the substrate). The circuit behavior is then simulated with a circuit simulator which further incorporates controls for various voltage sources representative of the conditions used in actual operation of the electrostatic chuck in semiconductor processing

equipment. The circuit simulation may also be used as a means for enabling the construction of an electrostatic chuck and associated control apparatus for use in processing equipment.

In an exemplary embodiment, the present invention is a method of using
5 a circuit simulator to simulate an effect of trapped charge in an electrostatic
chuck on the electrostatic chuck performance. The method includes creating a
trapped-charge electrical model by coupling a trapped charge capacitor to a gap-
trapped resistor, and to a grain resistor; selecting a capacitance value C_{trapped} for
the trapped charge capacitor; selecting a resistance value $R_{\text{gap-trapped}}$ for the gap-
10 trapped resistor; selecting a resistance R_{grain} for the grain resistor; creating an
electrostatic chuck simulation circuit by coupling a substrate-to-chuck interface
gap capacitor with a substrate-to-chuck interface gap capacitor, a substrate
resistor, at least one cable resistor, and a plurality of voltage sources; configuring
at least one of the plurality of voltage sources to provide a time-varying voltage;
15 coupling the trapped-charge electrical model with the electrostatic chuck
simulation circuit; and executing a first simulation in the circuit simulator to
determine time-varying voltage and currents responses within a plurality of
circuit nodes in the electrostatic chuck simulation circuit.

In another exemplary embodiment, the present invention is a circuit to
20 measure an effect of trapped charge in an electrostatic chuck system on the chuck
performance. The circuit includes an electrostatic chuck circuit portion having a
substrate-to-chuck interface gap capacitance C_{gap} coupled to a substrate-to-chuck
interface gap resistance R_{gap} , a substrate resistance R_{wafer} , at least one cable
resistance R_{cable} , and a trapped-charge circuit portion having a capacitance
25 C_{trapped} , a resistance $R_{\text{gap-trapped}}$, and a resistance R_{grain} . The circuit further includes
a plurality of voltage sources where at least one of the plurality of voltage
sources is capable of varying a voltage output as a function of time with the
plurality of voltage sources coupled to the electrostatic chuck circuit portion.

In another exemplary embodiment, the present invention is a method of
30 designing an electrostatic chuck. The method includes building in a circuit
simulator a circuit model for the electrical behavior of the electrostatic chuck
using an RC trapped-charge model; coupling the circuit model to a plurality of

voltage sources; simulating the circuit model with the circuit simulator to determine voltage potentials at a plurality of circuit nodes and further to determine currents within a plurality of circuit components; varying the circuit model in relation to changes in physical parameters of the electrostatic chuck; and simulating the circuit with the circuit simulator to determine changes produced by varying the circuit model.

In another exemplary embodiment, the present invention is a system for controlling an electrostatic chuck. The system includes a voltage-controlled voltage source means for providing a time-varying bias to the electrostatic chuck in proportion to a time-varying controlling voltage, the time-varying bias for controlling a substrate to chuck adhesion according to simulation results from a charge-trapped circuit model; a time-varying voltage means for providing the time-varying controlling voltage; a dc bias means for applying a dc bias to the electrostatic chuck; and a cable means coupling the electrostatic chuck, the voltage-controlled voltage source means, the time-varying voltage source means, and the dc bias means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is circuit schematic of an exemplary electrostatic chuck system used to model the performance of an electrostatic chuck within an apparatus for semiconductor processing.

Fig. 2 is a simulated voltage vs. time plot for an exemplary electrostatic chuck system.

Fig. 3 is a circuit schematic for an electrostatic chuck subsystem used to model a reduced charge trap area.

Fig. 4 is a simulated voltage vs. time plot for an electrostatic chuck system with a reduced charge trap area.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Fig. 1, an exemplary embodiment of the present invention comprises an electrostatic chuck system 100 having a baseline circuit portion 110 and a modified circuit portion 120. The baseline simulation portion 110 is used to provide a circuit simulation of an electrostatic chuck without the influence of trapped charge. The modified circuit portion 120 includes a trapped charge RC model 130 which enables the influence of trapped charge on the electrostatic chuck performance to be determined, by methods to be explained below. The trapped charge RC model 130 includes a resistor $R_{\text{gap-trapped}}$, a capacitor C_{trapped} , and a resistor R_{grain} .

Attention is directed back to the baseline circuit portion 110 which includes resistors $R_{\text{wafer_base}}$, $R_{\text{SiO2_base}}$, $R_{\text{gap_base}}$, $R_{\text{esc_base}}$, $R_{\text{cable_pos}}$, $R_{\text{filter_pos}}$, and $R1$. The baseline circuit portion 110 further includes a voltage-controlled voltage source $V1$ and capacitors $C_{\text{SiO2_base}}$, $C_{\text{gap_base}}$, $C_{\text{esc_base}}$, $C2$, and $C4$. In the notations for the capacitor and resistor circuit elements comprising the baseline circuit portion 110, the subscripted suffix “_base” is intended to identify that the circuit element is associated with a baseline case, i.e., the operation or simulation of an electrostatic chuck where the effects of trapped charge are ignored. In the discussion of the modified circuit portion 120, circuit elements will be introduced which have analogous functions, and are identified by corresponding names without the “_base” notation.

A first terminal of the resistor $R_{\text{wafer_base}}$ is coupled to a first terminal of the resistor $R_{\text{SiO2_base}}$ and to a first terminal of a capacitor $C_{\text{SiO2_base}}$. The resistor $R_{\text{SiO2_base}}$ simulates a resistance of a native oxide on a substrate on the electrostatic chuck. For this exemplary embodiment, $R_{\text{SiO2_base}}$ corresponds to resistance of native SiO_2 (silicon dioxide) on a silicon wafer, and the capacitor $C_{\text{SiO2_base}}$ corresponds to the capacitance of a layer of native SiO_2 which forms spontaneously on a silicon surface. A second terminal of the resistor $R_{\text{wafer_base}}$ is coupled to a first terminal of a resistor R_{wafer} and to a first terminal of a resistor R_{sheath} . The resistor $R_{\text{wafer_base}}$ simulates a bulk resistance of a substrate on the electrostatic chuck. A second terminal of the resistor $R_{\text{SiO2_base}}$ is coupled to a second terminal of the capacitor $C_{\text{SiO2_base}}$, to a first terminal of the resistor

$R_{\text{gap_base}}$, and to a first terminal of the capacitor $C_{\text{gap_base}}$. A second terminal of the resistor $R_{\text{gap_base}}$ is coupled to a second terminal of the capacitor $C_{\text{gap_base}}$, to a first terminal of the resistor $R_{\text{esc_base}}$, and to the first terminal of a capacitor $C_{\text{esc_base}}$. The resistor $R_{\text{gap_base}}$ and the capacitor $C_{\text{gap_base}}$ model the electrical characteristics of an interface between the semiconductor wafer and an electrostatic chuck surface. In particular, the resistor $R_{\text{gap_base}}$ is related to the electrical conductance associated with points of mechanical contact between the semiconductor wafer and the electrostatic chuck surface. The capacitor $C_{\text{gap_base}}$ is related to regions of separation between the semiconductor wafer and the electrostatic chuck surface. The resistor $R_{\text{esc_base}}$ models a bulk resistance of an electrostatic chuck; the capacitor $C_{\text{esc_base}}$ models a bulk capacitance of the electrostatic chuck.

A second terminal of the resistor $R_{\text{esc_base}}$ is coupled to a second terminal of the capacitor $C_{\text{esc_base}}$, to a first terminal of a resistor $R_{\text{cable-pos}}$ and to a first terminal of a resistor $R_{\text{pole-pole}}$. The resistor $R_{\text{pole-pole}}$ models parasitic leakage in the bulk of the electrostatic chuck material.

Attention is now directed to the modified circuit portion 120 which includes resistors R_{wafer} , R_{SiO_2} , R_{gap} , R_{esc} , R_{cable} , R_{filter} , and R_2 . The modified circuit portion 120 further includes a voltage-controlled voltage source V_2 and capacitors C_{SiO_2} , C_{gap} , C_{esc} , C_1 , and C_3 . With continued reference to the trapped charge RC model 130, a first terminal of the resistor $R_{\text{gap-trapped}}$ is coupled to a first terminal of the capacitor C_{gap} . A second terminal of resistor $R_{\text{gap-trapped}}$ is coupled to a first terminal of the capacitor C_{trapped} . A second terminal of the capacitor C_{trapped} is coupled to a first terminal of the resistor R_{grain} . A second terminal of the resistor R_{grain} is coupled to a second terminal of the capacitor C_{gap} . A first terminal of the capacitor C_{esc} is coupled to a first terminal of the resistor R_{esc} , and to the second terminal of the capacitor C_{gap} . A first terminal of the resistor R_{gap} is coupled to the first terminal of the capacitor C_{gap} and to the first terminal of the resistor $R_{\text{gap-trapped}}$. A second terminal of the resistor R_{gap} is coupled to the second terminal of the capacitor C_{gap} and to the second terminal of the resistor R_{grain} . The capacitor C_{SiO_2} has a first terminal coupled to the resistor R_{wafer} and to a first terminal of the resistor R_{SiO_2} . The capacitor C_{SiO_2} further has

a second terminal coupled to the first terminal of the resistor $R_{\text{gap-trapped}}$ and to the first terminal of the capacitor C_{gap} . A second terminal of the resistor R_{SiO_2} is coupled to the second terminal of the capacitor C_{SiO_2} . A first terminal of the resistor R_{wafer} is coupled to a resistor R_{wafer} and to the resistor R_{sheath} . A second
 5 terminal of the resistor R_{wafer} is coupled to the first terminal of the capacitor C_{SiO_2} and to the first terminal of the resistor R_{SiO_2} .

A voltage source $V_{\text{plasmabias}}$ having a positive terminal and a negative terminal is used to model a biasing effect produced by a plasma environment typical of a variety of semiconductor fabrication processes. The negative
 10 terminal of the voltage source $V_{\text{plasmabias}}$ is coupled to a power supply potential ground GND. The positive terminal of the voltage source $V_{\text{plasmabias}}$ is connected to the resistor R_{sheath} . A first terminal of the resistor R_{sheath} is coupled to a first terminal of the resistor R_{wafer} and to the second terminal of the resistor $R_{\text{wafer_base}}$.
 A second terminal of the resistor R_{sheath} is coupled to the positive terminal of the
 15 voltage source $V_{\text{plasmabias}}$. The resistor R_{sheath} models the resistance of a plasma sheath in a plasma environment. Together, the voltage source $V_{\text{plasmabias}}$ and the resistor R_{sheath} model the behavior of the plasma environment and its effect in the operation of the electrostatic chuck system 100. The voltage source $V_{\text{plasmabias}}$ is illustrated as having a potential of negative 50 volts. Skilled artisans will
 20 appreciate that the negative potential results in the terminal having the positive label is at a negative potential with respect to the supply potential GND. This labeling convention follows practice favored by skilled artisans and commonly employed in commercial circuit simulators. Furthermore, those skilled artisans will appreciate that the potential of negative 50 volts is representative of a typical
 25 operating condition associated with the presence of a plasma in the electrostatic chuck system 100. Other potentials, comprising both negative and positive values as well as zero volts, could be employed according to the specific processing conditions. For example, if the electrostatic chuck system were operated in a system having no plasma, e.g., in an ambient environment, then a
 30 potential of zero volts would be appropriate for $V_{\text{plasmabias}}$.

A second terminal of the resistor $R_{\text{pole-pole}}$ is coupled to a second terminal of the resistor R_{esc} , to a first terminal of a resistor $R_{\text{cable-neg}}$, and to a second

terminal of the capacitor C_{esc} . The resistors $R_{cable-pos}$ and $R_{cable-neg}$ model resistances associated with positive and negative cable connections applying controlling potentials in the electrostatic chuck system 100. A second terminal of the resistor $R_{cable-pos}$ is coupled to a first terminal of a resistor R_{filter_pos} and to a circuit node Pos_Pole. A first terminal of a capacitor C2 is coupled to the power supply potential GND. A second terminal of the capacitor C2 is coupled to the second terminal of the resistor $R_{cable-pos}$, to the circuit node Pos_Pole, and to the first terminal of the resistor R_{filter_pos} . A second terminal of the resistor R_{filter_pos} is coupled to a capacitor C4, to a first terminal of a resistor R1, and to a circuit node HV+. A first terminal of the capacitor C4 is coupled to the power supply potential GND, and a second terminal of the capacitor C4 is coupled to the second terminal of the resistor R_{filter_pos} .

A second terminal of the resistor $R_{cable-neg}$ is coupled to a first terminal of a resistor R_{filter_neg} , to a circuit node Neg_Pole, and to a first terminal of a capacitor C1. A second terminal of the capacitor C1 is coupled to the power supply potential GND. A second terminal of the resistor R_{filter_neg} is coupled to a first terminal of a capacitor C3, to a first terminal of a resistor R2, and to a circuit node HV-. A second terminal of the capacitor C3 is coupled to the power supply potential GND.

The resistors R_{filter_pos} , R_{filter_neg} , and capacitors C1, C2, C3, C4 will be familiar to those skilled in the art of circuit design as providing radio frequency (RF) bypass filters for shunting radio frequency signals to the circuit supply potential ground GND. Electrostatic chucks are often used in semiconductor processing equipment having a plasma generated by the application of radio frequency energy to a gas or gas mixture. An electrostatic chuck exposed to the plasma couples radio frequency energy to circuit elements (e.g., voltage sources) coupled to the electrostatic chuck. Therefore, it is common practice in physical systems to provide RF bypass filtering to shunt the RF energy to ground thereby preventing the RF energy from damaging circuit elements or creating a physical hazard. The RF bypass filters are also preferentially included into circuit simulations in order to permit modeling of their effect on the electrical performance of the system into which they are incorporated.

The electrostatic chuck system 100 further comprises a first voltage-controlled voltage supply V1 and a second voltage-controlled voltage supply V2. Voltage-controlled voltage supplies function as voltage amplifiers with a gain set by a potential associated with the supply and are a common feature in commercial circuit simulators known to those skilled in the art of circuit design and simulation. Each voltage-controlled voltage supply comprises a positive and a negative output terminal, indicated by the labels “+” and “-” respectively, within the circle symbol. In addition, each voltage-controlled voltage supply additionally has a positive and a negative control terminal, indicated by the labels “+” and “-” located outside the circle symbol on either of the left and right sides of the symbol. The second terminal of the resistor R1 is coupled to the positive output terminal of the first voltage-controlled voltage supply V1. The second terminal of the resistor R2 is coupled to the positive output terminal of the second voltage-controlled voltage supply V2. The negative output terminal of the first voltage-controlled voltage supply V1 is coupled to a resistor R_{bias} , to a circuit node Center_Tap, and to the negative terminal of the second voltage-controlled voltage supply V2.

A voltage source V_{bias} having a positive terminal and a negative terminal is used to model a control bias applied to the electrostatic chuck system. The negative terminal of the voltage source V_{bias} is coupled to the power supply potential GND. The positive terminal of the voltage source V_{bias} is coupled to a first terminal of the resistor R_{bias} . A second terminal of the resistor R_{bias} is coupled to the circuit node Center_Tap, to the negative output terminal of the first voltage-controlled voltage source V1, and to the negative output terminal of the second voltage-controlled voltage source V2. The voltage source V_{bias} and the resistor R_{bias} model the effect of a constant bias potential applied to the electrostatic chuck. The voltage source V_{bias} is illustrated as having a potential of negative 50 volts. Other values for the V_{bias} potential are possible, analogous to the discussions made above with respect to $V_{plasmabias}$.

The negative control terminal of the first voltage-controlled voltage source V1 is coupled to the positive control terminal of the second voltage-controlled voltage source V2, to a first terminal of a resistor R4, and to a first

terminal of a capacitor C5. A second terminal of the resistor R4 is coupled to the power supply potential GND. A second terminal of the capacitor C5 is coupled to the positive control terminal of the first voltage-controlled voltage source V1 and to the negative control terminal of the second voltage-controlled voltage source V2.

A voltage source V_{fall} has a negative terminal coupled to the power supply potential GND. A positive terminal of the voltage source V_{fall} is coupled to a negative terminal of a voltage source V_{Drive} . A positive terminal of the voltage source V_{Drive} is coupled to the second terminal of the capacitor C5, to the positive control terminal of the first voltage-controlled voltage source V1, and to the negative control terminal of the second voltage-controlled voltage source V2. In simulations to be described below, the voltage sources V_{fall} and V_{Drive} are operated as piece-wise linear sources having time-varying potentials in order to simulate the actions of applying controlling voltages to the electrostatic chuck for the purpose of varying the adhesion between the semiconductor wafer and the electrostatic chuck.

Those skilled in the art will appreciate that the circuit nodes Pos_Pole, Neg_Pole, HV+, HV-, and Center_Tap are labels employed as a convenience in the operation of circuit simulators to provide easily identifiable terminals for output of voltage potentials which may then be plotted or tabulated for further analysis.

Table I, shown below, summarizes the values employed for each of the resistive circuit elements described above, for a first exemplary embodiment of the present invention.

Circuit Element	Value (ohms)
R1	50 k
R2	50 k
R4	50 k
R _{bias}	3 Meg
R _{cable-neg}	1 Meg
R _{cable-pos}	1 Meg
R _{esc}	8 Meg
R _{esc base}	8 Meg
R _{filter neg}	250 k
R _{filter pos}	250 k
R _{gap}	100 Meg
R _{gap base}	100 Meg
R _{gap-trapped}	100 Meg
R _{grain}	100 Meg
R _{pole-pole}	150 Meg
R _{sheath}	1 k
R _{SiO2}	1 k
R _{SiO2 base}	1 k
R _{wafer}	100
R _{wafer base}	100

Table I

Further, values for capacitive circuit elements in the first exemplary embodiment are summarized in Table II, below.

5

Circuit Element	Value (Farads)
C1	470 e-12
C2	470 e-12
C3	1.1 e-9
C4	1.1 e-9
C5	1 e-6
C _{esc}	3 e-9
C _{esc base}	3 e-9
C _{gap}	10 e-9
C _{gap base}	10 e-9
C _{SiO2}	0.0021 e-6
C _{SiO2 base}	0.0021 e-6
C _{trapped}	50 e-9

Table II

Further, values for voltage source circuit elements in the first exemplary

embodiment are summarized in Table III, below.

Circuit Element	Value
V1	100
V2	100
V _{bias}	-50
V _{Drive}	PWL (0 0 1.99 0 2.0 10 40 10)
V _{fall}	PWL (0 0 19.7 0 20 -10 40 -10)
V _{plasmabias}	-50

Table III

Those skilled in the art of circuit design and simulation will appreciate that the values associated with V_{Drive} and V_{fall} represent time-varying voltages in a notation commonly employed in SPICE circuit simulators. In particular, and by way of example, the notation associated with the voltage source V_{Drive} is shorthand for the following voltage waveform description as detailed in Table IV, below.

Time (seconds)	Voltage Potential
(begin)	
0	0
19.7	0
20	-10
40	-10
(end)	

Table IV

For times which fall between those tabulated in Table IV, above, the SPICE circuit simulator performs a linear interpolation to compute a value for the voltage potential. Thus, the SPICE circuit simulator can associate a voltage value needed at any time required by a simulation. Configured according to Table III, the voltage sources V_{Drive} and V_{fall} simulate the application of a control bias initiating the clamping process between the substrate and the electrostatic chuck at a time of approximately two seconds, followed by the removal of the bias at approximately 20 seconds.

A skilled artisan will recognize that any of these parameters may be

readily varied to suit particular situations. By incorporating the element values as tabulated in Tables I-III into a circuit simulator and executing a simulation by techniques known to skilled artisans, voltage and current values within the circuit may be determined as a function of time for the first exemplary
 5 embodiment.

With continuing reference to Fig. 1, attention is now directed to Fig. 2 which provides a graphical representation of the circuit simulation results comprising a voltage versus time plot 200 including $VC_{\text{gap_base}}$ time dependent voltage curve 210, VC_{gap} a time dependent voltage curve 220, and a $VR_{\text{gap-trapped}}$
 10 time dependent voltage curve 230. Skilled artisans will recognize that the notation " VC_{gap} " is a compact method of representing "the voltage potential across the terminals of circuit element C_{gap} ." Similarly, the notations " $VC_{\text{gap_base}}$ " and " $VR_{\text{gap_trapped}}$ " represent voltage potentials across the terminals of circuit elements $C_{\text{gap_base}}$ and $R_{\text{gap-trapped}}$, respectively. Those skilled artisans
 15 will further appreciate that the circuit simulator is capable of indicating the voltage at any node within a simulated circuit, and is additionally capable of indicating the current through any circuit element. The voltage and current values not presented are excluded to avoid obscuring the present invention.

The $VC_{\text{gap_base}}$ time dependent voltage curve 210 is indicative of the
 20 voltage developed across the capacitor $C_{\text{gap_base}}$, i.e., between the substrate and the electrostatic chuck in the absence of any charge trapped in the chuck itself. The curve shows a rapid rise in voltage at approximately two seconds into the simulation as a result of the bias applied by voltage source V_{Drive} acting on voltage-controlled voltage sources V1 and V2. During the interval from
 25 approximately two seconds until approximately 20 seconds, the voltage indicated by the $VC_{\text{gap_base}}$ time dependent voltage curve 210 stays relatively constant. Therefore, the substrate would consequently experience a comparatively constant adhesion to the electrostatic chuck. At a time of approximately 20 seconds, the control bias is removed and the curve drops rapidly to approximately zero.
 30 Consequently, the adhesive force between the substrate and the electrostatic chuck also drops rapidly.

The VC_{gap} time dependent voltage curve 220 is indicative of the voltage

developed across the capacitor C_{gap} , which is representative of a potential between a substrate and an electrostatic chuck when including the influence of trapped charge in the electrostatic chuck. The curve 220 shows a rise in voltage at approximately two seconds into the simulation as a result of the bias applied by voltage source V_{Drive} acting on voltage-controlled voltage sources V1 and V2. In comparison with no trapped charge case represented by curve 210, the voltage rise for the trapped charge case curve 220 is less rapid. This shows that the adhesive force builds less rapidly when trapped charge is included in the electrostatic chuck model. During the interval from approximately two seconds until approximately 20 seconds, the voltage indicated by the VC_{gap} time dependent voltage curve 220 continues to rise, until it approximately matches the $VC_{\text{gap_base}}$ time dependent voltage curve 210 at a time of approximately 20 seconds. Thus, the simulation predicts that at approximately 20 seconds, the electrostatic chuck including the effect of trapped charge will have approximately the same chuck-to-substrate adhesive force as an electrostatic chuck without trapped charge. At approximately 20 seconds, the control bias is removed and the VC_{gap} time dependent voltage curve 220 falls. Comparison between the curves 210 and 220 shows that the effect of the trapped charge in the electrostatic chuck is to slow the rate at which the potential VC_{gap} returns toward zero. Consequently, the adhesive force between the substrate and the electrostatic chuck also drops less rapidly than for the case without trapped charge.

The $VR_{\text{gap-trapped}}$ time dependent voltage curve 230 illustrates the change in the potential across the gap-trapped resistor as the electrostatic chuck is biased. This potential may be used to interpret the charging and discharge of the trapped charge capacitor as the control bias is varied. The potential $VR_{\text{gap-trapped}}$ is also of interest because this potential is related to the electrostatic conditions at the wafer/electrostatic chuck interface and is responsible for wafer clamping and release processes. Examination of curve 230 shows that the potential $VR_{\text{gap-trapped}}$ rapidly increases at a time of approximately two seconds (as the control bias is applied), showing that the capacitor C_{trapped} (i.e., the electrostatic chuck trapped charge) is charging. From approximately two seconds to approximately 20 seconds, the potential $VR_{\text{gap-trapped}}$ diminishes as to

nearly zero, showing that the capacitor C_{trapped} is nearly fully charged during this interval. At approximately 20 seconds, the control bias is removed and the potential $V_{R_{\text{gap-trapped}}}$ becomes negative, indicating that the capacitor C_{trapped} is discharging. By a time of approximately 40 to 50 seconds, the potential $V_{R_{\text{gap-trapped}}}$ is nearly zero, indicating that the capacitor C_{trapped} (i.e., the electrostatic chuck trapped charge) is nearly discharged.

Attention will now be called to Fig. 3, comprising an exemplary electrostatic chuck subsystem 300, having a subsystem baseline circuit portion 310 and a subsystem modified circuit portion 320. The subsystem modified circuit portion 320 includes a modified trapped charge RC model 330, illustrating a second embodiment of the present invention. The components of the electrostatic chuck subsystem 300 are analogous in function to those components in Fig. 1 having identical names. Further, the components of the electrostatic chuck subsystem 300 are analogous in electrical value to the values of the first exemplary embodiment, *except* for the components comprising the modified trapped charge RC model 330. The resistance associated with $R_{\text{gap-trapped}}$ in this second exemplary embodiment is 500 Meg ohms; this is five times larger than the value of 100 Meg ohms employed in the first exemplary embodiment. This larger resistance represents the anticipated effect of reducing the trapped charge area of the electrostatic chuck, e.g., by decreasing the size of the chuck to one-fifth of its previous area, and hence reducing the number of points of contact between the chuck and substrate. If appropriate materials data are available, it is also possible to alter the value of C_{trapped} as the chuck geometry is altered

The resistor R_{grain} , which appears in the trapped charge RC model 110 of Fig. 1, is not included in the modified trapped charge RC model 330. The exclusion of the resistor R_{grain} models the electrical behavior of an electrostatic chuck in which the grain resistance is negligible. Skilled artisans will appreciate that an alternative to excluding the resistor R_{grain} for this situation from the modified trapped charge RC model 330 is to set the electrical value of its resistance to a sufficiently low value to make its effect negligible, e.g., to one milli-ohm. Yet another alternative is to retain the resistor R_{grain} in all simulations

and to select a value for R_{grain} appropriate to the physical situation being modeled, estimating for example, anticipated high and low extremes.

By incorporating the modified element values for the electrostatic chuck subsystem 300, as explained above, into the circuit simulator and again
5 executing a simulation, voltage and current values within the circuit may be determined as a function of time for the second exemplary embodiment.

With reference to Fig. 4, a graphical representation of the circuit simulation results comprising a modified trapped charge voltage versus time plot
400 including modified trapped charge $VC_{\text{gap_base}}$ time dependent voltage curve
10 410, a modified trapped charge VC_{gap} time dependent voltage curve 420, and a modified trapped charge $VR_{\text{gap-trapped}}$ time dependent voltage curve 430.

The modified trapped charge $VC_{\text{gap_base}}$ time dependent voltage curve 410 is indicative of the voltage developed across the capacitor C_{gap} , i.e., between the substrate and the electrostatic chuck in the absence of any charge trapped in the
15 chuck itself. Examination of this curve and comparison with the $VC_{\text{gap_base}}$ time dependent voltage curve 210 shows that the two results are comparable. This is to be expected as both results are associated with equivalent circuit portions representing the operation of an electrostatic chuck without any effect of trapped charge.

20 The modified trapped charge VC_{gap} time dependent voltage curve 420 is indicative of the voltage developed across the capacitor C_{gap} , which is again representative of the potential between a substrate and an electrostatic chuck when including the influence of the modified trapped charge in the electrostatic chuck. Comparison of the curve 420 with the curve 220 shows how the
25 modification of the electrostatic chuck trapped charge changes the performance of the electrostatic chuck. In comparison with the trapped charge case of the first embodiment, represented by the curve 220, the voltage rise for the modified trapped charge case curve 420 is more rapid. This shows that the adhesive force builds more rapidly when trapped charge is reduced in the electrostatic chuck
30 model. During the interval from approximately two seconds until approximately 20 seconds, the voltage indicated by the VC_{gap} time dependent voltage curve 420

5 closely approximates the modified trapped charge $VC_{\text{gap_base}}$ time dependent voltage curve 410. At approximately 20 seconds, the control bias is removed and the modified trapped charge VC_{gap} time dependent voltage curve 420 falls. Comparison between the curves 410 and 420 shows that the reduced trapped charge case more closely approximates the condition of an electrostatic chuck having no trapped charge. Consequently, the adhesive force between the substrate and the electrostatic chuck drops rapidly for the case having modified trapped charge.

10 The modified trapped charge $VR_{\text{gap-trapped}}$ time dependent voltage curve 430 illustrates the change in the potential across the gap-trapped resistor as the electrostatic chuck is biased. Examination of the curve 430 shows that the potential $VR_{\text{gap-trapped}}$ rapidly increases at a time of approximately two seconds (as the control bias is applied), showing that the capacitor C_{trapped} (i.e., the electrostatic chuck trapped charge) is charging. From approximately two
 15 seconds to approximately 20 seconds, the potential $VR_{\text{gap-trapped}}$ diminishes, but remains substantially above zero, indicating that the capacitor C_{trapped} continues to charge during this interval. At approximately 20 seconds, the control bias is removed and the potential $VR_{\text{gap-trapped}}$ becomes negative, indicating that the capacitor C_{trapped} is discharging. At a time of approximately 40 to 50 seconds,
 20 the potential $VR_{\text{gap-trapped}}$ is clearly negative, indicating that the capacitor C_{trapped} (i.e., the electrostatic chuck trapped charge) is continuing to discharge. Thus, the curve 430 indicates that the increased resistance associated with a reduction in an electrostatic chuck area will slow the rate at which trapped charge in the chuck equilibrates following changes in control bias potential. This information may
 25 be beneficially applied to modifications of an electrostatic chuck design.

For example, if it is desired to have the chuck respond rapidly to changes in a control bias, the area of the chuck could be increased to reduce $R_{\text{gap-trapped}}$. Alternately, if it is desirable to maintain adhesion for as long as possible after a control bias is removed, the electrostatic chuck area could be decreased, thereby
 30 increasing $R_{\text{gap-trapped}}$. Skilled artisans will appreciate that it is also possible to include effects relating to other physical parameters such as dielectric constant and grain size in order to control various aspects of the electrostatic chuck

performance.

In the foregoing specification, the present invention has been described with reference to specific embodiments thereof. It will, however, be evident to a skilled artisan that various modifications and changes can be made thereto
5 without departing from the broader spirit and scope of the present invention as set forth in the appended claims. For example, although a method of the present invention is described primarily in reference to the simulation of the electrical behavior of an electrostatic chuck, skilled artisans will appreciate that the present invention may also be practiced with an actual circuit, and that principles
10 embodied in the present invention may be beneficially applied to the design and operation of actual electrostatic chucks. For example, in a physical implementation of an electrostatic chuck using principles of the present invention, a movable electrode may be employed to apply a control bias to a substrate in place of a time-varying voltage source used in a simulation. The
15 specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method of using a circuit simulator to simulate an effect of trapped charge in an electrostatic chuck on the electrostatic chuck performance, the method comprising:
creating a trapped-charge electrical model by coupling a trapped charge capacitor to a gap-trapped resistor and to a grain resistor;
selecting a capacitance value C_{trapped} for the trapped charge capacitor;
selecting a resistance value $R_{\text{gap-trapped}}$ for the gap-trapped resistor;
selecting a resistance R_{grain} for the grain resistor;
creating an electrostatic chuck simulation circuit by coupling a substrate-to-chuck interface gap capacitor with a substrate-to-chuck interface gap capacitor, a substrate resistor, at least one cable resistor, and a plurality of voltage sources;
configuring at least one of the plurality of voltage sources to provide a time-varying voltage;
coupling the trapped-charge electrical model with the electrostatic chuck simulation circuit; and
executing a first simulation in the circuit simulator to determine time-varying voltage and currents responses within a plurality of circuit nodes in the electrostatic chuck simulation circuit.
2. The method of claim 1 wherein the step of creating a trapped-charge electrical model by coupling a trapped charge capacitor to a gap-trapped resistor, and to a grain resistor is performed by connecting a terminal of the gap-trapped resistor to a first terminal of the trapped-charge capacitor and by further connecting a terminal of the grain resistor to a second terminal of the trapped-charge capacitor.

3. The method of claim 1, further comprising:
optionally varying any of the capacitance value C_{trapped} , the resistance value $R_{\text{gap-trapped}}$, and the resistance value R_{grain} in relation to a plurality of electrostatic chuck physical parameters followed by executing a second simulation to determine changes in the time-varying voltage and current responses.

4. The method of claim 1, further comprising:
selecting a capacitance value C_{gap} for the substrate-to-chuck interface gap capacitor;
selecting a resistance value R_{gap} for the substrate-to-chuck interface gap capacitor;
selecting a resistance value R_{wafer} for the substrate resistor; and
selecting a resistance value R_{cable} for at least one cable resistor.

5. The method of claim 1, further comprising:
configuring one of the plurality of voltage sources to provide a bias voltage simulating a plasma potential; and
connecting a sheath resistor in series with the voltage source configured to provide a bias voltage simulating a plasma potential.

6. The method of claim 1, wherein the:
the step of selecting a capacitance value C_{trapped} uses a capacitance approximately equal to 50 nanoFarads;
the step of selecting a resistance $R_{\text{gap-trapped}}$ uses a resistance range from approximately 100 Megohms to 500 Megohms; and
the step of selecting a resistance R_{grain} uses a resistance range from approximately zero to 200 Megohms.

7. The method of claim 1 further comprising:
 adding a plurality of resistors and capacitors to the electrostatic chuck simulation circuit;
 selecting a capacitance value C_{gap} for at least one added capacitor;
 selecting a resistance value R_{gap} for at least one added resistor;
 selecting a resistance value R_{wafer} for at least another added resistor; and
 configuring the plurality of added resistors and capacitors so as to simulate an electrostatic chuck without trapped charge.

8. A circuit to measure an effect of trapped charge in an electrostatic chuck system on the chuck performance, the circuit comprising:
 an electrostatic chuck circuit portion comprising:
 - a substrate-to-chuck interface gap capacitance C_{gap} coupled to a substrate-to-chuck interface gap resistance R_{gap} , a substrate resistance R_{wafer} , at least one cable resistance R_{cable} , and a trapped-charge circuit portion having a capacitance C_{trapped} , a resistance $R_{\text{gap-trapped}}$, and a resistance R_{grain} ; and
 a plurality of voltage sources, at least one of the plurality of voltage sources being capable of varying a voltage output as a function of time, the plurality of voltage sources coupled to the electrostatic chuck circuit portion.

9. The circuit of claim 8, wherein the trapped charge circuit portion further comprises a first terminal of the capacitance C_{trapped} connected to a terminal of the resistance $R_{\text{gap-trapped}}$ and a second terminal of the capacitance C_{trapped} connected to a terminal of the resistance R_{grain} .

10. The circuit of claim 8 wherein the trapped-charge circuit portion comprises an electrostatic chuck.

11. The system of claim 8, wherein the electrostatic chuck circuit portion is comprised of a substrate placed on an electrostatic chuck.
12. The system of claim 8, wherein at least one of the plurality of voltage sources is further coupled to an electrical filter for isolating a voltage source from radio frequency (RF) energy.
13. A method of designing an electrostatic chuck, the method comprising:
building in a circuit simulator a circuit model for the electrical behavior of the electrostatic chuck using an RC trapped-charge model;
coupling the circuit model to a plurality of voltage sources;
simulating the circuit model with the circuit simulator to determine voltage potentials at a plurality of circuit nodes and further to determine currents within a plurality of circuit components;
varying the circuit model in relation to changes in physical parameters of the electrostatic chuck; and
simulating the circuit with the circuit simulator to determine changes produced by varying the circuit model.
14. The method of claim 13 wherein the step of using an RC trapped-charge model is performed by connecting a resistor $R_{\text{gap-trapped}}$, a capacitor C_{trapped} , and a resistor R_{grain} , in a series configuration.
15. The method of claim 13 wherein the step of varying the circuit model in relation to changes in physical parameters of the electrostatic chuck is performed by varying a gap-trapped resistance.

16. A system for controlling an electrostatic chuck comprising:
voltage-controlled voltage source means for providing a time-varying bias to the
electrostatic chuck in proportion to a time-varying controlling voltage,
the time-varying bias for controlling a substrate to chuck adhesion
according to simulation results from a charge-trapped circuit model;
time-varying voltage means for providing the time-varying controlling voltage;
dc bias means for applying a dc bias to the electrostatic chuck; and
cable means coupling the electrostatic chuck, the voltage-controlled voltage
source means, the time-varying voltage source means, and the dc bias
means.

17. The system of claim 16, further comprising:
filter means for isolating any of the voltage-controlled voltage source means, the
time-varying voltage source means, and the dc bias means, from radio
frequency energy coupled to the electrostatic chuck; and
additional cable means coupling the filter means to the voltage source means.

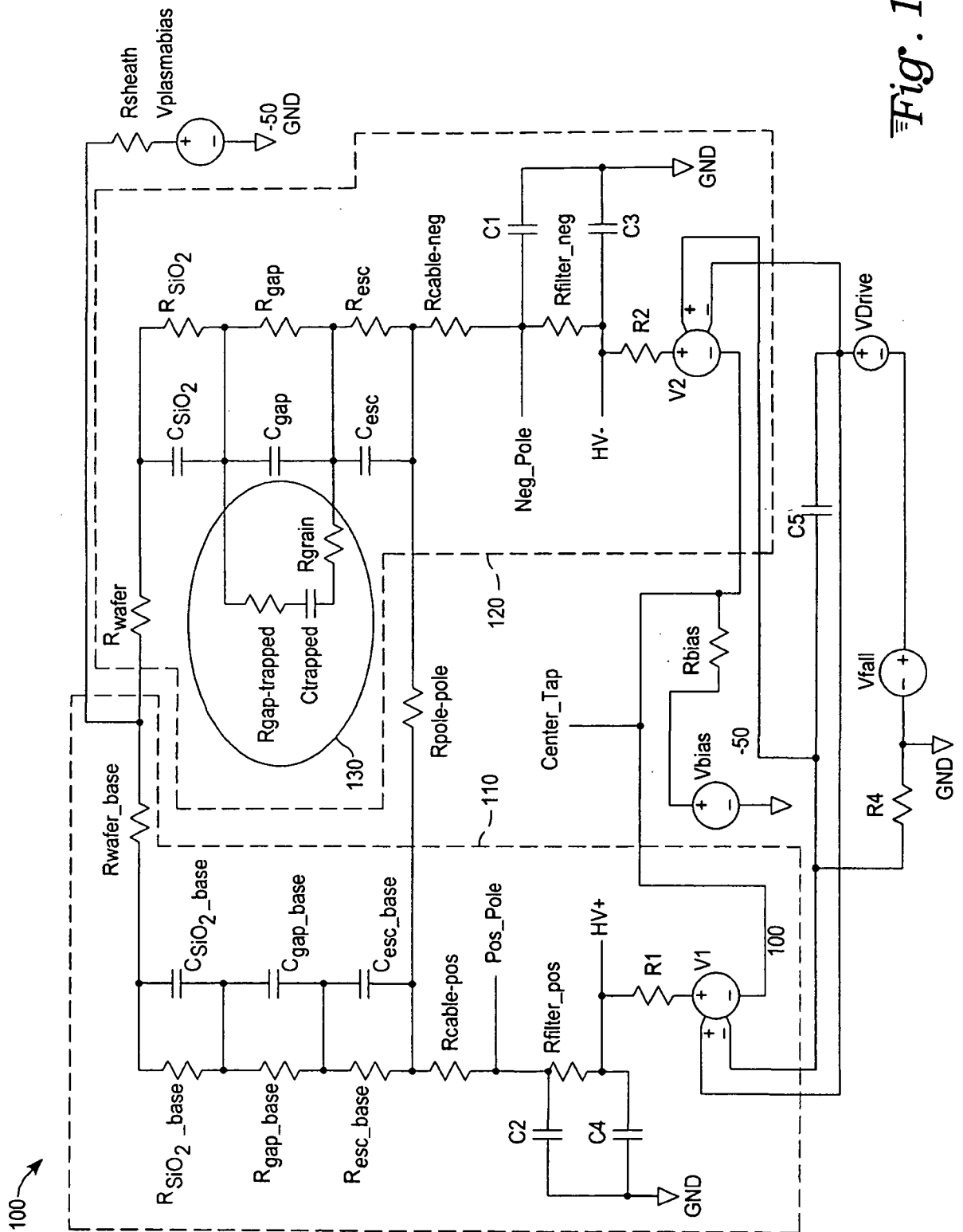


Fig. 1

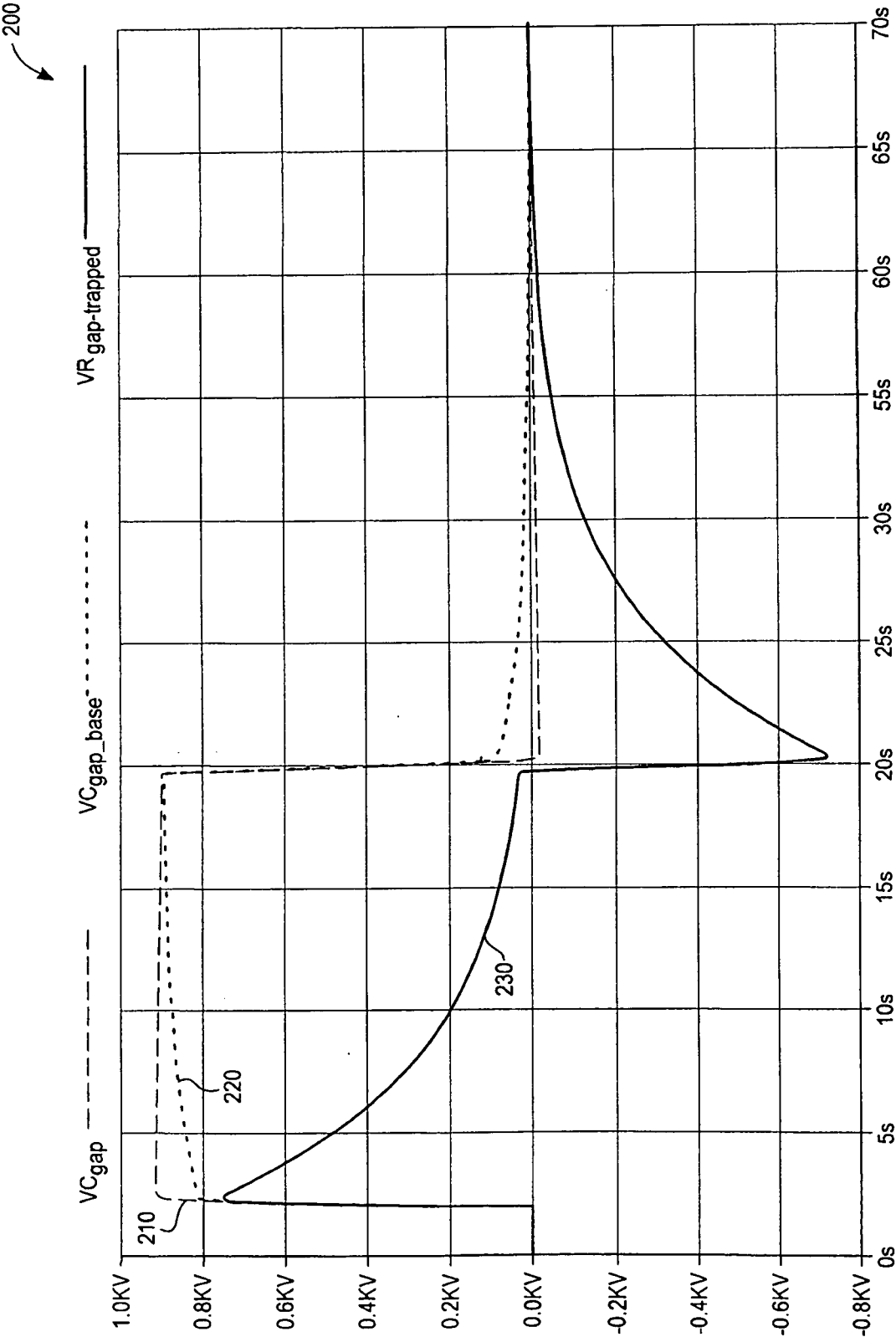


Fig. 2

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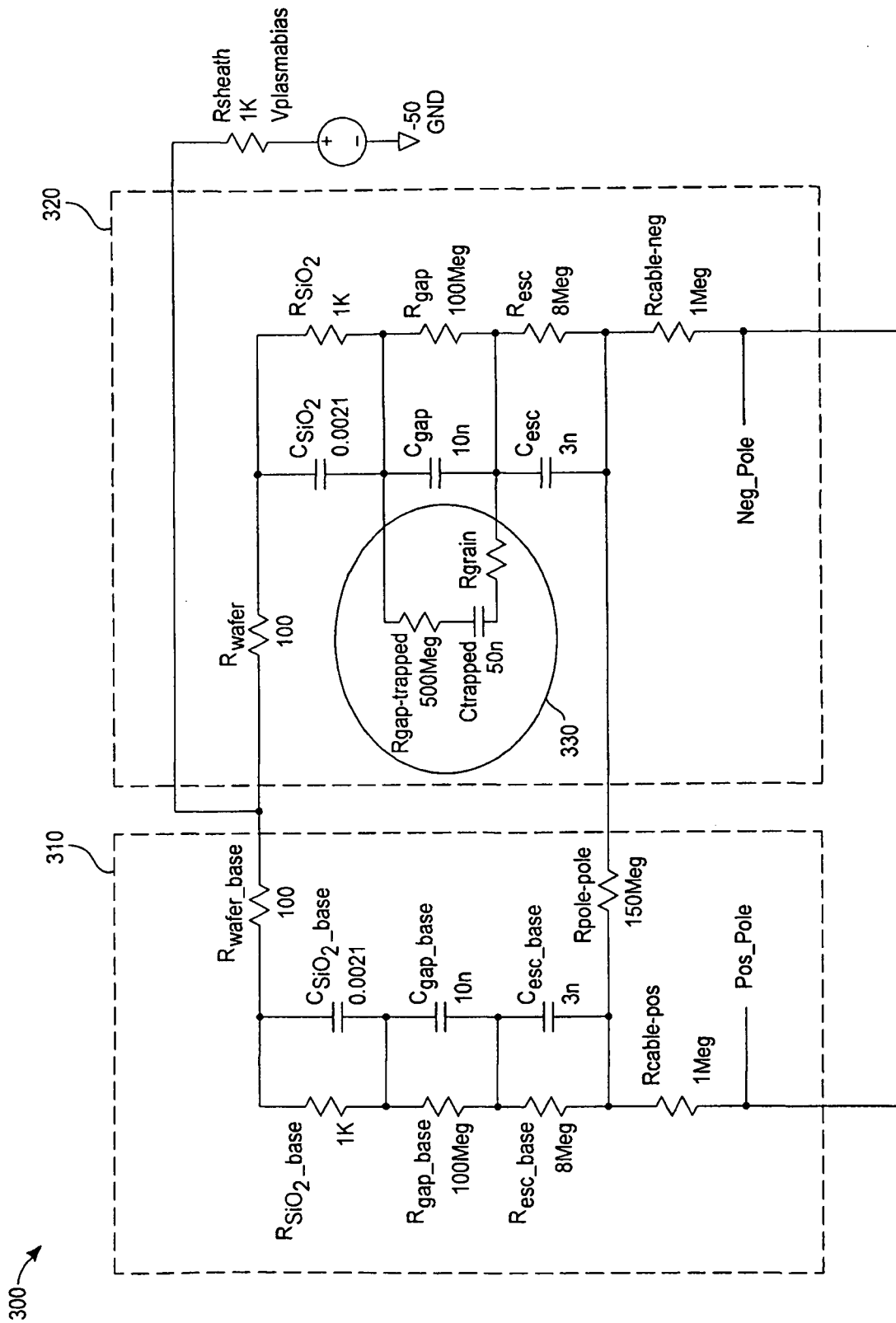


Fig. 3

400

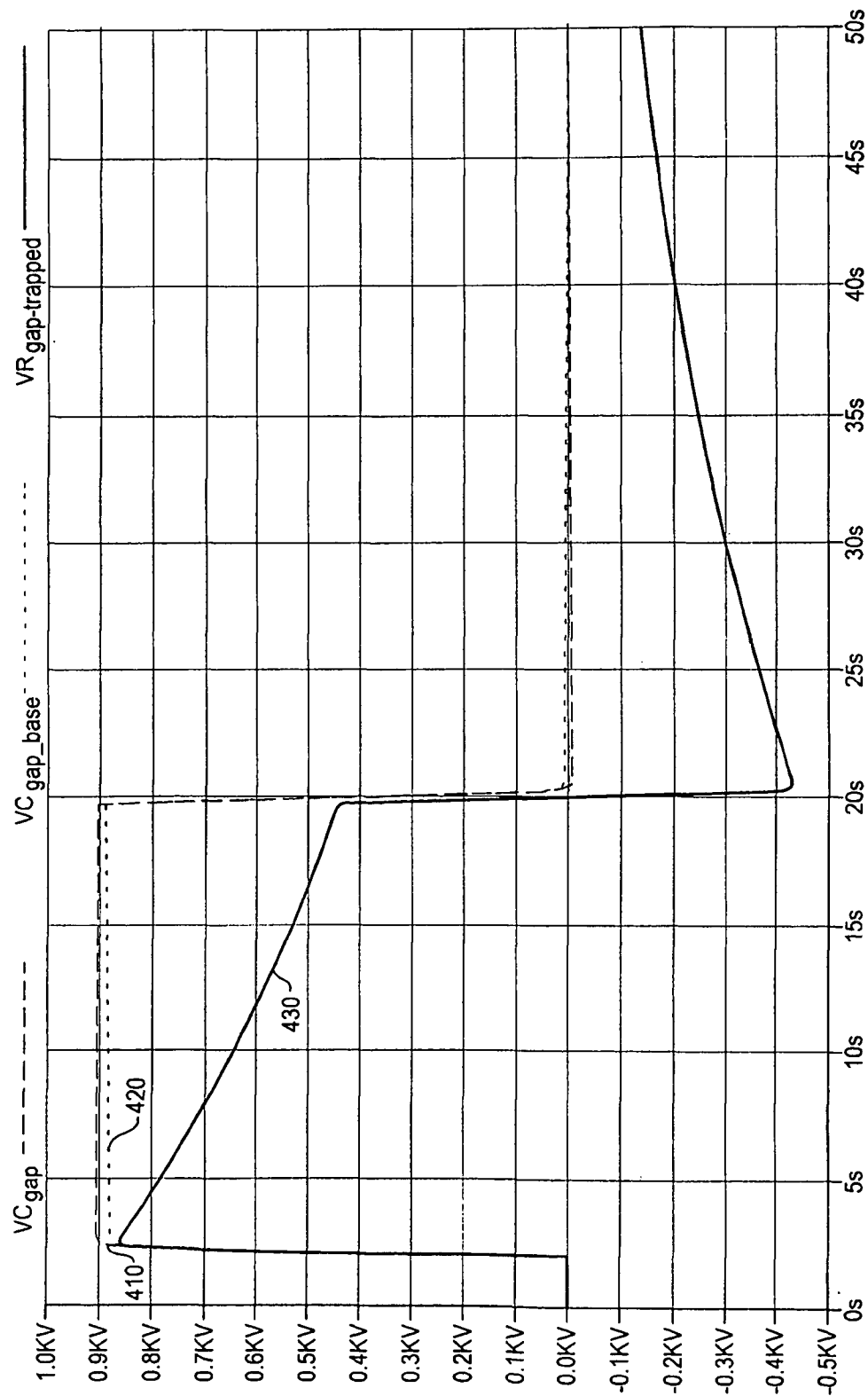


Fig. 4