United States Patent

[11] 3,577,087

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[45] Patented **May 4, 1971**
[73] Assignee **Radio Corporation of America**

[54] **SEQUENCE "AND" GATE WITH RESETTING MEANS**
6 Claims, 2 Drawing Figs.

[52] **U.S. Cl.** **328/110,** 179/1, 307/232, 307/234, 307/246, 328/119
[51] **Int. Cl.** **H03k 5/20**
[50] **Field of Search** ..... 307/201, 208, 217, 218, 219, 231, 232, 234, 238, 246, 269, 293; 328/109, 110, 119, 99, 151; 179/1 (AS)

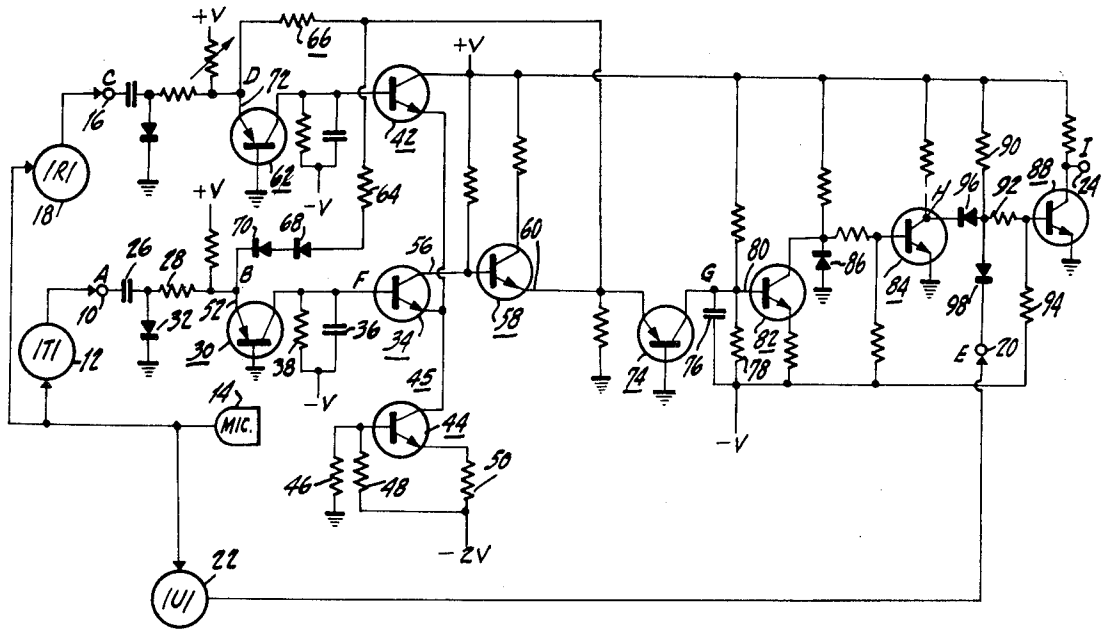
[56] **References Cited**

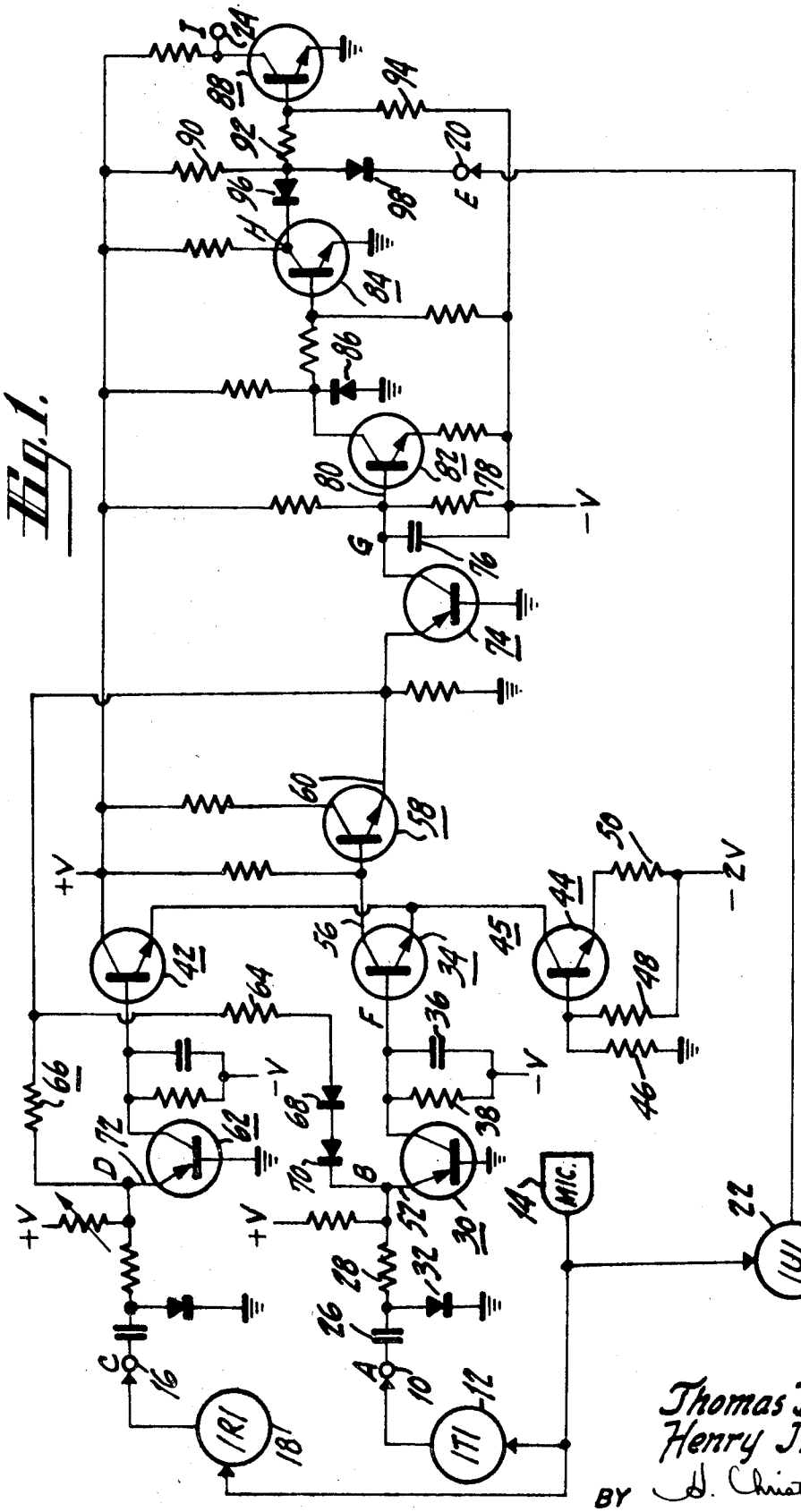
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ABSTRACT: Circuit for otting means two signals and producing an output when the signals are in sequence, with resetting means to inhibit the output after a specific time interval has elapsed between the two signals or whenever an intervening other signal occurs.



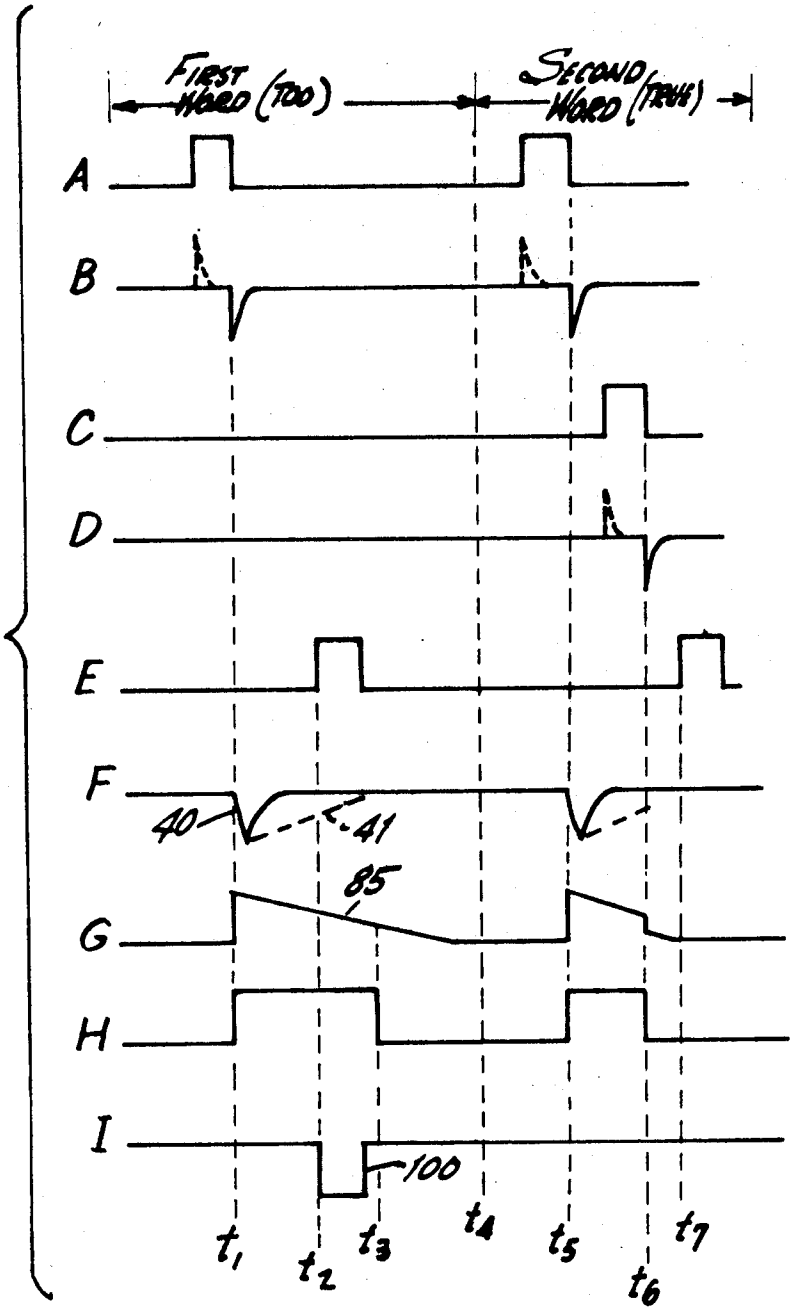


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Fig. 2.



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SEQUENCE "AND" GATE WITH RESETTING MEANS

BACKGROUND OF THE INVENTION

This invention relates to circuits for detecting two sequential events that occur within a given time interval and without another event between them. For example, in speech recognition circuits of the type deriving phonemes from input speech, the phonemes constituting a given word must be detected in a specific sequence for each word of the machine's vocabulary. In a machine with a vocabulary word TOO (TO or TWO), the two sequential phonemes to be recognized are /T/ and /U/. The circuit must not recognize the word TRUE as TOO because of the undesired intervening phoneme /R/. Furthermore, a word ending with the phoneme /T/ followed by a word beginning with the phoneme /U/ must not be recognized as TOO because of the pause or glottal stop between words.

It is an object of this invention to provide a simple sequential event detector which is reset by intervening undesired events or by an excessive time interval between the desired events.

BRIEF SUMMARY OF THE INVENTION

A circuit stores a charge when a first signal occurs. When a second signal occurs, an output is produced if the charge is being stored. The stored charge will be discharged by a third signal if it occurs prior to the time of the occurrence of the second signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic of the preferred embodiment of the invention.

FIG. **2** is a diagram illustrating the shapes of signals at various points in the schematic identified by upper case letters.

DETAILED DESCRIPTION OF THE INVENTION

The operation of the preferred embodiment of the invention shown in FIG. **1** will be explained in conjunction with the waveshape diagram of FIG. **2** and, for purposes of illustration, in terms of differentiating between the spoken words TOO and TRUE.

An enabling input **10** in FIG. **1** is connected to a source of signals indicative of a first desired event, e.g., a /T/ phoneme. A phoneme separator **12** will produce a positive square pulse whenever the input speech picked up by a microphone **14** contains a /T/ phoneme. A disabling input **16** will receive a positive square pulse from another phoneme separator **18** whenever the input speech contains an /R/ phoneme. A gating input **20** will receive a positive square pulse from the phoneme separator **22** whenever a /U/ phoneme occurs in the input speech. The output **24** produces a negative pulse whenever the spoken word TOO (including TO or TWO) occurs in the input speech.

FIG. **2**, line A, represents the signal to the enabling input **10**; FIG. **2**, line C, the signal to the disabling input **16**; and FIG. **2**, line E, the signal to the gating input **20**. The first word represented is TOO and the second is TRUE.

The signal applied to the input **10** is differentiated by a series RC circuit consisting of the capacitor **26** and the resistor **28** so that only trigger-shaped spikes tend to appear at the emitter **52** of the transistor **30**. The diode **32** suppresses the positive spikes so that only negative spikes actually appear at the emitter **52**. FIG. **2**, line B, illustrates the signal shape with the suppressed positive spikes shown by dotted lines. The transistor **30** is biased so the quiescent current maintains the base of the transistor **34** in the active region. The negative spike appearing at the emitter **52** acts to cutoff transistor **30** which reduces the current in transistor **34** causing the voltage at the collector **56** to rise toward +V. The negative spike also causes the capacitor **36** to discharge through the resistor **38**. The signal at the base of the transistor **34** (and collector of the transistor **30**) is shown in FIG. **2**, line F the slope of the negative-going edge **40** at time t_1 is determined by the RC constant of the resistor **38** and the capacitor **36** in FIG. **1**. After the emitter **52** returns to its quiescent voltage, the capacitor **36** begins to charge through the transistor **30**. The RC time constant for this charging rate is determined by the output impedance of the transistor **30** in combination with the resistor **38** and the value of the capacitor **36**. Because of feedback from the emitter **60** of the transistor **58** which is covered in more detail below, the effect of the signal at the base of the transistor **34** is the waveshape depicted by the dotted line **41** in FIG. **2**, line F.

The transistors **34** and **42** form a difference amplifier. The transistor **44** and its biasing resistors **46**, **48** and **50**, constitute a constant current source **45** for the transistors **34** and **42**.

The voltage at the collector **56** rises toward +V as described above and increases the current through the transistor **58**, causing the emitter **60** voltage to rise toward +V. This positive increase at the emitter **60** furnishes feedback current to the transistors **30** and **62** through the resistors **64** and **66**, respectively. The amount of feedback to the transistor **62** is initially greater than that to the transistor **30** because of the diodes **68** and **70** in series with the resistor **64**. In order for the feedback current to reach the emitter **52**, the voltage of the feedback must increase sufficiently to forward-bias the diodes **68** and **70**. The feedback current reaching the emitter **72** causes the current through the transistor **62** to increase and consequently, the current through the transistor **42** to increase. Because the total current through both transistors **34** and **42** is a fixed value determined by the constant current source **45**, an increase of current through the transistor **42** results in a decrease of current through the transistor **34** which in turn causes the collector **56** voltage to rise more toward +V. The feedback from the emitter **60** to the emitters **52** and **72** is, therefore, regenerative until the combines threshold voltages of the diodes **68** and **70** are exceeded. Thereafter, the effect of the feedback is cancelled because any tendency to increase current in either transistor **34** or **42** is countered by an equal tendency in the other. As a result, the feedback loop causes a sharp rise in the voltage in the emitter **60** for a small input signal.

The increase of voltage at the emitter **60** increases the current through the transistor **74**, which in turn increases the voltage across the capacitor **76** and at the base **80** of the transistor **82**. The capacitor **76** provides additional holding in the circuit at the base **80**. FIG. **2**, line G, shows the voltage waveshape across the capacitor **76**. The negative-going edge **85** has a time constant that is dependent both on the RC value of the capacitor **76** and the resistor **78** and on the signal waveshape at the emitter **60** of the transistor **58**. The positive-going edge of the waveshape shown in FIG. **2**, line G, at t_1 and t_5 is fast rising because of the regenerative feedback from the emitter **60**.

The signal at the base **80** of the transistor **82** is amplified by two stages consisting of the transistors **82** and **84** and their biasing resistors. The collector of the transistor **82** is clamped to ground by the diode **86**. The amplification of the signal by the transistor **82** si sufficient either to saturate or to cut off the transistor **84** between the highest and lowest voltages, respectively, at the collector of the transistor **82**. The output of the transistor **84** is a step function as shown in FIG. **2**, line H.

In the first word, TOO, and output from the phoneme separator **22** follows the output from the phoneme separator **12** and is applied to the gating input **20**. The transistor **88**, the biasing resistors **90**, **92** and **94**, and the input diodes **96** and **98** form a logical NAND gate that produces an approximately zero output voltage at the output **24** whenever positive signals of nearly +V volts are applied to both input diodes **96** and **98** simultaneously and an output voltage approaching +V whenever a signal of approximately zero volts is applied to either diode **96** or **98**. The input to the diode **96** is shown in FIG. **2**, line H, and the input to diode **98** is shown in FIG. **2**, line E, which is the output of the phoneme separator **22** applied to the gating input **20**. FIG. **2**, line I, illustrates the voltage waveshape of the output **24**. The negative square pulse **100** beginning at time t_2 indicates that the word TOO (TO or TWO) occurred in the input speech to the microphone **14**.

The negative-going edge 85 of the signal depicted in FIG. 2, line G, decreases in time to a value less than that required to keep the transistor 84 cutoff, at which point, time t_3, the transistor 84 is turned on causing the input signal to the diode 96 to approach ground thereby inhibiting a signal at the output 24 if a positive signal to the gating input 20 subsequently occurs. This time-dependence prevents recognition of widely spaced /T/ and /U/ phonemes as a single word.

In the second word, beginning at time t_4 on FIG. 2, the /R/ phoneme follows the /T/ phoneme and precedes the /U/ phoneme. The following description will illustrate how an output is inhibited by the occurrence of the intervening /R/ phoneme.

The /T/ phoneme signal at the input 10 causes a cycle of operation that is identical to that described above, i.e., time t_5 of FIG. 2 corresponds to time t_1, until the occurrence of the negative edge of the /R/ phoneme pulse at the input 16 at time t_6. The waveshape at the emitter 72 of the transistor 62 caused by the input signal from the phoneme separator 18 is illustrated in FIG. 2, line *D*. The result is a circuit operation analogous to that described above for the signal occurring at the emitter 52 of the transistor 30. As the voltage at the base of the transistor 42 decreases, more current flows through the transistor 34 (because of the constant current source 45 as explained above) so that the collector 56 voltage is decreased. This, in turn, causes the voltage at the emitter 60 to approach ground, and a negative-going signal is fed back via the resistors 66 and 64. Because the feedback diodes 68 and 70 are forward-biased from action of the /T/ phoneme, the feedback from the emitter 60 is applied equally to the emitters of the transistors 30 and 62. The voltage at the emitter 60 of the transistor 58 decreases because of the decrease in voltage at the collector 56 of the transistor 34. When the voltage at the emitter 60 has decreased to the point where the diodes 68 and 70 are no longer forward-biased, the feedback from the emitter 60 becomes regenerative because it no longer affects the transistor 30, thereby causing a sharp drop in the emitter 60 voltage and consequently that at the emitter of the transistor 74. The capacitor 76 discharges through the resistor 78 turning off the transistor 82 and turning on the transistor 84. The input to the diode 96 is close to ground, inhibiting an output from the transistor 88 when the phoneme separator 22 applies an input pulse at time t_7 to the gating input 20.

The use of several stages of amplification and biasing the leading stages in the active region permits use of the described circuit in applications where the input signals are small. It is apparent to those skilled in the art that the input signals need not be differentiated and the positive-going signals can be utilized to perform different timing functions. It is also apparent that with sufficiently large input signals, several of the stages shown in FIG. 1 can be eliminated.

We claim:

1. The combination comprising:

input means responsive to a first signal for storing a charge indicative of the occurrence of said first signal;

coincidence gating means responsive to a third signal and the charge being stored for producing an output isolated from said input means; and

means responsive to the occurrence of a second signal, prior to the third signal, for discharging said stored charge.

2. The combination as claimed in claim 1 including means for discharging said stored charge within a predetermined time interval after the occurrence of said first signal.

3. The combination comprising:

first charge storage means responsive to a first signal for storing a charge representing the occurrence of said first signal;

second charge storage means responsive to a second signal for storing a charge representing the occurrence of said second signal;

means responsive to said first and second charge storage means for producing an enabling signal whenever said first charge storage means is storing a charge and the second charge storage means is not; and

coincidence gating means responsive to a third signal and said enabling signal for producing an output.

4. The combination as claimed in claim 3 including means for discharging said stored charges in a predetermined interval of time.

5. The combination comprising:

first and second input stages, each having input means, output means, and charging means for maintaining an output signal for a predetermined time interval after removal of an input signal for the stage;

differencing means, having an output means and first and second input means, for producing an output according to the difference between the signals applied to said first and second input means thereof;

gating means, having first and second input means, for producing an output whenever signals are applied simultaneously to said first and second input means of said gating means;

means for coupling a first signal to the input means of said first input stage;

means for coupling a second signal to the input means of said second input stage;

means for coupling a third signal to the second input means of said gating means;

means coupling the output means of said first input stage to the first input means of said differencing means;

means coupling the output means of said second input stage to the first input means of said differencing means; and

means coupling the output means of said differencing means to the first input means of said gating means.

6. The combination as claimed in claim 5 including feedback means coupled between the output of the differencing means and the input means of said first and second input stages.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,577,087 Dated May 4, 1971

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It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Abstract, first line, delete "otting means" and inse therefor --- sensing ---.
Column 2, line 56, "si" should read --- is ---.
Column 3, line 9, after "time" insert --- t_4 ---.
Column 4, line 30, "for" should read --- from ---.

Signed and sealed this 15th day of February 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents