A semiconductor wafer and method for producing the same A semiconductor wafer (12) with a thinned central portion (2) has a first side (3) and a second side (4) and at least one reinforcement structure for increasing the radial bending resistance of the semiconductor wafer (12). The reinforcement structure provides at least one passage (10) for a fluid flow between an inner face (9) of said reinforcement structure towards an outer face (8) of the reinforcement structure.
Description

Title of Invention: Semiconductor wafer and method for producing same

[1] The present application relates to a semiconductor wafer with a reinforcing structure and to a method for producing said semiconductor wafer. One further aspect of the application relates to a chuck for holding said semiconductor wafer. This semiconductor wafer comprises a thinned central portion having a first side and a second side surrounded by at least one protruding edge portion.

[2] In a known semiconductor wafer, there is provided an annular rim. Said rim comprises a top face, a bottom face, an outer face and an inner face. A method of producing such a wafer with a thin central portion and an annular protruding rim is known from the document US 2008/0090505 A1. A thinned central portion is formed in an area of a rear surface of a standard wafer corresponding to a device formation area on the front side of a processed standard wafer. This thin central portion is performed by grinding with a grinding unit and the annular rim is concurrently formed around said thinned central portion. The annular rim shall increase the stability such that warping of such a thinned central portion of the wafer is avoided.

[3] The application provides a semiconductor wafer with a thinned central portion having a first side and a second side and at least one reinforcement structure for increasing the radial bending resistance of the semiconductor wafer. The reinforcement structure provides one or more passages for a fluid flow between an inner face of said one reinforcement structure towards an outer face of the reinforcement structure. The fluids can be gaseous or liquid.

[4] The reinforcement structures can be provided as elevated areas over the central portion while said passages can be slits which separate at least two elevated areas from each other. The slits can also be provided within the elevated areas.

[5] The slits can also be provided with a spatial orientation that includes a horizontal inclination angle $\sigma$ (sigma) between the slit and a horizontal direction of the wafer at the location of the respective slit. The slits can also be provided with a radial inclination angle $\phi$ (phi) between the slit and a radial direction of the wafer.

[6] It is preferred that a spatial orientation of at least one slit is provided such that there is no radial overlap of an inner orifice and a respective outer orifice of the slit. This increases the stability of the wafer.

[7] In a further example, the passage can be a ramp which is provided at the elevated area.

[8] The semiconductor wafer of the application will usually be a standard semiconductor
wafer with a thinned central portion which is a planar polished mirror-like front surface of the wafer and said first side comprises a plurality of integrated electronic circuits or semiconductor devices. The second side of said thinned central portion can be a recessed portion of a rear surface the wafer which also comprises a plurality of integrated electronic circuits or semiconductor devices, the first side and the second side having electrical interconnections through TSV holes.

The application also provides a chuck for holding a semiconductor wafer, the chuck comprising a circular base plate surrounded by a chuck rim having perforations, the perforations corresponding to at least one position of said passage of said wafer.

The chuck according can have a double ring structure with an inner ring and with an outer ring, wherein said rings are perforated and rotatable arranged to each other to variegate the cross section of a combined perforation size.

The application also provides a method with
1. providing a semiconductor wafer (40) comprising a front surface (11) and a rear surface (16); D
1. producing integrated electronic circuits (15) or semiconductor device structures at the front surface (11); D
1. providing at least one fluid (can be gas or liquid) passage (10) at a circumference on the front surface (11) extending radially at least from an outer face (8) of the wafer (40) towards an inner face (9) of said wafer (40); D
1. providing a recess at the rear surface (16) of the wafer (40) to provide a thinned central portion (2) having a first side (3) and a second side (4) surrounded by at least one reinforcement structure. D

The application provides a wafer on which it is easy to build a structured metallization on said second side of the thinned central portion. Any method step comprising rinsing, spraying, stripping or etching by liquids on the second side of said thinned central portion will not cause problems, since these liquids can easily be discharged from at the intersecting corner between said second side of said thinned central portion and said inner face of said rim. This accumulation of liquids makes correctly structured metallization layers possible and avoids contamination problems.

The present application also relates to a semiconductor wafer with a reinforcement structure and to a method for producing said semiconductor wafer. One further aspect of the application relates to a chuck for holding said semiconductor wafer.

This semiconductor wafer comprises a thinned central portion having a first side and a second side surrounded by at least one protruding edge portion. Said protruding edge portion comprises a top face, a bottom face, an outer face and an inner face. The protruding edge structure has a plurality of perforations extending radially at least from said inner face of said rim towards said outer face of said protruding edge structure,
wherein said top face of said protruding edge structure remains unperforated. An inclination angle of the perforation is applied between 0 and ± 60 degrees, between 0 and ± 20 degrees, preferably between 5 and ± 15 degrees off the radial direction.

Such a semiconductor wafer has the advantage that excess process liquids applied to the second surface of said thinned central portion of said semiconductor wafer can escape or bypass through said plurality of perforations extending radially from the inner face of said protruding edge structure towards its outer face. An accumulation of liquid in the intersection corner between the second surface of said thinned central portion and said inner face of said edge structure is decreased or even avoided and a better planarity of sprayed-on liquids is achieved. Further, contaminations can be avoided.

According to one embodiment of the application, a height of said perforations is larger than the thickness of said thinned central portion. With the increasing height of said perforations the bypassing and escaping of liquids through said perforations are increased.

In an further embodiment, the first side of said thinned central portion and said bottom face of said protruding edge structure provide a planar polished mirror-like front surface of a standard semiconductor wafer. This has the advantage that no intersecting corner between the central thinned portion and the protruding edge structure is present on the first side of said semiconductor wafer, so that standard semiconductor processes can be performed on the first side.

If the wafer provides a double sided recessed portion surrounded by the protruding edge structure, there will be not only an intersecting corner between the second side and the inner face of the protruding edge structure, but also an intersecting corner between the first side of the thinned central portion and said inner face of said protruding edge structure. In this case and in other cases, it is of advantage to provide perforations which are extending in an inclined form radially from said inner face towards said outer face, similar to the orientation of turbine blades in a turbine wheel.

In a further embodiment, said first side of said thinned central portion, which is equal to the front surface of a standard wafer, comprises a plurality of rectangular sections predetermined by notional dividing lines, wherein each section comprises an integrated electronic circuit or a semiconductor device structure. Said second side of the thinned central portion is provided by a recessed portion of a rear surface of a standard semiconductor wafer.

In a further embodiment, said second side of said thinned central portion comprises one metallization structure of a metallization layer. Such a metallization structure can have conducting lines and contact pads or even bumps for providing interconnections on the rear surface of semiconductor chips.
Furthermore, it is possible that said second side of said thinned central portion comprises a plurality of metallization structures comprising insulation layers between said metallization structures and comprising through contacts through said insulation layers. Such complex multilayer metallization structures are possible since excess process liquids can now bypass or escape through said perforated protruding edge structure of the semiconductor wafer.

Preferably said contact bumps comprise a seed layer portion and at least a plated body of a copper alloy coated by a gold or a silver alloy layer. To provide such complex contact bumps on the second side of said thinned central portion several different coating, spraying-on and spinning and rinsing process steps can be successfully processed since the wafer protruding edge structure of the rim comprises said perforations.

Furthermore, it is possible that the semiconductor wafer comprises on each side of a plurality of coordinated rectangular sections determined by dividing lines, wherein each coordinated section comprises an integrated electronic circuit or a semiconductor device structure. In this case, the process of creating integrated circuits has to be applied on both sides of the wafer in a very precise manner supported by alignment marks and wafer orientation marks provided at the wafer.

A further aspect of the invention is related to a chuck for holding a semiconductor wafer with a reinforcing annular wafer rim, wherein said wafer has a plurality of perforations extending radially at least from an inner face of said wafer towards an outer face of said wafer. A portion of said wafer rim remains unperforated. Said chuck comprises a circular base plate surrounded by a chuck rim having perforations. The base plate of the chuck fits to the semiconductor wafer, and said chuck rim circumferences said wafer. With such a chuck, a secure holding of semiconductor wafer with a thinned central portion is possible.

Furthermore, it is possible to align the perforations of the chuck rim to the perforations of the wafer edge, so that bypassing or escaping of process liquids is enabled. Therefore, the positions of said perforations of said chuck rim correspond to positions of said perforations of said wafer rim.

In a further embodiment of the chuck, the chuck rim has a double ring structure with an inner ring and an outer ring, wherein said rings are perforated and rotatable arranged to each other to vary the size of the cross section of a combined perforation. It is then possible to partially or fully close the perforations as well as to fully open the perforations to a maximum size with such a double ring rim of a chuck. If the maximum opening of the perforation is not enough to secure the bypassing or escaping of liquids it is possible to connect a vacuum container to the chuck rim of said chuck and to support an escaping or a bypassing of excess liquids through said perforations of
said wafer rim and said perforations of said chuck rim.

[27] One method for producing a semiconductor wafer with a reinforcement structure comprises the following steps. First, a standard semiconductor wafer is provided. Integrated electronic circuits or semiconductor device structures are produced in a plurality of predetermined rectangular sections in the front surface of the wafer. A plurality of perforations and protruding structures are provided. These perforations and protruding structures are positioned along a circumference of the wafer. These perforations extend radially between an outer face of a predetermined area of the wafer and an inner face of said area, whilst other areas of said wafer remain unperforated, providing protruding portions.

[28] For that purpose at last a recess is ground or etched into the rear surface of said standard wafer with prepared perforations along the circumference of said wafer. With this grinding step, a thinned central portion is provided, having a first side and a second side. This thinned central portion is then surrounded by a protruding annular edge portion. Which in turn can be provided with perforations so that protruding edge structures remain.

[29] One possible advantage of this method is that the perforation structure and the protruding portions are provided after the semiconductor processing steps.

[30] A further method for producing a semiconductor wafer with a reinforcement structure comprises the following steps. First a standard semiconductor wafer is provided. Then, a plurality of perforations and protrusions along a circumference of the wafer is provided. After that, a grinding or an etching of recesses into the surface is done. After that, integrated electronic circuits or semiconductor device structures can be provided on one or two sides of the wafer. These device structures are positioned in a plurality of predetermined rectangular sections.

[31] Said plurality of perforations can be in the form of slits, cut by a dicing saw blade which is inclined radially at least from said outer face of the wafer towards its inner face. A top face of said wafer can remain uncut. Cutting slits for providing perforations is very cost effective and not very complicated, but contaminations of the wafer surfaces during this cutting step might occur. Therefore it is an advantage to cut these slits after semiconductor processing steps are finished and before any thinning of a central portion of the wafer takes place.

[32] Such a cutting can be done such that the cutting depth for said slits is smaller than a thickness of said protruding structure and deeper than a thickness of said thinned central portion. The inclined radial cutting length for said slits can extend into said thinned central portion as minimal as possible if the cutting into said thinned central portion initiates micro cracks.

[33] A modified method to make said plurality of perforations and protrusions is an etch
process, which can be a dry etching process preferable by RIE-plasma etching (reactive ion etching). Nevertheless it is also possible to apply a wet etching process to build said plurality of perforations along the circumference of said wafer.

When such a wafer with a perforated protruding structure is provided, it is possible to perform a deposition of a metal or carbon seed layer for a metallization structure or a bump plating structure onto said second side of said thinned central portion. Such a seed layer of metal or carbon may be necessary if the plating structure shall be achieved by an electrochemical plating process. Said metal or carbon seed layer can then be structured to said metallization structure if it is also possible to plate it to said electrical bumps, by at least one of the steps of spray-on and spinning a photo-resist, of spraying-on developing liquids, of sprayed-on etch liquids, of rinsing-on cleaning liquids, of spraying-on stripping liquids, of plating or of coating by electrolytic liquids under bypassing or escaping of excess liquids through said plurality of perforations of said rim.

When said metal or carbon seed layer is structured and plated to said metallization structure and/or to said electrical bumps depositing of a thin metal or carbon seed layer to the second side of the thinned central portion by a sputter process is provided. A sprayed-on and spinning of a resist layer under escaping of excess resist through said perforations is performed. Then a drying the resist layer takes place. The dried layer is structured by exposition through a mask. Then the exposed resist layer is developed by spinning-on developing liquid under escaping of excess resist and excess developing liquid through said perforations.

After these steps, a rinsing of the structured resist layer by spraying-on a rinsing liquid is performed whilst rinsing liquid excess through said perforations. The developed resist structure is then hardened to a plating mask. During the plating process the uncoated resist free seed layer is performed to a metallization structure and/or to metallic bumps in an electrochemical bath by circulating the electrochemical liquid over the structured seed layer and bypassing said liquid through said perforations.

After plating a stripping off of the resist of said plating mask from the second side of the thinned central portion is performed by spraying-on a stripping liquid under escaping of excess stripping liquid and stripped resist through said perforations. Then the stripped structure is cleaned by a cleaning liquid under escaping of excess cleaning liquid through said perforations. Then follows a wet etching of remaining parts of the thin seed layer by spraying-on of an etch liquid under escaping of excess etch liquids through said perforations.

After wet etching, the etched structure rinsed by spraying-on a rinsing liquid under escaping of excess rinsing liquids through said perforations. Finally a cleaning of the
second side with bumps is performed by a cleaning liquid under escaping of excess cleaning liquids through said perforations and drying the semiconductor wafer. The results of these method steps are contact bumps positioned on the second side of the thinned central portion, which can be used to stack semiconductor chips one above the other in a very compact manner to form a block of stacked semiconductor devices or a block of stacked integrated circuits.

[39] A semiconductor wafer according to the application has a thinned central portion having a first side and a second side and at least one reinforcement structure for increasing the radial bending resistance of the semiconductor wafer, the reinforcement structure providing at least one passage for a fluid flow between an inner face of said one reinforcement structure towards an outer face of the reinforcement structure.

[40] The passages can be slits which are provided within the elevated areas, the slits being provided with a spatial orientation that includes a horizontal inclination angle $s$ (sigma) between the slit and a horizontal direction of the wafer at the location of the respective slit. The slits can also be provided with a spatial orientation that provides a radial inclination angle $j$ (phi) between the slit and a radial direction of the wafer at the location of the respective slit.

[41] Good bending resistance can be obtained when a spatial orientation of at least one slit is provided such that there is no radial overlap of an inner orifice and a respective outer orifice of the slit.

[42] Instead of a slit or in addition to the slit, said passage can comprise a ramp which is provided at the elevated area.

[43] The application provides also a chuck for holding such a semiconductor wafer, the chuck being adapted to the passage in the semiconductor wafer.

[44] The above and other objects, features and advantages of the present application and the manner of realising them will become more appearing and the application itself will best be understood from a study of the following description and appended claims with reference to the attached drawings showing some preferred embodiments of the application.

[45] Figure 1 shows a schematic front view of a modified semiconductor wafer with alignment marks;

[46] Figures 2 to 8 show schematic views illustrating a method for forming a wafer having a recessed and thinned central portion, an annular rim and circumferential perforations;

[47] Figure 2 shows a schematic cross sectional view of a standard semiconductor wafer;

[48] Figure 3 shows a schematic cross sectional view according to figure 2 after processing of semiconductor device structures;

[49] Figure 4 shows the cross sectional view of the wafer according to figure 3 after
sawing inclined radially extending slits into the circumference of the wafer;

Figure 5 shows a schematic front side view of the wafer according to figure 4;

Figure 6 shows the cross sectional view of figure 4 in an upside down position;

Figure 7 shows the cross sectional view of the wafer according to figure 6 after grinding a recess into the rear surface of the wafer;

Figure 8 shows a schematic back side view of the wafer according to figure 7;

Figure 9 shows a schematic cross sectional view of a grinding stone to grind a recessed central portion;

Figure 10 shows a schematic cross sectional view of a modified grinding stone;

Figure 11 shows a schematic perspective view of a perforated semiconductor wafer;

Figure 12 shows a schematic cross sectional view of the wafer according to figure li;

Figure 13 shows a schematic cross sectional view of the wafer according to figure 11 having a double recessed central portion with a surrounding rim;

Figure 14 shows a schematic back side view of a modified wafer;

Figure 15 shows a schematic back side view of a modified wafer;

Figure 16 shows a schematic back side view of a modified wafer;

Figure 17 shows a schematic back side view of a modified wafer;

Figure 18 shows a schematic cross sectional of the wafer view according to figure 7 after depositing a seed layer to the second side of the thinned central portion;

Figure 19 shows the schematic cross sectional view of the wafer according to figure 18 after depositing a resist layer to the seed layer;

Figure 20 shows the schematic cross sectional view of the wafer according to figure 19 after an exposition step and a development step for processing openings into the resist layer;

Figure 21 shows a schematic view of a plating process for bumps plated in said openings of said resist layer;

Figure 22 shows a schematic view of the wafer according to figure 21 after stripping-off a resist mask;

Figure 23 shows a schematic view of the wafer according to figure 21 after etching the seed layer;

Figure 24 shows a schematic cross sectional view with a multilayer structure on the second side of the thinned central portion of the wafer;

Figure 25 shows a front view of a wafer holding chuck;

Figure 26 shows a schematic cross sectional view of the wafer holding chuck according to figure 25;

Figure 27 shows a schematic cross sectional view of a wafer holding chuck with vacuum connections;
Figure 28 shows a schematic cross sectional view according to figure 27 with the chuck in an upside down position.

Figure 29 shows a schematic cross sectional view of a further semiconductor device structure;

Figure 30 shows a schematic bottom view of the semiconductor device structure of figure 29;

Figure 31 shows a schematic view of the semiconductor device structure of figures 29 and 30 along a cut line A-A;

Figure 32 shows a schematic view of the semiconductor device structure of figures 29 to 31 as seen from outside;

Figure 33 shows a schematic view of the semiconductor device structure of figures 7 and 8 as seen from outside;

Figure 34 shows a schematic bottom view of a further semiconductor device structure;

Figure 35 shows a schematic bottom view of a further semiconductor device structure;

Figure 36 shows a schematic view of the semiconductor device structure of figure 35 as seen from outside;

Figure 37 shows a schematic top view of a further semiconductor device structure;

Figure 38 shows a schematic top view of a further semiconductor device structure which is similar to the semiconductor device structure of Figure 10;

Figure 39 shows a schematic cross sectional view of the semiconductor device structure of figure 38;

Figure 40 shows a schematic top view of a further semiconductor device structure;

Figure 41 shows a schematic top view of a further semiconductor device structure;

Figure 42 shows a schematic view of the semiconductor device structures of figures 37 and 40 along a cut line A-A, respectively;

Figure 43 shows a schematic view of a further semiconductor device structure as seen from outside;

Figure 44 shows a schematic view of a further semiconductor device structure as seen from outside; and

Figure 45 shows a schematic cross sectional view of a further semiconductor device structure.

Figure 1 shows a schematic front view of a modified semiconductor wafer 12 with orientation marks 33 instead of a standard orientation line 38. The orientation marks 33 relate to the crystal orientation of the mono crystalline silicon wafer 12 and are very small marks compared to said orientation line 38 of a conventional semiconductor wafer. These small orientation marks 33 can be cut or etched into a predetermined area.
on the circumference of said wafer 12. Furthermore, figure 1 shows an alignment mark 34 to ease the adjustment of said wafer 12 to a wafer chuck. Most recently, orientation marks are omitted and simply replaced by an alignment notch, since wafers with diameters above 200 mm are delivered with just one standard <100> crystal orientation.

[92] In the center of the wafer 12, its virtual symmetry axis 63 is provided in Figure 1.

[93] Figures 2 to 8 show schematic views illustrating one of the several possible methods for forming a wafer having reinforcement structures of segments with perforations between them and with a recessed thinned central portion.

[94] Figure 2 shows a cross sectional view of a standard silicon semiconductor wafer 40 having a thickness D in the range of 600 to 700 µm (micrometer) and a radius r of about 50 to 150 mm (millimeter). Furthermore, this standard silicon semiconductor wafer comprises a polished mirror-like front surface 11 and a ground rear surface 16. Said polished mirror-like front surface 11 is provided to introduce structures of integrated circuits or structures of semiconductor devices by known processes of the semiconductor technology.

[95] Figure 3 shows the cross sectional view according to figure 2 after processing of semiconductor device structures or said integrated circuits 15 onto the polished mirror-like front surface 11 of the standard semiconductor wafer 40. The dashed lines are virtual dividing lines 14 of a dicing saw, which later divides said semiconductor wafer 40 into semiconductor chips of integrated circuits 15 or into semiconductor chips of semiconductor devices. For connecting the front face and the rear face of a semiconductor chip with integrated circuits by electrically conducting vias at a later time, it is possible to etch blind holes into the polished surface before grinding is performed. These holes can be plated with conducting layers. After grinding and thinning of said wafer, the vias can be connected to a conducting structure which is later provided at the rear side of said wafer (not shown here).

[96] Figure 4 shows the cross sectional view of the wafer 40 according to figure 3 after sawing radially extending slits 31 into the circumference of the wafer. This cutting step will end up with a modified semiconductor wafer 12 as shown in figure 5. The slits 31 are sawn by a dicing saw blade 32, which is moved in the direction of arrow A and simultaneously in the direction of arrow B. The sawing length 1 is limited by the area of integrated circuits 15 and the cutting depths c in the direction B is limited by the thickness D of the semiconductor wafer and the condition, that a predetermined rim shall be provided with an unperforated top face. Instead of a cutting step an etching step is alternatively possible, to provide a perforated rim. Further it is preferred to apply an etch step after sawing for stress release and minimisation of crystal defects.

[97] In an embodiment which is not shown here, an inclination angle Ψ is applied
between 0 and ± 20 degrees, preferably between 10 and ± 15 degrees, off the radial
direction. The inclining angle Ψ is illustrated in the lower right part of the wafer with
an inclined slots drawn with a dotted line in Figure 5.

Figure 5 shows a schematic front side view of the wafer 12 according to figure 4
after finishing the perforation cuts to the circumference of the wafer 12. The pitch
between two perforation cuts or slits 31 is governed by an angle α of 11.75° (Degree)
in this embodiment, which results in 32 cuts of equidistant perforations 10 around the
front surface 11 of the wafer 12. The active area of this wafer 12 provides virtual
rectangular sections 13 surrounded by virtual dividing lines 14 for a dicing saw blade.
In this embodiment, an integrated circuit 15 is arranged in each rectangular section.

Figure 6 shows the cross sectional view of the wafer 12 according to figure 4 in an
upside down position. The front surface 11 is now in a down position, comprising said
integrated circuits 15, whilst the ground rear surface of the wafer is now in an upside
position, so that a grinding stone can be applied to this rear surface 16 to produce a
thinned central portion at the backside of the integrated circuits 15.

Figure 7 shows the cross sectional view of the wafer 12 according to figure 6 after
grinding a recess into the rear surface 16 of the wafer 12. A recessed central thinned
portion 2 can be produced by said grinding with a first side 3 comprising the integrated
circuit 15 and a second side 4, which forms the backside of said integrated circuits 15.
An annular rim 1 will be produced by grinding such a recess, wherein the rim provides
a top face 6, which is part of the original rear surface 16 of the wafer. Further, the rim
1 has a bottom face 7, which is in this embodiment coplanar with the front surface 11
of the wafer. Further, said rim has an outer face 8, which is identical with the outer cir-
cumference area of the wafer. An inner face 9 is produced during the grinding of said
recessed thinned central portion 2 of the wafer 12. Openings of perforations 10 are
processed with grinding the inner face 9 in the range of the slits 31. These perforations
10 allow a bypassing and an escaping of processing liquids during the preparation of
the back side of the different integrated circuits 15 or semiconductor device structures.

Figure 8 shows a schematic back side view of the wafer according to figure 7. The
rim 1 surrounds said thinned central portion 2, which is shown with its second side 4,
so that the integrated circuits 15 are shown with dashed lines. Since the top face 6 of
the rim 1 providing an annular edge portion 5 is unperforated, the perforations 10 are
only shown by inclined radial extending dashed lines. The orientation marks 33 and the
adjustment mark 34 are smaller than the width w of the rim 1, so that a top face 6 of
the rim 1 is not disturbed.

Figure 9 shows a schematic cross sectional view of a grinding stone 41 to grind a
recessed thinned central portion 2. This grinding stone 41 is fixed to a rotatable
grinding stone holder 42. This grinding stone holder 42 is moved in the direction of
arrow C to grind into the rear surface 16 of the wafer 12 said thinned central portion 2 with a second side 4 and an intersection between said section side 4 and said inner face 9 of said rim 1. Since the grinding stone 41 has a grinding angle $\alpha$ of 90°, the intersection between the second surface 4 and the inner face 9 of the rim 1 is also rectangular. This causes the above mentioned agglomeration of process liquids and contaminations unless perforations can be provided by a dicing saw blade which contour is marked by a dashed line.

[103] Figure 10 shows a schematic cross sectional view of a modified grinding stone 41 providing a smooth intersection between the second surface 4 of the thinned central portion 2 and the inner surface 9 of the rim 1 produced by an grinding angle $\alpha$ of 45° in this example. Though this smooth intersection decreases the problem of agglomeration of process liquids as well as the agglomeration of contaminations, the area for the rim of such a smooth intersection has to be larger and the area for integrated circuits will be smaller than by an abrupt intersection like in figure 9. Therefore it is reasonable to provide the rim 1 with a sufficient number and a sufficient size of perforations around the circumference of the wafer 12.

[104] Figure 11 shows a schematic prospective view of a perforated semiconductor wafer 12. Again the thinned central portion 2 is surrounded by a rim 1, which has an unperforated top face 6 and an outer face 8 as well as an inner face 9, which shows the perforations 10. At the outer face 8 of the rim 1 orientation marks 33 and an adjustment mark 34 are positioned without disturbing the top face 6 of the rim 1.

[105] Figure 12 shows a schematic cross sectional view of the wafer according to figure 11. In this case the wafer 12 has only one recessed portion to build said thinned central portion 2, whilst in the next figure a modification of this thinned central portion is shown.

[106] Figure 13 shows a schematic cross sectional view of a double recessed central portion 29 of a wafer 12. In this case a grinding and/or an etching of recesses is provided into the rear surface 16 of the wafer 12 and into the front surface 11 of the wafer 12. This double recessed thinned central portion 29 has a first side 3 and a second side 4 surrounded by a protruding annular edge portion 5 to provide an annular rim 1. In this embodiment a semiconductor processing can be performed on both sides 3 and 4 after the grinding process is finished.

[107] Figures 14 to 17 show schematic back side views of modified wafers comprising different orientation mark and/or adjustment mark arrangements. The wafer 12 of Figure 14 has an orientation line 38 providing a very small width W compared to the width of an orientation line of a standard semiconductor wafer. This small width should be small enough to gain a continuous unperforated top face 6 of the rim 1. The perforations 10 in this embodiment have a pitch angle of just 10°, so that 36 per-
forations 10 are positioned on the annular rim 1.

Figures 15 shows a schematic back side view of modified wafer 12, which comprises the orientation marks and the alignment mark shown in figure 1. The alignment marks provide only small cuts into the annular rim 1. Therefore the width W from a left side orientation mark 33 to a right side orientation mark 33 can be wider than in Figure 14.

Figures 16 shows a schematic back side view of modified wafer 12, which provides buried orientation and alignment marks 33 and 34. These marks do not disturb the unperforated top face 6 of the wafer rim 1.

Figure 17 shows a schematic back side view of a modified wafer 12. The orientation and the alignment marks are achieved by varying the pitch angle of some perforations 10, so that a chuck with corresponding feather keys can be adjusted to said wafer.

The next figures 18 to 24 show some steps to form a structured metallization on the second side 4 of said thinned central portion 2 of a wafer 12.

Figure 18 shows a schematic cross sectional view according to figure 7 after depositing a seed layer 21 onto the second side 4 of the thinned central portion 2. This seed layer 21 of a thickness of several nanometers increase the conductivity of the second side 4 of the thinned central portion 2 and provides an electrical contact for an electrochemical plating of metallization structures or bumps to the second side 4 of the thinned central portion 2. This seed layer 21 can be sputtered-on to the second surface 4 or can be deposited by a metal or carbon deposition process.

Figure 19 shows the schematic cross sectional view according to figure 18 after depositing a resist layer 35 to the seed layer 21. This resist layer has to be structured to form a plating mask before creating bumps or metallization structures on the seed layer by plating.

Figure 20 shows the schematic cross sectional view according to figure 19 after an exposition step and a development step for openings 43 of the resist layer. With the development step a developing liquid is sprayed-on in the arrow direction F onto the resist layer 4 in the thinned central portion 2 of the wafer 12 and the excess developing liquid can bypass or escape through said perforations 10 of the rim 1 of the wafer 12.

Figure 21 shows a schematic view of a plating unit for bumps to the second side 4 of the thinned central portion 2 of the wafer 12. This plating unit has a spraying nozzle 44 with a perforated copper plate 45. This copper plate 45 is connected to the positive potential of a direct current source and an electrochemical liquid is sprayed-on through said perforated copper plate 45 in the direction of arrow G and forms a liquid film 46 as an electrochemical bath 37 on the second surface 4 of the thinned central portion 2 of the wafer 12.

The wafer 12 is positioned inside a container 47. The outer face 8 of the rim 1 fits to the inner face 48 of the container 47, which is connected to the negative potential of
the direct current source. The wafer 12 is positioned at the bottom of the container 47 and a conductive seal 49 is liquid tight contacting the second side 3 of the wafer 12, so that copper ions can decorate and plate the free portions of the seed layer 21 through said openings 43 of said resist layer 35, which acts as a plating mask 36. The excess liquid of the electrochemical bath 37 can bypass and escape through the perforation 10 of the wafer 12 and through openings 50 of the container 47. If the container 47 is rotated with the wafer 12 the excess processing liquid can escape supported by centrifugal force in the direction of arrows H.

[117] Figure 22 shows a schematic view of the wafer 12 according to figure 21 after stripping-off the resist. For stripping-off the resist a stripping liquid is sprayed-on to the second side 4 of the thinned central portion and can escape through the perforation 10 of the wafer 12. The plated bumps 20 are then shown on the seed layer 21 of the second side 4 of the thinned central portion 2 of the wafer 12. To avoid a short circuit by the remaining seed layer 21, the seed layer has to be etched by an etch liquid.

[118] Figure 23 shows a schematic cross sectional view of the wafer 12 according to figure 21 after etching the seed layer. During this etching the etch liquid can escape or bypass through the perforations 10 of the wafer 12 and after etching a rinsing is necessary, so that a sprayed-on rinsing liquid also bypasses and escapes through these perforations 10.

[119] Figure 24 shows a schematic cross sectional view of the wafer 12 with a multilayer structure 51 on the second side 4 of the thinned central portion 2 of the wafer 12. This multilayer structure 51 can have a plurality of metallization layers 17 with conducting lines and with insulation layers 18 between said metallization layers 17. It is also possible, that on top of this multilayer structure 51 bumps 20 are positioned with through contacts 52 through the different insulation layers 18 toward the metallization layers 17. The formation of said multilayer structures 51 requires a lot of spraying-on of processing liquids, which now can be bypassed or escape through the perforated rim 1 of wafer 12.

[120] Figure 25 shows a front view of a wafer holding chuck 22. The wafer holding chuck 22 is able to support and hold a semiconductor wafer 12 as shown in figure 22 with a reinforcing annular wafer rim 1, wherein said wafer rim 1 has a plurality of perforations 10 extending radially at least from an inner face 9 of said rim 1 towards an outer face 8 of said rim 1. A top face 6 of said wafer rim 1 remains unperforated. Said chuck 22 comprises a circular base plate to support the semiconductor wafer 12 surrounded by said chuck rim 30 having perforations 24. The base plate of the chuck 22 fits to the semiconductor wafer and said chuck rim 30 circumferences said wafer rim 1.

[121] The embodiment of the chuck 22 according to figure 25 shows, that the chuck 22
provides a chuck rim 30 comprising a double ring structure with an inner ring 26 and
an outer ring 27, wherein said rings 26 and 27 are perforated and rotatable arranged to
each other to variegate the cross section of a combined perforation size. With a handle
53 the rings 26 and 27 can be moved in a close direction C or in an open direction O up
to an maximum opening of the perforations 24. Process liquids can therefore bypass or
escape through the perforation 10 of the wafer rim 1 and the perforations of the rings
26 and 27 of the chuck rim 30 in a direction of arrows K.

Figure 26 shows a schematic cross sectional view of the wafer holding chuck 22
according to figure 25. On the right hand side of the figure 26 the handle 53 is shown,
which cooperates with a gear 54. The gear 54 has a gear wheel 56 connected to said
handle 53. The gear wheel 56 has a small tooth number. The gear wheel 56 matches
with a toothed portion of the base plate 23. The bearings of the shaft 55 of the gear
wheel 56 are arranged to the outer ring 27 of the chuck rim 30, so that by moving the
handle 53 said variegating of a combined crossed section size of the perforations 24 of
the chuck rim 30 is possible.

Figure 27 shows a schematic cross sectional view of a wafer holding chuck 22 with a
vacuum connection 57. This vacuum connection 57 supports the bypassing and
escaping of processing liquids L form the second side 4 of the thinned central portion 2
of the wafer 12 through the perforations 10 at the wafer rim 1 and through the per-
forations 24 of the chuck rings 26 and 27. This vacuum connection 57 sucks the
processing liquids towards a vacuum container 28, where the processing liquids can be
collected and recycled.

Figure 28 shows a schematic cross sectional view according to figure 27 with the
chuck 22 in an upside down position. This figure 28 demonstrates, that a chuck is also
 applicable in an upside down position, especially when it is supported by a vacuum
connection 57 toward vacuum container 28.

Figures 29, 30, 31, and 32 show a further semiconductor device structure. Parts
which are similar to parts of the aforementioned semiconductor device structures have
the same reference numbers.

As one can see best in Figure 30 from a bottom side of the wafer 12, the slits 31 are
provided such that they intersect with the central portion 2, cutting the bottom face 7
and the outer face 8. The top face 6 on the upper side of the wafer 12 is not cut. The
semiconductor device structure of the Figures 29 to 32 is insofar similar to the semi-
conductor device structure of Fig. 7. This provides reinforcement structures as elevated
areas over the central portion 2, the reinforcement structures comprising parts of the
rim 1.

Different from the semiconductor device structure of Fig. 7, the slits 31 semi-
conductor device structure of the Figures 29 to 32 are provided in with a spatial ori-
entation that provides a radial inclination angle \( j \) (phi) between each slit 31 and a radial direction of the wafer 12 at the location of the respective slit 31. It turned out that this can provide an improvement of the stability of the wafer 12.

Figure 31 shows a cut section through a line A - A in Figure 30. Figure 31 illustrates the passage from the outer face 8 to the inner face 9 of the wafer 12 which is provided through the slits 31.

Figure 32 together with Figure 29 illustrates the impact of the inclined orientation of the slits 31 on the flexibility of the wafer 12. The slits 31 have inner orifices 31' which are - in a radial direction of the wafer 12 - out-of-line not with outer orifices of the same slits 31. That means that one cannot see completely through a slot 31 when looking into a radial direction of the wafer 12. If the radial inclination angle \( j \) is chosen properly, here as 60° (degrees), the effective geometricalmomentofinertia of the radial cross section of the wafer 12 is different as compared with the design of Figure 12. One way to choose the radial inclination angle \( j \) is to provide the slits in such a way that there is no radial overlap between the inner orifice 31' and the respective outer orifice of the slits 31. This means that if one is looking from an outside of the wafer 12 through the slits 31 in a radial direction, one cannot see the inner orifice 31' but only the inner walls of the slits 31 within the rim 1 of the wafer 12.

For a better comparison, Figure 33 shows the a view of the wafer 12 of Figure 7 from outside which corresponds with the view of the wafer 12 of Figures 32. As one can see in Figure 33, the radial inclination angle \( j \) is here 0° (degrees), so that there is a full radial overlap of the inner orifice 31' and the respective outer orifice of the slits 31. If their dimensions of the wafer 12 and the slits 31 are the same, the effective geometricalmomentofinertia of the radial cross section of the wafer 12 of the Figures 19 to 32 is different from the corresponding geometricalmomentofinertia of the wafer of Figure 7.

It is believed that not only does the actual size of the geometricalmomentofinertia of the radial cross-section of the wafer plays a role. The smallest absolute size of the radial geometricalmomentofinertia along the circumference of the wafer is important, too, because a breaking of the wafer often occurs at the location of the smallest radial geometricalmomentofinertia. An appropriate location and orientation of the slits in the rim of the wafer can improve this behaviour.

It can be of further advantage to place the slits into a direction which is different from the crystallographically preferred or main breaking lines along the main symmetry axes of the crystal which was used for manufacturing the wafer.

Figure 34 shows a schematic bottom view of a further semiconductor device structure which is similar to the semiconductor device structure of Figures 29 - 32. Parts which are similar to parts of the aforementioned semiconductor device structure have the same reference numbers.
The slits 31 are bent in a plane of the wafer 12 and they are similar to the shape of turbine blades. One way of producing the bent slits would be to use a cylindrical or conical milling head which is moved into the rim 1 of the wafer 12. The resulting slits 31 are provided such that they intersect with the central portion 2, cutting the bottom face 7 and the outer face 8. The top face 6 on the upper side of the wafer 12 is not cut. The slits 31 can also be provided at least partly by an etching process.

This provides reinforcement structures as elevated areas over the central portion 2, the reinforcement structures comprising parts of the rim 1.

The radial geometrical moment of inertia of the wafer 12 can be further improved and there may be a reduced local stress concentration in the slits 31 which then improves the fracture strength of the wafer 12. The bent slits 31 may also have positive effects for discharging liquids through the perforations 10 in the slits 31 when the wafer 31 is spinning.

Figure 35 and 36 show a schematic bottom view and an outside view of a further semiconductor device structure which is similar to the semiconductor device structures of Figures 29 - 32 or of Figure 34. Parts which are similar to parts of the aforementioned semiconductor device structure have the same reference numbers.

The slits 31 are made with a bevelled or sloped cutting blade which is moved into the rim 1 of the wafer 12, starting at its bottom face 7 and outer face 8. The resulting slits 31 are provided such that they intersect with the central portion 2, cutting the bottom face 7 and the outer face 8. The top face 6 on the upper side of the wafer 12 is not cut. The slits 31 can also be provided at least partly by an etching process.

This provides reinforcement structures as elevated areas over the central portion 2, the reinforcement structures comprising parts of the rim 1.

The slits 31 which have bevelled grounds in the bottom face 7 and in the outer face 8 have, as compared with the design of Figure 7, an increased cross-section area for a given cutting depth. This can have positive effects for discharging liquids through the perforations 10 in the slits 31.

In a further alternative not shown here, the slits 31 with bevelled grounds in the bottom surface 7 and in the rim 1 and outer face 8 are provided with an inclined orientation with respect to the radial direction of the wafer 12. This is design is insofar similar to the design of Figures 29 - 32.

Figure 37 shows a schematic top view of a further semiconductor device structure. Parts which are similar to parts of the aforementioned semiconductor device structure have the same reference numbers. Different from the foregoing designs, the design of Figure 37 has slits 31 which are provided in the rim 1 on the top face 6 of the wafer 12 such that the slits 31 extend through the upper part of the rim 1. There are reinforcement structures provided as elevated blocks between two neighbouring slits 31.
Figure 37 shows a design with a radial inclination angle $j$ which is here $0^\circ$ (degrees), so that there is a full radial overlap of the inner orifice 31' at the perforation 10 and the respective outer orifice of the slits 31. There appears, no important advantage with respect to stability against bending in a radial direction of the wafer 12 as compared with a wafer without the reinforcement structures but this design may have advantages with respect to discharging fluids from a spinning wafer 12.

Figure 38 shows a schematic top view of a further semiconductor device structure which is similar to the semiconductor device structure of Figure 10 before cutting of the rim 1. Parts which are similar to parts of the aforementioned semiconductor device structure have the same reference numbers.

As can be best seen in Figure 39 which shows a schematic cross sectional view of the semiconductor device structure of figure 38, a grinding stone with a grinding angle $\alpha$ (alpha) of about $45^\circ$ has produced an upper edge 60 at a top face 6 and a lower edge 61 at a second side 4 with a sloping surface extending between the upper edge 60 and the lower edge 61. Other angles $\alpha$ (alpha) for the sloping surface between the upper edge 60 and the lower edge 61 are possible, especially between $10^\circ$ and $60^\circ$. In a further embodiment which is not shown here, the upper edge 60 and the lower edge 61 can be rounded so that there is no literal edge line present. This can facilitate the flow of fluids over the top face 6. Good results can be obtained if the outline of the sloping surface follows the shape of a mathematical tangens hyperbolicus curve.

The wafer 12 of Figure 38 can immediately be used for providing electronic circuits and semiconductor device structures on its front surface 11 and on its second side 4, for example as shown in the foregoing Figures, especially as shown with reference to Figures 1 to 28. Liquids which are used in these process steps can escape over the rim 1 by simply flowing over the sloping surface between the upper edge 60 and the lower edge 61.

Not shown here is a further embodiment which is a combination of the teachings of Figures 37 and Figures 38 and 39. There are reinforcement structures as elevated areas over the central portion provided, the reinforcement structures comprising parts of the rim which are separated by slits. The reinforcement structures have an upper edge at a top face and a lower edge at a second side of the wafer with a sloping surface extending between the upper edge and the lower edge. Such a wafer can be used for providing electronic circuits and semiconductor device structures on its front surface and on its second side. Liquids which are used in these process steps can escape over the rim by flowing over the sloping surface or ramp between the upper edge and the lower edge and through the slits between the reinforcement structures.

Figure 40 shows a schematic top view of a further semiconductor device structure. Parts which are similar to parts of the aforementioned semiconductor device structure
have the same reference numbers. Similar to the design of Figure 37, the design of Figure 40 has slits 31 which are provided in the rim 1 on the top face 6 of the wafer 12 such that the slits 31 extend through the upper part of the rim 1. Reinforcement structures are thereby provided as elevated blocks between two neighbouring slits 31. Figure 40 shows a design with a radial inclination angle j which is here about 60° (degrees), so that there is no radial overlap of the inner orifice 31' at the perforation 10 and the respective outer orifice of the slits 31.

This involves an increased stability against bending in a radial direction of the wafer 12 as compared with a wafer without the reinforcement structures and advantages with respect to discharging fluids from a spinning wafer 12.

The wafer 12 can be manufactured easily because most of the manufacturing steps and especially the mechanical steps thereof such as the grinding of the second side 4 and the provision of the slits 31 can be provided from one single side without intermediate handling of the wafer between the respective manufacturing steps. If a wet treatment takes place at the wafer 12, the wafer chuck is prevented from contamination with chemicals. Further, effective cross-section of the slits 31 can be increased which enhances a fluid flow through the slits 31.

Figure 42 shows a cut section through a line A - A in Figure 40, illustrating the passage from the outer face 8 to the inner face 9 of the wafer 12 which is provided through the slits 31.

Figure 41 shows a schematic top view of a further semiconductor device structure which is similar to semiconductor device structure of Figures 40 and 42. Parts which are similar to parts of the aforementioned semiconductor device structure have the same reference numbers.

The slits 31 are bent in a plane of the wafer 12 and they are similar to the shape of turbine blades. One way of producing the bent slits would be to use a cylindrical or conical milling head which is moved into the rim 1 of the wafer 12. The resulting slits 31 are provided such that they intersect with the central portion 2, cutting the bottom face 7 and the outer face 8. The top face 6 on the upper side of the wafer 12 is not cut. The slits 31 can also be provided at least partly by an etching process.

This provides reinforcement structures as elevated areas over the central portion 2, the reinforcement structures comprising parts of the rim 1.

The radial geometrical moment of inertia of the wafer 12 can be further improved and there may be a reduced local stress concentration in the slits 31 which then improves the fracture strength of the wafer 12. The bent slits 31 may also have positive effects for discharging liquids through the perforations 10 in the slits 31 when the wafer 31 is spinning.

Figure 43 shows a further semiconductor device structure. Parts which are similar to
parts of the aforementioned semiconductor device structures have the same reference numbers.

[156] The slits 31 of the semiconductor device structure of the Figures 29 to 32 are provided with a spatial orientation that provides a horizontal inclination angle $s$ (sigma) between each slit 31 and a horizontal direction of the wafer 12 at the location of the respective slit 31. It turned out that this can also provide an improvement of the stability of the wafer 12.

[157] The spatial orientation of the slits 31 can also be combined with a radial inclination angle $j$ as in Figure 32. A radial overlap of the inner orifice 31' and the respective outer orifice of the slits 31 can be avoided, leaving the second side 4 uncut and essentially with less or even without any damage or cracking.

[158] Figure 44 shows a further semiconductor device structure. Parts which are similar to parts of the aforementioned semiconductor device structures have the same reference numbers.

[159] While the semiconductor device structure of Figure 42 has slits 31 with a spatial orientation that provides a horizontal inclination angle $s$ (sigma) and with a radial inclination angle $j$ through the top face 6, leaving the bottom face 7 essentially uncut, the semiconductor device structure of Figure 43 has slits 31 with a similar spatial orientation through the bottom face 7, leaving the top face 6 essentially uncut.

[160] Figure 45 shows a cross-section through a further semiconductor device structure, having a slit 31 with a spatial orientation that provides a horizontal inclination angle $s$ (sigma) and with a radial inclination angle $j$ (phi), the slit 31 extends through the top face 6 and through the bottom face 7. A virtual radial bending axis 62, an upper bending area Au, and a lower bending area Al are provided for the specific position on the circumference of the rim 1. These areas are useful for calculating and improving the local geometrical moment of inertia of the wafer against radial bending around the virtual radial bending axis 62 and ultimately for improving the stress levels in the wafer 12.

[161] For producing the aforementioned semiconductor wafers with reinforcement structures, one can first create the passage in the form of slits 31 and then creating the recess in the rear surface 16 of the wafer 12. Alternatively, one can first create the recess in the rear surface 16 of the wafer 12 followed by creating the passages in the form of slits 31. With certain production methods and if the passage in the form of a ramp 60, 61 or slits 31 and the recess in the rear surface 16 are provided at the same side of the wafer 12 - such as in Figures 37, 40, 41, 42, 43, and 45 - the recess in the rear surface 16 of the wafer 12 and the passage in the form of a ramp 60, 61 or passages in the form of slits 31 can be created together and even in the same process period.
It is of advantage to provide the fluid passage in the form of slits 31 and the recess in the rear surface 16 at the same side of the wafer 12 because the reinforcement structures between the slits 31 do not form a continuous rim 1. These reinforcement structures are a collection of separate block segments which are discontinuously arranged at the circumference of the wafer 12. For such reinforcement structures, one can even use plasma etching without any mechanical grinding.

The passages in the form of slits 31 or in the form of a ramp 60, 61 can be provided by a dicing saw or in a more general sense with a circumferential grinding tool with a numerical control. Further ways to provide passages in the form of slits 31 or in the form of a ramp 60, 61 comprise using a laser abrasive method or a finger mill or an end mill, which is especially suited for providing bent slits as in Figures 34 or 41. It is also possible to provide a lithographic structure followed by at least one etching step such as dry etching of silicon or wet etching or a combination of both etching methods.

If a grinding step is provided for the recess in the rear surface of the wafer 12, this is often followed by a plasma process for a relief of stress in the wafer material. This can also be done by a wet etching step. The wafer 12 of the application provides the advantage of an easy drain of the plasma gases or of the etching liquid from the recess in the rear surface of the wafer through the passages in the form of slits 31 or in the form of a ramp 60, 61. This has not been possible easily with the known wafers with a recess in their rear surface.
Claims

[Claim 1] A semiconductor wafer (12) with a central portion (2) having a first side (3) and a second side (4) and at least one reinforcement structure, the reinforcement structure providing at least one passage (10) for a fluid flow between an inner face (9) of said one reinforcement structure towards an outer face (8) of the reinforcement structure.

[Claim 2] The semiconductor wafer according to claim 1, wherein the reinforcement structure increases the radial bending resistance of the semiconductor wafer (12).

[Claim 3] The semiconductor wafer according to claim 1 or claim 2, wherein the passage (10) comprises an inner orifice (31').

[Claim 4] The semiconductor wafer according to claim 3, wherein a height (h) of at least a portion of said passage (10) is larger than the thickness (d) of said thinned central portion (2).

[Claim 5] The semiconductor wafer according to one of the previous claims, wherein said reinforcement structures comprise elevated areas over the central portion 2.

[Claim 6] The semiconductor wafer according to claim 5, wherein said passages (10) comprise slits (31) which separate at least two elevated areas from each other.

[Claim 7] The semiconductor wafer according to claim 5 or claim 6, wherein said passages (10) comprise slits (31) which are provided within the elevated areas.

[Claim 8] The semiconductor wafer according to claim 6 or claim 7, wherein slits (31) are provided with a spatial orientation that includes a horizontal inclination angle s (sigma) between the slit (31) and a horizontal direction of the wafer (12) at the location of the respective slit (31).

[Claim 9] The semiconductor wafer according to one of the claim 6 to 8, wherein slits (31) are provided with a spatial orientation that provides a radial inclination angle j (phi) between the slit (31) and a radial direction of the wafer (12) at the location of the respective slit (31).

[Claim 10] The semiconductor wafer according to one of the claim 6 to 9, wherein a spatial orientation of at least one slit (31) is provided such that there is no radial overlap of an inner orifice (31') and a respective outer orifice of the slit (31).

[Claim 11] The semiconductor wafer according to one of claims 1 to 4, wherein said passage (10) comprises a ramp (60, 61) which is provided at the
elevated area.

[Claim 12] The semiconductor wafer according to one of the previous claims, wherein said first side (3) of said thinned central portion (2) comprises a front surface (11) of a standard semiconductor wafer (12).

[Claim 13] The semiconductor wafer according to one of the previous claims, wherein said first side (3) comprises a plurality of integrated electronic circuits (15) or semiconductor devices.

[Claim 14] The semiconductor wafer according to one of the previous claims, wherein said second side (4) of said thinned central portion (2) comprises a portion of a rear surface (16) of a standard semiconductor wafer (12).

[Claim 15] The semiconductor wafer according to one of the previous claims, wherein said second side (4) of said thinned central portion (2) comprises a metallization structure (19) of a metallization layer (17).

[Claim 16] The semiconductor wafer according to one of the previous claims, wherein said second side (4) of said central portion (2) comprises a plurality of metallization structures comprising insulation layers (18) between said metallization structures (19) and comprising through contacts through said insulation layers (18).

[Claim 17] The semiconductor wafer according to one of the previous claims, wherein said second side (4) of said central portion (2) comprises a metallization structure (19) with contact bumps (20).

[Claim 18] The semiconductor wafer according to claim 17, wherein said contact bumps (20) comprise a seed layer (21) portion and at least a plated body of a copper or tin alloy coated with another metal, e.g. Au, Ag or Sn.

[Claim 19] The semiconductor wafer according to one of the previous claims, wherein said first side (3) and said second side (4) of said thinned central portion (2) comprise recessed portions of a rear surface (16) and a front surface (11) of a standard semiconductor wafer (12), wherein each surface (11, 16) comprises a plurality of coordinated rectangular areas (13), wherein each coordinated area (13) comprises an integrated electronic circuit (15) or a semiconductor device.

[Claim 20] A chuck for holding a semiconductor wafer (12), which comprises a circular base plate (23) surrounded by a chuck rim (30) that comprises perforations (24).

[Claim 21] The chuck according to claim 20, wherein positions of said perforations (24) of said chuck rim (30) correspondent to at least one position of
said passage (10) of a semiconductor wafer (12) according to one of claims 1 to 19.

[Claim 22] The chuck according to claim 20 or claim 21, wherein said chuck rim (30) has a double ring (25) structure with an inner ring (26) and an outer ring (27), wherein said rings (26, 27) are perforated and rotatably arranged with respect to each other to variegate the cross section of a combined perforation size.

[Claim 23] The chuck according to one of claims 20 to 22, wherein said perforations (24) of said chuck rim (30) are connected to a vacuum container (28) for supporting a discharging or a bypassing of excess liquids through said said perforations (24) of said chuck rim (30).

[Claim 24] A method comprising
- providing a semiconductor wafer (40) comprising a front surface (11) and a rear surface (16);
- producing integrated electronic circuits (15) or semiconductor device structures at the front surface (11);
- providing at least one fluid passage (10) at a circumference on the front surface (11) extending radially between an outer face (8) of the wafer (40) and an inner face (9) of said wafer (40);
- providing a recess at the rear surface (16) of the wafer (40) to provide a thinned central portion (2) having a first side (3) and a second side (4) surrounded by at least one reinforcement structure.

[Claim 25] Method according to claim 24, comprising the provision of holes for electrical connections between the front surface (11) and the rear surface (16) of the thinned central wafer portion.

[Claim 26] Method according to claim 25, comprising etching or laser ablating of the holes.

[Claim 27] Method according to one of claims 24 to 26, comprising the provision of a recess into the rear surface (16) of the wafer (40) and into the front surface (11) of the wafer (40) for providing a double recessed thinned central portion (29) having a first side (3) and a second side (4).

[Claim 28] Method according to one of claims 24 to 27, wherein providing said passage (10) comprises cutting of slits (31) by a dicing saw blade (32).

[Claim 29] The method according to claim 28, wherein a cutting depth (c) for said slits (31) is deeper than a thickness (d) of said thinned central portion (2).

[Claim 30] The method according to claim 28 or claim 29, wherein the cutting is done with a radial inclination.
[Claim 31] The method according to one of claims 28 to 30, wherein the cutting is done with a horizontal inclination.

[Claim 32] The method according to one of claims 24 to 27, wherein providing said passage (10) comprises dry etching.

[Claim 33] The method according to claim 32, wherein said etching comprises a RIE-plasma etching process.

[Claim 34] The method according to one of claims 24 to 27, wherein providing said passage (10) comprises wet etching.

[Claim 35] The method according to one of claims 24 to 34, wherein a deposition of a metal or carbon seed layer (21) for a metallization structure or a bump (20) plating structure is performed onto said second side (4) of said thinned central portion (2).

[Claim 36] The method according to claim 35, wherein said metal or carbon seed layer (21) is structured to said metallization structure and/or plated to said electrical bumps (34), by at least one of the steps of sprayed-on and spinning a photo-resist (35), of spraying-on developing liquids, of spraying-on etch liquids, of rinsing-on cleaning liquids, of spraying-on stripping liquid, of plating or of coating by electrolytic liquids under bypassing or escaping of excess liquids over said passage (10).

[Claim 37] The method according to claim 35 or claim 36, wherein said metal or carbon seed layer (19) is structured and plated to said metallization structure and/or said electrical bumps (20), comprising
- depositing a thin metal or carbon seed layer (21) to the second side (4) of the thinned central portion (2);
- spraying-on and spinning of a resist layer (35) under escaping of excess resist over said passage (10);
- drying the resist layer (35);
- structuring the dried layer by exposition through a mask;
- developing the exposed resist layer (35) by spraying-on developing liquid under escaping of excess resist and excess developing liquid over said passage (10);
- rinsing the structured resist layer (35) by spraying-on a rinsing liquid under escaping of excess rinsing liquid over said passage (10);
- hardening the developed resist structure to a plating mask (36);
- plating the uncoated resist free seed layer (19) to a metallization structure and/or to metallic bumps (34) in an electrochemical bath (37) by circulating the electrochemical liquid over the structured seed layer (19) and bypassing said liquid over said passage (10);
- stripping off the resist of said plating mask (36) from the second side (4) by spraying-on a stripping liquid under escaping of excess stripping liquid and stripped resist over said passage (10);
- cleaning the stripped structure by a cleaning liquid under escaping of excess cleaning liquid over said passage (10);
- wet etching remaining parts of the thin seed layer (19) by spraying-on of etch liquid under escaping of excess etch liquid over said passage (10);
- rinsing the etched structure by spraying-on a rinsing liquid under escaping of excess rinsing liquid over said passage (10);
- cleaning the second side with bumps by a cleaning liquid under escaping of excess cleaning liquid over said passage (10) and drying the semiconductor wafer (12).