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(71) Applicant: **STMicroelectronics S.r.l.**
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Gaeta, Marco**
  26866 Sant'Angelo Lodigiano (IT)
- **Bollati, Giacomino**
  29015 Castel San Giovanni (IT)
- **Bongiorni, Marco**
  29015 Castel San Giovanni (IT)

(74) Representative: **Pellegri, Alberto et al**
c/o Società Italiana Brevetti S.p.A.
Piazza Repubblica, 5
21100 Varese (IT)

(54) Logarithmic linear variable gain CMOS amplifier

(57) In a logarithmic linear variable gain CMOS amplifier comprising a differential input pair of transistors with diode-connected load transistors, a second differential pair of transistors sharing the same diode-connected load transistors, a pair of current mirrors for programmably injecting respective bias currents in the common source modes of said two differential pairs of transistors, generated by a digital-to-analog converter, the groups delay is rendered independent from the gain and linearity inversely proportional to the gain by cross connnecting the control nodes of the second differential pair to the control nodes of the first differential input pair of transistors and by biasing the two differential pair of transistors such that the sum of their respecive bias current is maintained constant.

Preferably, transistor means connected in parallel to each of said diode-connected load transitors are added for subtracting a constant amount of current from said sum current that would otherwise be flowing through the diode-connected load transistors.

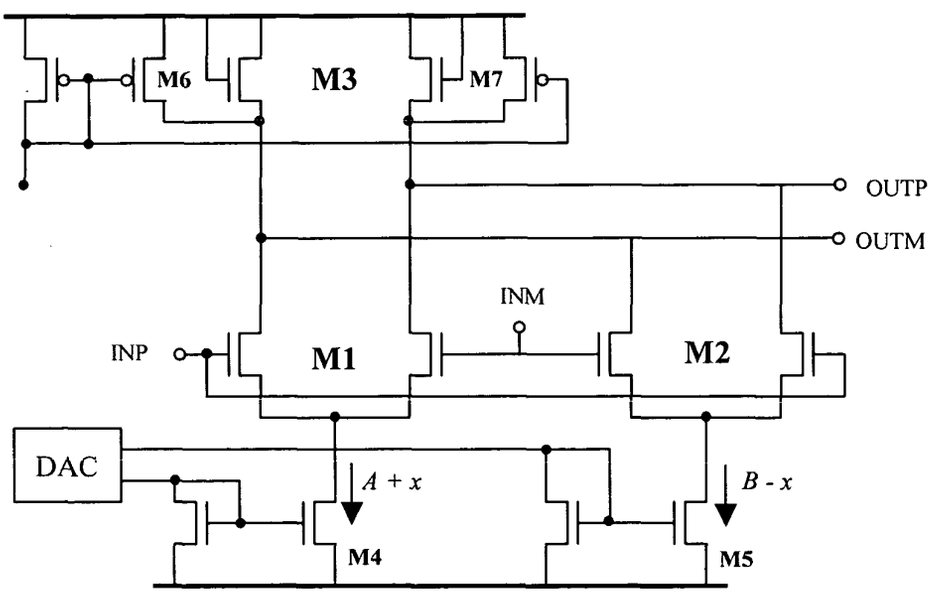

FIG. 2

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Description

[0001] The present invention relates in general to integrated analog circuits and more in particular to an integrated logarithmic linear variable gain CMOS amplifier.

[0002] State of the art logarithmic linear amplifiers are based on a circuit structure as that depicted in Figure 1. Such a structure is disclosed in the published patent application No. US 2002/0048109 A1.

[0003] The gain of these amplifiers commonly employing two stages for increasing the gain range is given by an expression of the form:

$$Gain = \sqrt{\frac{1 + x}{1 - x}} \tag{1}$$

[0004] The linear logarithmic gain (dB gain) variation range of the function is relatively restricted. Generally the value of x of the gain expression for remaining in substantially linear dB gain variation range is limited to $-0.7<x<0.7$.

[0005] The variation of the bias current in a transistor notably alters its transconductance thus obtaining the desired behaviour of the circuit according to equation 1, but the variation of the bias current affects also the bandwith and the linearity of the amplifier.

[0006] The group delay of the amplifier circuit is (inversely) proportional to the bandwith.

[0007] On the other hand it would be strongly desirable to render the group delay independent from the gain to prevent interaction between gain loop and phase loop.

[0008] Variable gain amplifiers work with fixed output voltage swing (fixed by the control loop) and the gain is inversely proportional to the input voltage swing.

[0009] While it would be highly desirable that linearity should be inversely proportional to the gain, the known amplifier structures such as the one depicted in Figure 1 unfortunately have the opposite behaviour.

[0010] Therefore, there is a clear need and/or usefulness of a logarithmic linear variable gain amplifier wherein the group delay is rendered substantially independent from the gain and the linearity of the amplifier made to be inversely proportional to the gain.

[0011] It has been found that the above-identified objectives may be obtained in a relatively simple manner, without substantially adding complexity to the basic circuit of an integrated logarithmic linear variable gain amplifier, by cross connecting two differential pairs of transistors that share the same diode loads and by biasing the two differential pairs of transistors so connected with currents such that their sum remains constant. In practice this is achieved by mirroring in the common current node of the two differential pairs of transistors the required bias currents provided by the linear dac and which have value A + x and B - x, respectively, where A and B are the respective bias current and *x* is the variable factor.

[0012] In this way the sum of the two currents is kept constant and so is the bandwith that depends on it.

[0013] According to an optional but highly preferred embodiment, the diode loads, common to the two cross connected differential input stages have transistor means connencted in parallel to the diode loads for subtrackting a constant current of a desired value from the current that would otherwise be flowing through the diode loads. This permits to translate the gain curve of the amplifier according to needs.

[0014] **Figure 1** represents, as already noted above, the basic circuit of a state of the art integrated logarithmic linear variable gain CMOS amplifier.

[0015] **Figure 2** shows the circuit diagram of a logarithmic linear variable gain CMOS amplifier according to a preferred embodiment of this invention.

[0016] **Figure 3** is a diagram of the gain characteristics of an amplifier according to the present invetion.

[0017] As depicted in Figure 2, the two differential transistor pairs, M1 and M2, sharing the same diode-connected load transistors M3, are cross connected to the inpuit nodes INP and INM of the amplifier, according to an essential feature of the novel circuit of this invention.

[0018] Being gm_1 the transconductance of the first input differential pair of transistors M1, gm_2 the transconductance of the second input differential pair of transistors M2, and gm_3 the transconductance of the diode-connected load transistors M3 , it may be demonstrated that the gain is given by the following equation:

$$Gain = \frac{gm_1 - gm_2}{gm_3} = \frac{\sqrt{K_1 \cdot I_1} - \sqrt{K_2 \cdot I_2}}{\sqrt{K_3 \cdot I_3}} \tag{2}$$

where K_i is the transistor's gain constant proportional its "aspect ratio" W/L, I_1, I_2 and I_3 are the bias currents of M1, M2 and M3 respectively, and the bandwith is given by the following equation:

$$Bandwidth \cong \frac{\sqrt{K_3 \cdot I_3}}{\pi \cdot C_{out}} \tag{3}$$

wherein C_{out} is the capacitance of the output node, referred to the virtual ground node of the circuit.

[0019] Customarily, the two differential pairs of transistors M1 and M2 are biased by respective currents output by a linear digital-to-analog converter through respective current mirrors M4 and M5, and the pair M3 of diode connected load transistors is biased by the difference between the sum of these currents and the currents flowing in M6 and M7.

[0020] According to an essential condition of this invention, the two bias current have a value given by expressions of the type: A + *x* and B - *x*, where A and B are the pre-estabilished bias current values while *x* represents the variable factor. Therefore, the sum of the two bias currents is kept constant such that $I_3 = I_1 + I_2$.

[0021] In the case of the preferred embodiment depicted in Figure 2, wherein transistor means M6 and M7 are included for subtracting a constant amount of the current that would otherwise be flowing in the two diode-connected load transistors M3, the sum current I_{TOT} will be equal to the actual bias current I_3 plus the constant amount that is subtracted by flowing through the optionally added transistors M6 and M7. In any case the effective bias current I_3 of the bandwidth equation 3 will be constant, ensuring constancy of the bandwidth.

[0022] Accordingly, the gain in dB is given by the following expression:

$$\left(\frac{v_{out}}{v_{in}}\right)_{dB} = 20 \cdot \log\left(\sqrt{K_1 \cdot Id_1} - \sqrt{K_2 \cdot Id_2}\right) - 10 \cdot \log\left(K_3 \cdot Id_3\right) \quad \text{with} \quad Id_1 > \frac{K_2}{K_1} \cdot Id_2 \tag{4}$$

[0023] By observing equation 4, it may be easily recognized the fact that the gain of the amplifier is linearly controlled by I_1 and I_2, while by modifying the current I_3, it is possible to translate the gain characteristic.

[0024] According to the highly preferred embodiment shown in Figure 2, additional transistors M6 and M7 respectfully connected in parallel to the diode-connected load transistors M3, are used to subtrac a certain constant amount for the total current that would be flowing through the diode-connected load transistors M3. In this way, the current that actually flows through the diode-connected load transistors M3 may be fixed for setting the gm of the M3 transistors and therefore to translate the gain characteristic.

[0025] By substituting $I_3 = I_1 + I_2$ in equation 4, the following equation is obtained

$$\left(\frac{v_{out}}{v_{in}}\right)_{dB} = 20 \cdot \log\left(\sqrt{I_3 - I_2} - \sqrt{\frac{K_2}{K_1} \cdot Id_2}\right) - 10 \cdot \log\left(\frac{K_1}{K_3 \cdot Id_3}\right) \quad \text{with} \quad I_3 > \left(\frac{K_2}{K_1} + 1\right) \cdot Id_2 \tag{5}$$

[0026] The expression 5 may be plotted as shown in Figure 3 in order to show the linear variation range of the dB gain figure.

[0027] The amplifier provides for an output signal of fixed amplitude while the input signal varies its amplitude.

[0028] When the gain is relatively high, the current in the first input differential pair of transistors M1 is much larger than the current in the second input differential pair of transistors M2. Under these conditions, linearity of the first differential input pair of transistors M1 is very good beacause its overdrive is relatively high, while the linearity of the other differential input pair of transistors M2 is relatively poor. However, this is not a problem because the contribution of the second differential pair M2 to the output current is proportionally very small and even its distortion has a negligible impact on the output current.

[0029] The gain is reduced by reducing the current in the first differential input pair M1 and complementarily increasing the current in the second input differential pair M2.

[0030] By reducing the current in the first differential input pair M1 while the input signal swing is increasing is detrimental to its linearity but at the same time, the linearity of the other differential input pair M2 is improving and in

addition, the third harmonic of M2 is subtracted from the third harmonic of M1 thus enhancing the overall linearity of the amplifier, as may be inferred by the following expression:

$$i_{tot} = i_{1|H1} + i_{1|H3} - \left(i_{2|H1} + i_{2|H3}\right) \qquad (6)$$

where $i_1|H1$ indicates the first harmonic of the respective current signal i_1.

[0031] In conclusion, the novel amplifier of this invention has a markedly improved linearity in comparison with the known amplifier circuit of Figure 1.

[0032] Although the variable gain logarithmic linear amplifier with improved linearity characteristic of this invention may have innumerable applications, a particularly important application in which the amplifier of this invention is particularly useful is in data acquisition channels from a mass storage drive, such as a hard disk.

Claims

1. A logarithmic linear variable gain CMOS amplifier comprising a differential input pair of transistors with diode-connected load transistors, a second differential pair of transistors sharing the same diode-connected load transistors, a pair of current mirrors for programmably injecting respective bias currents in the common source modes of said two differential pairs of transistors, generated by a digital-to-analog converter, **characterized in that**

said second differential pair of transistors have respective control nodes cross connected in parallel to the control nodes of said first differential input pair of transistors;

said bias currents injected in the two differential pair of transistors are such that their sum is maintained constant.

2. The variable gain amplifier according to claim 1, **characterized by** the fact that it further includes transistor means connected in parallel to each of said diode-connected load transitors for subtracting a constant amount of current from said sum current that would otherwise be flowing through the diode-connected load transistors.

3. The variable gain amplifier according to claim 1, **characterized in that** said bias currents output by a linear digital-to-analog converter have values (A + x) and (B - x), respectively, A and B being programmed constant bias current values and x being a variable factor.

5. The variable gain amplifier according to anyone of the preceding claims, **characterized in that** the current in the diode-connected load transistors is varied for translating the gain characteristics of the amplifier.

6. The variable gain amplifier according to claim 2, **characterized in that** said transistor means connected in parallel to each of said diode-connected load transitors are of opposite type of conductivity of said diode-connected load transistors.

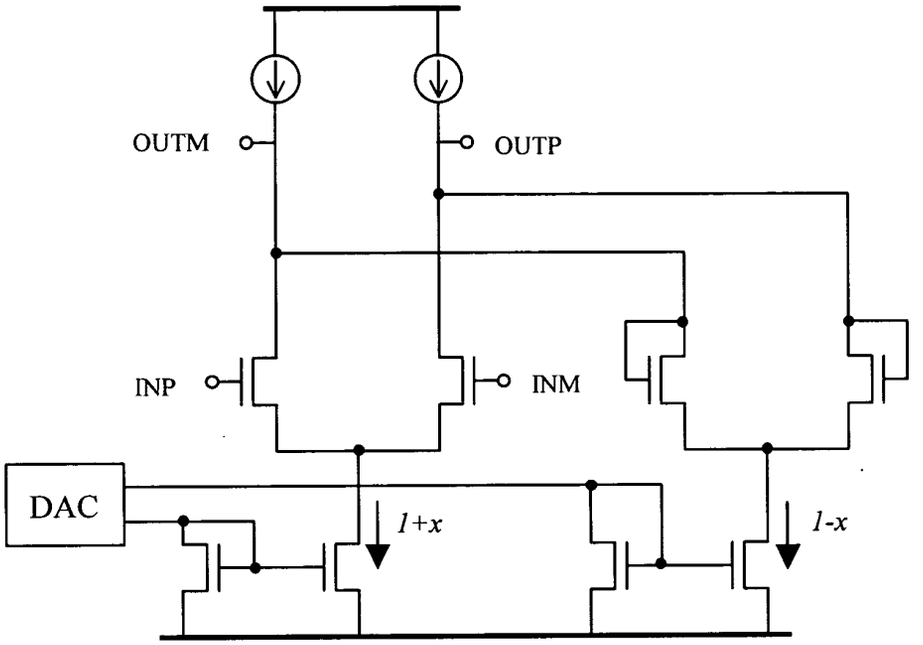
OUTM
OUTP
INP
INM
DAC
1+x
1-x

FIG. 1

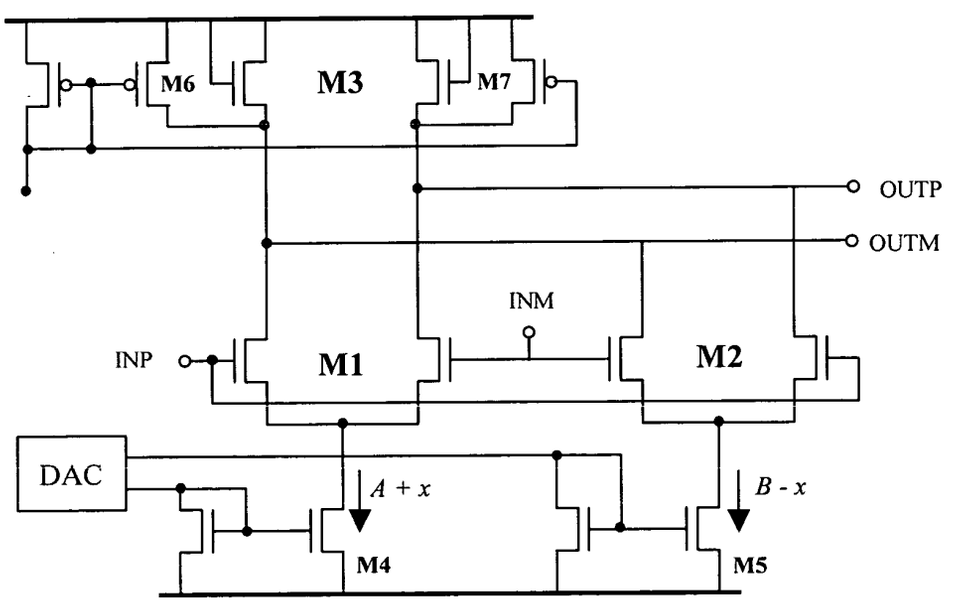
M6
M3
M7
OUTP
OUTM
INM
INP
M1
M2
DAC
A + x
B - x
M4
M5

FIG. 2

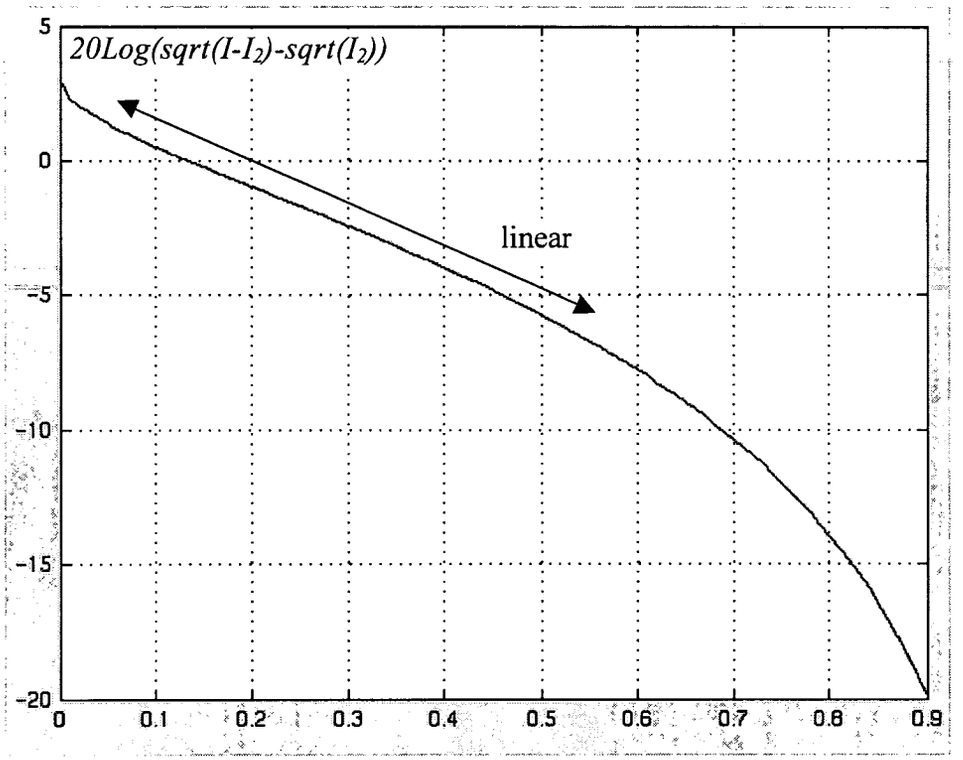
20Log(sqrt(I-I2)-sqrt(I2))
linear
5
0
-5
-10
-15
-20
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9

FIG. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 03 42 5568

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	EP 1 024 450 A (LUCENT TECHNOLOGIES INC) 2 August 2000 (2000-08-02)	1,3,5	H03G7/00 H03G7/06
A	* abstract * * paragraph [0005] - paragraph [0007] * * paragraph [0009] - paragraph [0011] * * claim 14; figures 1-3 * ---	2,6	
Y	US 6 584 486 B1 (TARKOEY FELIX ET AL) 24 June 2003 (2003-06-24)	1,3,5	
A	* column 2, line 66 - column 3, line 19 * * column 4, line 5 - column 5, line 14; figures 3,4 * ---	2,6	
A,D	US 2002/048109 A1 (CHAIKEN ALAN I ET AL) 25 April 2002 (2002-04-25) * abstract * * paragraph [0008]; figures 2,3 * ---	1-6	
A	US 5 886 579 A (MANGELSDORF CHRISTOPHER W) 23 March 1999 (1999-03-23) * abstract * * column 1, line 56 - column 2, line 62; figure 7 * -----	1-6	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H03G
G06G
G11B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	22 December 2003	Wichert, B

CATEGORY OF CITED DOCUMENTS

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82