(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 November 2004 (25.11.2004)

PCT

(10) International Publication Number
WO 2004/102765 A1

(51) International Patent Classification[7]: H02H 9/00, 3/087

(21) International Application Number:
PCT/US2004/012834

(22) International Filing Date: 20 April 2004 (20.04.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/429,399 6 May 2003 (06.05.2003) US

(71) Applicant *(for all designated States except US)*: **SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.** [US/US]; Patent Administration - A700, 5008 E. McDowell Road, Phoenix, AZ 85008 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **ROBB, Stephen P.** [US/US]; 13530 N. Sunridge Drive, Fountain Hills, AZ 85268 (US).

(74) Agent: **JACKSON, Kevin B.**; Patent Administration - A700, P.O. Box 62890, Phoenix, AZ 85082-2890 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

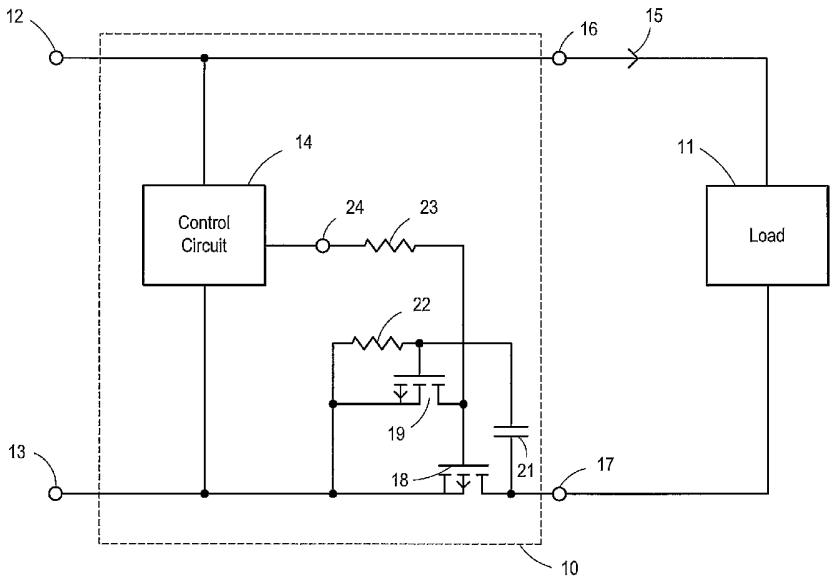
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM,*

[Continued on next page]

(54) Title: METHOD OF FORMING A PROTECTION CIRCUIT AND STRUCTURE THEREFOR



(57) Abstract: A protection circuit (10) is formed to protect a load (11) when a short circuit develops during operation of the load (11). A load transistor (18) is formed to couple the load to a voltage return terminal. A disable transistor (19) is formed to disable the load transistor (18) when a short circuit occurs.

WO 2004/102765 A1

PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

METHOD OF FORMING A PROTECTION CIRCUIT AND STRUCTURE THEREFOR

Background of the Invention

The present invention relates, in general, to electronics, and more particularly, to methods of forming semiconductor devices and structure.

In the past, the electronics industry utilized various methods and devices to protect circuits from shorts and other voltage transient. In some applications it was desirable to plug or unplug electronic circuits from their power source without removing the power. This may occur when a circuit card was inserted or removed from a small system such as a personal computer or from a large system such as a telecommunications system that may have a large rack full of electronic cards. Cards often were removed and re-inserted without powering down the entire system. These situations were referred to as "hot swap" or "hot plug" applications since the power lines remain "hot" during the transfers.

During some hot plug events, the card being plugged in was defective and presented a permanent short to the power bus. This short often pre-existed on the card before it was plugged into the system. Control circuits often were used to detect such shorts that existed as the card was inserted into the system. However, shorts also could develop after the card was plugged into the system. The control circuit did not protect from such a short that developed after the card was inserted. The short often result in damage to the card or to the overall system.

Accordingly, it is desirable to have a method of protecting a circuit from a short that occurs after the card is plugged into a system.

Brief Description of the Drawings

FIG. 1 schematically illustrates an embodiment of a portion of a protection circuit in accordance with the present invention;

FIG. 2 schematically illustrates a block diagram of an embodiment of a portion of the protection circuit of FIG. 1 in accordance with the present invention;

FIG. 3 schematically illustrates an enlarged cross-sectional portion of an embodiment of a capacitor of the protection circuit of FIG. 1 in accordance with the present invention; and

FIG. 4 schematically illustrates an enlarged plan view of a semiconductor device that includes the protection circuit of FIG. 1 in accordance with the present invention.

For simplicity and clarity of illustration, elements in the figures are not necessarily to scale, and the same reference numbers in different figures denote the same elements. Additionally, descriptions and details of well known steps and elements are omitted for simplicity of the description. As used herein current carrying electrode means an element of a device that carries current through the device such as a source or a drain of an MOS transistor or an emitter or a collector of a bipolar transistor, and a control electrode means an element of the device that controls current through the device such as a gate of an MOS transistor or a base of a bipolar transistor.

Detailed Description of the Drawings

FIG. 1 schematically illustrates an embodiment of a portion of a protection circuit 10 that is formed to quickly protect a load 11 from short circuits and other damaging voltages. Circuit 10 includes a control circuit 14, a first transistor or load transistor 18, a second transistor or discharge transistor 19, a coupling capacitor 21, a discharge resistor 22, a voltage input 12, a voltage return 13, a load voltage terminal 16, and a load return terminal or load return 17. Load 11 is coupled between load voltage terminal 16 and load return 17. Load 11 and circuit 10 typically are a portion of a sub-system or a card that is a portion of a larger external system (not shown) that has cards or elements that are removed and inserted into the external system. For example, load 11 and circuit 10 may be a portion of a line card of a telephone system or a portion of a modem card of a personal computer, or other type of card for another type of system. Circuit 10 is formed to permit connecting load 11 and circuit 10 to the larger external system without removing power from the external system and to protect load 11 during such operations. Typically circuit 10 receives power from the external system on voltage input 12 and voltage return 13. In most situations, the power is applied as the card containing circuit 10 and load 11 are inserted into the external system. Control circuit 14 detects power being applied to input 12 and return 13, and responsively controls transistor 18 to slowly charge load by-pass capacitances and to slowly increase a load current 15, illustrated by an arrow, to load 11 in order to protect load 11 while the power is applied.

FIG. 2 schematically illustrates a block diagram of an embodiment of a portion of control circuit 14 that is referred in the description of FIG. 1. Circuit 14 includes a variety of functional blocks that facilitate protecting load 11 when power is applied to load 11. Circuit 14

typically includes an Under Voltage Lockout block, an Over Voltage Lockout block, a Voltage Reference block, a Current Limit block, and a Thermal Limit block. Some blocks may be omitted in other embodiments. Circuit 14 receives the input voltage applied to voltage input 12. The Reference Voltage block provides various reference voltages that are used by each of the other blocks during the operation of circuit 14. The Under Voltage Lockout block typically does not allow circuit 14 to drive output 24, thus does not enable transistor 18, if the input voltage is less than a value established by the Reference Voltage block. The Over Voltage Block reduces the drive to transistor 18 if the input voltage is greater than a desired value. The Current Limit block disables transistor 18 if the current flowing from input 12 to load voltage terminal 16 exceeds a desired value. The Thermal Limit block disables transistor 18 if the temperature of circuit 14 exceeds a desired value. The functions provided by circuit 14 are well known to those skilled in the art.

Referring now to both FIG. 1 and FIG. 2, when power is applied control circuit 14 slowly enables transistor 18 to slowly ramp up a value of load current 15 until control circuit 14 fully enables transistor 18 to provide a low resistance connection between load return 17 and voltage return 13. If a short exists in load 11 when power is applied, control circuit 14 slowly ramps up load current 15 until reaching a current limit value established by the Current Limit block of control circuit 14. Under such a condition, load 11 will continue to consume the high load current value and dissipate the associated power until the Thermal Limit block disables transistor 18. These and other functions of control circuit 14 are well known to those skilled in the art.

Circuit 10 is also formed to include a transient suppression circuit that quickly disables transistor 18

when a short circuit occurs during operation in order to prevent damaging load 11. The transient suppression circuit includes transistor 19, resistor 22, and capacitor 21. Without the transient suppression circuit if a short occurs during the operation of load 11, transistor 18 would be fully enabled in a low resistance state and the short would cause a very large increase in load current 15. If transistor 18 were to remain enabled, the high value of load current 15 would last until the Thermal Limit block of circuit 14 disabled transistor 18. However, it may take several micro-seconds before the Thermal Limit block reduced load current 15. During this time, load 11 would be damaged. Additionally, a large value of load current 15 may cause the input voltage applied to input 12 to sag and result in incorrect operation of other circuits connected to the power bus of the external system.

The transient suppression circuit is formed to detect the short circuit condition during operation and to disable transistor 18 in order to protect load 11. When a short occurs, the voltage on terminal 16 is coupled to return 17 causing the voltage on return 17 to almost instantaneously increase. The increased voltage is applied to the drain of transistor 18 causing an increased drain-to-source voltage on transistor 18. The increased voltage or voltage step is conducted through capacitor 21 and quickly increases the gate voltage of transistor 19 thereby quickly enabling transistor 19. Transistor 19 then discharges the gate capacitance of transistor 18 and disables transistor 18. Thus, quickly enabling transistor 19 also quickly disables transistor 18 without having to wait for the thermal limit function of circuit 14 to disable transistor 18. Consequently, the function of the transient suppression circuit minimizes damage to load 11. Typically, transistor 19 is enabled when the value of the voltage coupled to

transistor 19 exceeds the threshold voltage of transistor 19.

After transistor 18 is disabled, resistor 22 slowly discharges capacitor 21. Eventually capacitor 21 is discharged to a value that is less than the threshold voltage of transistor 19 and transistor 19 is disabled. The values of resistor 22 and capacitor 21 form a time period that determines the time that transistor 19 is enabled for discharging the capacitance of transistor 18 in order to disable transistor 18. After transistor 19 is disabled, transistor 18 is slowly enabled once again by circuit 14 through a resistor 23. The short condition typically still exists, thus, as transistor 18 is slowly enabled by circuit 14 the value of load current 15 also slowly increases to the current limit value established by the Current Limit block of circuit 14. Typically the current limit value is much greater than the operational value of load current 15 but is much less that the short circuit value. Eventually, the Thermal Limit block will once again disable transistor 18.

In one example of a circuit without the transient suppression circuit, a short occurred during the operation of load 11. The short resulted in a load current spike from an operational value of about five Amps (5 Amps) prior to the short to a short circuit current of over one hundred Amps (100 Amps) after the short. The Current Limit block of circuit 14 became active after about ten (10) micro-seconds and limited the load current to a current limit value of about fourteen Amps (14 Amps). The long duration of the high load current value could damage load 11. The large current spike over such a long time may also cause the voltage on the bus that is connected to input 12 and return 13 to sag to a lower than desired value.

Adding the transient suppression circuit that includes transistor 19, capacitor 21, and resistor 22, reduced the

duration of the short circuit current spike to about one (1) micro-second. This short duration is not sufficient to damage load 11. Additionally the voltage on input 12 and return 13 remained stable.

In order to facilitate this operation, transistor 18 has a drain connected to return 17, a source connected to return 13, and a gate connected to an output of circuit 14 through resistor 23. Transistor 19 has a drain connected to the gate of transistor 18, a gate connected to a first terminal of resistor 22, and a source connected to return 13. A second terminal of resistor 22 is connected to return 13. Capacitor 21 has a first terminal connected to the drain of transistor 18 and a second terminal connected to the gate of transistor 19. Load 11 has a voltage supply input connected to terminal 16 and a voltage common terminal connected to return 17.

FIG. 3 schematically illustrates an enlarged cross-sectional portion of an embodiment of capacitor 21. Capacitor 21 must be formed to withstand the full voltage applied between input 12 and return 13. Preferably, capacitor 21 is formed on a semiconductor die with transistor 18. In the preferred embodiment, transistor 18 is a vertical N-channel power FET and transistor 19 is a lateral N-channel power FET that has a lower current capacity that transistor 18. Capacitor 21 is formed as a junction capacitor on an N-type semiconductor substrate 30. An N-type epitaxial layer 31 is formed on substrate 30. A P-type well 32 is formed on layer 31 and the junction between well 32 and layer 31 forms the junction capacitor. Preferably, one side of capacitor 21 is tied to the drain of transistor 18 to facilitate forming the junction capacitor utilizing the same high voltage junction as transistor 18. Additionally, the capacitance value may be increased by forming another parallel capacitor using a dielectric layer 33, such as an interlayer dielectric, and

a conductor 34. This capacitor would be in parallel with the junction capacitor. Typically the interlayer dielectric breakdown voltage is well in excess of 100V and facilitates forming a high breakdown voltage for capacitor 21.

FIG. 4 schematically illustrates an enlarged plan view of a portion of an embodiment of a semiconductor device 40 that is formed on a semiconductor die 41. Die 41 includes substrate 30, layer 31, and well 32. Protection circuit 10 is formed on die 41. In most embodiments, load 11 is external to die 41. Die 41 may also include other circuits that are not shown in FIG. 4 for simplicity of the drawing.

In view of all of the above, it is evident that a novel device and method is disclosed. Included, among other features, is disabling an output transistor when a short circuit is detected. Coupling the short circuit voltage to a gate of a disable transistor facilitates quickly disabling the load transistor and preventing damage to the load.

While the invention is described with specific preferred embodiments, it is evident that many alternatives and variations will be apparent to those skilled in the semiconductor arts. More specifically the invention has been described for a particular N channel power transistor structure, although the method is directly applicable to other transistors.

CLAIMS

1. A method of forming a protection circuit comprising:

forming a first transistor to couple a load return of the protection circuit to a voltage return of the protection circuit; and

coupling a second transistor to disable the first transistor when a voltage value of the load return exceeds a first voltage value.

2. The method of claim 1 wherein coupling the second transistor to disable the first transistor when the voltage value of the load return exceeds the first voltage value includes forming the protection circuit to couple the voltage value of the load return to a control electrode of the second transistor.

3. The method of claim 2 wherein forming the protection circuit to couple the voltage value of the load return to the control electrode of the second transistor includes forming a capacitor coupled between the control electrode of the second transistor and the load return and coupling a resistor to discharge the capacitor.

4. The method of claim 2 further including forming the protection circuit to disable the first transistor after a time period.

5. A method of protecting a circuit comprising:

enabling a first transistor to couple a load return of the circuit to a voltage return of the circuit; and

enabling a second transistor to disable the first transistor for a time period when a voltage value of the load return exceeds a first value.

6. The method of claim 5 further including disabling the second transistor after the time period expires.

7. The method of claim 5 wherein enabling the second transistor to disable the first transistor for the time period includes coupling the voltage value of the load return through a capacitor to a control electrode of the second transistor.

8. The method of claim 5 wherein enabling the first transistor to couple the load return to the voltage return includes enabling a vertical MOS power FET and wherein enabling the second transistor includes enabling a lateral MOS power FET.

9. A protection circuit comprising:

a voltage input;

a voltage return;

a load return;

a first transistor coupled between the load return and the voltage return, the first transistor having a control electrode;

a second transistor coupled between the control electrode of the first transistor and the voltage return, the second transistor having a control electrode; and

a capacitor coupled between the load return and the control electrode of the second transistor.

10. The protection circuit of claim 9 further including a resistor coupled between the control electrode of the second transistor and the voltage return.

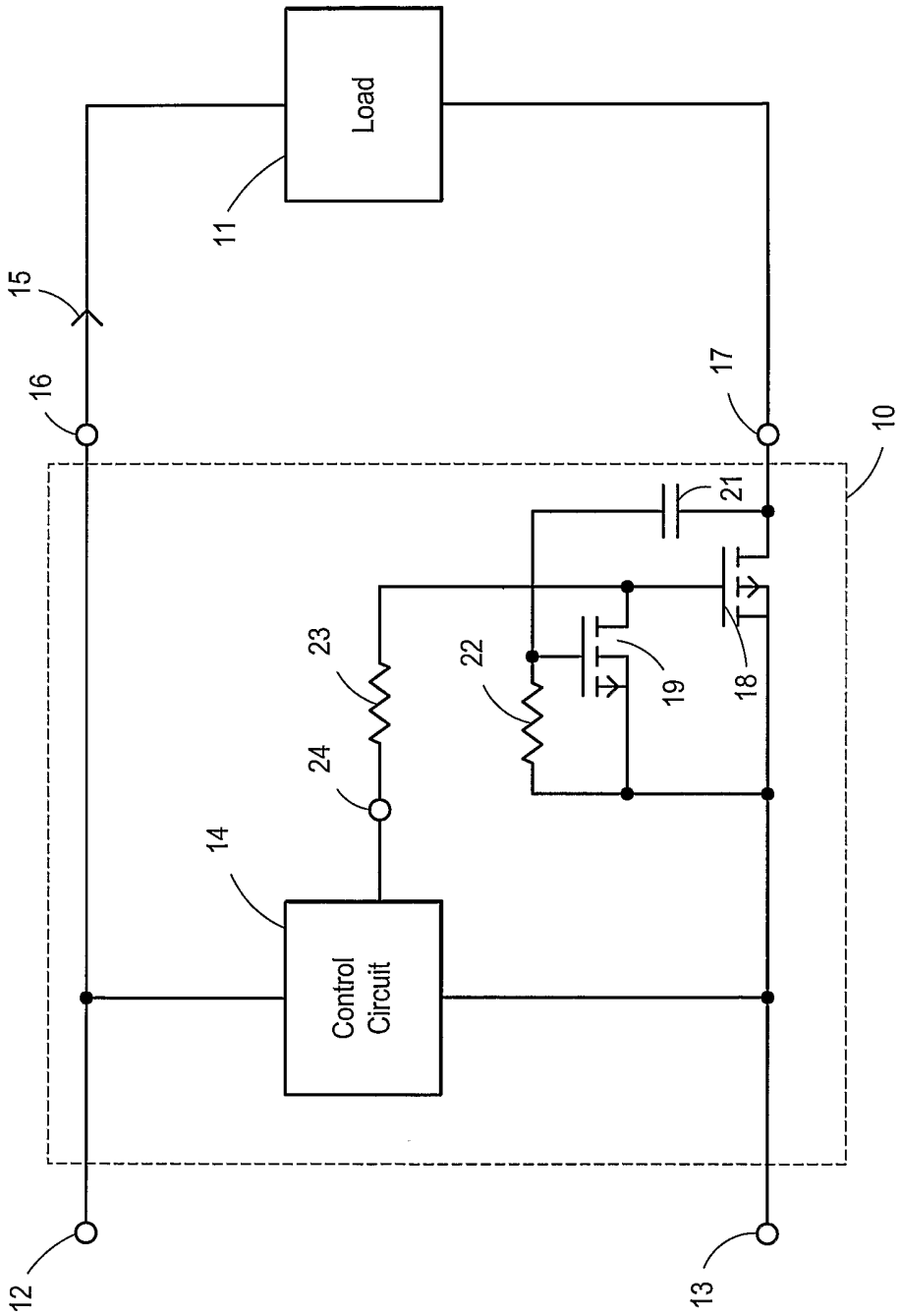


FIG. 1

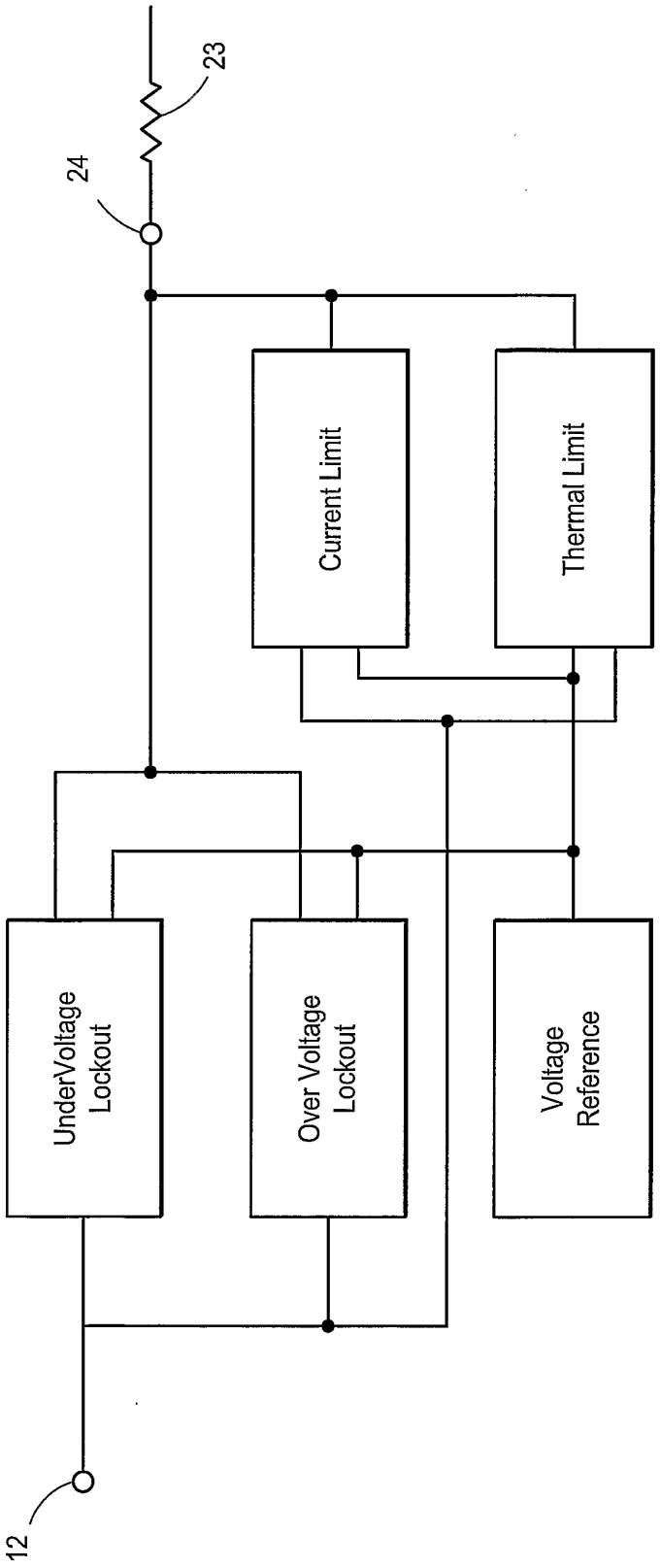

23
24
Current Limit
Thermal Limit
14
UnderVoltage Lockout
Over Voltage Lockout
Voltage Reference
12

FIG. 2

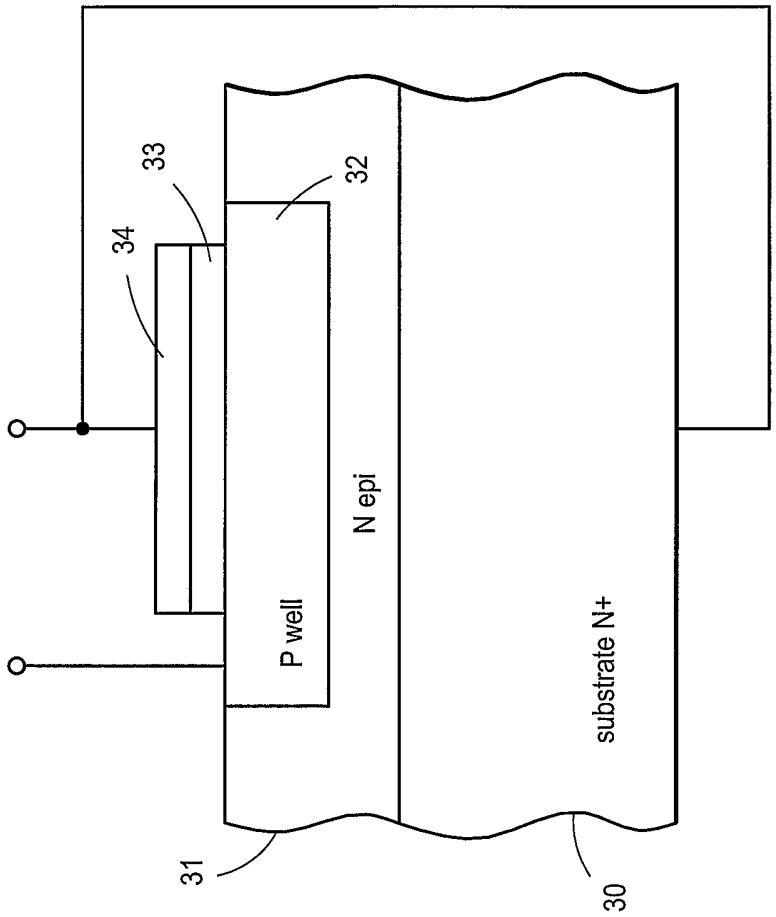


FIG. 3

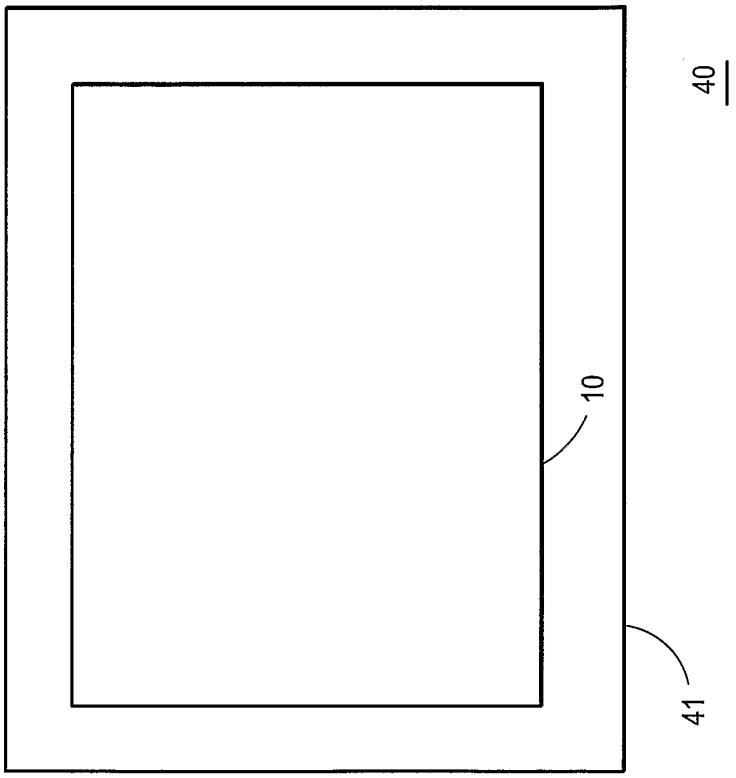


FIG. 4

INTERNATIONAL SEARCH REPORT

Inte ial Application No
PCT/US2004/012834

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02H9/00 H02H3/087

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"HOT-PLUG PROTECTION CIRCUIT" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 32, no. 9B, 1 February 1990 (1990-02-01), pages 424-429, XP000082404 ISSN: 0018-8689 page 427, paragraphs 4,5; figure	1-10
A	EP 0 356 186 A (STC PLC) 28 February 1990 (1990-02-28) figures 2,3	1,5,9

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 October 2004	29/10/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Salm, R

INTERNATIONAL SEARCH REPORT

Inter[illegible]al Application No
PCT/US2004/012834

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0356186 A	28-02-1990	EP 0356186 A2	28-02-1990
		GB 2222329 A	28-02-1990