



(51) International Patent Classification:
H01L 21/8232 (2006.01)

(21) International Application Number:
PCT/US2019/055328

(22) International Filing Date:
09 October 2019 (09.10.2019)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
16/156,769 10 October 2018 (10.10.2018) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 16/156,769 (CON)
Filed on 10 October 2018 (10.10.2018)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant (for JP only): **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).

(72) Inventor: **EDWARDS, Henry, Litzmann**; 705 Ballybunion Circle, Garland, TX 75044 (US).

(74) Agent: **ABRAHAM, Ebby et al.**; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,

(54) Title: LOCOS WITH SIDEWALL SPACER FOR TRANSISTORS AND OTHER DEVICES

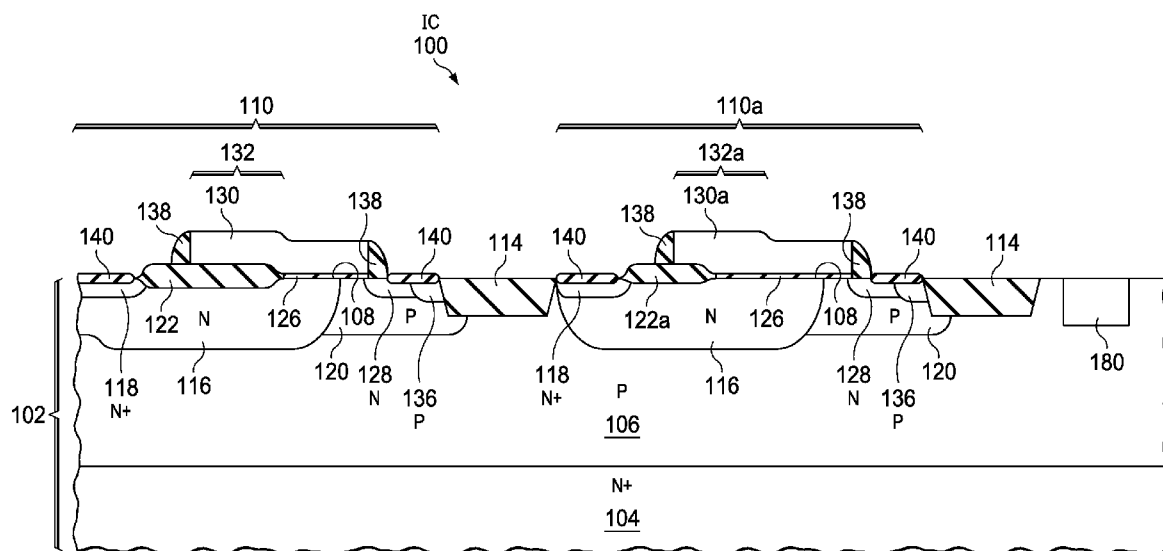


FIG. 1A

(57) Abstract: An integrated circuit (IC) (100) includes a first field-plated field effect transistor (FET) (110), and a second field-plated FET (110a), and functional circuitry (180) configured together with the field-plated FETs for realizing at least one circuit function in a semiconductor surface layer on a substrate (102). The field-plated FETs include a gate structure including a gate electrode (130, 130a) partially over a LOCOS field-relief oxide (122, 122a) and partially over a gate dielectric layer (126). The LOCOS field-relief oxide thickness for the first field-plated FET is thicker than the LOCOS field-relief oxide thickness for the second field-plated FET. There are sources (128) and drains (118) on respective sides of the gate structures in the semiconductor surface layer.

MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*

LOCOS WITH SIDEWALL SPACER FOR TRANSISTORS AND OTHER DEVICES

[0001] This Disclosure relates to integrated circuits having field-plated field effect transistors and other field-plated devices.

BACKGROUND

[0002] Some integrated circuits (ICs) contain field effect transistors (FETs) that have drift regions with a field relief oxide layer thereon that enables higher voltage operation. The drift regions deplete under high drain voltage conditions, allowing the FET to block the voltage applied between the drain and source while supporting conduction during the ON-state of the device. A higher voltage FET tends to be formed with the gate electrode extending over field oxide in order to act as a field plate for the drift region.

[0003] LOCAl Oxidation of Silicon (LOCOS) is a semiconductor fabrication oxidation process that uses a patterned oxygen diffusion barrier layer, commonly a silicon nitride layer, over areas not meant to be oxidized, where a thermally grown silicon dioxide layer is formed within aperture regions of the oxygen diffusion barrier layer at a given thickness, with a thinner tapered silicon oxide region being formed along the edges of the oxygen diffusion barrier layer. Although the active areas widths bordered by LOCOS oxide can be varied, LOCOS provides a single given oxide thickness across the die and across the wafer.

SUMMARY

[0004] This Summary is provided to introduce a brief selection of disclosed concepts in a simplified form that are further described below in the Detailed Description including the drawings provided. This Summary is not intended to limit the claimed subject matter's scope.

[0005] Disclosed aspects include an IC with a semiconductor surface layer on a substrate including a first field-plated FET, a second field-plated FET, and functional circuitry configured together with the field-plated FETs for realizing at least one circuit function. The field-plated FETs include a gate structure including a gate electrode partially over a LOCOS field relief oxide and partially over a gate dielectric layer. The LOCOS field relief oxide thickness for the first field-plated FET is thicker than the LOCOS field relief oxide thickness for the second field-plated FET. There are sources and drains on respective sides of the gate structures in the

semiconductor surface layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Reference will now be made to the accompanying drawings, which are not necessarily drawn to scale, wherein:

[0007] FIG. 1A is a cross sectional depiction of an example IC including a first and a second field-plated FET that have different LOCOS field relief oxide thicknesses, shown by example as being laterally diffused metal oxide semiconductor (LDMOS) devices, according to an example aspect.

[0008] FIG. 1B is a cross sectional depiction of an example IC including a first and a second power diode both made from the LDMOS devices shown in FIG. 1A that have different LOCOS field relief oxide thicknesses, according to an example aspect.

[0009] FIGS. 2A-2G are cross-sectional diagrams showing processing progression for an example method of forming an IC including a first and a second field-plated FET that have different LOCOS field relief oxide thicknesses, shown again by example as being LDMOS devices, according to an example aspect.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0010] Example aspects are described with reference to the drawings, wherein like reference numerals are used to designate similar or equivalent elements. Illustrated ordering of acts or events should not be considered as limiting, as some acts or events may occur in different order and/or concurrently with other acts or events. Furthermore, some illustrated acts or events may not be required to implement a methodology in accordance with this disclosure.

[0011] Also, the terms "coupled to" or "couples with" (and the like) as used herein without further qualification are intended to describe either an indirect or direct electrical connection. Thus, if a first device "couples" to a second device, that connection can be through a direct electrical connection where there are only parasitics in the pathway, or through an indirect electrical connection via intervening items including other devices and connections. For indirect coupling, the intervening item generally does not modify the information of a signal but may adjust its current level, voltage level, and/or power level.

[0012] Disclosed aspects recognize for field-plated FETs that have a field relief oxide to electronically isolate a field plate from the drift region, the thickness of this field relief oxide is important to the performance of the FET, such as its voltage rating. The field plate can comprise

polysilicon or a metal comprising material. The field-plated FET can also be configured as a power diode. An example of a field-plated power FET is a diffused (or drain extended) metal oxide semiconductor (DMOS) device, such as an LDMOS device, where the field-plated power FET can be an n-channel device or a p-channel device.

[0013] If the field relief oxide is too thin the field-plated FET's breakdown voltage (from D to G and S) will suffer, whereas if the field relief oxide is too thick the field plate will be ineffective at shaping the electric field lines in off-state, and the ON-resistance of the device will increase due to reduced carrier accumulation in ON-state. The field relief oxide thickness needed is thus recognized to vary depending upon the off-state drain voltage rating of the FET. For field-plated FETs integrated into a Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) process, this presents a cost and/or complexity problem, because multiple voltage rating power transistors need to co-exist in the same technology, including in some cases on the same IC product.

[0014] It is also recognized that known LOCOS approaches for forming field relief oxide have the disadvantage of only providing a single given oxide thickness, thus limiting the ability to support field-plated FETs that operate two or more drain voltages. This Disclosure describes a LOCOS process flow that utilizes sidewall spacers to produce two or more distinct LOCOS field relief oxide thicknesses, making disclosed LOCOS processing capable of providing good FET performance across a wider voltage range as compared to known LOCOS processes for forming a field relief oxide.

[0015] The sidewall spacers in different width oxygen diffusion barrier (ODB) layer openings to the silicon surface enable creating at least two different silicon oxide thicknesses from a single mask level and patterning step. The sidewall spacers (e.g., comprising silicon nitride) inside an ODB layer opening creates two (or more) different LOCOS oxide layer thicknesses, which depend on the width of the ODB layer opening. The width of the wider ODB layer opening is generally at least 0.05 μm wider than the width of the narrower ODB layer opening. For example, the ODB layer opening width can be 0.2 μm for a 9V rated LDMOS device, and can be 0.3 μm wide for an 11V rated LDMOS device.

[0016] FIG. 1A is a cross sectional depiction of an example IC 100 including a higher voltage rated n-channel field-plated FET 110 and a lower voltage rated n-channel field-plated FET 110a, shown by example as both being LDMOS devices, according to an example aspect. The IC 100 also includes functional circuitry 180 shown as a block that comprises circuit elements

(including transistors, and generally diodes, resistors, capacitors, etc.) formed in the semiconductor surface layer shown as a p-type layer 106 that is configured together with the field-plated FETs 110, 110a for realizing at least one circuit function such as analog (e.g., an amplifier, power converter or power FET, radio frequency (RF), digital, or a memory function.

[0017] Although a pair of n-channel field-plated FETs is described, an analogous p-channel field-plated FET is readily understood from the Disclosure with appropriate changes to the polarities of dopants. The IC 100 includes a substrate 102, with an optional heavily doped n-type (shown as n+) buried layer 104 and a p-type layer 106 over the n-type buried layer 104. The p-type layer 106 extends to a top surface 108 of the substrate 102. Although the IC 100 is shown including n-channel field-plated FET 110 and n-channel field-plated FET 110a, the IC 100 may also optionally include conventional planar FETs, such as within the functional circuitry 180. Components of the IC 100, such as the field-plated FET 110 and the field-plated FET 110a may be laterally separated by the field oxide 114 shown. The field oxide 114 may comprise a shallow trench isolation (STI) structure as depicted in FIG. 1A, or may also have a LOCOS oxide structure.

[0018] The field-plated FETs 110, 110a include an n-type drift region 116 disposed in the p-type layer 106. The drift region 116 extends from an n-type drain contact region 118 to a p-type body 120 of the field-plated FETs 110, 110a. An average dopant density of the drift region 116 may be, for example, $5 \times 10^{15} \text{ cm}^{-3}$ to $5 \times 10^{16} \text{ cm}^{-3}$. The drift region 116 may have a heavier-doped top portion and a lighter doped bottom portion, to provide desired values of breakdown voltage and specific resistance for the field-plated FETs 110, 110a. A layer of thicker LOCOS field relief oxide 122 shown having a LOCOS oxide bird's beak edge shape is disposed over the drift region 116 for the field-plated FET 110 and a layer of thinner LOCOS field relief oxide 122a as compared to the LOCOS field relief oxide 122 having a LOCOS oxide bird's beak edge shape is disposed over the drift region 116 for the field-plated FET 110a. Being LOCOS derived, the LOCOS field relief oxides 122, 122a have a tapered profile at their lateral edges, commonly referred to as a bird's beak. The LOCOS field relief oxides 122, 122a are generally thinner than the field oxide 114. The drift regions 116 extend past the LOCOS field relief oxides 122, 122a by a lateral distance adjacent to the p-type body 120.

[0019] A gate dielectric layer 126 of the field-plated FET 110, 110a is disposed on the top surface 108 of the substrate 102, extending from the LOCOS field relief oxide 122, 122a to an n-

type source 128 of the field-plated FETs 110, 110a abutting the body 120 opposite from the drift region 116. The gate dielectric layer 126 is disposed over a portion of the drift region 116 which extends past the LOCOS field relief oxides 122, 122a, and over a portion of the body 120 between the drift region 116 and the source 128. The LOCOS field relief oxide 122, 122a thickness are both generally at least twice as thick as the gate dielectric layer 126.

[0020] The field-plated FETs 110, 110a each include a gate electrode 130, 130a disposed over the gate dielectric layer 126, extending from the source 128, over the portion of the body 120 between the drift region 116 and the source 128, and over the portion of the drift region 116 which extends past the LOCOS field relief oxide 122. In the instant example, the gate electrodes 130, 130a extends partway over the LOCOS field relief oxide 122, 122a, to provide a field plate 132, 132a over a portion of the drift region 116. In an alternate version of the instant example, the field plate may be provided by a separate structural element from the gate electrodes 130, 130a. The thicknesses of the respective LOCOS field relief oxide 122, 122a may be separately selected to provide a desired maximum value of electric field in the drift region 116 during operation of the field-plated FETs 110, 110a.

[0021] The field-plated FETs 110, 110a may also include a p-type body contact region 136 disposed in the substrate 102 in the body 120. Gate sidewall spacers 138 may be disposed on side surfaces of the gate 130. A metal silicide 140 may be disposed on the drain contact region 118, the source 128, and the body contact region 136. The field-plated FETs 110, 110a may have a drain-centered configuration in which the drain contact region 118 that is surrounded by the LOCOS field relief oxide 122, 122a which is surrounded by the body 120 and the source 128. Other configurations of the field-plated FET 110, 110a are within the scope of the instant example.

[0022] FIG. 1B is a cross sectional depiction of an example IC 150 including a first power diode 110' and a second power diode 110a' both made from the LDMOS devices referred to as field-plated FETs 110, 110a in FIG. 1A that have different LOCOS field relief oxide thicknesses, according to an example aspect. As known in power electronics, a power diode can be made from a power MOS device such as an LDMOS device by grounding the gate, such as using a metal 1 connection, and optionally also grounding the source, to a ground node on the IC, with the gates 130, 130a and sources 128 shown in FIG. 1B as being connected to a "GND node" that

is on the IC 150. Being power diodes there is also the option to also remove the sources 128, although the sources 128 are shown in FIG. 1B. The diode junction utilized by power diodes 110' and 110a' is between the drift region 116 which for an NLD MOS device is the n-type side that is contacted by the drain contact 118 and the p-type layer 106 generally through a p+ contact (not shown).

[0023] FIGS. 2A through FIG. 2G are successive cross sections of the field-plated FETs 110, 110a of the IC 100 shown in FIG. 1A, depicting successive stages of an example method of formation. Referring to FIG. 2A, the substrate 102 may be formed by starting with a p-type silicon wafer, possibly with at least one epitaxial layer thereon, and forming the n-type buried layer 104 by ion implanting n-type dopants such as antimony or arsenic at a dose of $1 \times 10^{15} \text{ cm}^{-2}$ to $1 \times 10^{16} \text{ cm}^{-2}$. A thermal drive process heats the wafer to activate and diffuse the implanted n-type dopants. The p-type layer 106 may be formed on the wafer by an epitaxial process with in-situ p-type doping. The epitaxially formed material may be, for example 4 microns to 6 microns thick. The n-type dopants diffuse partway into the epitaxially grown material, so that the n-type buried layer 104 overlaps a boundary between the original silicon wafer and the epitaxially grown material. An average bulk resistivity of the p-type layer 106 may be, for example, 1 ohm-cm to 10 ohm-cm. An optional p-type buried layer may be formed in the p-type layer 106 by implanting boron at an energy, for example, of 2 mega-electron volts (MeV) to 3 MeV.

[0024] The field oxide 114 is formed at the top surface 108 of the substrate 102, for example by an STI process or a LOCOS process. An example STI process includes forming a chemical mechanical polish (CMP) stop layer of silicon nitride and a layer of STI pad oxide over the substrate 102. Isolation trenches are etched through the CMP stop layer and the STI pad oxide and into the substrate 102. The isolation trenches are filled with silicon dioxide using a plasma enhanced chemical vapor deposition (PECVD) process using tetraethyl orthosilicate (TEOS), a high density plasma (HDP) process, a high aspect ratio process (HARP) using TEOS and ozone, an atmospheric chemical vapor deposition (APCVD) process using silane, or a sub-atmospheric chemical vapor deposition (SACVD) process using dichlorosilane (SiH_2Cl_2). Excess silicon dioxide is generally removed from over the CMP stop layer by an oxide CMP process. The CMP stop layer is subsequently removed, leaving the field oxide 114. An example LOCOS process includes forming a silicon nitride mask layer over a layer of LOCOS pad oxide over the

substrate 102. The silicon nitride mask layer is removed in areas for the field oxide 114, exposing the LOCOS pad oxide. Silicon dioxide is formed in the areas exposed by the silicon nitride mask layer by thermal oxidation, to form the field oxide 114. The silicon nitride mask layer is subsequently removed, leaving the field oxide 114 in place.

[0025] A layer of pad oxide 158 is formed at the top surface 108 of the substrate 102. The pad oxide 158 may be, for example, 20 to 250Å thick, 100Å thick being typical, and may be formed by thermal oxidation or by any of several chemical vapor deposition (CVD) processes. A first ODB layer 160 is formed over the layer of pad oxide 158. The first ODB layer 160 may include, for example, silicon nitride, formed by a low pressure chemical vapor deposition (LPCVD) process using dichlorosilane and ammonia. Alternatively, silicon nitride for the first ODB layer 160 may be formed by decomposition of bis(tertiary-butyl-amino) silane (BTBAS). Other processes to form the first ODB layer 160 are possible.

[0026] An etch mask 162 is formed over the first ODB layer 160 which exposes an area of the top surface 108 of the substrate 102 for growing the LOCOS field relief oxide 122, 122a of FIG. 1A in the area for the field-plated FETs 110, 110a. The etch mask 162 may include photoresist formed by a photolithography process, and may also include hard mask material such as amorphous carbon, and may include an anti-reflection layer such as an organic bottom anti-reflection coat (BARC). The exposed area of the top surface 108 of the substrate 102 for the LOCOS field relief oxide 122 for the field-plated FETs 110 has lateral dimensions that are sufficiently wide so that after etching the first ODB layer 160, a central portion of the etched area remains clear after formation of dielectric sidewalls.

[0027] The first ODB layer 160 is removed in the areas exposed by the etch mask 162, exposing the layer of pad oxide 158. A portion of the pad oxide 158 may also be removed in the areas exposed by the etch mask 162. Removing the first ODB layer 160 in the area for the field-plated FETs 110, 110a forms different width openings in the first ODB layer 160 comprising a 1st first ODB layer opening 164 for field-plated FET 110 shown relatively wider and a 2nd first ODB layer opening 164a for field-plated FET 110a shown relatively narrower in width.

[0028] The first ODB layer 160 may be removed by a wet etch, for example an aqueous solution of phosphoric acid, which undercuts the etch mask 162 as depicted in FIG. 2A. Alternatively, the first ODB layer 160 may be removed by a plasma etch using fluorine radicals, which may produce less undercut. The etch mask 162 may optionally be removed after etching

the first ODB layer 160, or may be left in place to provide additional stopping material in a subsequent ion implant step. At this point there is an option for a silicon etch by etching the pad oxide 158 to expose the top surface 108 in the first ODB layer openings 164, 164a and performing a silicon etch in the openings before the first LOCOS process described below to enable deeper current flow for the field-plated FETs 110, 110a.

[0029] Referring now to FIG. 2B, this FIG. shows the results after growing a first LOCOS layer 122', 122a with a typical thickness of 200 to 1,000Å, so that a first portion of the LOCOS field relief oxide 122', 122a providing the first LOCOS layer is formed by thermal oxidation in the 1st first ODB layer opening 164 in the area for the field-plated FET 110 and in 2nd first ODB layer opening 164a in the area for the field-plated FET 110a, both growing essentially the same the LOCOS field relief oxide thickness. The LOCOS field relief oxides 122', 122a providing first LOCOS layer has the characteristic LOCOS oxidation bird's beaks shown.

[0030] An example furnace thermal oxidation process for growing a first LOCOS oxide layer may include ramping a temperature of the furnace to about 1000° C in a time period of 45 minutes to 90 minutes with an ambient of 2 percent to 10 percent oxygen, maintaining the temperature of the furnace at about 1000° C for a time period of 10 minutes to 20 minutes while increasing the oxygen in the ambient to 80 percent to 95 percent oxygen, maintaining the temperature of the furnace at about 1000° C for a time period of 60 minutes to 120 minutes while maintaining the oxygen in the ambient at 80 percent to 95 percent oxygen and adding hydrogen chloride gas to the ambient, maintaining the temperature of the furnace at about 1000° C for a time period of 30 minutes to 90 minutes while maintaining the oxygen in the ambient at 80 percent to 95 percent oxygen with no hydrogen chloride, and ramping the temperature of the furnace down in a nitrogen ambient.

[0031] There can be an optional self-aligned (un-masked) ion implant before the depositions described below, to place boron below what will later be formed a drift region (see drift region 116 in FIG. 1A described above). For an NMOS device, this ion implantation can comprise boron at 200 keV to 2 MeV at a dose level of $5 \times 10^{11} \text{ cm}^{-2}$ to $5 \times 10^{12} \text{ cm}^{-2}$.

[0032] FIG. 2C shows results after depositing a second ODB layer 181 and then depositing a sacrificial sidewall film 182 thereon that functions as a sacrificial sidewall layer. The second ODB layer 181 can comprise silicon nitride (SiN) that is 100 to 500Å thick. The sacrificial sidewall film 182 can comprise polysilicon or a dielectric material, such as being 400 to 1,500Å

thick.

[0033] FIG. 2D shows results after patterning, generally using photoresist, and then etching the sacrificial sidewall film 182 to form sidewall spacers 182a in the 1st first ODB layer opening 164, but not forming sidewall spacers shown as a continuous region of the sacrificial sidewall film 182 and second ODB layer 181 in the 2nd first ODB layer opening 164a, and then removing the 2nd ODB layer 181 in the 1st first ODB layer opening 164 to form spacers 181a under the sidewall spacers 182a where not protected by the sacrificial sidewall film 182.

[0034] FIG. 2E shows results after stripping the sacrificial sidewall film 182 and sidewall spacers 182a shown in FIG. 2D, where the spacers 181a are still in the 1st first ODB layer opening 164. FIG. 2F shows results after growing a second LOCOS oxide layer resulting in an additional LOCOS portion shown as LOCOS 2 having a portion above and below the LOCOS field relief oxide 122' being previously formed LOCOS oxide to together provide the LOCOS field relief oxide 122, generally being 500 to 1,500Å of LOCOS 2 at the center of the 1st first ODB layer opening 164 for FET 110, with no LOCOS 2 shown grown in the 2nd first ODB layer opening 164a due to the presence of the second ODB layer 181 over the whole opening.

[0035] Thus for the 2nd first ODB layer opening 164a being narrower the sidewalls of the second ODB layer 181 remain merged so that only the first LOCOS oxidation process is able to oxidize the exposed silicon at the top surface 108 of the substrate 102. This thinner oxide is used to form the LOCOS field relief oxide for the lower voltage FET 110a. For the 1st first ODB layer opening 164 which is wider than the 2nd first ODB layer opening 164a, the sidewalls of the second ODB layer are distinct to provide spacers 181a, so that the second LOCOS oxidation can thicken the LOCOS layer in the 1st first ODB layer opening 164. The LOCOS oxide will be tapered under the spacers 181a, which is equivalent to a bird's beak region that is controlled by the spacer thickness. This thicker LOCOS oxide is used to form the LOCOS field relief oxide for the higher voltage field-plated FET 110.

[0036] This completes the LOCOS field relief oxide 122, 122a thickness so that the LOCOS field relief oxide 122 is thicker for the field-plated FET 110 as compared to the LOCOS field relief oxide 122a thickness for the field-plated FET 110a. FIG. 2G shows results after removing the first ODB layer 160 and the second ODB layer 181 and spacers 181a.

[0037] Described below is front-end-of-the-line (FEOL) LDMOS processing to complete formation of the field-plated FETs 110, 110a, comprising forming a gate structure for the first

field-plated field FET 110 with its gate partially over the LOCOS layer 122 and a gate structure for second field-plated field FET 110a with its gate partially over the LOCOS layer 122a, and then forming sources and drains. The p-type body 120 of the field-plated FETs 110, 110a are formed. The p-type body 120 may be formed by implanting p-type dopants implanted through the LOCOS field relief oxide 122, 122a such as boron at one or more energies, to provide a desired distribution of the p-type dopants. An example implant operation may include a first implant of boron at a dose of $1 \times 10^{14} \text{ cm}^{-2}$ to $3 \times 10^{14} \text{ cm}^{-2}$ at an energy of 80 keV to 150 keV, and a second implant of boron at a dose of $1 \times 10^{13} \text{ cm}^{-2}$ to $3 \times 10^{13} \text{ cm}^{-2}$ at an energy of 30 keV to 450 keV. A subsequent anneal process, such as a rapid thermal anneal at 1000° C for 30 seconds, activates and diffuses the implanted boron.

[0038] A layer of gate dielectric material shown as 126 in FIG. 1A is formed on exposed semiconductor material at the top surface 108 of the substrate 102, including in the areas for the field-plated FETs 110, 110a. The layer of gate dielectric material 126 may include silicon dioxide, formed by thermal oxidation, and/or hafnium oxide or zirconium oxide, formed by CVD processes, and may include nitrogen atoms introduced by exposure to a nitrogen-containing plasma. A thickness of the layer of gate dielectric material 126 reflects operating voltages of the field-plated FETs 110, 110a. A layer of gate electrode material shown as 130 in FIG. 1A is formed over the layer of gate dielectric material 126 and the LOCOS field relief oxides 122, 122a. The layer of gate electrode material 130 may include, for example, polycrystalline silicon, referred to herein as polysilicon, possibly doped with n-type dopants. Other gate materials, such as titanium nitride or other metal comprising material for the layer of gate electrode material 130 are within the scope of the instant example. Polysilicon as the layer of gate electrode material 130 may be, for example, 300 nanometers to 800 nanometers thick.

[0039] A gate mask is then formed over the layer of gate electrode material 130 to cover areas for the gates for the field-plated FETs 110, 110a. The gate mask can extend partway over the LOCOS field relief oxides 122, 122a to cover an area for the field plate 132 of FIG. 1A. The gate mask may include photoresist formed by a photolithographic process. The gate mask may also include a layer of hard mask material such as silicon nitride and/or amorphous carbon. Further, the gate mask may include a layer of anti-reflection material, such as a layer of BARC.

[0040] A gate etch process is performed which removes the layer of gate electrode material where exposed by the gate mask, to form the gate electrodes 130 of the field-plated

FETs 110, 110a. The gate etch process may be, for example, a reactive ion etch (RIE) process using fluorine radicals.

[0041] Gate sidewall spacers shown as 138 in FIG. 1A may be formed on side surfaces of the gates of the field-plated FETs 110, 110a by forming a conformal layer of sidewall material, possibly comprising more than one sub-layer of silicon nitride and/or silicon dioxide, over the gate electrode 130 and the top surface 108 of the substrate 102. Subsequently, an anisotropic etch such as a reactive ion etch (RIE) process removes the layer of sidewall material from top surfaces of the gate electrode 130 and the substrate 102, leaving the gate sidewall spacers 138 in place.

[0042] The n-type source 128 and n-type drain contact region 118 of the field-plated FETs 110, 110a may be formed by implanting n-type dopants such as phosphorus and arsenic, for example at a dose of $1 \times 10^{14} \text{ cm}^{-2}$ to $5 \times 10^{15} \text{ cm}^{-2}$ into the substrate 102 adjacent to the gate electrode 130 and the LOCOS field relief oxides 122, 122a, followed by an anneal operation, such as a spike anneal or a flash anneal, to activate the implanted dopants. An n-type drain extension portion of the source 128 which extends partway under the gate electrode 130 may be formed prior to forming the gate sidewall spacers 138 by implanting n-type dopants into the substrate adjacent to the gate electrodes 130, 130a.

[0043] The p-type body contact region 136 in the body 120 of the field-plated FETs 110, 110a may be formed by implanting p-type dopants such as boron, for example at a dose of $1 \times 10^{14} \text{ cm}^{-2}$ to $5 \times 10^{15} \text{ cm}^{-2}$ into the substrate 102, followed by an anneal operation, such as a spike anneal or a flash anneal, to activate the implanted dopants. The drift region 116 shown in FIG. 1A can then formed to be self-aligned with the LOCOS field relief oxides 122, 122a to provide a desired low value of the lateral distance that the gate overlaps the drift region 116, advantageously providing a low gate-drain capacitance. Alternatively, the drift region 116 may be formed at a significantly earlier stage of the process. Further, the self-aligned configuration may provide the lateral distance to be controllable from device to device without undesired variability due to unavoidable photolithographic alignment variations, sometimes referred to as alignment errors.

[0044] Applied to BiMOS processes, particularly for deep submicron processes, it is recognized that they need separate isolation oxides for CMOS device-to-device isolation (usually shallow-trench isolation or STI is used to isolate CMOS devices) and field plate formation for an

LDMOS power transistor or other drain extended transistor. Some recent technology nodes have used a thin LOCOS layer to isolate the polysilicon field plate from the drift region. However the performance scaling in terms of specific on-resistance (RSP) general requires smaller half-pitches and more vertical current flow paths, similar to what the state-of-the-art discrete LDMOS transistors such as NEXFET power transistors from Texas Instruments use. To support these needs, a field relief oxide for LDMOS is needed that allows (i) a smaller and more controllable bird's beak region and (ii) a deeper, rounded bottom edge to support deeper current flow. Furthermore, integrated power technologies generally need a range of LDMOS voltage ratings to be supported. Therefore it is advantageous to have the disclosed ability to create more than one thickness of LOCOS field relief oxide as described in this Disclosure.

[0045] Disclosed aspects can be used to form semiconductor die that may be integrated into a variety of assembly flows to form a variety of different devices and related products. The semiconductor die may include various elements therein and/or layers thereon, including barrier layers, dielectric layers, device structures, active elements and passive elements including source regions, drain regions, bit lines, bases, emitters, collectors, conductive lines, conductive vias, etc. Moreover, the semiconductor die can be formed from a variety of processes including bipolar, Insulated Gate Bipolar Transistor (IGBT), CMOS, BiCMOS and MEMS.

[0046] Those skilled in the art to which this Disclosure relates will appreciate that many other aspects are possible within the scope of the claimed invention, and further additions, deletions, substitutions and modifications may be made to the described aspects without departing from the scope of this Disclosure.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit (IC), comprising:
 - depositing a first oxygen diffusion barrier (ODB) layer on a pad oxide layer on a semiconductor surface layer on a substrate;
 - patterning and then etching the first ODB layer stopping on the pad oxide to form a 1st first ODB layer opening and at least a 2nd first ODB layer opening, wherein the 1st first ODB layer opening has a width that is larger than a width of the 2nd first ODB layer opening;
 - growing a first LOCOS layer in the 1st first ODB layer opening and in the 2nd first ODB layer opening;
 - depositing a second ODB layer and then depositing a sacrificial sidewall film on the second ODB layer;
 - etching the sacrificial sidewall film to form a spacer in the 1st first ODB layer opening but not in the 2nd first ODB layer opening which remains blocked by the sacrificial sidewall film and removing the second ODB layer where not protected by the sacrificial sidewall film;
 - stripping the sacrificial sidewall film;
 - growing a second LOCOS layer in the 1st first ODB layer opening but not in the 2nd first ODB layer opening;
 - removing the first and the second ODB layer, and
 - forming a gate structure including a gate electrode for a first field-plated field effect transistor (FET) with its gate electrode partially over the first and second LOCOS layer and a gate structure for a second field-plated FET in with its gate electrode partially over the first LOCOS layer, and then forming sources and drains.
2. The method of claim 1, further comprising stripping the pad oxide in the 1st first ODB layer opening and in 2nd first ODB layer opening, and then etching the semiconductor surface layer to a predetermined depth.
3. The method of claim 1, further comprising between growing the first LOCOS layer and the depositing the second ODB layer self-aligned ion implanting into the semiconductor surface layer.
4. The method of claim 1, further comprising after etching the sacrificial sidewall film at least partially etching the first LOCOS layer where exposed by the spacer.

5. The method of claim 1, wherein a thickness of the first LOCOS layer is 200 to 1,000 Å.
6. The method of claim 1, wherein the first ODB layer and the second ODB layer both comprise silicon nitride.
7. The method of claim 1, wherein the width of the 1st first ODB layer opening is at least 0.05 µm greater than the width of the 2nd first ODB layer opening.
8. The method of claim 1, wherein the first ODB layer comprises silicon nitride and is 300 to 2,000 Å thick.
9. The method of claim 1, wherein the gate electrode comprises polysilicon.
10. The method of claim 1, further comprising connecting sources of the first field-plated FET and second field-plated FET to a ground node on the IC so that the first field-plated FET and second field-plated FET are configured as power diodes.
11. An integrated circuit (IC), comprising:
 - a first field-plated field effect transistor (FET) and a second field-plated FET, the field-plated FETs comprising:
 - a gate structure including a gate electrode partially over a LOCOS field relief oxide and partially over a gate dielectric layer, wherein a thickness of the LOCOS field relief oxide for the first field-plated FET is thicker than the thickness of the LOCOS field relief oxide for the second field-plated FET, and
 - sources and drains on respective sides of the gate structures in the semiconductor surface layer.
12. The IC of claim 11, wherein the thickness of the LOCOS field relief oxide for the second field-plated FET 110a is 200 to 1,000 Å, and wherein the thickness for the LOCOS field relief oxide for the first field-plated FET is at least 500 Å thicker than the thickness for the LOCOS field relief oxide for the second field-plated FET.
13. The IC of claim 11, wherein said semiconductor surface layer is recessed under the LOCOS field relief oxide for the first field-plated FET and for the second field-plated FET.
14. The IC of claim 11, wherein the field-plated FETs comprise laterally diffused metal oxide semiconductor (LDMOS) devices.
15. The IC of claim 11, wherein a width of a second opening for the LOCOS field relief oxide for the second field-plated FET is at least 0.05 µm greater than a width of a first opening for the LOCOS field relief oxide for the second field-plated FET.

16. The IC of claim 11, wherein the gate electrode comprises polysilicon.
17. The IC of claim 11, wherein the semiconductor surface layer comprises an epitaxial layer.
18. The IC of claim 11, wherein the thickness of the LOCOS field relief oxides are both generally at least twice as thick as the gate dielectric layer.
19. The IC of claim 11, wherein the first and second field-plated FETs each comprise n-channel laterally diffused metal oxide semiconductor (LDMOS) devices.
20. The IC of claim 11, wherein sources of the first field-plated FET and second field-plated FET are connected to a ground node on the IC to be both configured as power diodes.

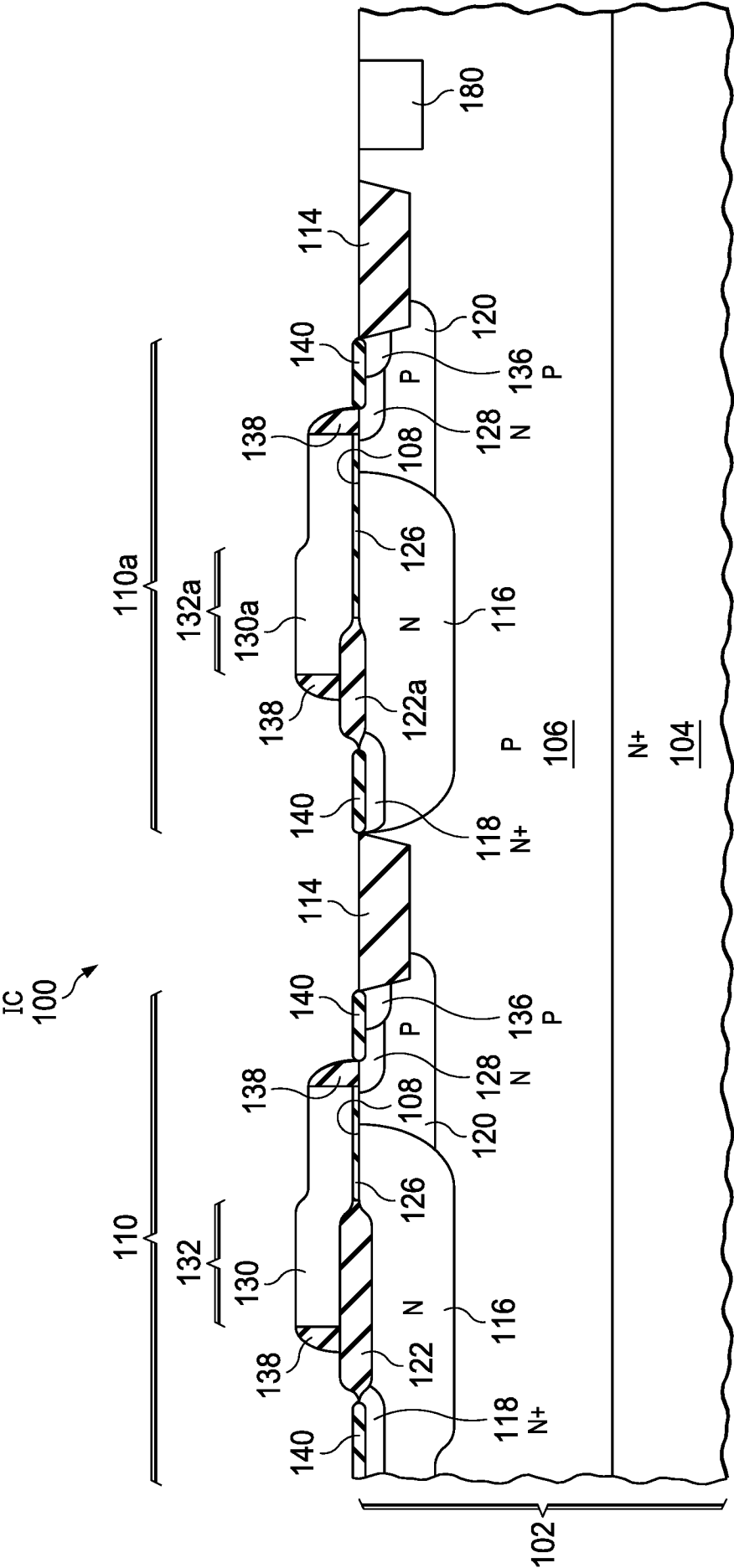


FIG. 1A

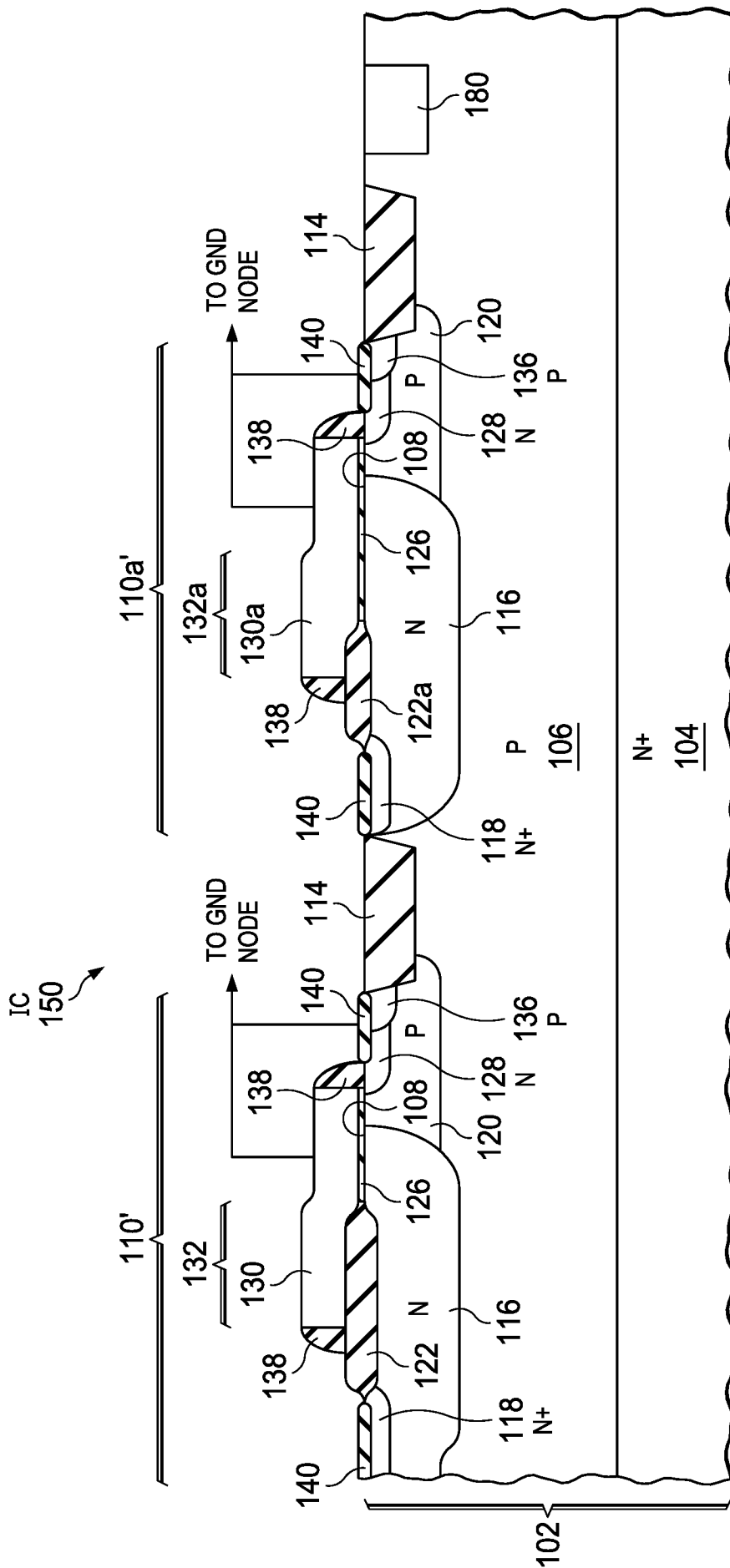


FIG. 1B

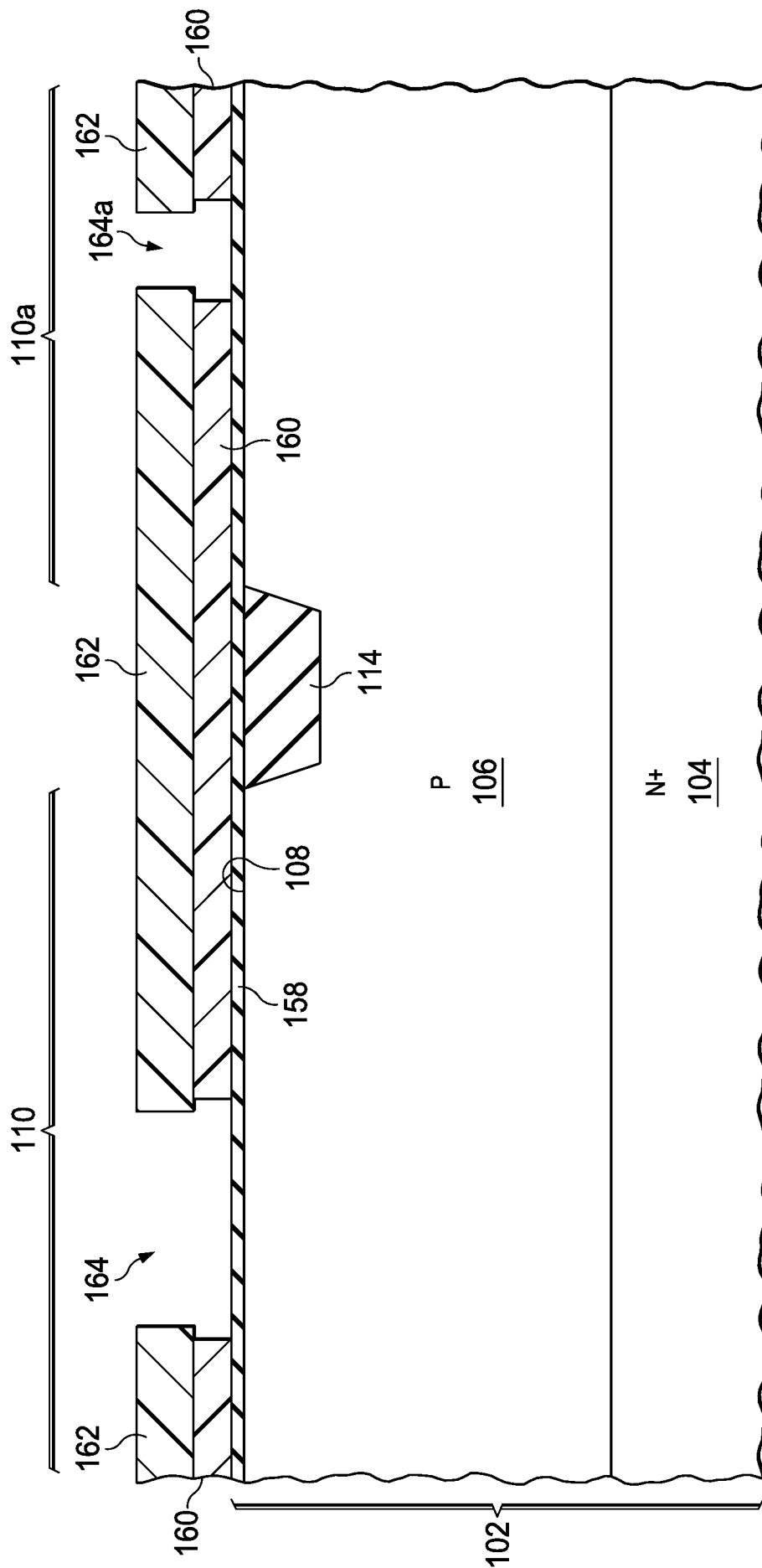


FIG. 2A

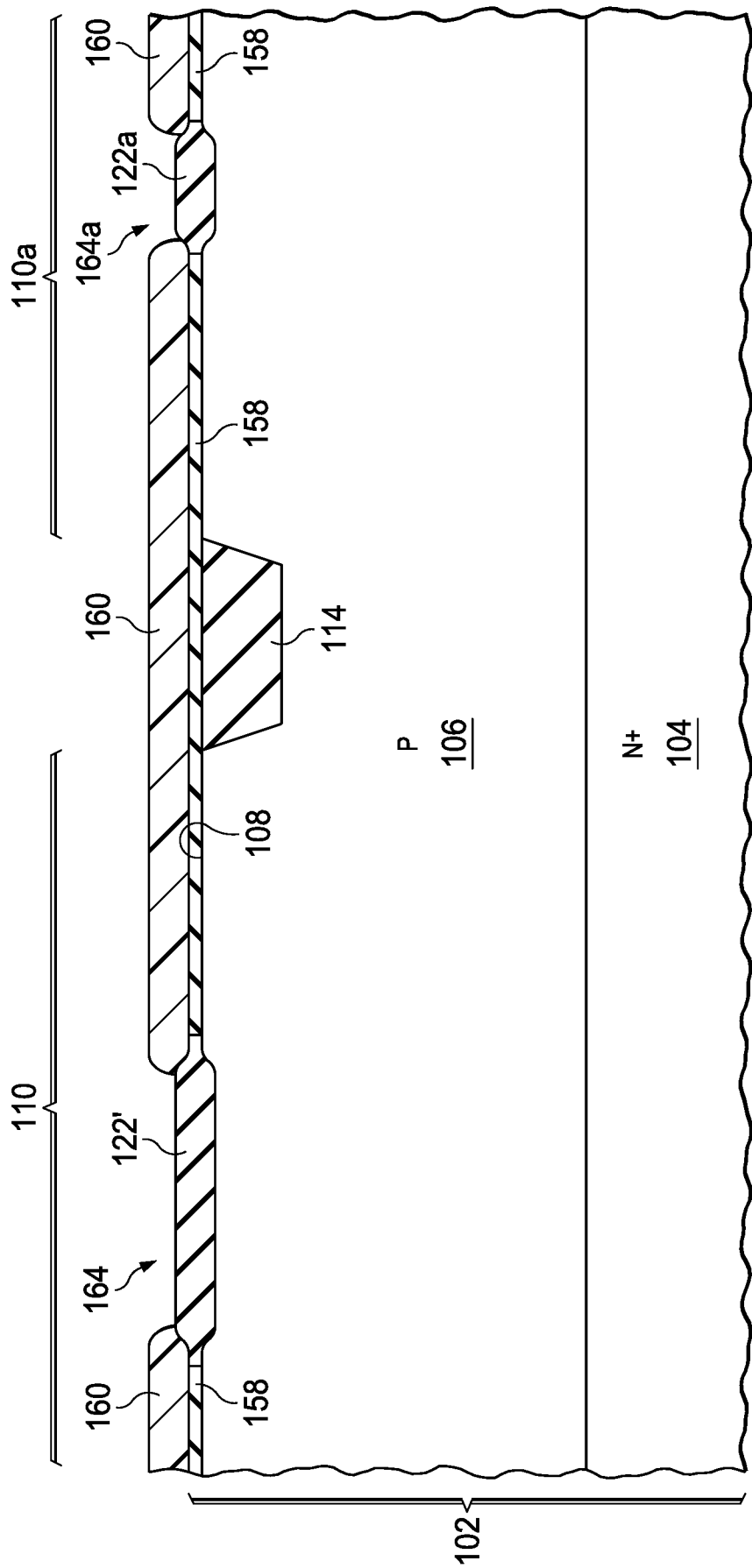


FIG. 2B

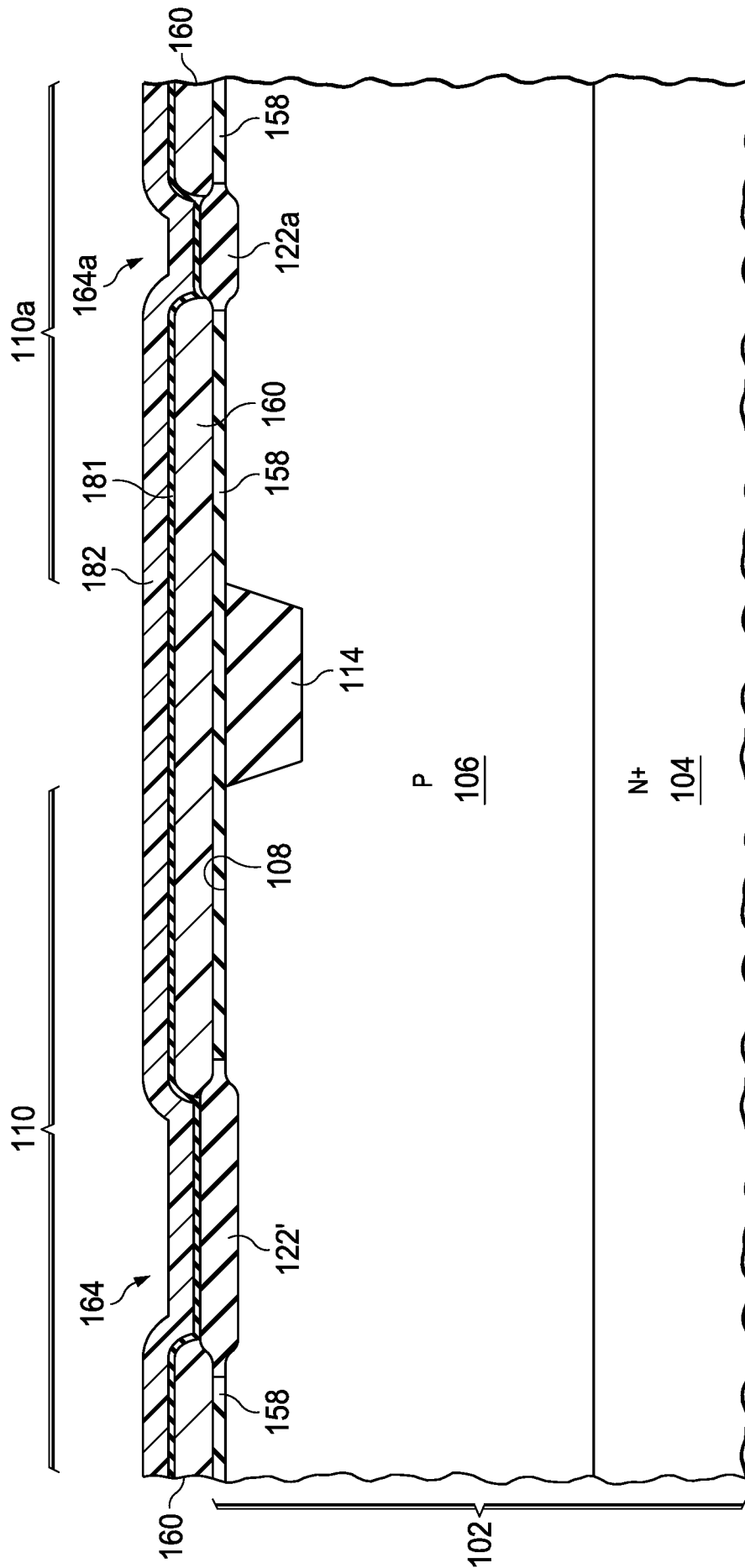


FIG. 2C

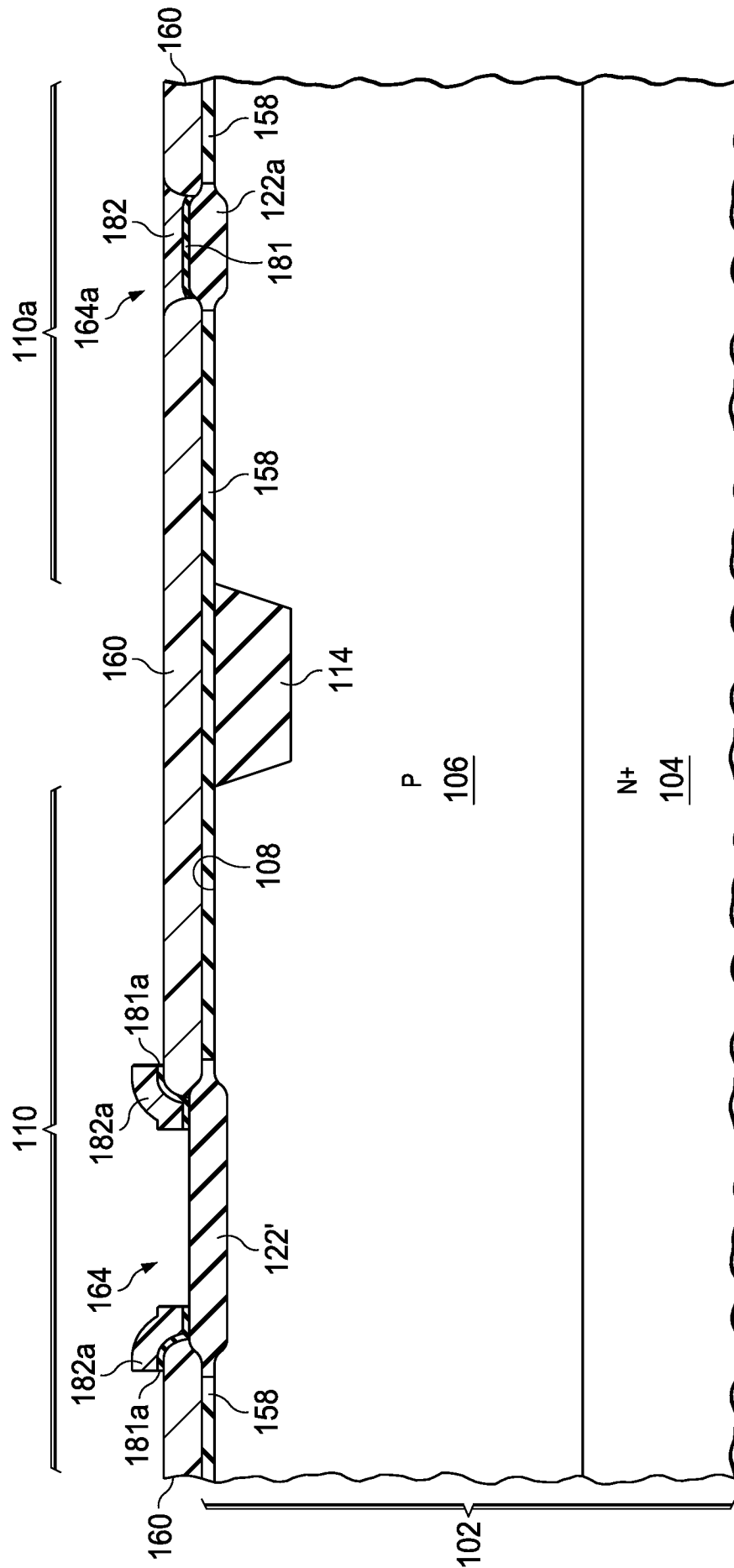


FIG. 2D

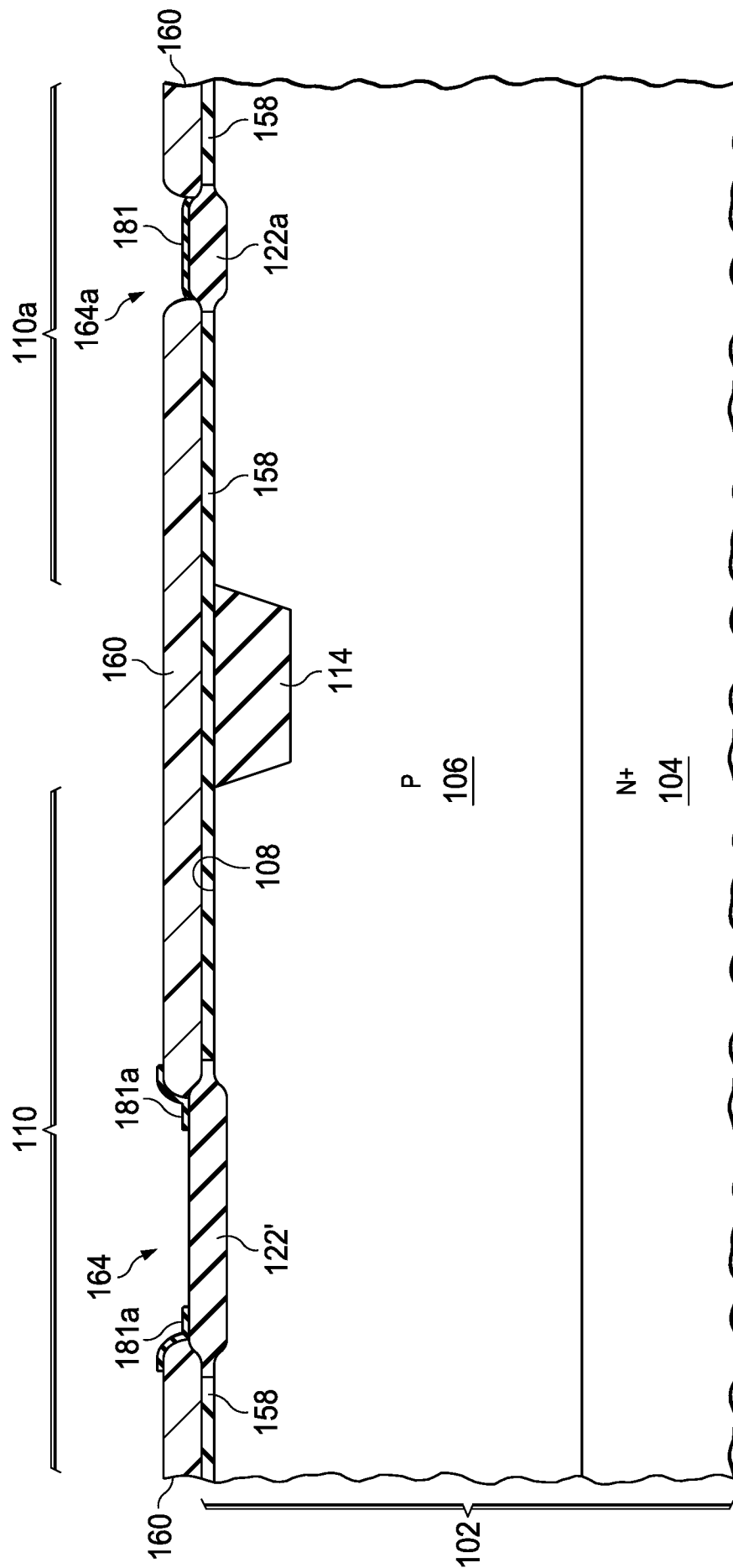


FIG. 2E

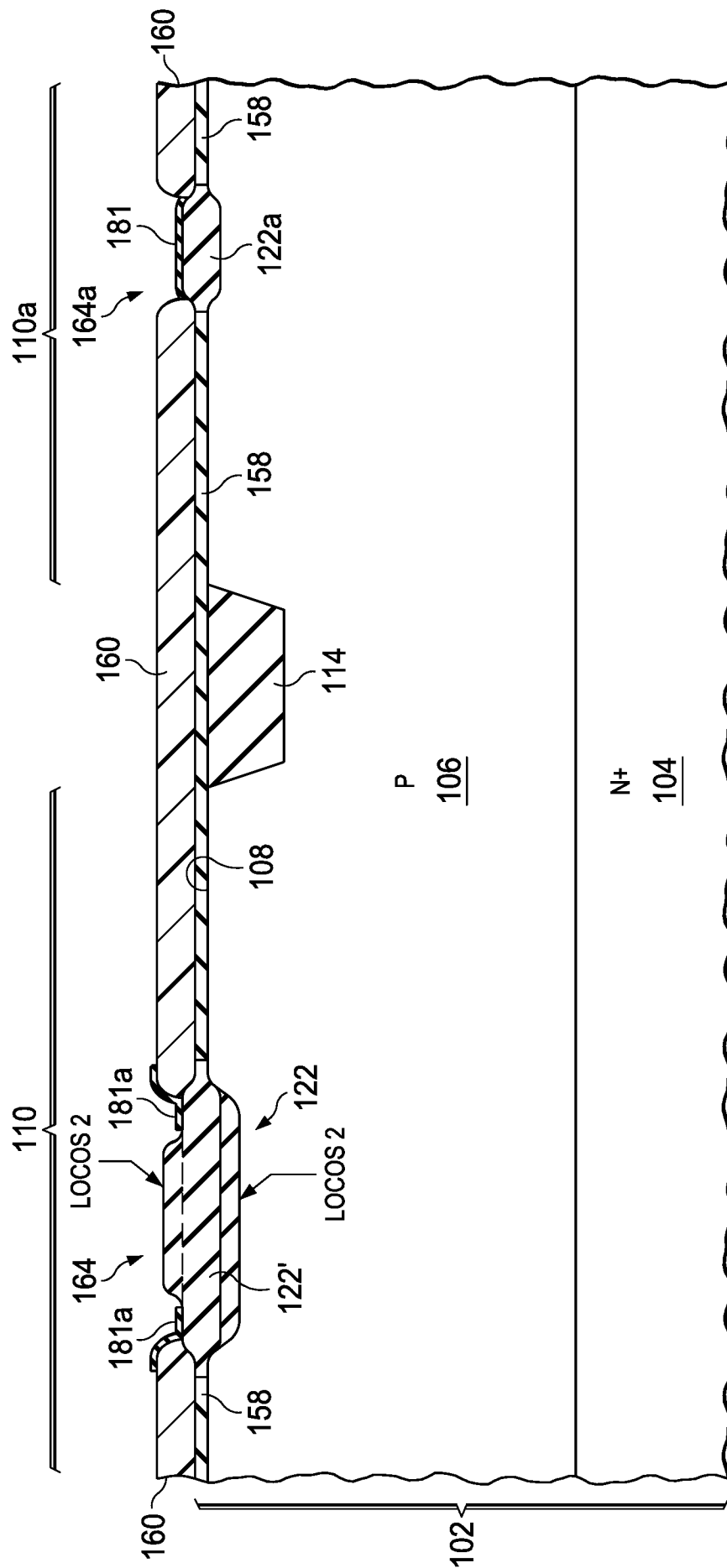


FIG. 2F

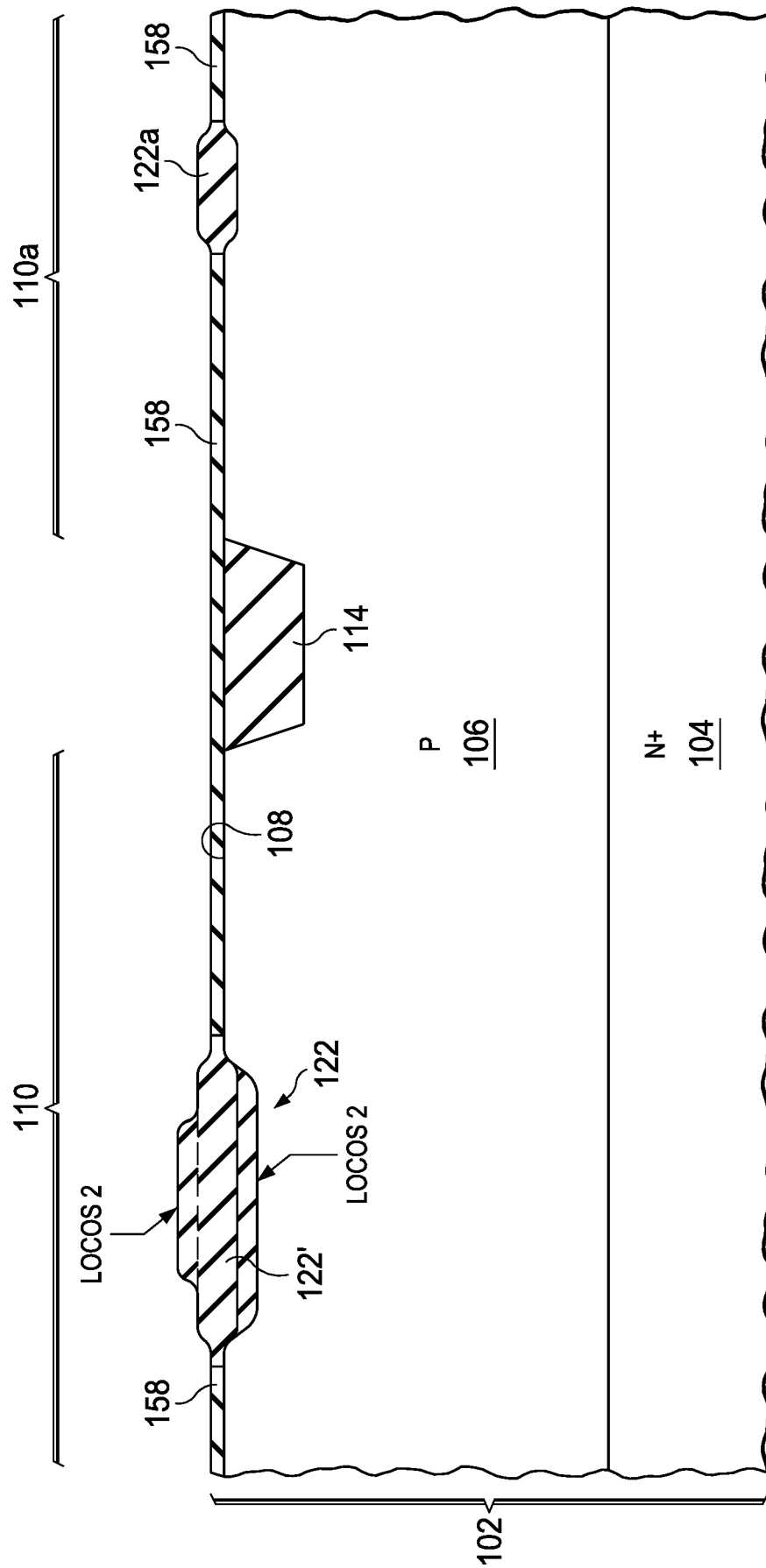


FIG. 2G

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2019/055328

A. CLASSIFICATION OF SUBJECT MATTER
H01L 21/8232 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/02, 21/265, 21/324, 21/82, 21/8232, 29/00, 29/06, 29/10, 29/40, 29/423, 29/66, 29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017/0213895 A1 (TEXAS INSTRUMENTS INCORPORATED) 27.07.2017	1-20
A	US 2016/0351699 A1 (NXP B.V.) 01.12.2016	1-20
A	US 4466174 A1 (TEXAS INSTRUMENTS INCORPORATED) 21.08.1984	1-20
A	US 2017/0162690 A1 (TEXAS INSTRUMENTS INCORPORATED) 08.06.2017	1-20
A	US 2018/0233561 A1 (TEXAS INSTRUMENTS INCORPORATED) 16.08.2018	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

17 January 2020 (17.01.2020)

Date of mailing of the international search report

23 January 2020 (23.01.2020)

Name and mailing address of the ISA/RU:
Federal Institute of Industrial Property,
Berezhkovskaya nab., 30-1, Moscow, G-59,
GSP-3, Russia, 125993
Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37

Authorized officer

M. Adireeva

Telephone No. (499) 240-25-91