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(54) **PEER-TO-PEER REGISTER EXCHANGE CONTROLLER FOR PLCS**

VERMITTLUNGSSTEUERUNG ZWISCHEN GLEICHRANGIGEN REGISTERN FÜR PROGRAMMIERBARE LOGISCHE STEUERUNGEN

CONTROLEUR D'ECHANGE DE REGISTRE ENTRE HOMOLOGUES POUR PLC

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(73) Proprietor: **Schneider Automation Inc.**
North Andover, Massachusetts 01845 (US)

(72) Inventors:
- **WATT, Kim, J.**
  Milwaukee, WI 53224 (US)
- **GATES, Dirk, I.**
  Woodlands hills, CA 91364 (US)
- **JANKE, Donald, R.**
  Milwaukee, WI 53215 (US)

(74) Representative: **Molyneaux, Martyn William et al**
Langner Parry
52-54 High Holborn
London WC1V 6RR (GB)

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- **PATENT ABSTRACTS OF JAPAN vol. 10, no. 80 (P-441)(2137) 29 March 1986 & JP-A-60 217 446**

EP 0 365 673 B1

Description

Technical Field

This invention relates generally to interconnecting programmable logic controllers to effect sequential program instructions and particularly relates to interconnecting image memory portions of several programmable logic controllers to enable operation at a speed much greater than the operating speed of the programmable logic controllers functioning independently.

Background of the Invention

In the past, programmable logic controllers have received sensor information over a communications network or over discrete leads from the machine tool being controlled. The programmable logic controller or PLC processes the sensor information according to sequential instructions contained in its program memory portion. The result of the processing of the sensor information often results in command information that the PLC transmits to switches or actuators on the controlled machine tool over the communications network or on discrete leads.

PLCs normally include an image memory which contains registers and addresses assigned to reflect the condition of the various sensors monitoring the machine tool. Information from the sensors, and received at the PLC becomes stored at certain registers and the processing instructions in the PLC operate on the information contained in the image memory. One such arrangement is shown in EP-A-200 365 on which the pre-characterising part of claim 1 below is based. Some PLCs include two processors to obtain increased operating speed: one is a control processor that handles communications with the sensors and drivers to move information to and from the image memory and that assigns tasks to the second processor; and the second is a SCAN processor that effects the sequential processing instructions to obtain information from the image memory and provide solutions to other certain addresses in the image memory under control of the control processor.

While this latter arrangement has obtained higher processing speeds, further speed increases are desired.

Summary of the Invention

The invention as particularly defined in the appended claims provides a high-speed interconnection between the image memory portions of several PLCs operating together.

This allows each PLC to operate on a portion of a sequential instruction set and for the solution obtained by each PLC to appear in the image memory portions of the other PLCs at a time that is effectively simultaneous with the solution.

Moreover, the high-speed image memory transfers between the PLCs occur with parity and CRC checking at each PLC before the information is written into the image memory of that PLC to verify the accuracy of the information transfer between the image memories. The foregoing not only obtains increased operating speed but guarantees the accuracy of the information transferred between image memory portions of the PLCs.

Other advantages and aspects of the invention will become apparent upon making reference to the specification, claims, and drawings to follow.

Description of the Drawings

Figure 1 is a block diagram of four programmable logic controllers (PLCs) connecting to a communications network;

Figure 2 is a block diagram of a modification of the diagram of Figure 1 which includes a high-speed memory transfer network in accordance with the invention;

Figure 3 is a block diagram showing transferable register of each of the four PLCs and indicating transfer of blocks between the registers by the arrowed lines; and,

Figure 4 shows the manner of connection between two communication networks.

Detailed Description of the Invention

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail a preferred embodiment of the invention. The present disclosure is to be considered as an exemplification of the principles of the invention.

Fig. 1 shows a presently used PLC network 11 including a group of 4 programmable logic controllers (PLCs) numbered 1 to 4A. Each of the PLCs include a control processor 12A, a scan processor 14A and an image memory 16A. As noted in Fig. 1, the memory 16A is accessed by the control processor 12A to obtain or provide communications and control data. The scan processor 14A in turn accesses the image memory 16A and then through the control

processor 12A to the comnunications network 20A.

Fig. 2 shows a PLC network 21 of the invention including four programmble logic controllers (PLCs) 1 to 4, although up to 16 PLC's can be used. Each of the PLCs includes a control processor 12, a scan processor 14, and a memory 16. Referring to Fig. 2, the memory 16, for a device with peer-to-peer communications, is further divided into three sections, the normal memory, image memory and the two port shared memory. It is this shared memory and its operation that allow these pragrammable logic controllers to operate in a peer-to-peer (slave-to-slave) fashion. Importantly, each of the PLCs further include a communications processor 18, a local RAM (Random Access Memory) 19 and a local area network interface 22. The local area network interface 22 connects to high spedd image memory transfer network 17.

As mentioned above, and as will be explained in detail hereinbelow, the image memories 16 of each of the PLCs 1 to 4 are interconnected and are, in effect, commonly accessed by the network devices and by the other PLCs to provide a higher speed of network communication and transfer of data.

Refer now to Fig. 3 which shows the image memory 16 map 16-1, 16-2, 16-3 and 16-4 of each of the PLCs 1 to 4. The memory maps of the PLCs are similar and each consists of 2 to 6 blocks. For simplicity of explanation, the transferable memory of each PLC represented in Fig. 3 will be divided with 4 blocks. As each block of registers has an assigned time slot when it transfers blocks of registers, each device sends a different block of registers. This is shown in Fig. 3 wherein the arrowed line generally marked as 30 indicates the transfer of block register 1 of PLC 1 to PLC 2, PLC 3 and PLC 4. PLC 3 transfers the block register 3 to PLC 1, PLC 2 and PLC 4, and FIG 4 transfers the block of registers 4 to PLC 1, PLC 2 and PLC 3.

Fig. 4 shows circuitry for coupling from a first communications network 23 to a second communications network 25. This is accomplished through a dual port network interface module 26. As clearly shown in Fig. 4, a second communications network 25 communicates through a network interface module 26 with RS-422 port in PLC 3 and a software switch 29 to a first communications network 23. This type of connection may be made necessary when the first network 23 is supporting or has connected to it its maximum load of 100 network interface modules 26 and 200 devices (machines to be controlled, printers, terminals, computers, etc.).

The peer-to-peer network is able to transfer blocks of registers between 2 to 16 PLCs, each PLC sending a different block of registers. Each block of registers is assigned a mailbox location. The location of the mailbox is dependent on the ID number that each device is assigned.

When first powered up, when a PLC is added or removed from the network or in the event of noise, the network will need to be reformed.

In the formation process, each PLC sends a loop formation packet onto the network. The packet is identified as a loop formation packet, and contains information on the address of the sender, and size of blocks. During loop formation, the following is set up. The number of units on the network is determined, verification is made that all PLCs have the same block size, each PLC tests its address against the address of the other PLCs, and time slices for each PLC on the network are defined, that is, each PLC on the network calculates during what time slice it is to transmit, and what block it should be receiving during any given time slice. Each PLC sends a packet when it detects that the network is free. In the event there is a collision, the colliding units back off, and after a random delay, they resend their packets.

After a formation packet is sent, the sending PLC delays the time necessary to receive and process one packet. If a packet is received, it will again delay the time necessary to receive and process a packet. This will continue until no more packets are received. This means that all PLCs will have time to send their packets to all other PLCs. After the last packet has been received, and the last time out, normal loop operation commences.

During the first loop, the transmitter waits one packet time before sending the first packet. The receivers will wait three packet times before timing out.

As mentioned above, loop formation is a function of the block size, and the number of units on the network. In general, formation time is determined by the following equation:

"Formation Time = K+Block Size (Number of PLCs on the Network)"

Each PLC on the network sends its packet during the time slice defined during loop formation. The transmitted data is direct memory accessed out of the shared register RAM allowing the communication processor to handle necessary processing tasks such as updating the overall communication status bits.

When not transmitting data, each PLC waits for a packet from another PLC. When a packet is received, its CRC is validated, and a check is made if the sender of the packet is in the correct time slice. If the packet is totally validated, it is moved to the shared RAM.

If, during normal operation, a loop formation packet is received, the PLC will drop out of normal operation and go to loop formation mode.

The update time for a given installation can be determined by multiplying the block time for a single update by the

actual number of units on the network.

The communication update rate is a function of the actual number of PLCs on the network and the block size.

Ladder scans of some or all of the processors on the network can be automatically synchronized. This allows the processors to scan at the same time and facilitates parallel processing.

The serial network interface receives and transmits data over the peer-to-peer network. The data is sent in block form with CRC protection and parity protection on each block. The transmission method does not use collision detection schemes and is completely deterministic in the time domain. The serial network interface uses the shared register area (two port) as storage or the location to get messages.

The communication processor takes care of all processing required by the peer-to-peer network. It has access to the serial network interface and two port memory. It also has inputs to the setup switches. The communication processor sets up the network protocols and reports network status to the user through the two port memory.

The communication processor does most communication with the control processor through the two port memory.

Each PLC device has a bank of switches for setup. The state of the switches is read once at power up by the communication processor.

One switch is a rotary switch to set up the identification number of the device from 0 to F. Every PLC connected to the peer-to-peer network must have a unique identification number or the network will not operate properly. Labeling on the front panel allows the user to indicate the PLC ID number.

The other switches are arranged as follows:

1. (Bit 1-2) This code indicates the maximum number of units in the network. For fastest network formation time, the smallest possible number should be selected. All devices on the network must have the same code set up or the network will not operate properly. The code is as follows:

Code	Max. Number of PLCs on the Network
0	2
1	4
2	8
3	16

2. (Bit 3-4) This code indicates the block size. The block size is the number of registers sent from a PLC on the network to all other PLCs on the network. All PLCs on the network must have the same code or the network will not operate properly. The code is as follows:

Code	Size of Block (Registers)
0	32
1	64
2	128
3	-AUTO-

The AUTO position automatically configures the maximum number of registers possible based on the setting of the Maximum Number of units on the Network switch. The following table describes this relationship:

Max. Number of Units On The Network	Number of AUTO Register
2	512
4	256
8	128
16	64

The 1024 "shared data registers" can be arranged in any one of 4 different block size configurations. They are: 2 blocks of 512 registers, 4 blocks of 256 registers, 8 blocks of 128 registers or 16 blocks of 64 registers.

In addition to the above shared registers, the PLC device has a "peer-to-peer control register" at location 8096. This register will allow the user to configure the shared registers for the particular application. The bits in this register are dynamic in that they can be changed by the user program at any time.

Table 1 contains a map of the shared registers which are divided into 5 main sections. There are: 8 control data

registers, 5 spare registers, 3 miscellaneous registers, 16 communications status registers, and 1024 data registers. An explanation of the register follows:

TABLE 1

SHARED REGISTERS MEMORY MAP		
Control Date Write Protected (8)	8000	Error Code
	7999	DIP Switch Image
	7998	Device ID
	7997	Block Size
	7996	Number of Blocks
	7995	Comm to CPU Handshake
	7994	Main-CPU Handshake
	7993	Reflectometry Counter
Share (5)	7992	Spare
	7991	Spare
	7990	Spare
	7989	Spare
	7988	Spare
Misc (3)	7987	Count of Loop Formations
	7986	Max Consecutive Block Errors
	7985	Failure Override Control
	7984	PLC Device 0
	7983	1
	7982	2
	7981	3
	7980	4
Communication Status Registers (16)	7979	5
	7978	6
	7977	7
	7976	8
	7975	9
	7974	10
	7973	11
	7972	12
	7971	13
	7970	14
	7969	15
Data Registers (1024)	7968	Shared Data
	"	"
	"	"
	6945	Shared Data

Error Code (8000)

If the communication processor detects an error, it will post an error code in this register. The following error codes are supported:

	Code	Meaning
A	0	No error
B	1	Address Error
C	2	Bus Error
D	3	Parity Error
E	4	Handshake Failure
F	5	Main Processor Failure
G	6	PROM Checksum Test Failure
H	7	Local RAM Read AFter Write Test Failure
I	8	Local RAM Destructive Test Failure
J	9	Shared RAM Read After Write Test Failure
K	10	Shared RAM Destructive Test Failure
L	11	Local Area Network Controller Test Failure
M	12	Shared Register Block Exceeds 1024 Registers

N	13	Incorrect Block Size Received
O	14	Address greater than Number of Devices on the Network
P	15	Duplicate Address Detected
Q	16	Block Error Limit Exceeded

The Dip Switch Image (7999) register contains an image of the peer-to-peer dip switch. The user can read this register to find out how the dip switch is set without removing the device from the rack. The communication processor writes the data to this location.

The Device ID (7998) register contains the ID code assigned to this PLC. The communication processor decodes the ID code from the dip switch settings and places it here.

The Block Size (7997) register contains the peer-to-peer block size. The communication processor decodes the block size from the dip switch settings and places it here.

The Number of Blocks (7996) register contains the maximum number of blocks transferred by the peer-to-peer network. The communication processor decodes the maximum number of blocks from the dip switch setting and places it here.

The Comms to CPU Handshake (7995) is an internal register used by communication processor to handshake with the control processor.

The Main CPU Handshake (7994) is an internal register used by control processor to handshake with the communication processor.

The Time Domain Reflectometry Counter (7993) counts proportional to the length of the cable. A counter is started when a transmission is started from a PLC. Reflections from the cable end terminate the count. The value should be constant for a given installation and device on the network. It has value as a trouble shooting tool.

Spare Registers for Future Expansion (7992-7988) are registers reserved for future expansion.

During power up and conditions of extraordinary network disturbances, the network may be automatically reformed. The Count of Loop Formations (7987) register contains a count of the number of times the network has been reformed.

The Maximum Consecutive Block Errors (7986) register is programmed by the user to indicate the maximum number of consecutive block errors before the system automatically generates an error and goes to HALT.

When the bits in the Failure Override control (7985) registers are zero, the PLC Will generate an error if the communication processor detects (n) consecutive errors in a row where (n) is determined by the contents of the previous maximum consecutive block errors. If a bit is set to one, the error will not be generated. Bit 1 corresponds to PLC device 1, Bit 2 to PLC device 2 and so on, up to PLC device 15.

The Communication Status Registers (CSR) (7984-7969) are written to by the communication processor to give the status of individual communication channels. There is one register for each communications register.

While the invention has been described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof.

Claims

1. A high speed peer-to-peer programmable logic controller (PLC) system (21) comprising:

a plurality of programmable logic controllers (PLCs);

a communications network (20) connected to each of said plurality of PLCs for providing communication between each of said plurality of PLCs as well as with external devices; and

wherein each of said plurality of PLCs includes:

a multi-port image memory (16) for storing status and control informations having a plurality of memory blocks

corresponding to said plurality of PLCs,

a control processor (12) for sequentially performing a series of instructions and for transferring data between said multi-port image memory (16) and said communications network (20),

characterized in that there is further provided a high speed memory transfer network (17) connected to each of said plurality of PLCs for transferring data between each of said plurality of PLCs, and each PLC includes a communications processor (18) for transferring data from each of said plurality of memory blocks to each of said plurality of memory blocks of each other of said plurality of PLCs on said high speed memory transfer network (17) to allow an independent update of said image memories, the transfer occurring independent of said communications network (20) and independent of the operation of said control processor (12).

2. A high speed peer-to-peer PLC network according to claim 1, wherein the first one of said plurality of memory blocks for each PLC corresponds to a first PLC of said plurality of PLCs and each other of said plurality of memory blocks, for each PLC respectively, corresponds to each other PLC of said plurality of PLCs.

3. A high speed peer-to-peer PLC network according to claim 2, wherein each of said multi-port memories includes registers containing data which is transferrable between the others of said multi-port memories.

4. A high speed peer-to-peer PLC network according to claim 3, wherein the memory block size of the registers for data to be transferred from one memory means matches the blocks of said registers of the memory means to which said data is to be transferred.

5. A high speed peer-to-peer PLC network according to claim 2, 3 or 4, wherein each of said registers contains an address which includes first and second PLC ID numbers and a mailbox number, wherein the mailbox numbers of the blocks of registers are identical.

6. A high speed peer-to-peer PLC network according to any preceding claim, wherein each of said plurality of control processors (PLC) can be selectively connected to a said communication network (20).

Patentansprüche

1. Schnelles, gleichrangiges, programmierbares logisches Steuerungssystem (21), das folgendes umfaßt:

eine Mehrzahl programmierbarer logischer Steuerungen;
ein Kommunikationsnetz (20), das mit jeder programmierbaren logischen Steuerung der Mehrzahl dieser programmierbaren logischen Steuerungen verbunden ist, um zwischen diesen einzelnen programmierbaren logischen Steuerungen sowie mit externen Vorrichtungen eine Übertragungsverbindung vorzusehen; und

wobei jede programmierbare logische Steuerung der genannten Mehrzahl programmierbarer logischer Steuerungen folgendes umfaßt:

einen mehrtorigen Bildspeicher (16) zur Speicherung von Status- und Steuerungsinformationen, wobei der Speicher eine Mehrzahl von Speicherblöcken aufweist, die in der Anzahl der genannten Mehrzahl der programmierbaren logischen Steuerungen entsprechen;
einen Steuerungsprozessor (12) zur sequentiellen Ausführung einer Reihe von Befehlen sowie zur Datenübertragung zwischen dem genannten mehrtorigen Bildspeicher (16) und dem genannten Kommunikationsnetz (20), dadurch gekennzeichnet, daß ferner ein schnelles Speicherübertragungsnetz (17) vorgesehen ist, das mit jeder der programmierbaren logischen Steuerungen der genannten Mehrzahl programmierbarer logischer Steuerungen verbunden ist, und wobei jede programmierbare logische Steuerung einen Kommunikationsprozessor (18) aufweist, der dazu dient, Daten auf dem genannten schnellen Speicherübertragungsnetz (17) von dem Speicherblock der genannten Mehrzahl von Speicherblöcken zu jedem anderen Speicherblock der genannten Mehrzahl von Speicherblöcken jeder anderen programmierbaren logischen Steuerung der genannten Mehrzahl programmierbarer logischer Steuerungen zu übertragen, um eine unabhängige Aktualisierung der genannten Bildspeicher zu ermöglichen, wobei die Übertragung unabhängig von dem genannten Kommunikationsnetz (20) sowie unabhängig von dem Betrieb des genannten Steuerungsprozessors (12) erfolgt.

2. Schnelles, gleichrangiges, programmierbares logisches Steuerungssystem nach Anspruch 1, wobei der erste Speicherblock der genannten Mehrzahl von Speicherblöcken für jede programmierbare logische Steuerung einer ersten programmierbaren logischen Steuerung der genannten Mehrzahl programmierbarer logischer Steuerungen entspricht, und wobei jeder andere Speicherblock der genannten Mehrzahl von Speicherblöcken in bezug auf jede entsprechende programmierbare logische Steuerung jeder anderen programmierbaren logischen Steuerung der genannten Mehrzahl programmierbarer logischer Steuerungen entspricht.

3. Schnelles, gleichrangiges, programmierbares logisches Steuerungssystem nach Anspruch 2, wobei jeder der genannten mehrtorigen Speicher Register aufweist, die Daten enthalten, die zwischen anderen mehrtorigen Speichern der genannten Mehrzahl mehrtoriger Speicher übertragen werden können.

4. Schnelles, gleichrangiges, programmierbares logisches Steuerungssystem nach Anspruch 3, wobei die Speicherblockgröße der Register einer Speichereinrichtung für die zu übertragenden Daten den Blöcken der genannten Register der Speichereinrichtung entspricht, in die die genannten Daten übertragen werden sollen.

5. Schnelles, gleichrangiges, programmierbares logisches Steuerungssystem nach Anspruch 2, 3 oder 4, wobei jedes der genannten Register eine Adresse aufweist, die erste und zweite Identifikationsnummern für die programmierbaren logischen Steuerungen und eine Mailbox-Nummer umfaßt, wobei die Mailbox-Nummern der Blöcke der Register identisch sind.

6. Schnelles, gleichrangiges, programmierbares logisches Steuerungssystem nach einem der vorstehenden Ansprüche, wobei jeder Steuerungsprozessor der genannten Mehrzahl von Steuerungsprozessoren wahlweise mit einem genannten Kommunikationsnetz (20) verbunden werden kann.

Revendications

1. Système de contrôleur logique programmable entre homologues à grande vitesse (PLC) (21) comprenant :

une pluralité de contrôleurs logiques programmables (PLC) ;
un réseau de communication (20) connecté à chacun de ladite pluralité de PLC permettant de fournir une communication entre chacun de ladite pluralité de PLC ainsi qu'avec des dispositifs extérieurs ; et

dans lequel chacun de ladite pluralité de PLC comporte :

une mémoire d'image multiports (16) permettant de mémoriser les informations d'état et de commande, présentant une pluralité de blocs de mémoire correspondant à ladite pluralité de PLC, et
un processeur de commande (12) permettant d'effectuer de manière séquentielle une série d'instructions et permettant de transférer les données entre ladite mémoire d'image multiports (16) et ledit réseau de communication (20),

caractérisé en ce qu'il est en outre prévu un réseau de transfert de mémoire à grande vitesse (17) connecté à chacun de ladite pluralité de PLC pour transférer les données entre chacun de la pluralité de PLC, et en ce que chaque PLC comporte un processeur de communication (18) permettant de transférer les données en provenance de chacun de ladite pluralité de blocs de mémoire vers chacun de ladite pluralité de blocs de mémoire de l'un ou l'autre de ladite pluralité de PLC dudit réseau de transfert de mémoire à grande vitesse (17), afin de permettre une mise à jour indépendante desdites mémoires d'image, le transfert se produisant indépendamment dudit réseau de communications (20) et indépendamment du fonctionnement dudit processeur de commande (12).

2. Réseau de PLC entre homologues à grande vitesse selon la revendication 1, dans lequel le premier de ladite pluralité de blocs de mémoire pour chaque PLC correspond à un premier PLC d'une pluralité de PLC et l'un ou l'autre de ladite pluralité de blocs de mémoire, pour chaque PLC respectivement, correspond à l'un ou l'autre PLC de ladite pluralité de PLC.

3. Réseau de PLC entre homologues à grande vitesse selon la revendication 2, dans lequel chacune desdites mémoires multiports comporte des registres contenant une donnée qui est transférable entre les autres desdites mémoires multiports.

4. Réseau de PLC entre homologues à grande vitesse selon la revendication 3, dans lequel la taille en bloc de mémoire des registres pour qu'une donnée soit transférée depuis un moyen de mémoire correspond aux blocs desdits registres du moyen de mémoire vers lequel ladite donnée doit être transférée.

5. Réseau de PLC entre homologues à grande vitesse selon la revendication 2,3 ou 4, dans lequel chacun desdits registres contient une adresse qui inclut un premier et un second numéro identificateur et un numéro de boîte à lettres et dans lequel les numéros de boîte à lettres des blocs de registres sont identiques.

6. Réseau de PLC entre homologues à grande vitesse selon l'une quelconque des revendications précédentes, dans lequel chacun desdits contrôleurs logiques programmables (PLC) peut être sélectivement connecté à un réseau de communication (20).

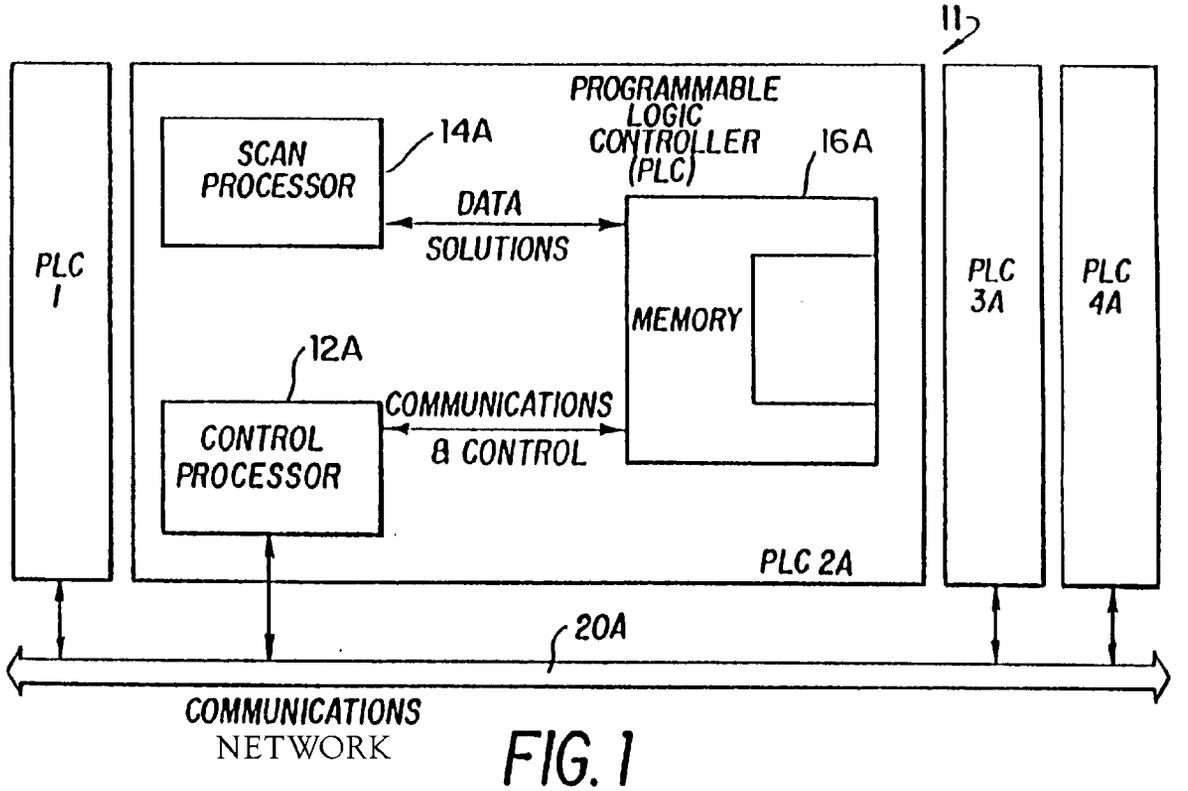
11
PROGRAMMABLE LOGIC CONTROLLER (PLC)
SCAN PROCESSOR
14A
16A
DATA
SOLUTIONS
MEMORY
PLC 1
PLC 3A
PLC 4A
12A
COMMUNICATIONS & CONTROL
CONTROL PROCESSOR
PLC 2A
20A
COMMUNICATIONS NETWORK

FIG. 1

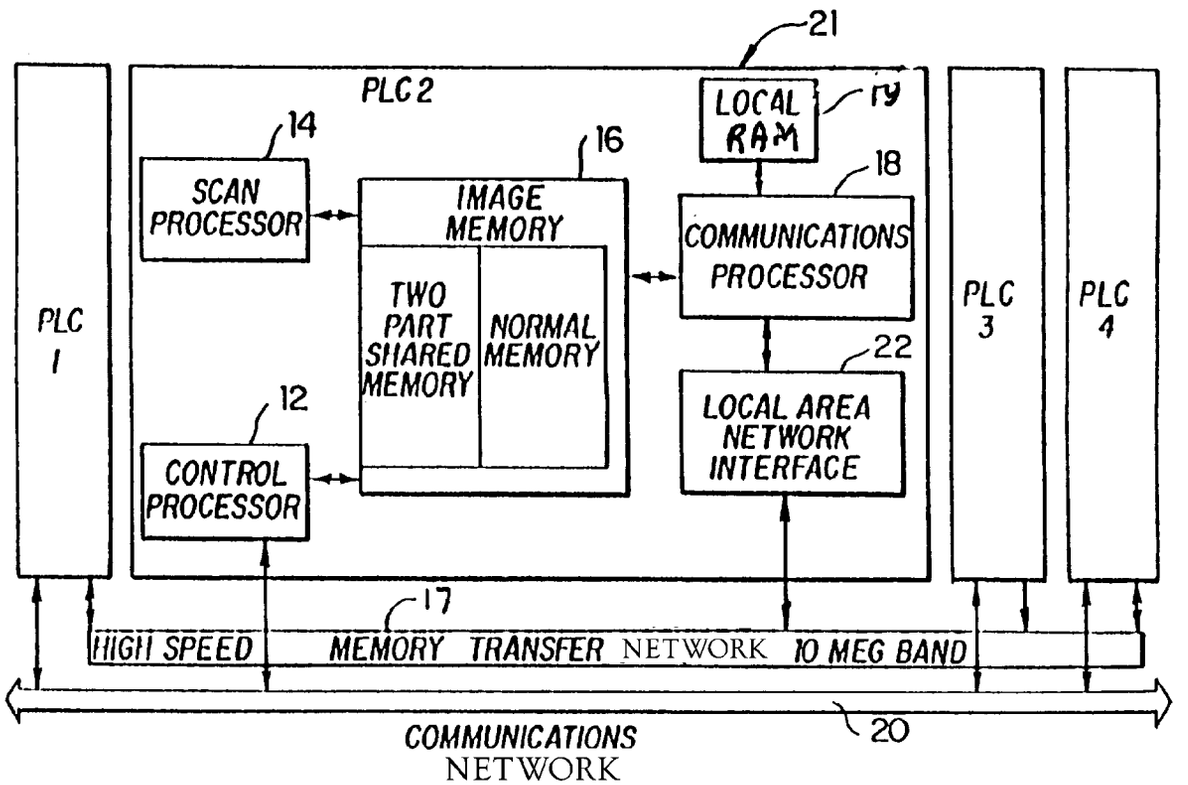
21
PLC 2
LOCAL RAM
19
14
16
18
SCAN PROCESSOR
IMAGE MEMORY
COMMUNICATIONS PROCESSOR
TWO PART SHARED MEMORY
NORMAL MEMORY
PLC 1
PLC 3
PLC 4
22
12
LOCAL AREA NETWORK INTERFACE
CONTROL PROCESSOR
17
HIGH SPEED MEMORY TRANSFER NETWORK 10 MEG BAND
20
COMMUNICATIONS NETWORK

FIG. 2

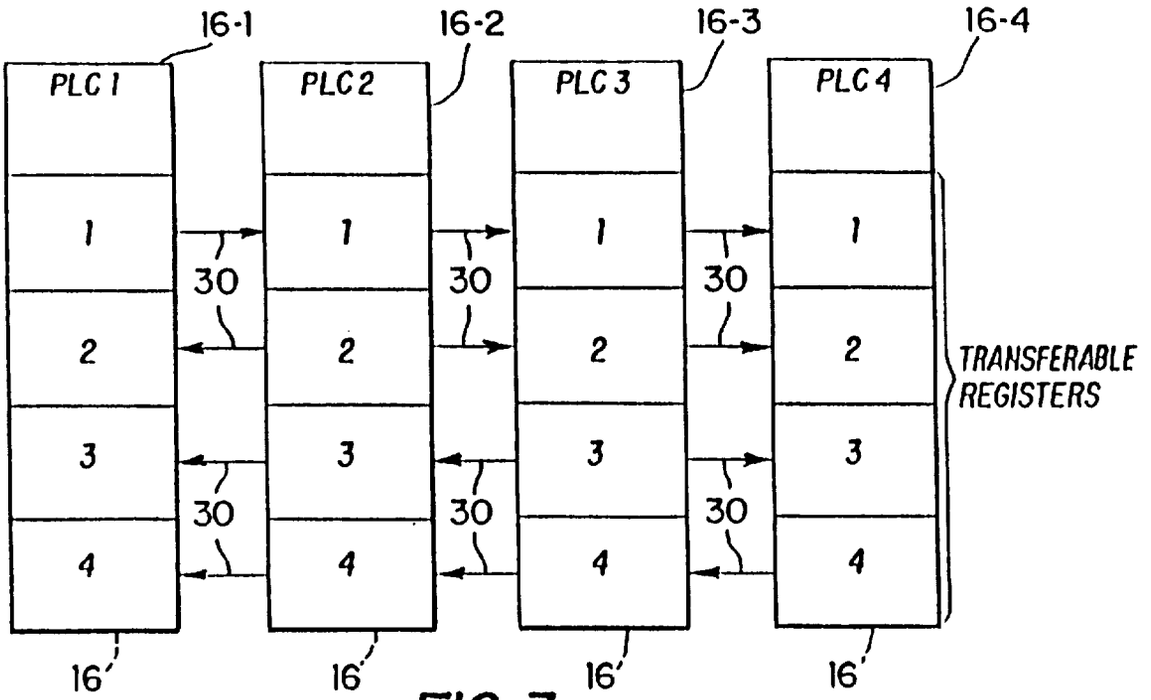
16-1
16-2
16-3
16-4
PLC 1
PLC 2
PLC 3
PLC 4
1
2
3
4
30
TRANSFERABLE REGISTERS
16'

FIG. 3

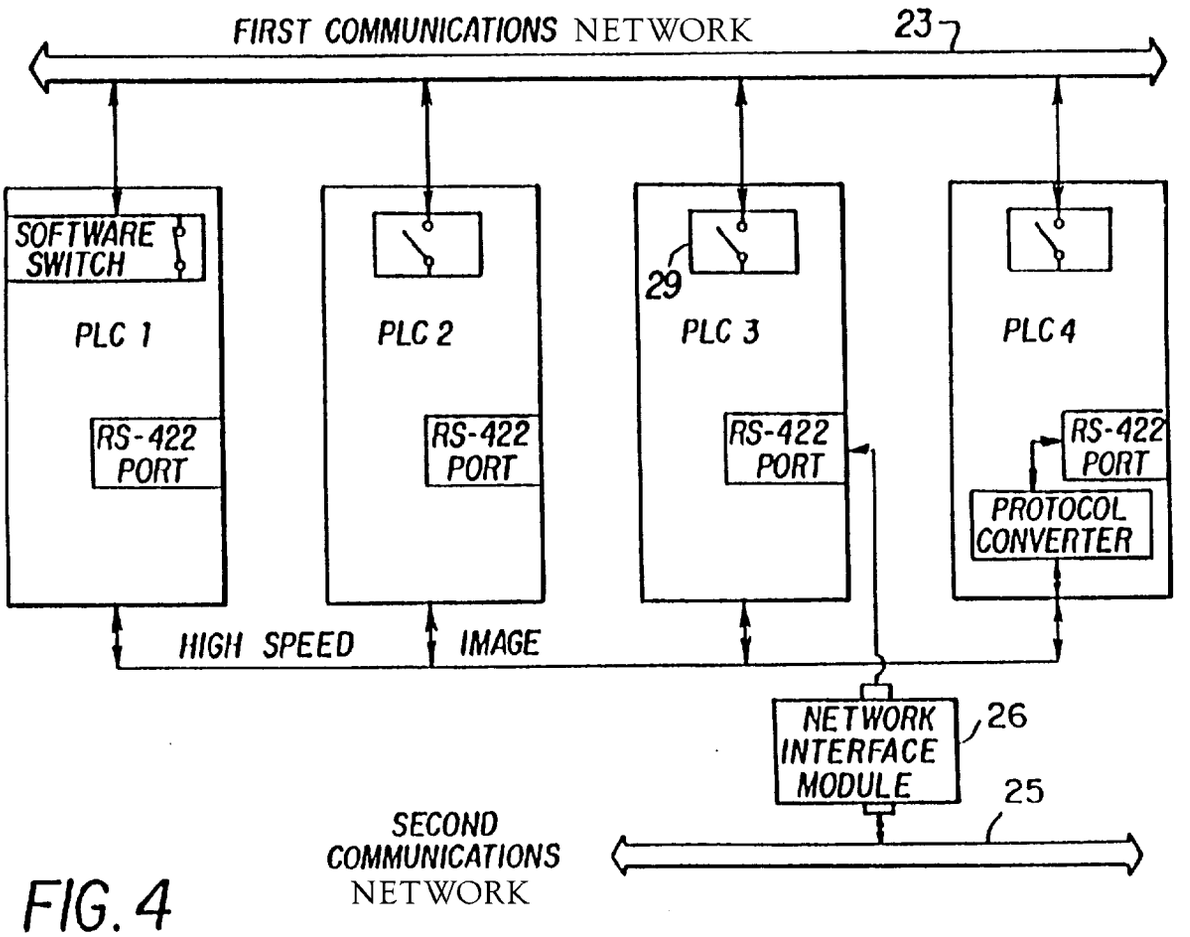
FIRST COMMUNICATIONS NETWORK
23
SOFTWARE SWITCH
PLC 1
PLC 2
PLC 3
PLC 4
29
RS-422 PORT
PROTOCOL CONVERTER
HIGH SPEED IMAGE
NETWORK INTERFACE MODULE
26
25
SECOND COMMUNICATIONS NETWORK

FIG. 4