

[54] **PLASMA DISPLAY PANEL**

[75] Inventors: **Shizuo Andoh; Toshinori Urade**,
both of Kobe; **Tadatsugu Hirose**,
Akashi, all of Japan

[73] Assignee: **Fujitsu Limited**, Nakahara-ku,
Kawasaki, Japan

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[51] **Int. Cl.**..... **H01j 61/30**

[58] **Field of Search**..... 313/182, 188, 192, 196,
313/108 B, 220, 308; 315/169 R

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Primary Examiner—James W. Lawrence
Assistant Examiner—B. C. Anderson
Attorney, Agent, or Firm—Staas, Halsey & Gable

[57] **ABSTRACT**

A plasma display panel in which two transparent base plates are assembled together to define a discharge gas space therebetween. On each transparent base plate, a plurality of strip-like main electrodes are provided and a dielectric layer is formed to cover them and, further, third electrodes are each provided between adjacent ones of the main electrodes. The two transparent base plates are assembled together in opposing relation to each other in such a manner that their main electrodes and third electrodes are disposed substantially perpendicular to each other in the form of a matrix. By impressing a voltage to selected ones of the main electrodes of the both transparent base plates, a discharge spot is produced at their intersecting point to provide a display. The discharge spot becomes enlarged or reduced or extends in a certain direction according to the polarity of a voltage impressed between the third electrodes of both transparent base plates and to the selection of the third electrodes to be supplied with the voltage. The discharge spot can be shifted in either direction of the row and column of the matrix.

8 Claims, 13 Drawing Figures

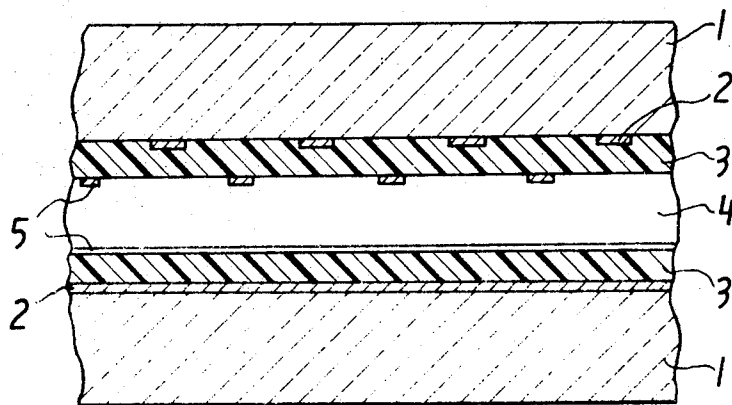


FIG. 1

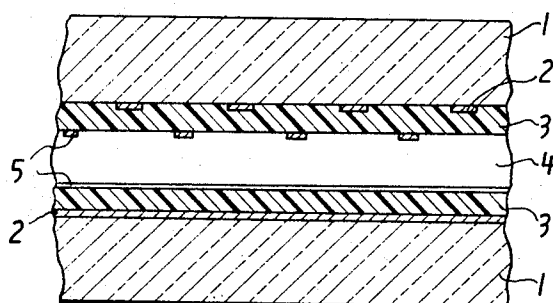


FIG. 2

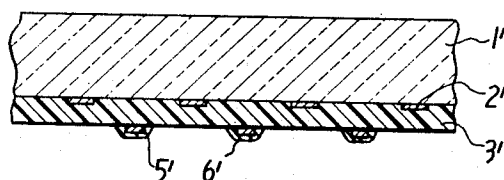


FIG. 3

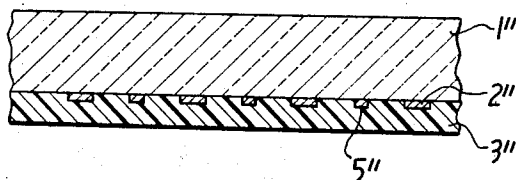


FIG. 4

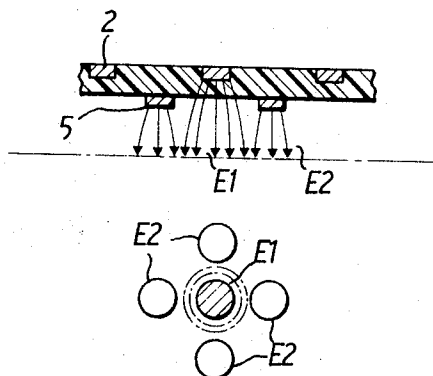


FIG. 5

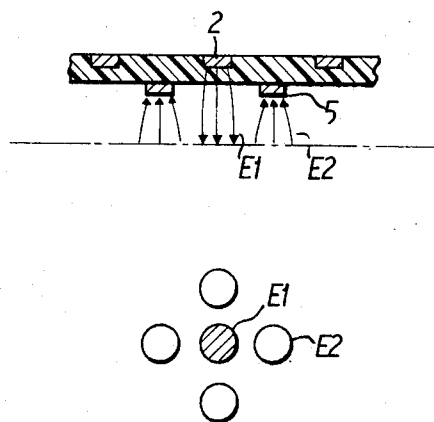


FIG. 6

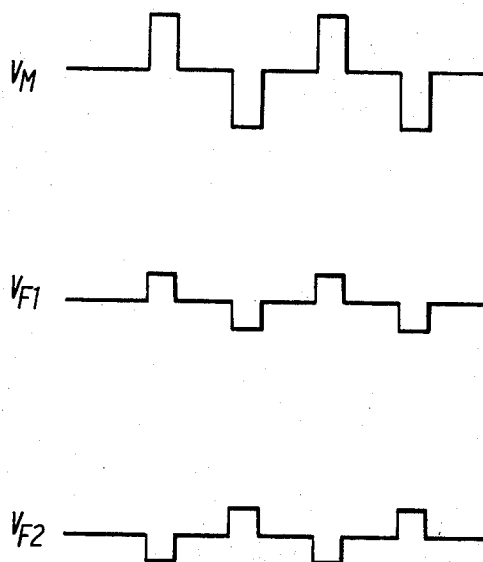


FIG. 7

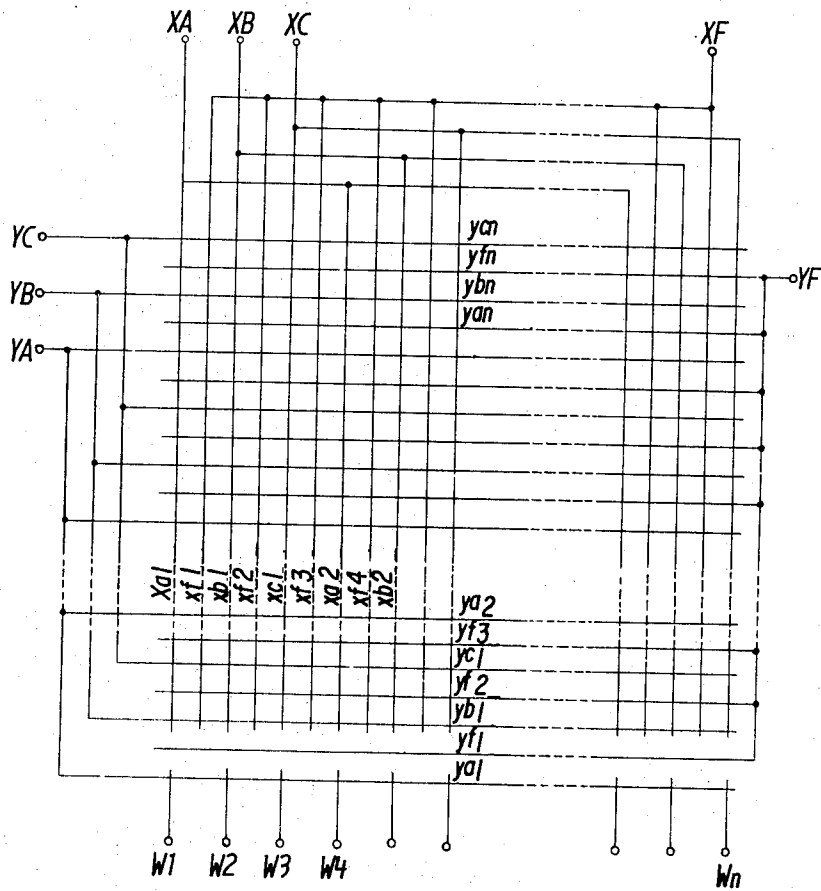


FIG. 8A

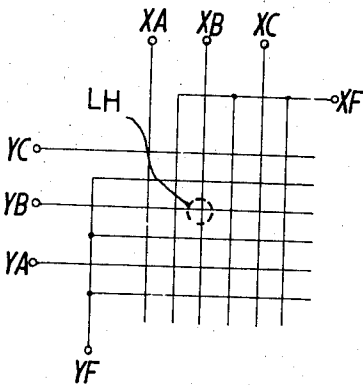


FIG. 9A

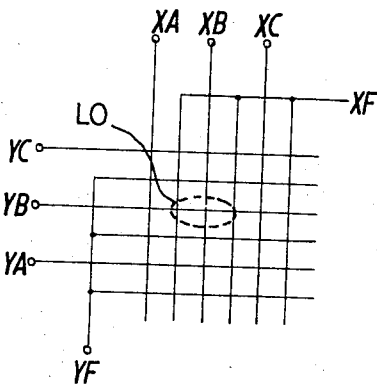


FIG. 8B

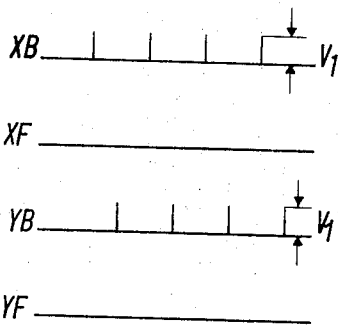


FIG. 9B

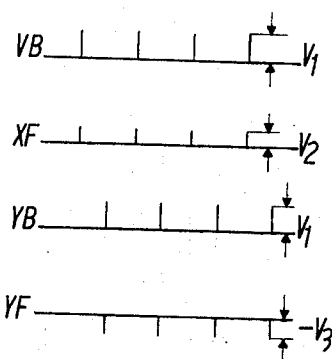
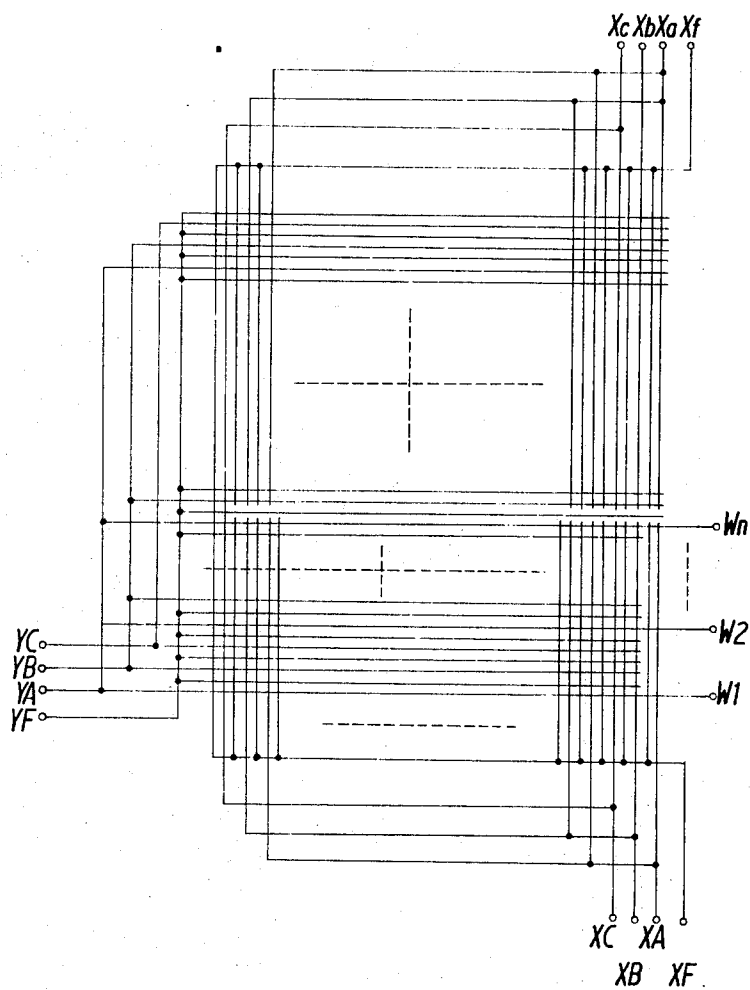


FIG. 10



PLASMA DISPLAY PANEL

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a plasma display panel which is provided with main electrodes causing a plasma discharge and electrodes for controlling the electric field of the plasma discharge.

2. Description of the Prior Art

As disclosed in the Japanese Patent Application Publication No. 10704/1960, in conventional plasma display panels, a glass plate having formed therein apertures serving as discharge cells is interposed between glass base plates having electrodes, a mixed gas composed of Ne and N₂ is sealed in the cells and an AC voltage is impressed to the electrodes to cause plasma discharge in the discharge cells when the impressed voltage exceeds a discharge voltage, thereby to provide a display. Further the plasma display panels have a memory function due to wall charge. Even if the glass plate having the apertures and serving as the discharge cells is left out to provide a continuous discharge space, only a matrix display can be provided if a voltage is also impressed a little to unselected intersecting points resulting in lowered resolution of the display. Further, a self shift panel of the type in which kindling radiation is effected to spread electric field to adjacent cells and then firing radiation is achieved by impression of a sustain voltage is defective in that when it is controlled, coupling of adjacent cells is likely to be insufficient to cause erroneous shift.

SUMMARY OF THE INVENTION

Thus it is an object to provide a plasma display panel free from the aforementioned defects experienced in the prior art and to control the electric field of plasma discharge at will by the provision of a third electrode in addition to main electrodes.

This and other objects are accomplished by providing a plasma display panel in which dielectric layers are formed on main electrodes and disposed opposite to each other with a discharge gas space therebetween and third electrodes are provided to control electric field between the main electrodes and in which electric field of plasma discharge is controlled by the third electrodes to enlarge, reduce or extend a discharge spot in a certain direction.

The third electrodes are provided in dielectric layers and in which electric field of the plasma discharge can be controlled by an extremely low voltage applied thereto.

A further feature of this invention is to provide a plasma display panel in which the third electrodes are covered with insulating layers to prevent damage to the third electrodes by direct bombardment of ions thereon, thereby to provide for lengthened service life of the plasma display panel.

In an illustrative embodiment of this invention, the plasma display panel is provided with the third electrodes and the main electrodes simultaneously formed in the same plane, thereby to simplify the manufacturing process of the display panel and lengthen the service life thereof.

As a further aspect of this invention, one of the third electrodes is replaced with the main electrode, thereby to simplify the manufacturing process of the display

panel and hence lower the manufacturing cost thereof.

In a further embodiment of this invention, the plasma display panel includes a plurality of third electrodes disposed between the main electrodes or the third electrodes adjacent to the main electrodes of the one side, thereby to control electric field of plasma discharge more in various ways.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, preferred embodiments are disclosed in the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a fragmentary cross-sectional view of one example of this invention;

FIG. 2 and 3 are fragmentary, cross-sectional views showing arrangements of third electrodes of the one side in other examples of this invention, respectively;

FIGS. 4 and 5 are schematic diagrams, for explaining the operation of the third electrode, respectively;

FIG. 6 is a series of voltage waveform diagrams, for explaining this invention;

FIG. 7 is a schematic diagram illustrating one example of a matrix electrode construction in a plasma display panel of this invention;

FIG. 8A is a schematic diagram, for explaining generation of a discharge spot;

FIG. 8B is a time chart of a voltage impressed to electrodes for generating the discharge spot shown in FIG. 8A;

FIG. 9A is a schematic diagram, for explaining generation of a discharge spot being controlled;

FIG. 9B is a time chart of a voltage impressed to the electrodes for generating the discharge spot depicted in FIG. 9A;

FIG. 10 is a schematic diagram showing another example of the matrix electrode construction of FIG. 7; and

FIG. 11 is a circuit diagram illustrating one example of a circuit for driving the plasma display panel of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to the drawings, this invention will hereinafter be described in detail.

In FIG. 1, there is illustrated in section one example of this invention. Reference numeral 1 indicates glass base plates, numeral 2 refers to main electrodes, numeral 3 identifies dielectric layers, numeral 4 indicates a discharge gas space, and numeral 5 refers to third electrodes. Usually, the main electrodes 2 are arranged in the form of a matrix and plasma discharge is produced at selected intersecting points of the main electrodes 2 to cause radiation. The third electrodes 5 are shown to be exposed in the discharge gas space 4 but they may be covered with dielectric layers 6' as depicted in FIG. 2 or may be formed in the same plane as the main electrodes 2' as shown in FIG. 3. Further, each third electrode 5 is shown to be disposed midway between adjacent main electrodes 5 but it may be located near either of the electrodes 5 or a plurality of third electrodes 5, may be provided between adjacent

electrodes 5. It is also possible to use the third electrodes 5 of the one side as the main electrodes 2.

The third electrodes 5 are used while being held at the same polarity as the main electrodes 2 or opposite in polarity thereto or grounded. Where the third electrodes 5 are of the same polarity as the main electrodes 2, an electric field provided by the main electrode 2 spreads to widen a radiation area as depicted in FIG. 4. Namely, an electric field E1 of the main electrode 2 and an electric field E2 of the third electrodes 5 are in the same direction, so that plasma discharge spreads as indicated by the dotted lines. On the other hand, where the third electrodes 5 are opposite in polarity to the main electrodes 2, the electric field E1 of the main electrode 2 is opposite in direction to the electric field E2 of the third electrodes 5, and hence is narrow as if focused and the plasma discharge is also narrow in area to limit the radiation area, thus providing a display with high resolution. Further, where the third electrodes 5 are grounded, an intermediate operation between the above-described operations is carried out. The area of the electric field E1 of the main electrode 2 can also be controlled by a voltage impressed to the third electrodes 5.

FIG. 6 shows the relationships between a voltage V_M impressed to the main electrodes 2 and voltages V_{F1} and V_{F2} impressed to the third electrodes 5, in which the voltage V_{F1} shows the case of the main and third electrodes being of the same polarity and the voltage V_{F2} the case of the both electrodes being opposite in polarity to each other. The relationship in magnitude between the voltages V_M , V_{F1} and V_{F2} can be selected as desired and their relationships in phase and frequency can also be selected different from one another.

Driving the third electrodes 5 in only the x- or y-direction while holding them in the same polarity as the main electrodes 2, a channel is formed in the x- or y-direction to strengthen the plasma coupling between adjacent ones of the x- or y-direction main electrodes 2, thereby facilitating self shift in that direction. While, where the third electrodes 5 are driven opposite in polarity to the main electrodes 2, it is possible to prevent mis-shift in a direction perpendicular to a shift direction. Accordingly, in the case of the self shift panel, it is sufficient to provide the third electrodes 5 only in a desired shift direction.

To facilitate a better understanding of the plasma display panel of this invention, a detailed description will be given of its mode of operation.

FIG. 7 illustrates one example of the matrix electrode arrangement used in the plasma display panel of this invention. This electrode arrangement is of particular utility when employed in graphic display.

In FIG. 7, electrodes $xa1$, $xf1$, $xb1$, $xf2$, $xc1$, $xf3$, $xa2$, ... and write electrodes $W1$, $W2$, $W3$, ... Wn are provided on the first base plate, while electrodes $ya1$, $yf1$, $yb1$, $yf2$, $yc1$, $yf3$, $ya2$, ... are provided on the other or second base plate.

Buses XA, XB, XC and XF have connected thereto the main electrodes $xa1$, $xa2$, ..., $xb1$, $xb2$, ..., $xc1$, $xc2$, ... and the third electrodes $xf1$, $xf2$, ... respectively. While, buses YA, YB, YC and YF have similarly connected thereto the main electrodes $ya1$, $ya2$, ..., $yb1$, $yb2$, ..., $yc1$, $yc2$, ... and the third electrodes $yf1$, $yf2$, ... respectively.

With such an arrangement as illustrated, where a write voltage higher than a firing voltage is impressed between any one of the write electrodes $W1$ to Wn , for example, $W1$ and the main electrode $ya1$, a discharge spot is generated at the intersecting point of the write electrode $W1$ with the main electrode $ya1$.

Then, by impressing a voltage to the main electrode $yb1$, the aforesaid discharge spot is shifted to the intersecting point of the main electrodes $yb1$ and $xa1$. In this case, the voltage previously impressed to the main electrode $ya1$ is cut off after impression of the voltage to the main electrode $yb1$.

In a similar manner, upon impression of a voltage to the main electrodes $yc1$, $ya2$, $yb2$, ..., the discharge spot is sequentially shifted.

Thus, it is possible that the discharge spot is generated at a desired position to provide a display by selective combinations of the main electrodes $ya1$, $yb1$, ... and those $xa1$, $xb1$, ... and the write electrodes $W1$ to Wn .

A description will be made in connection with the effect of the third electrodes $xf1$, $xf2$, ... and $yf1$, $yf2$, ...

FIGS. 8A and 9A each show one part of the matrix electrode arrangement of FIG. 7 for convenience of explanation and in the figures each electrode group is shown for each bus.

Assume that voltages as shown in FIG. 8B are impressed to the electrode arrangement of FIG. 8A. Namely, a pulse voltage $+V1$ is impressed alternately between the buses XB and YB. Assuming that the voltages of the buses XF and YF are zero, a discharge spot LH is produced at the intersecting point of the buses XB and YB as indicated by a broken line.

FIG. 9A shows exactly the same electrode arrangement as that depicted in FIG. 8A. Let it be assumed that voltages are applied to the electrodes in such a manner as shown in FIG. 9B. Namely, the pulse voltage $+V1$ is impressed between the buses XB and YB alternately. Assuming that pulse voltages $+V2$ and $-V3$ are applied to the buses XF and YF respectively or that the bus YF is held at zero volt, the discharge spot lengthens in the direction of the bus YB and shortens in the direction of the bus XB for the same reasons as those described previously in connection with FIGS. 4 and 5, as indicated by a broken line LO in FIG. 9A.

The aforementioned voltages bear the following relation:

$$\begin{aligned} V2 &< V1, \\ V3 &< V1 \\ V1 + V3 &< VF \end{aligned}$$

VF: a firing voltage

The direction in which the discharge spot LO lengthens is dependent upon suitable selection of the buses XF and YF for voltage impression thereto. By lengthening the discharge spot LO in the same direction as that in which the discharge spot is shifted, shift can be achieved correctly.

With reference to FIGS. 10 and 11, a description will be given of one example of a drive circuit for the plasma display panel of this invention.

FIG. 10 illustrates a matrix electrode arrangement suitable for character display by self shift, which electrode arrangement is employed in the plasma display panel described hereinbelow in connection with FIG. 11.

In FIG. 10, electrodes on the side X are divided into electrode groups associated with the buses XA, XB, XC and XF and those associated with the buses Xa, Xb, Xc and Xf and write electrodes W1, W2, W3, . . . Wn correspond to the electrode groups associated with the buses XA, XB, XC and XF as shown.

When the discharge spot written by the write electrodes W1 to Wn and the bus XA is sequentially shifted to desired positions by the buses XA, XB, XC and XF and letters for one line is formed by a subsequent discharge spot, these letters are shifted upwardly by the buses YA, YB, YC and YF. Each of the letters is shifted to a desired display position on the matrix electrode plane.

Thus, the matrix electrode arrangement depicted in FIG. 10 is effective for two-dimensional shift.

FIG. 11 illustrates one example of a drive circuit for the plasma display panel employing the matrix electrode arrangement described above in connection with FIG. 10.

For convenience of explanation, an example in which one letter is displayed by 5×7 dots will be given; for the sake of clarity in FIG. 11, the buses Xa, Xb, Xc and Xf of FIG. 10 are left out. Accordingly, the write electrodes W1 to W7 are represented with seven lines.

In FIG. 11, reference numeral 100 indicates a key board, numeral 101 refers to a diode matrix circuit, numerals 102 and 103 identify R-S flip-flop circuits, numeral 104 indicate an oscillator, numeral 105 refers to a frequency divider circuit, numerals 106 to 117 identify AND gate circuits, numerals 118 to 120 represent ring counters, numeral 121 refers to a flip-flop circuit, numerals 121a and 121b indicate AND gate circuits, numeral 122 refers to a gate circuit, numeral 123 represents a 10-stage counter, numeral 124 represents a plasma display panel, S1 identifies a switch and +V1, +V2, and -V3 refer to power source voltages respectively. Further, reference characters XF, XA, XB, XC, YF, YA, YB and YC designate the aforesaid buses and W1 to W7 designate the aforementioned write electrodes.

An output of the oscillator 104 is frequency divided by the frequency divider circuit 105 to $1/n$.

Operating a key (not shown) of the key board 100 to produce a start signal for writing, the R-S flip-flop circuit 102 is set by the start signal.

When supplied with an output of the R-S flip-flop circuit 102, the AND gate circuit 106 derives therefrom an output frequency divided by the frequency divider circuit 105, which output is applied to the three-stage ring counter 119.

Outputs of the respective stages of the three-stage ring counter 119 are fed to the buses XA, XB and XC through the AND gate circuits 113, 114 and 115 respectively.

The ring counter 118 is supplied with the output of the final stage of the ring counter 119 and an output of the diode matrix circuit 101 which is supplied with a character selecting signal from the key board 100 is sequentially applied to the gate circuit 122 by the output of each stage of the aforementioned ring counter 118 and a write voltage is impressed to one of the write electrodes W1 to W7 which is selected by the diode matrix circuit 122.

The voltage V1 is sequentially supplied by the output of the ring counter 119 to the buses XA, XB and XC, for example, in the manner of a three-phase voltage. In

this case, since the ring counter 120 is inoperative, the voltage V1 is applied to the bus XA only.

The bus XF is supplied with the voltage V2 through the AND gate circuit 117. The bus YF is supplied with the voltage -V3 through the AND gate circuit 112.

Consequently, information displayed by a written discharge spot becomes lengthened in a lateral direction in the same manner as shown in FIG. 9A and is shifted from right to left in FIG. 11.

Upon completion of writing one character, the flip-flop circuit 102 is reset by the output of the final stage of the ring counter 118 to stop the ring counter 119.

Deriving a start signal from key board keyboard 100 for writing a second character, similar operations to the aforesaid ones are carried out to achieve the writing.

In the case of upward shifting the character group of one line after completion of writing, it is sufficient only to close the line shift switch S1 of the key board 100.

Thus, the flip-flop circuit 103 is reset and the output of the frequency divider 105 is applied to the ring counter 120 from the AND gate circuit 107.

An output of the ring counter 120 is applied to the buses YA, YB and YC and the manner of this application is exactly the same as the aforesaid one for the buses XA, XB and XC and the voltage V1 is sequentially impressed to the buses.

In this case, the bus YF is supplied with the voltage V2 through the AND gate circuit 111 and the bus XF is supplied with the voltage -V3 through the AND gate circuit 116.

Accordingly, the buses YA, YB and YC are sequentially supplied with the voltage V1 and the discharge spot extends in a direction perpendicular to that LO depicted in FIG. 9A, that is, becomes longer in a vertical direction and it is shifted upwardly in the figure. The voltage impressed to the buses YA, YB, YC and YF is displaced 180° apart in phase from that impressed to the buses XA, XB, XC and XF by a circuit including the flip-flop circuit 121 and the AND gate circuits 121a and 121b.

The output of the final stage of the ring counter 120 is counted by the 10-stage counter 123 and the flip-flop circuit 103 is reset by its output to stop the line shift. The reason for the use of the 10-stage counter 123 is to provide a space for three dots between lines in the case of forming one character with 5×7 dots.

When the characters have thus been shifted upwardly by one line, the shift operation is stopped. Closing the line shift switch S1 again, the above operation is repeated to achieve the shift operation again.

While the shift operation is not being carried out, the flip-flop circuits 102 and 103 are both in their reset condition, so that the AND gate circuits 111, 112, 116 and 117 are all closed and no voltage is applied to the buses XF and YF.

The impression of the voltage V2 to the buses XF and YF enlarges the discharge spot and the impression of the voltage -V3 thereto reduces it.

As has been described in the foregoing, the present invention makes it possible that the luminous spot is enlarged or the self shift operation is facilitated by forming the electric field by the third electrode in the same direction as that by the main electrode, and that the luminous spot is narrowed to provide a display with high resolution by forming the both electric fields in reverse

directions. The degree of enlargement and reduction of the spot can readily be controlled by the shape, the arrangement and the number of the third electrode and a voltage impressed thereto.

It will be apparent that many modifications and variations may be effected without departing from the scope of the novel concepts of this invention.

What is claimed is:

1. A plasma display system comprising:

- a. a plasma display device including first and second base plates disposed opposite to each other for defining a discharge gas region therebetween, first and second sets of main electrodes disposed respectively upon said first and second base plates whereby said first and second sets of main electrodes intersect each other;
- b. discharge energizing means for impressing a voltage between selected main electrodes of said first and second sets whereby an electrical discharge is established at the intersecting points of said selected main electrodes;

wherein the improvement comprises:

- c. auxiliary electrodes disposed between adjacent main electrodes of at least one of said first and second sets; and
- d. auxiliary energizing means for applying a control voltage to said auxiliary electrodes to control the size and configuration of the electrical discharge established between said selected main electrodes of said first and second sets.

2. A plasma display system as claimed in claim 1, wherein said auxiliary electrodes comprise a first set thereof and are disposed between adjacent main elec-

trodes of said first set, and there is further included a second set of auxiliary electrodes disposed between the adjacent main electrodes of said second set.

3. A plasma display system according to claim 2, wherein said first-mentioned and said second sets of auxiliary electrodes are each covered with a dielectric layer.

4. A plasma display system as claimed in claim 1, wherein said second set of main electrodes and said second set of auxiliary electrodes each extend in a direction substantially perpendicular to said main electrodes of said first set.

5. A plasma display system according to claim 1, wherein said auxiliary electrodes for controlling electric fields established between said main electrodes are formed in substantially the same plane as said first set of electrodes and are covered with a dielectric layer.

6. A plasma display system according to claim 1, wherein said auxiliary electrodes for controlling electric fields established between said main electrodes are formed in substantially the same plane as said second set of electrodes and are covered with a dielectric layer.

7. A plasma display system according to claim 1, wherein said auxiliary electrodes are formed between adjacent ones of said main electrodes formed on the same base plate.

8. A plasma display system according to claim 1, wherein each of said auxiliary electrodes is located between adjacent main electrodes formed on a base plate, and is disposed closer to one of said adjacent main electrodes than the other of said adjacent main electrodes.

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